

HAT3036R

Silicon N/P Channel Power MOSFET Power Switching

R07DS1373EJ0501

Rev.5.01

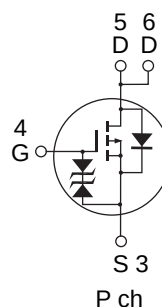
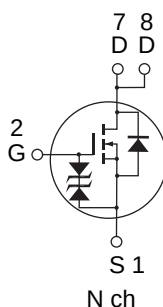
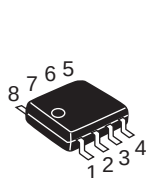
Jan 20, 2017

Features

- Capable of 4.5 V gate drive
- Low drive current
- High density mounting

Outline

RENESAS Package code: PRSP0008DD-D
(Package name: SOP-8<FP-8DAV>)



1, 3 Source
2, 4 Gate
5, 6, 7, 8 Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		Nch	Pch	
Drain to source voltage	V_{DSS}	30	-30	V
Gate to source voltage	V_{GSS}	± 20	-20/+10	V
Drain current	I_D	4.8	-4.8	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	38.4	-38.4	A
Body-drain diode reverse drain current	I_{DR}	4.8	-4.8	A
Channel dissipation	P_{ch} ^{Note2}	1.3		W
Channel dissipation	P_{ch} ^{Note3}	2.0		W
Channel temperature	T_{ch}	150		°C
Storage temperature	T_{stg}	-55 to +150		°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$

2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

3. 2 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics

• N Channel

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	40	50	$\text{m}\Omega$	$I_D = 2.4 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	60	87	$\text{m}\Omega$	$I_D = 2.4 \text{ A}$, $V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	3.6	6.0	—	S	$I_D = 2.4 \text{ A}$, $V_{DS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	260	—	pF	$V_{DS} = 10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	70	—	pF	
Reverse transfer capacitance	C_{rss}	—	30	—	pF	
Total gate charge	Q_g	—	2.2	—	nC	$V_{DD} = 10 \text{ V}$ $V_{GS} = 4.5 \text{ V}$ $I_D = 4.8 \text{ A}$
Gate to source charge	Q_{gs}	—	1.0	—	nC	
Gate to drain charge	Q_{gd}	—	0.8	—	nC	
Turn-on delay time	$t_{d(on)}$	—	7.0	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 2.4 \text{ A}$ $V_{DD} \cong 10 \text{ V}$ $R_L = 4.16 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	17.5	—	ns	
Turn-off delay time	$t_{d(off)}$	—	35.5	—	ns	
Fall time	t_f	—	3.8	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.88	1.15	V	$I_F = 4.8 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	18	—	ns	$I_F = 4.8 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

• P Channel

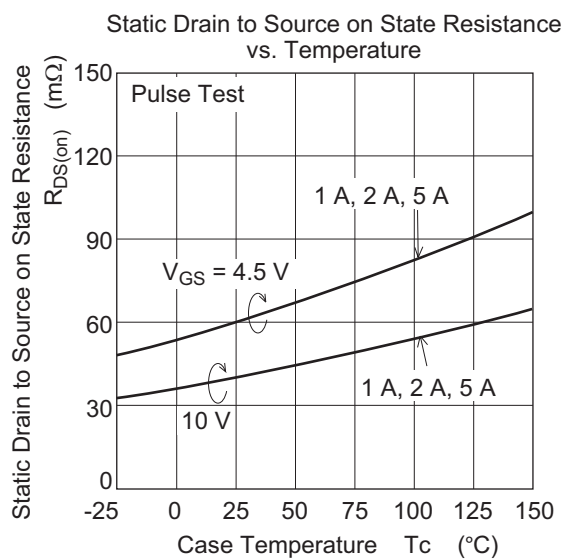
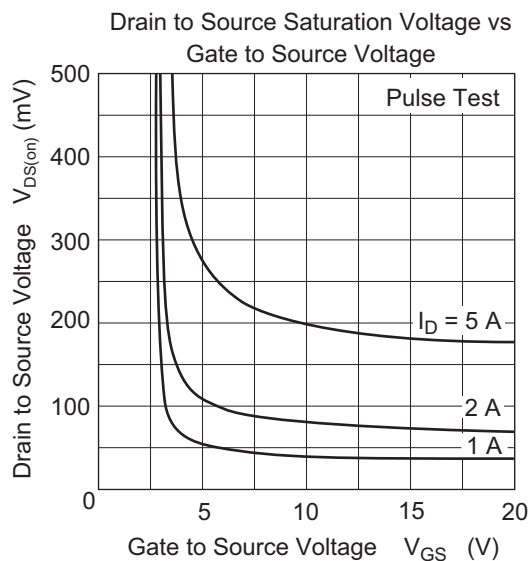
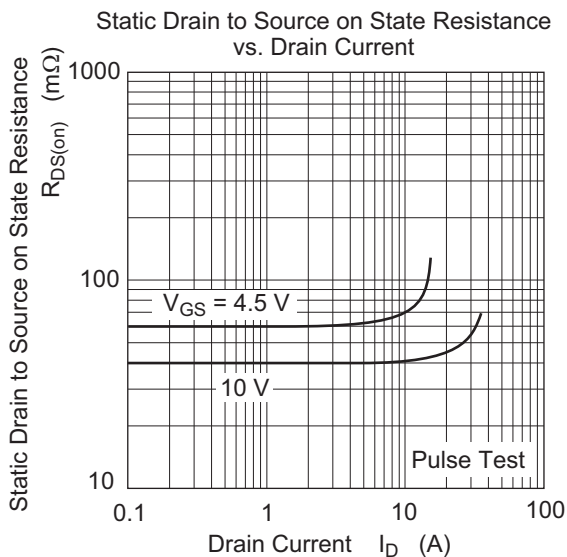
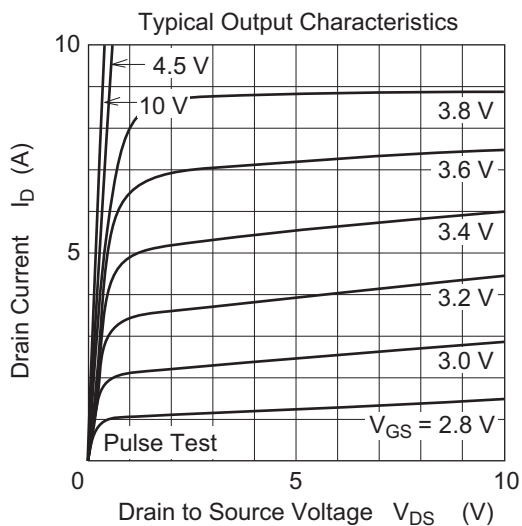
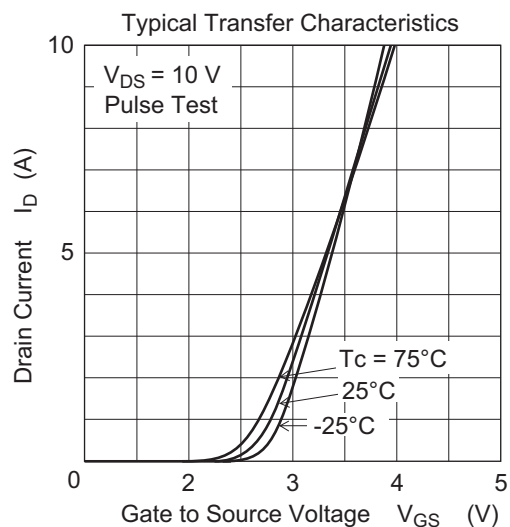
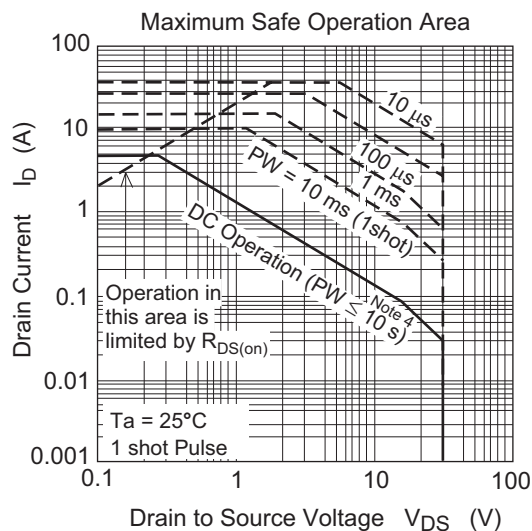
(Ta = 25°C)

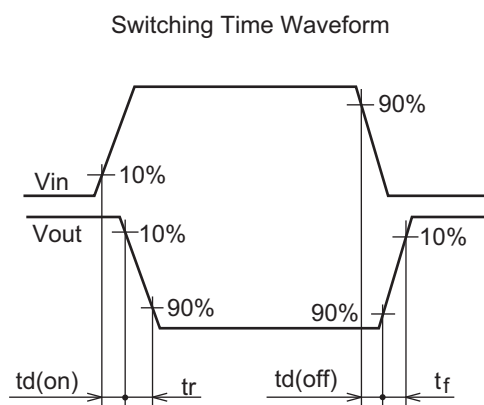
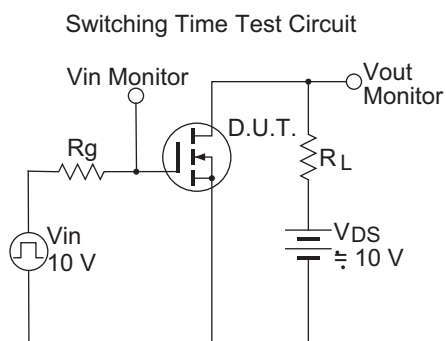
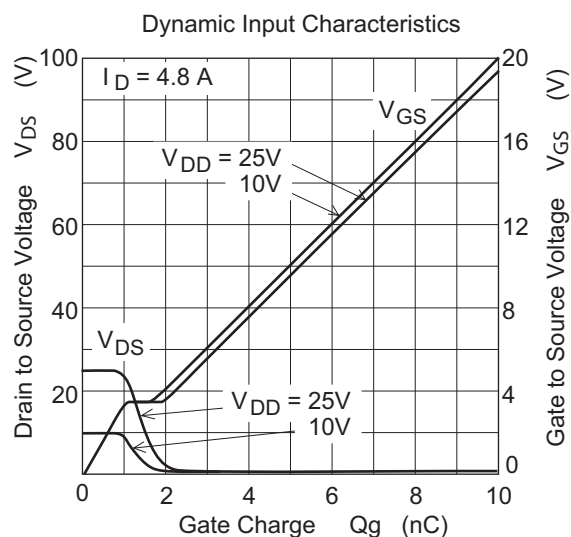
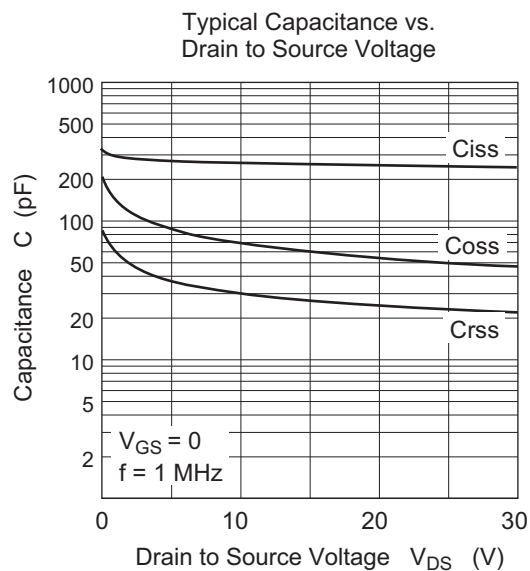
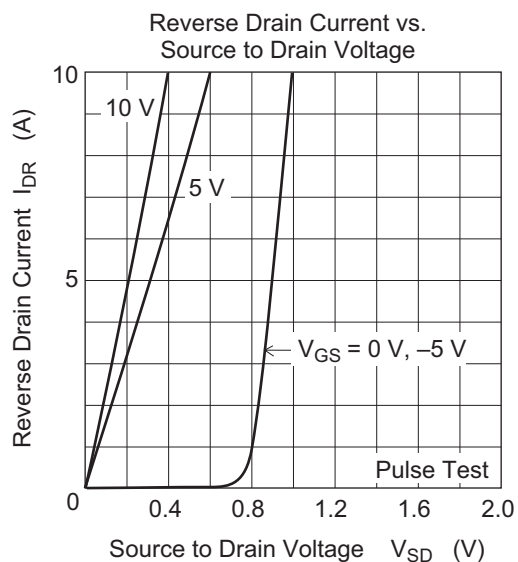
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	-30	—	—	V	$I_D = -10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-20/+10	—	—	V	$I_G = \pm 100 \text{ }\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = -16, +8 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-1	μA	$V_{DS} = -30 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.0	—	-2.5	V	$V_{DS} = -10 \text{ V}$, $I_D = -1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	50	63	$\text{m}\Omega$	$I_D = -2.4 \text{ A}$, $V_{GS} = -10 \text{ V}$ Note4
	$R_{DS(on)}$	—	75	109	$\text{m}\Omega$	$I_D = -2.4 \text{ A}$, $V_{GS} = -4.5 \text{ V}$ Note4
Forward transfer admittance	$ y_{fs} $	3.0	5.0	—	S	$I_D = -2.4 \text{ A}$, $V_{DS} = -10 \text{ V}$ Note4
Input capacitance	C_{iss}	—	505	—	pF	$V_{DS} = -10 \text{ V}$ $V_{GS} = 0$ $f = 1 \text{ MHz}$
Output capacitance	C_{oss}	—	125	—	pF	
Reverse transfer capacitance	C_{rss}	—	70	—	pF	
Total gate charge	Q_g	—	4.7	—	nC	$V_{DD} = -10 \text{ V}$ $V_{GS} = -4.5 \text{ V}$ $I_D = -4.8 \text{ A}$
Gate to source charge	Q_{gs}	—	1.5	—	nC	
Gate to drain charge	Q_{gd}	—	1.2	—	nC	
Turn-on delay time	$t_{d(on)}$	—	16	—	ns	$V_{GS} = -10 \text{ V}$, $I_D = -2.4 \text{ A}$ $V_{DD} \approx -10 \text{ V}$ $R_L = 4.16 \text{ }\Omega$ $R_g = 4.7 \text{ }\Omega$
Rise time	t_r	—	15	—	ns	
Turn-off delay time	$t_{d(off)}$	—	32	—	ns	
Fall time	t_f	—	7	—	ns	
Body-drain diode forward voltage	V_{DF}	—	-0.88	-1.15	V	$I_F = -4.8 \text{ A}$, $V_{GS} = 0$ Note4
Body-drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = -4.8 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

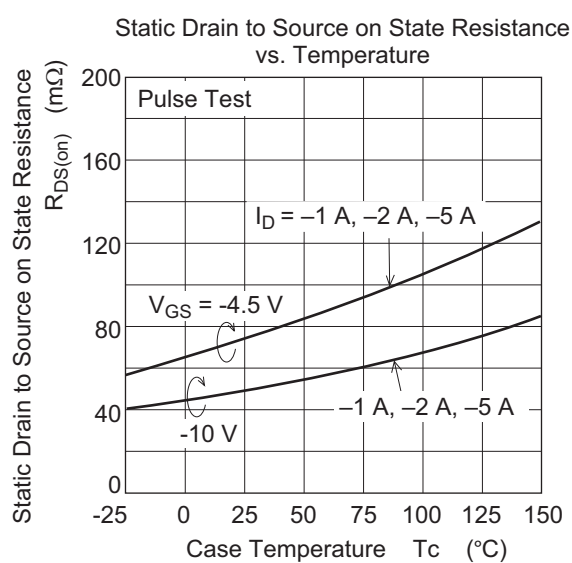
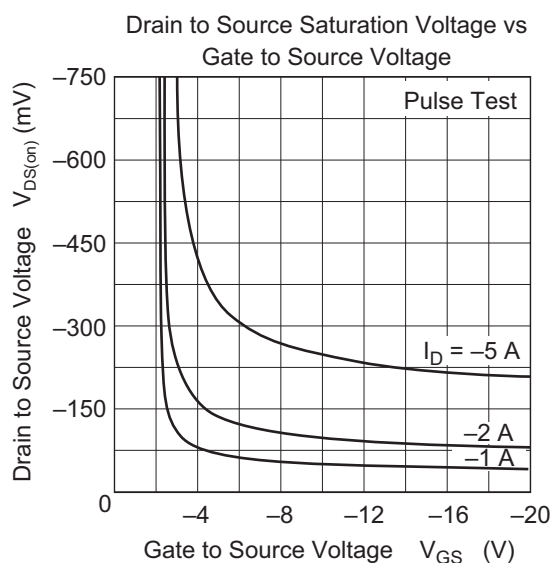
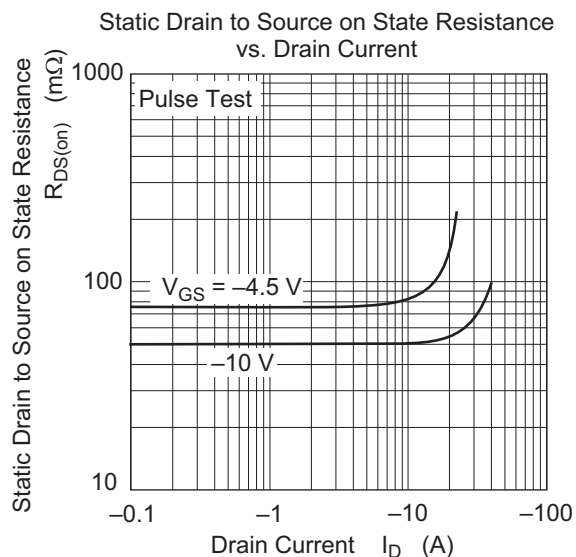
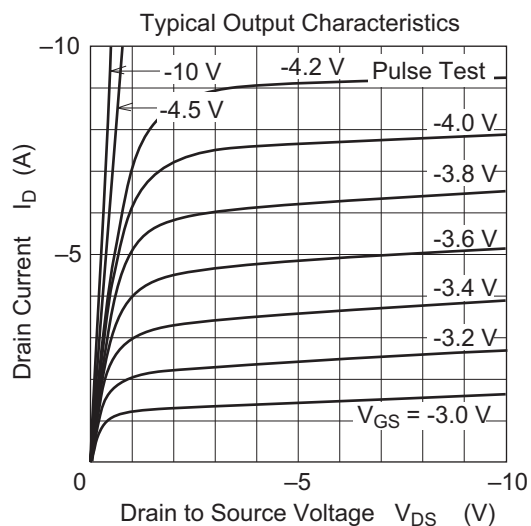
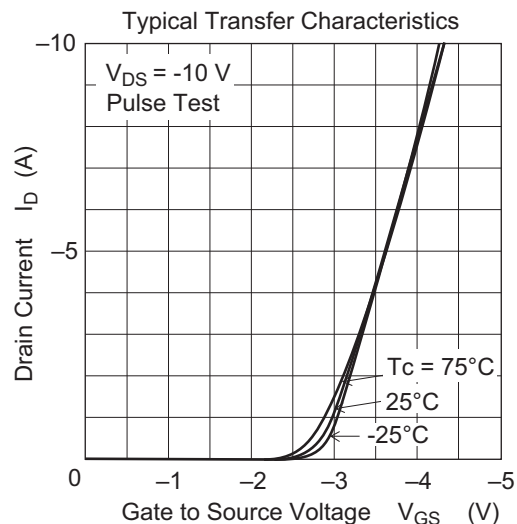
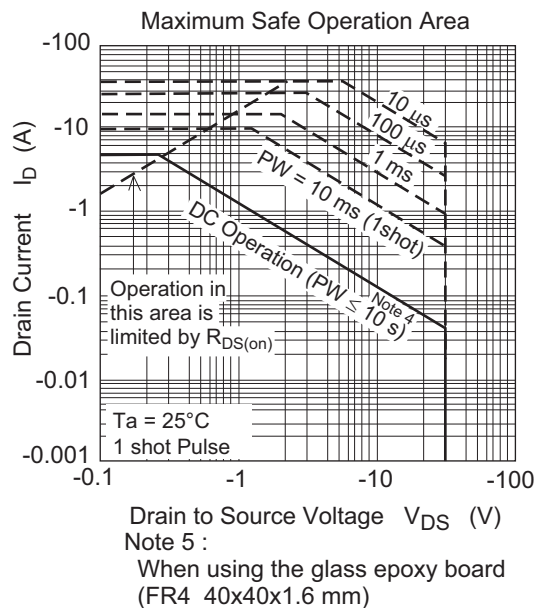
Main Characteristics

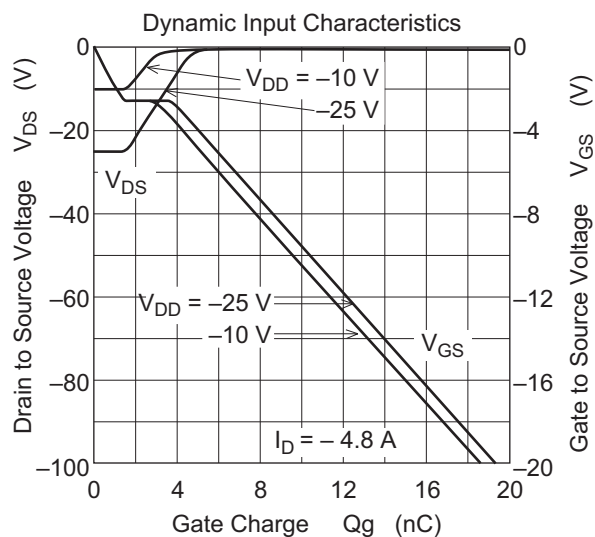
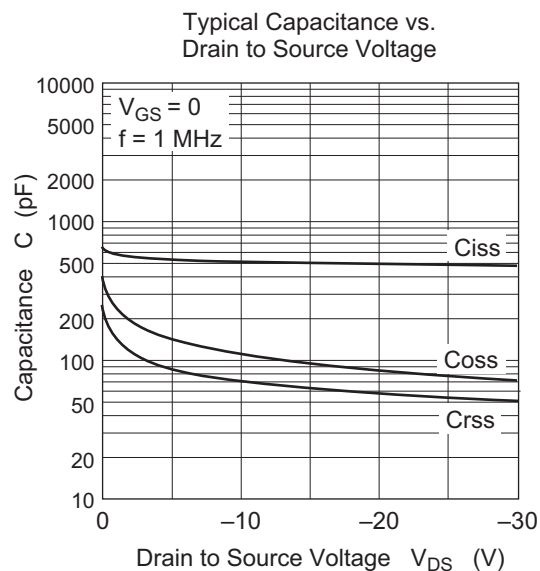
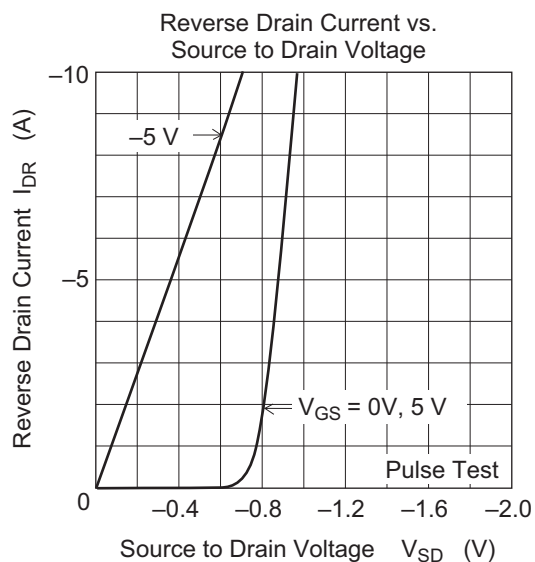
• N Channel



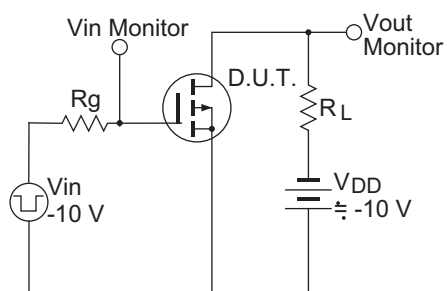


• P Channel

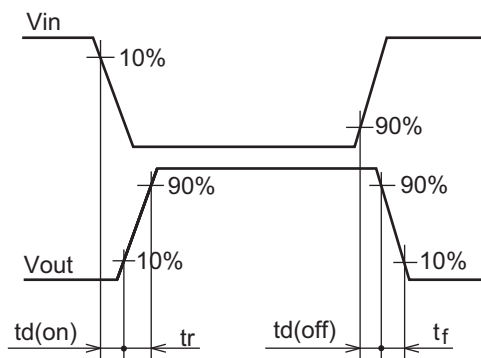




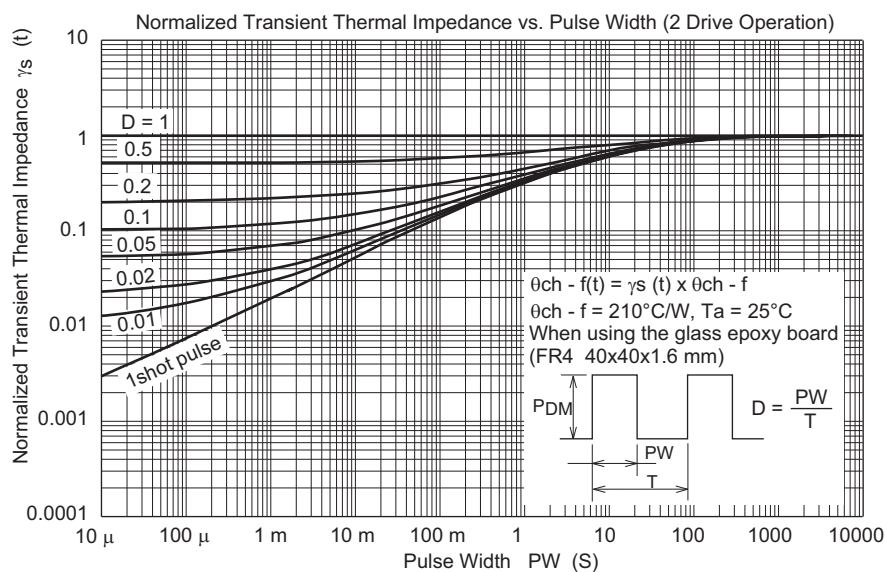
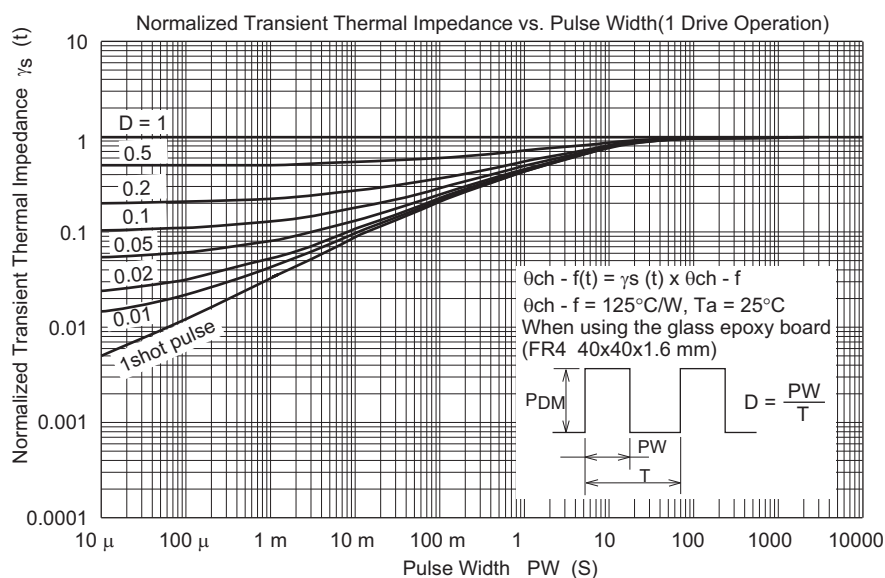
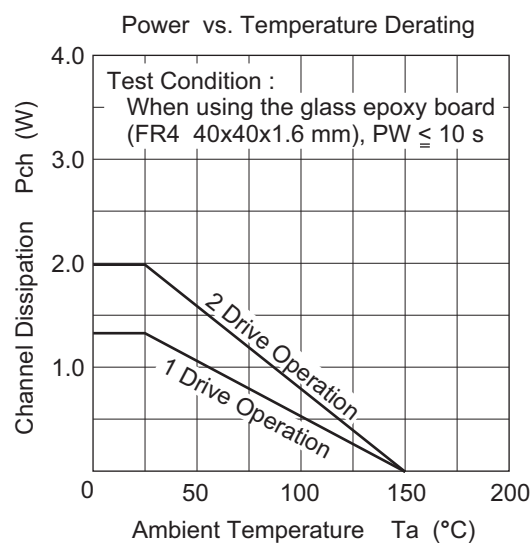
Switching Time Test Circuit



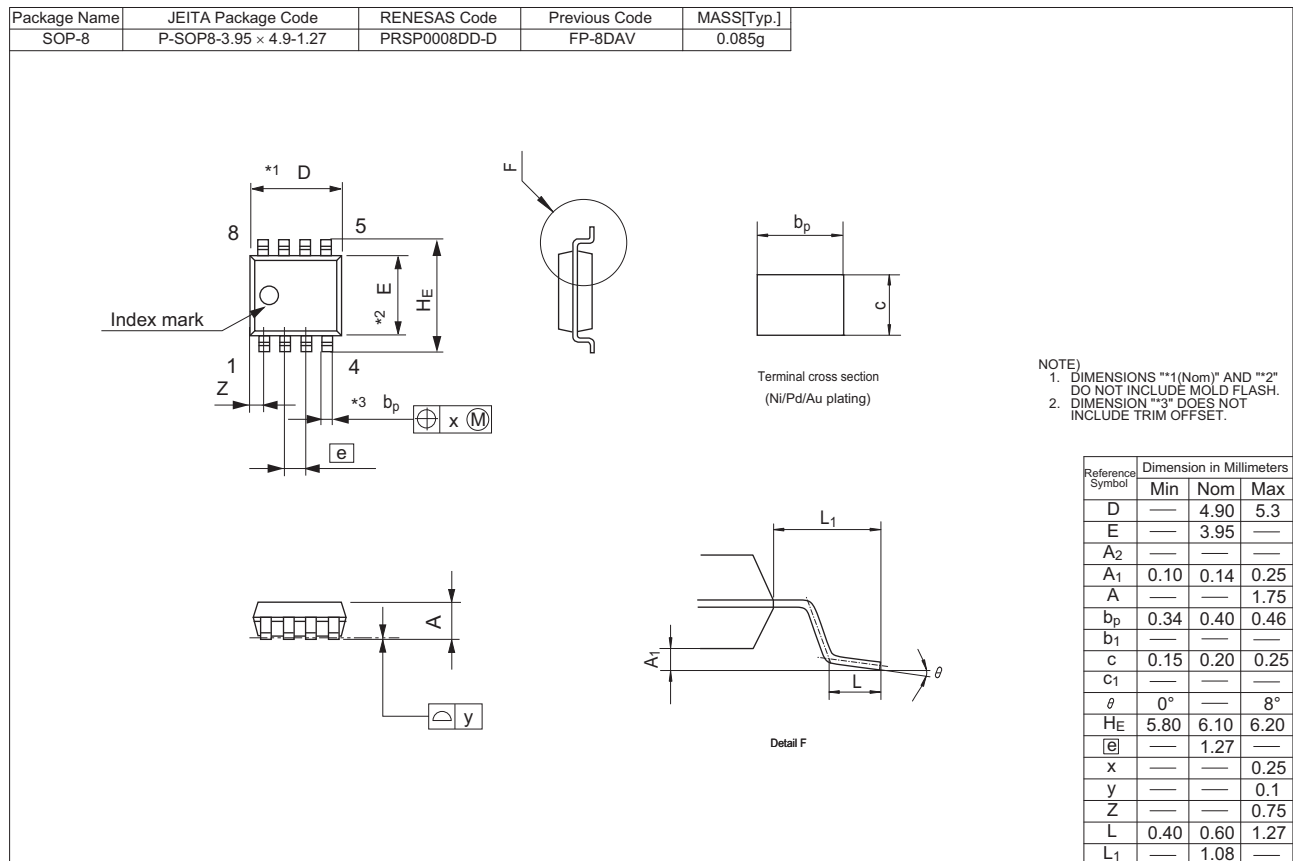
Switching Time Waveform



• Common



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
HAT3036R-EL-E	2500 pcs	Taping

Note: For some grades, production may be terminated. Please contact the Renesas sales Office to check the state of production before ordering the product.

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 7. 虽然瑞萨电子一直致力于提高瑞萨电子产品的质量和可靠性，但是，半导体产品有其自身的具体特性，如一定的故障发生率以及在某些使用条件下会发生故障等。此外，瑞萨电子产品均未进行防辐射设计。所以请采取安全保护措施，以避免当瑞萨电子产品在发生故障而造成火灾时导致人身事故、伤害或损害的事故。例如进行软硬件安全设计（包括但不限于冗余设计、防火控制以及故障预防等）、适当的老化处理或其他适当的措施等。由于难于对微机电系统单独进行评估，所以请用户自行对最终产品或系统进行安全评估。
 8. 关于环境保护方面的详细内容，例如每种瑞萨电子产品的环境兼容性等，请与瑞萨电子的营业部门联系。使用瑞萨电子产品时，请遵守对管制物质的使用或含量进行管理的所有相关法律法规（包括但不限于《欧盟RoHS指令》）。对于因用户未遵守相应法律法规而导致的损害或损失，瑞萨电子不承担任何责任。
 9. 不可将瑞萨电子产品和技术用于或者嵌入日本国内或海外相应的法律法规所禁止生产、使用及销售的任何产品或系统中。也不可将本文件中记载的瑞萨电子产品或技术用于与军事应用或者军事用途有关的目的（如大规模杀伤性武器的开发等）。在将本文件中记载的瑞萨电子产品或技术进行出口时，应当遵守相应的出口管制法律法规，并按照上述法律法规所规定的程序进行。
 10. 向第三方分销或处分产品或者以其他方式将产品置于第三方控制之下的瑞萨电子产品买方或分销商，有责任事先向上述第三方通知本文件规定的内容和条件；对于用户或第三方因非法使用瑞萨电子产品而遭受的任何损失，瑞萨电子不承担任何责任。
 11. 在事先未得到瑞萨电子书面认可的情况下，不得以任何形式部分或全部转载或复制本文件。
 12. 如果对本文件所记载的信息或瑞萨电子产品有任何疑问，或者用户有任何其他疑问，请向瑞萨电子的营业部门咨询。
- (注1) 瑞萨电子：在本文件中指瑞萨电子株式会社及其控股子公司。
(注2) 瑞萨电子产品：指瑞萨电子开发或生产的任何产品。



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