

To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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HAT2126RP

Silicon N Channel Power MOS FET with Schottky Barrier Diode
High Speed Power Switching

RENESAS

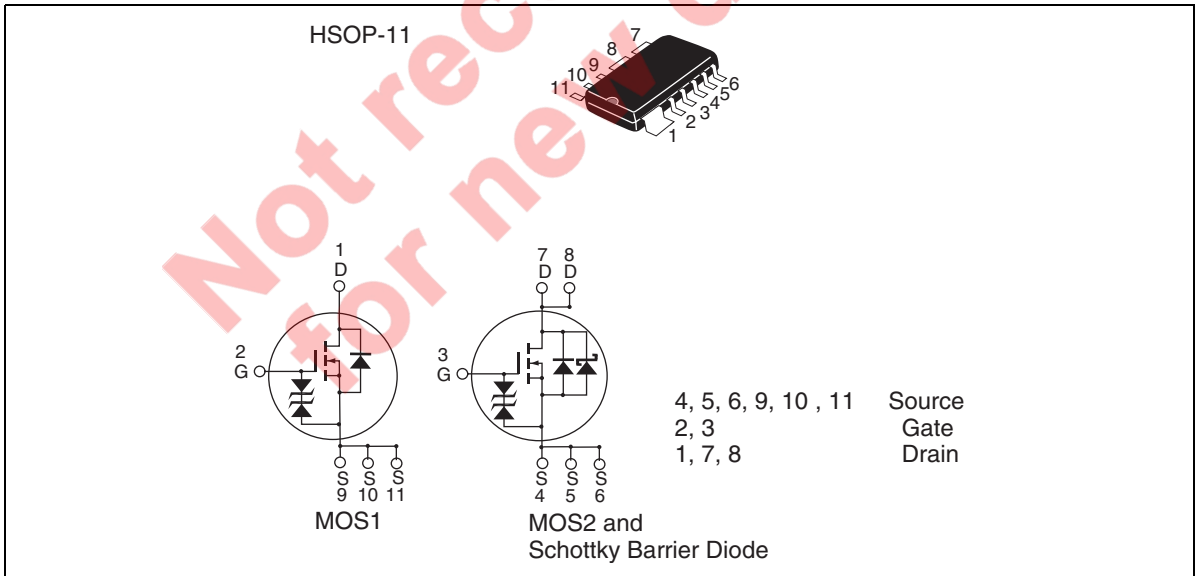
ADE-208-1576D (Z)

5th. Edition
Dec. 2002

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Built-in Schottky Barrier Diode

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2 & SBD	
Drain to source voltage	V_{DSS}	30	30	V
Gate to source voltage	V_{GSS}	±20	±12	V
Drain current	I_D	12	16	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	96	128	A
Reverse drain current	I_{DR}	12	16	A
Channel dissipation	P_{ch} ^{Note2}	2.0	3.5	W
Channel temperature	T_{ch}	150	150	°C
Storage temperature	T_{stg}	-55 to +150	-55 to +150	°C

Notes: 1. $PW \leq 10\mu s$, duty cycle $\leq 1\%$

2. 1 Drive operation; When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), $PW \leq 10s$

Electrical Characteristics

(Ta = 25°C)

• MOS1

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10\text{mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30\text{V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$V_{DS} = 10\text{V}, I_D = 1\text{mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	10	13	$\text{m}\Omega$	$I_D = 6\text{A}, V_{GS} = 10\text{V}$ ^{Note3}
	$R_{DS(on)}$	—	18	27	$\text{m}\Omega$	$I_D = 6\text{A}, V_{GS} = 4.5\text{V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	12	20	—	S	$I_D = 6\text{A}, V_{DS} = 10\text{V}$ ^{Note3}
Input capacitance	Ciss	—	1000	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	Coss	—	280	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	160	—	pF	$f = 1\text{MHz}$
Total gate charge	Qg	—	9	—	nc	$V_{DD} = 10\text{V}$
Gate to source charge	Qgs	—	3.6	—	nc	$V_{GS} = 5\text{V}$
Gate to drain charge	Qgd	—	3.2	—	nc	$I_D = 16\text{A}$
Turn-on delay time	$t_{d(on)}$	—	12	—	ns	$V_{GS} = 10\text{V}, I_D = 6\text{A}$
Rise time	t_r	—	22	—	ns	$V_{DD} \approx 10\text{V}$
Turn-off delay time	$t_{d(off)}$	—	55	—	ns	$R_L = 1.67\Omega$
Fall time	t_f	—	9	—	ns	$R_g = 4.7\Omega$
Body-drain diode forward voltage	V_{DF}	—	0.82	1.07	V	$I_F = 12\text{A}, V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	25	—	ns	$I_F = 12\text{A}, V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

Notes: 3. Pulse test

HAT2126RP

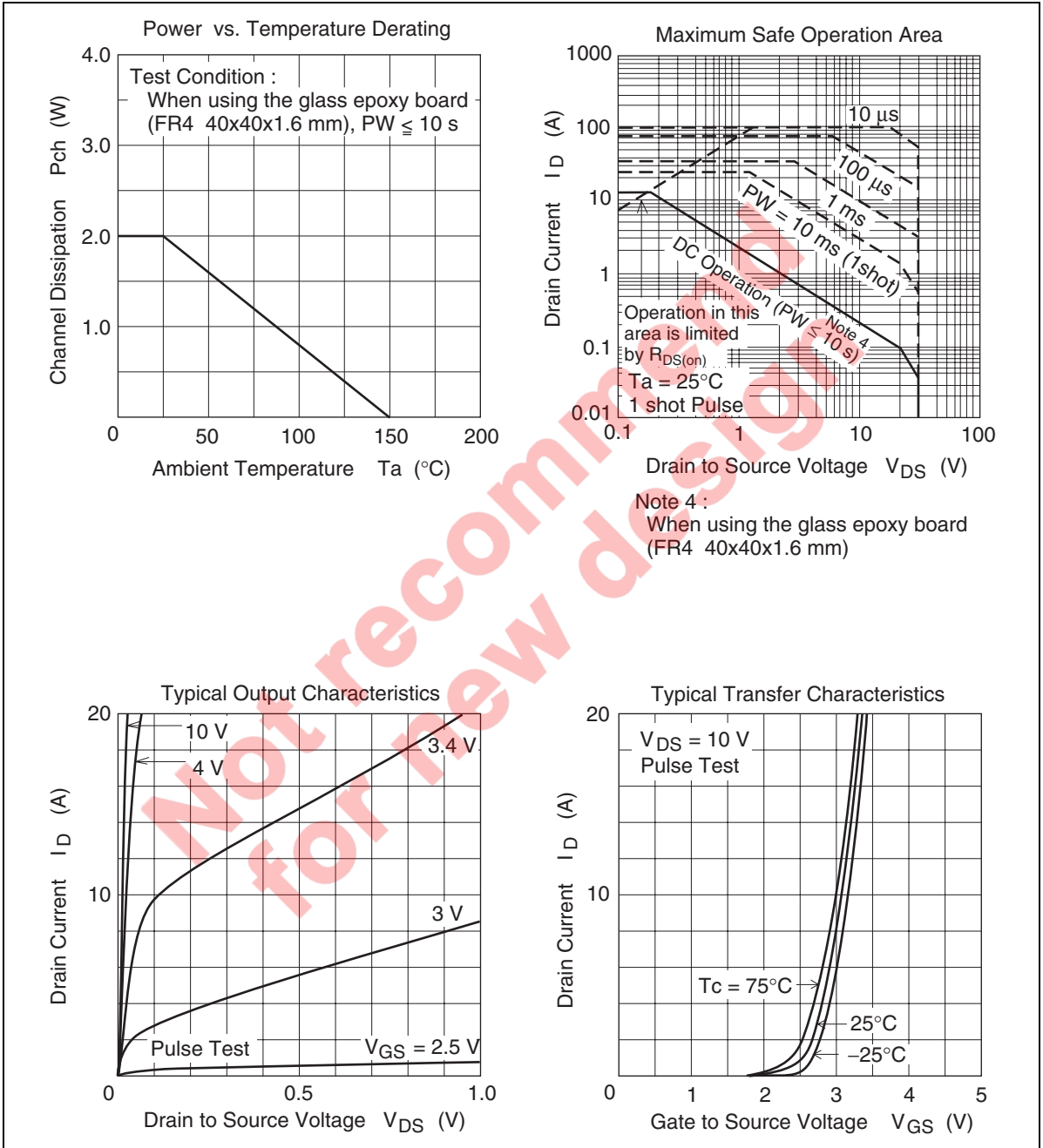
• MOS2 & Schottky Barrier Diode

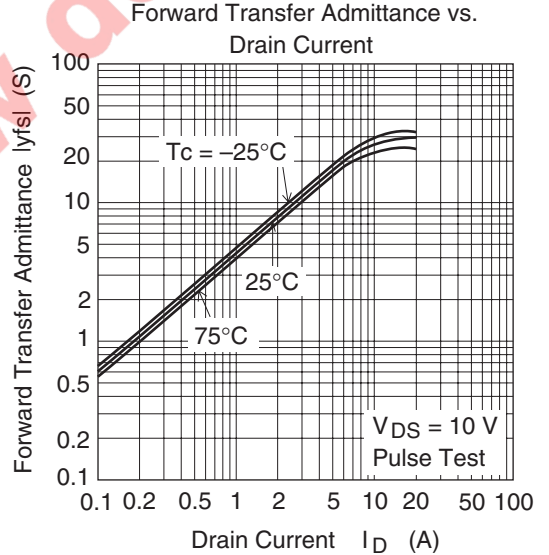
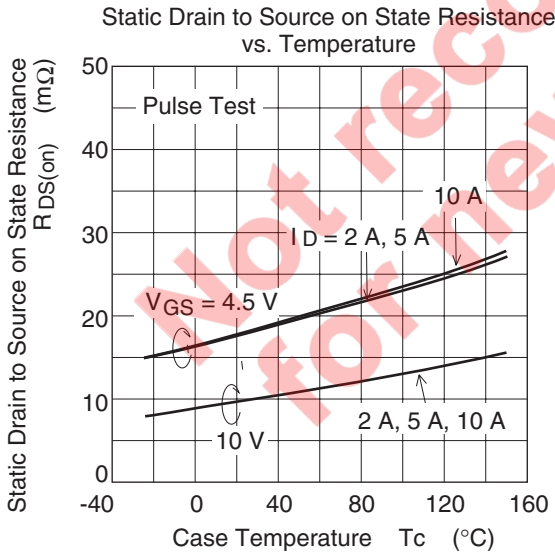
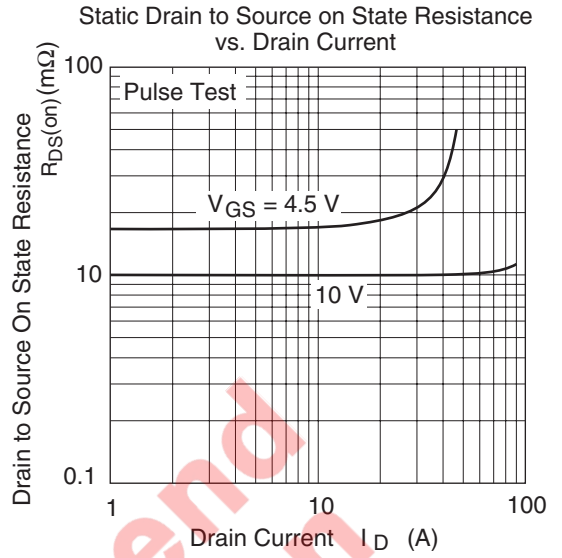
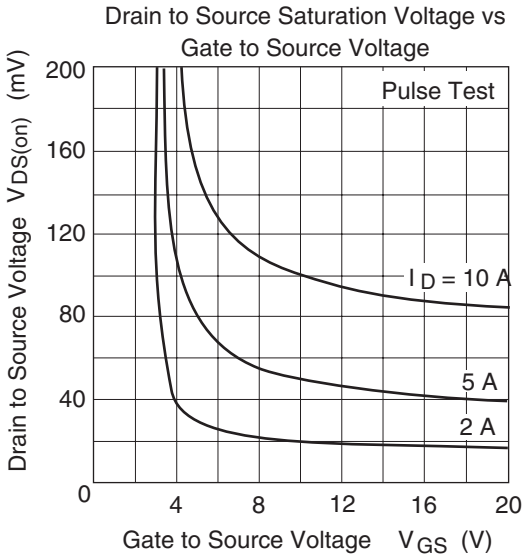
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10\text{mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 12	—	—	V	$I_G = \pm 100\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 10\text{V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	m A	$V_{DS} = 30\text{V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.4	—	2.5	V	$V_{DS} = 10\text{V}, I_D = 1\text{mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	5.6	7.3	$\text{m}\Omega$	$I_D = 8\text{A}, V_{GS} = 10\text{V}$ ^{Note3}
	$R_{DS(on)}$	—	7.3	9.5	$\text{m}\Omega$	$I_D = 8\text{A}, V_{GS} = 4.5\text{V}$ ^{Note3}
Forward transfer admittance	$ y_{fs} $	25	41	—	S	$I_D = 8\text{A}, V_{DS} = 10\text{V}$ ^{Note3}
Input capacitance	Ciss	—	3800	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	Coss	—	745	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	300	—	pF	$f = 1\text{MHz}$
Total gate charge	Qg	—	34	—	nc	$V_{DD} = 10\text{V}$
Gate to source charge	Qgs	—	10	—	nc	$V_{GS} = 5\text{V}$
Gate to drain charge	Qgd	—	8	—	nc	$I_D = 16\text{A}$
Turn-on delay time	$t_{d(on)}$	—	18	—	ns	$V_{GS} = 10\text{V}, I_D = 8\text{A}$
Rise time	t_r	—	22	—	ns	$V_{DD} \approx 10\text{V}$
Turn-off delay time	$t_{d(off)}$	—	88	—	ns	$R_L = 1.25\Omega$
Fall time	t_f	—	9.0	—	ns	$R_g = 4.7\Omega$
Schottky Barrier diode forward voltage	V_F	—	0.5	—	V	$I_F = 3.5\text{A}, V_{GS} = 0$ ^{Note3}
Body-drain diode reverse recovery time	t_{rr}	—	35	—	ns	$I_F = 16\text{A}, V_{GS} = 0$ $diF/dt = 50\text{A}/\mu\text{s}$

Notes: 3. Pulse test

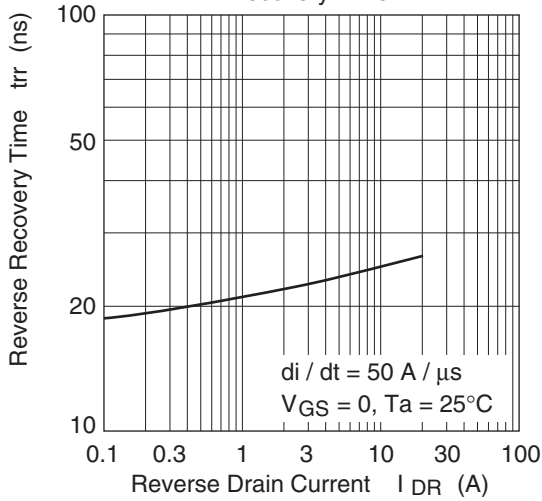
Main Characteristics

• MOS1

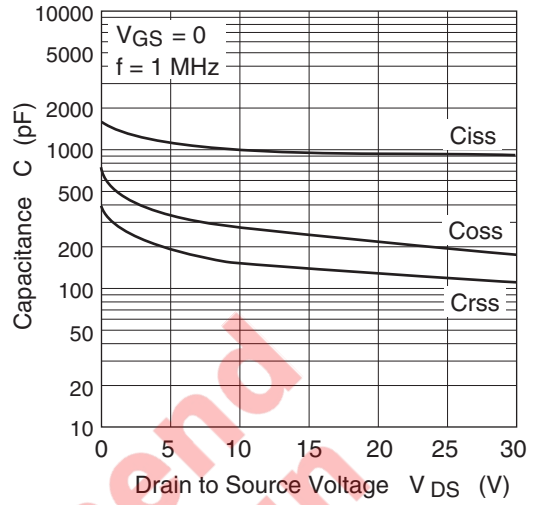




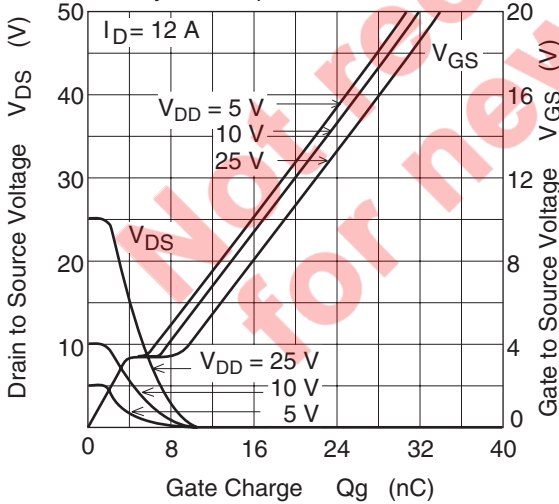
Body-Drain Diode Reverse Recovery Time



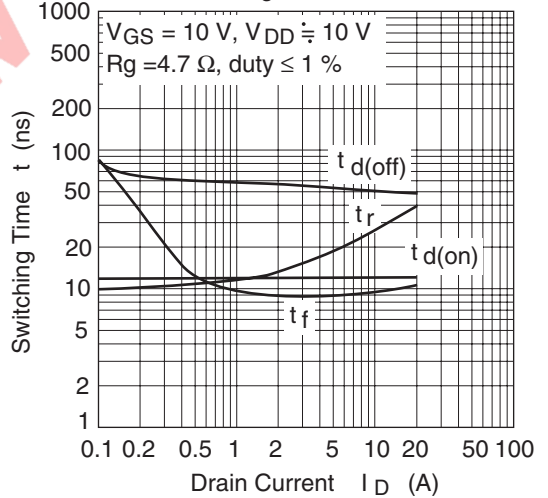
Typical Capacitance vs. Drain to Source Voltage

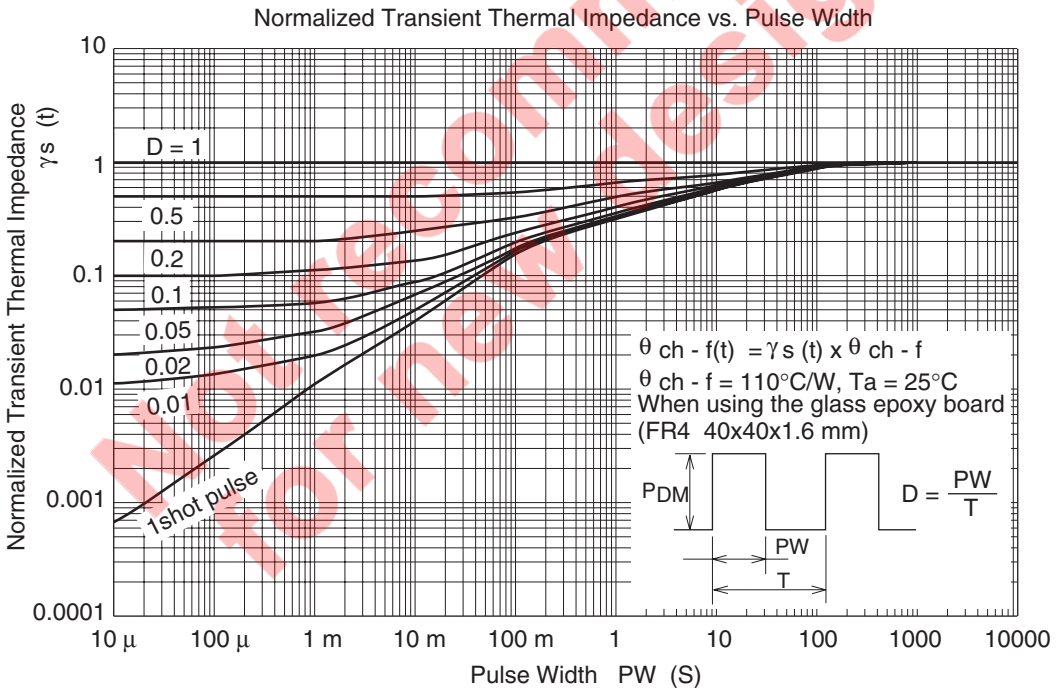
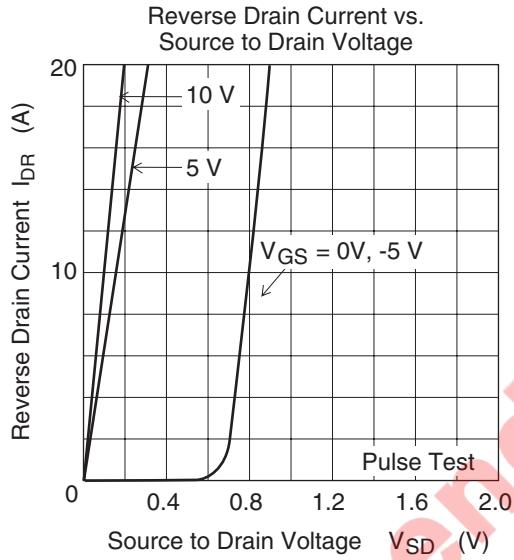


Dynamic Input Characteristics

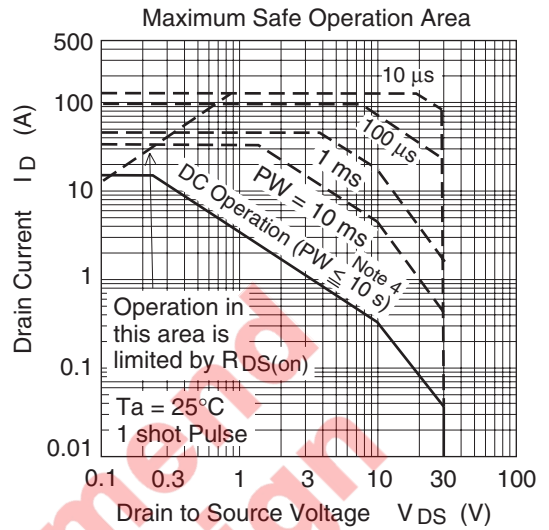
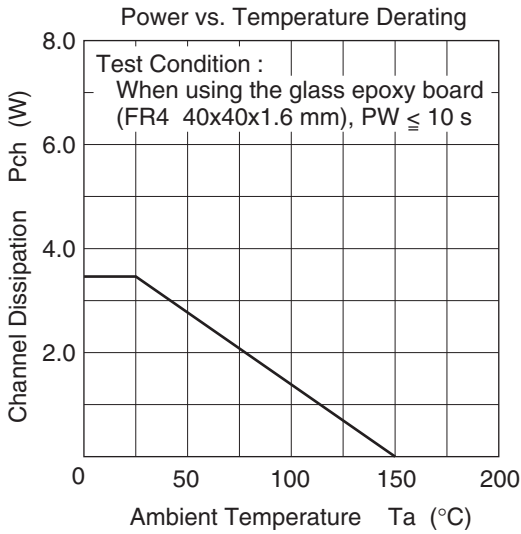


Switching Characteristics

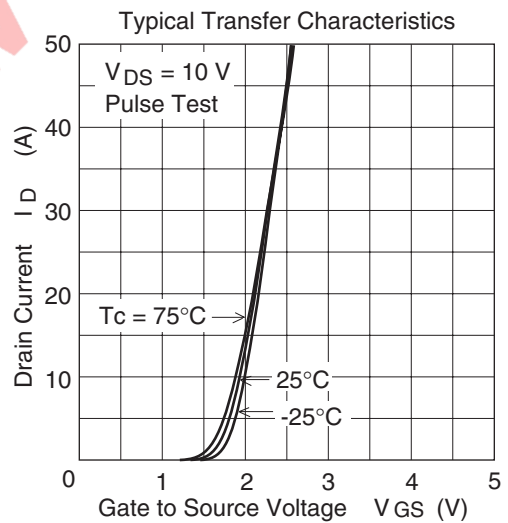
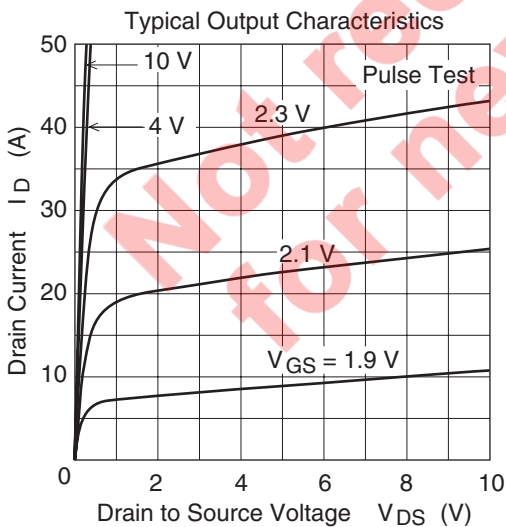


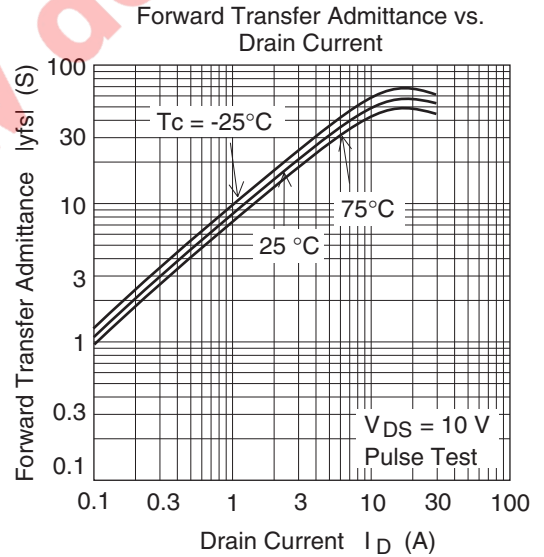
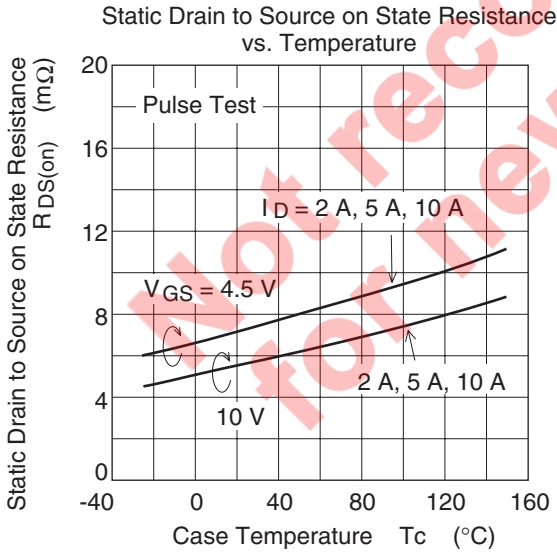
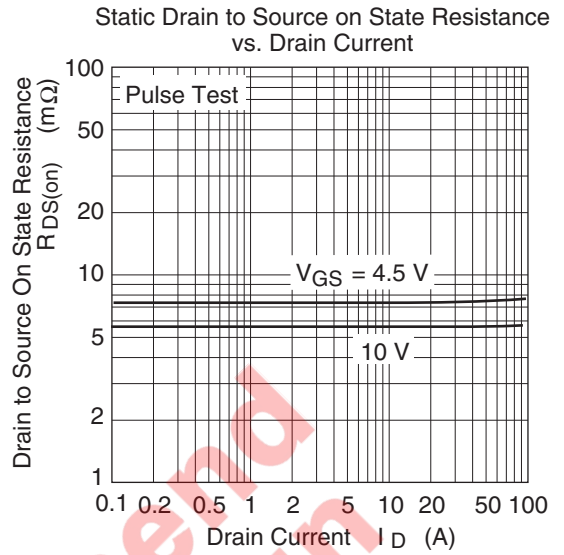
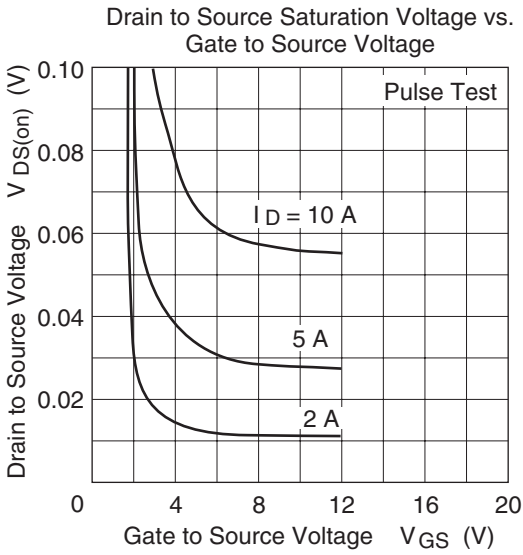


• MOS2 & Schottky Barrier Diode

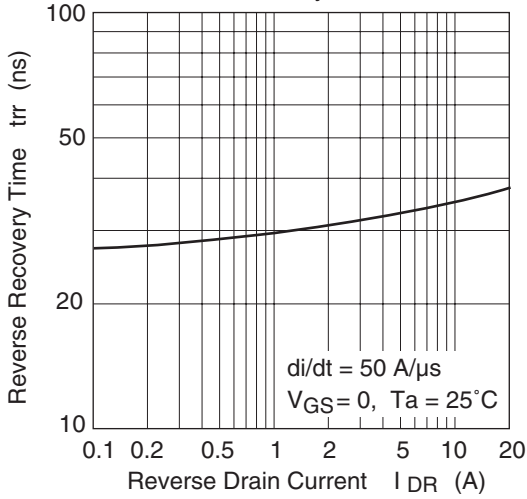


Note 4 :
When using the glass epoxy board (FR4 40x40x1.6 mm)

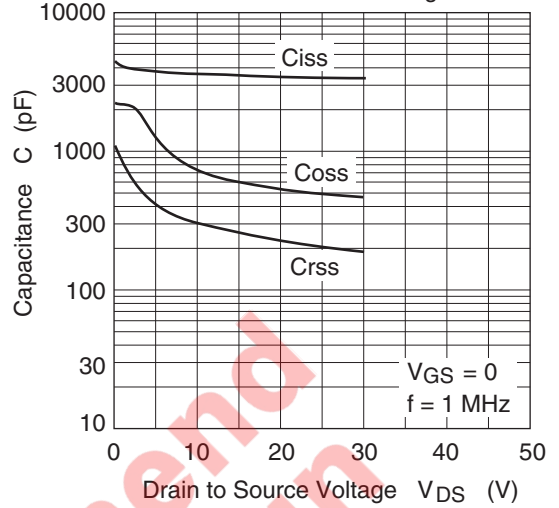




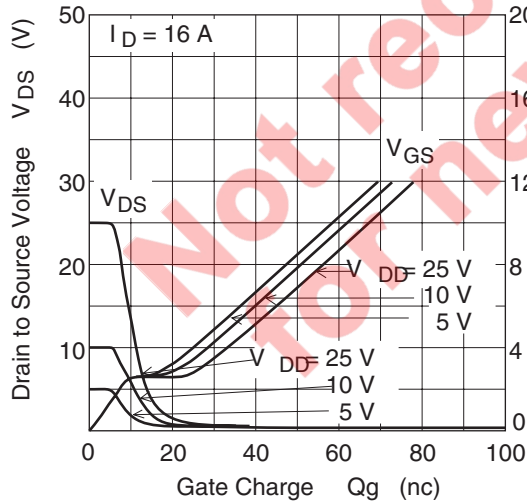
Body - Drain Diode Reverse Recovery Time



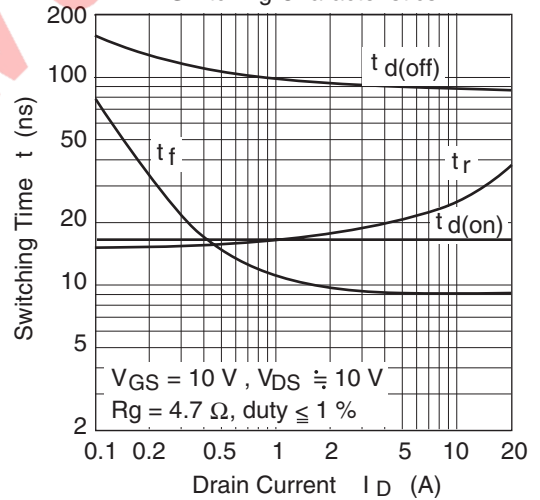
Typical Capacitance vs. Drain to Source Voltage

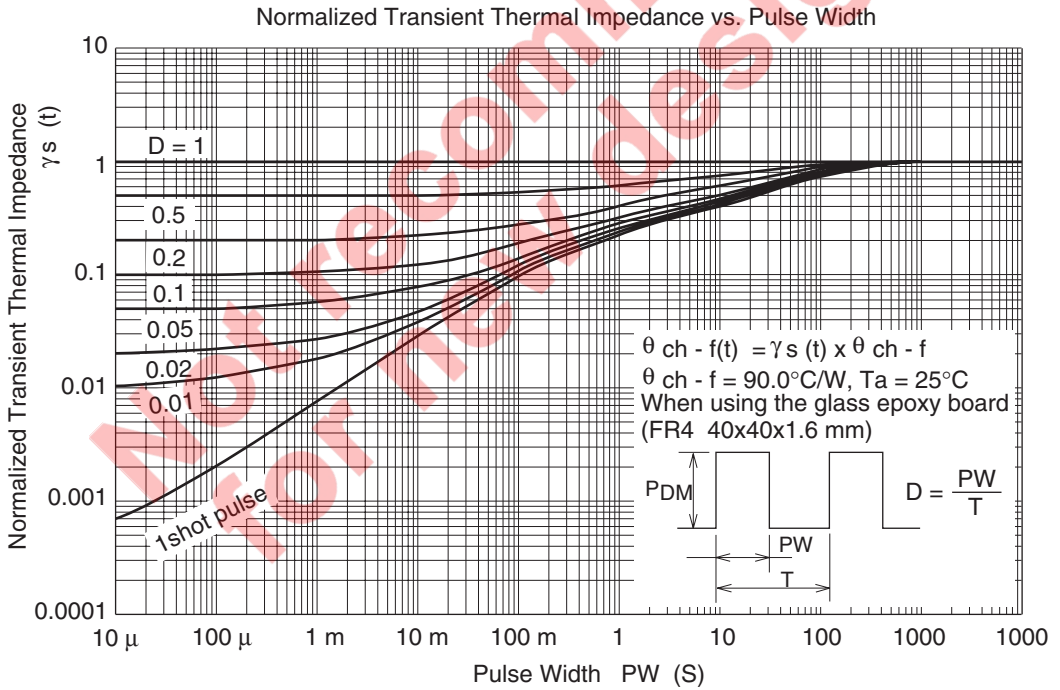
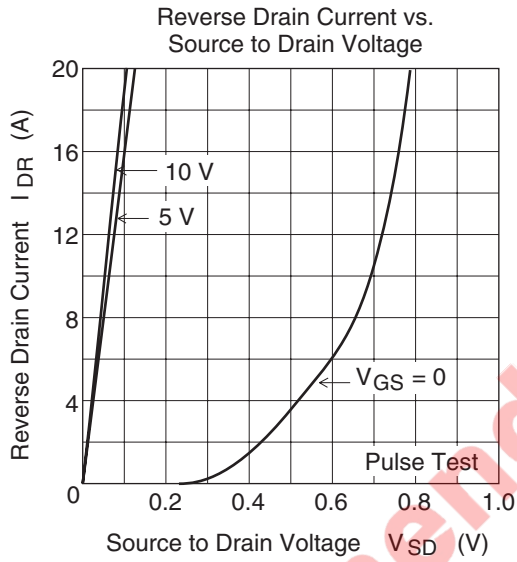


Dynamic Input Characteristics

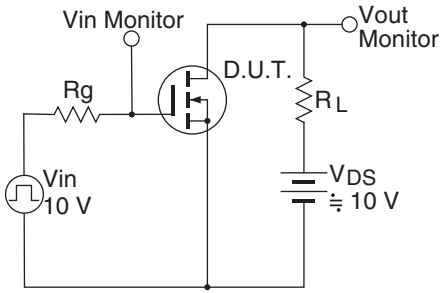


Switching Characteristics

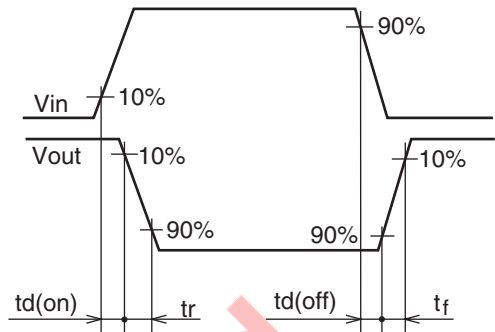




Switching Time Test Circuit

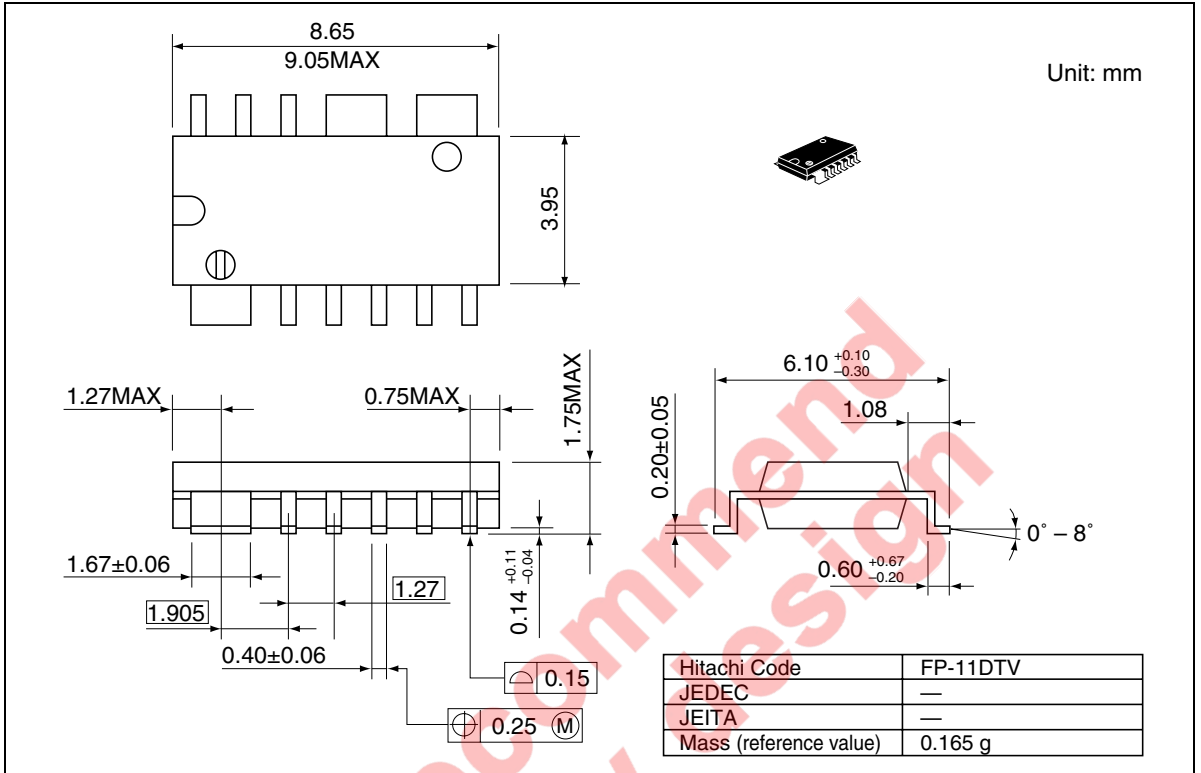


Switching Time Waveform



Not recommended
 for new design

Package Dimensions



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