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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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HAT1043M

Silicon P Channel Power MOS FET
Power Switching

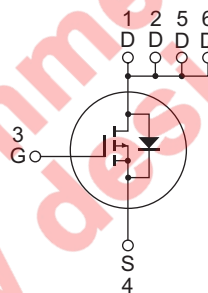
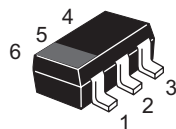
REJ03G1151-0600
(Previous: ADE-208-754D)
Rev.6.00
Sep 07, 2005

Features

- Low on-resistance
- Low drive current
- High density mounting
- 2.5 V gate drive device can be driven from 3 V source

Outline

RENESAS Package code: PTSP0006FA-A
(Package name: TSOP-6)



4 Source
3 Gate
1, 2, 5, 6 Drain

Not recommend for new design

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-20	V
Gate to source voltage	V _{GSS}	±12	V
Drain current	I _D	-4.4	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-17.6	A
Body-drain diode reverse drain current	I _{DR} ^{Note 2}	-4.4	A
Channel dissipation	P _{ch (pulse)} ^{Note 2}	2.0	W
Channel dissipation	P _{ch (continuous)} ^{Note 3}	1.05	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. When using the alumina ceramic board (50 × 50 × 0.7 mm), PW ≤ 5 s, Ta = 25°C

3. When using the alumina ceramic board (50 × 50 × 0.7 mm), Ta = 25°C

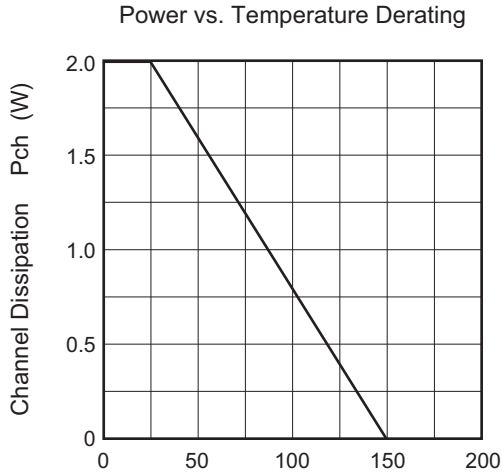
Electrical Characteristics

(Ta = 25°C)

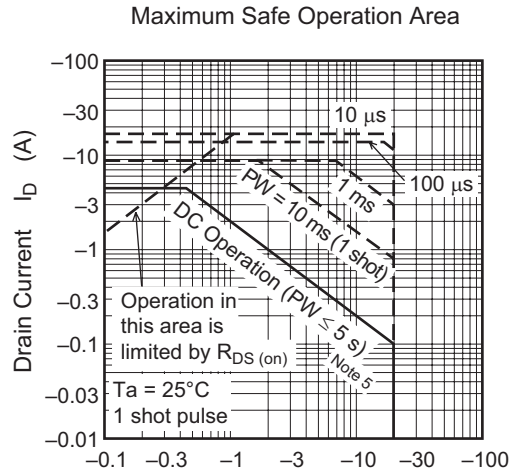
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	V _{(BR) DSS}	-20	—	—	V	I _D = -10 mA, V _{GS} = 0
Gate to source leak current	I _{GSS}	—	—	±0.1	μA	V _{GS} = ±12 V, V _{DS} = 0
Zero gate voltage drain current	I _{DSS}	—	—	-1	μA	V _{DS} = -20 V, V _{GS} = 0
Gate to source cutoff voltage	V _{GS (off)}	-0.4	—	-1.4	V	I _D = -1 mA, V _{DS} = -10 V
Static drain to source on state resistance	R _{DS (on)}	—	55	65	mΩ	I _D = -3 A, V _{GS} = -4.5 V ^{Note 4}
	R _{DS (on)}	—	85	110	mΩ	I _D = -3 A, V _{GS} = -2.5 V ^{Note 4}
Forward transfer admittance	y _{fs}	4	7	—	S	I _D = -3 A, V _{DS} = -10 V ^{Note 4}
Input capacitance	C _{iss}	—	750	—	pF	V _{DS} = -10 V
Output capacitance	C _{oss}	—	310	—	pF	V _{GS} = 0
Reverse transfer capacitance	C _{rss}	—	220	—	pF	f = 1 MHz
Total gate charge	Q _g	—	11	—	nC	V _{DD} = -10 V
Gate to source charge	Q _{gs}	—	2	—	nC	V _{GS} = -4.5 V
Gate to drain charge	Q _{gd}	—	3.5	—	nC	I _D = -4.4 A
Turn-on delay time	t _{d (on)}	—	15	—	ns	V _{GS} = -4.5 V, I _D = -3 A, R _L = 3.3 Ω
Rise time	t _r	—	100	—	ns	
Turn-off delay time	t _{d (off)}	—	85	—	ns	
Fall time	t _f	—	100	—	ns	
Body-drain diode forward voltage	V _{DF}	—	-0.95	-1.23	V	I _F = -4.4 A, V _{GS} = 0
Body-drain diode reverse recovery time	t _{rr}	—	50	—	ns	I _F = -4.4 A, V _{GS} = 0 di _F /dt = -20 A/μs

Note: 4. Pulse test

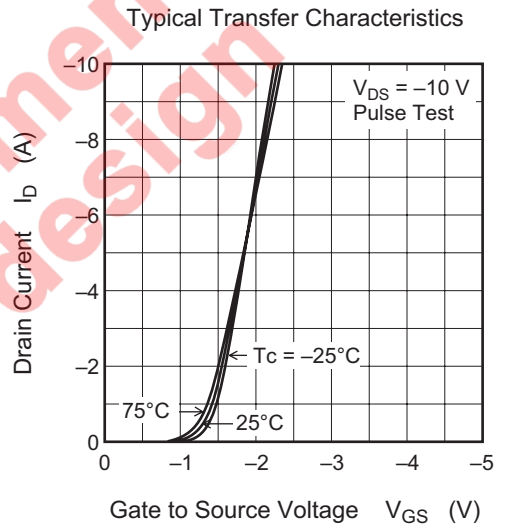
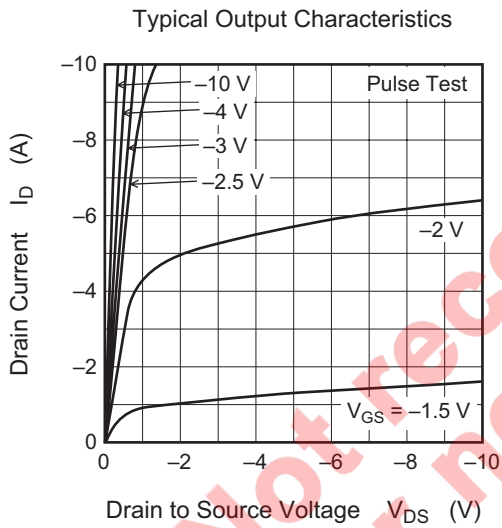
Main Characteristics



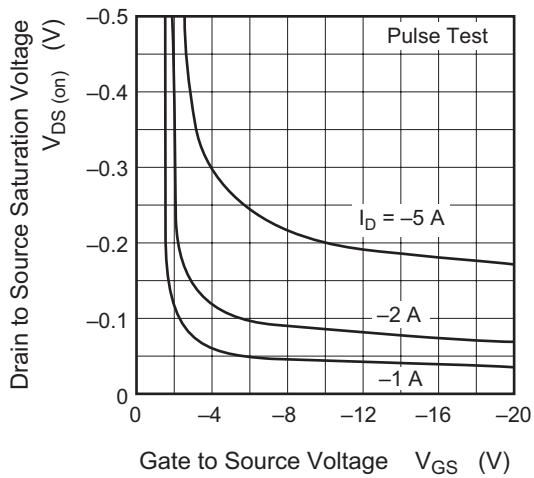
Test Condition:
When using the alumina ceramic board
(50 × 50 × 0.7 mm), (PW ≤ 5 s)



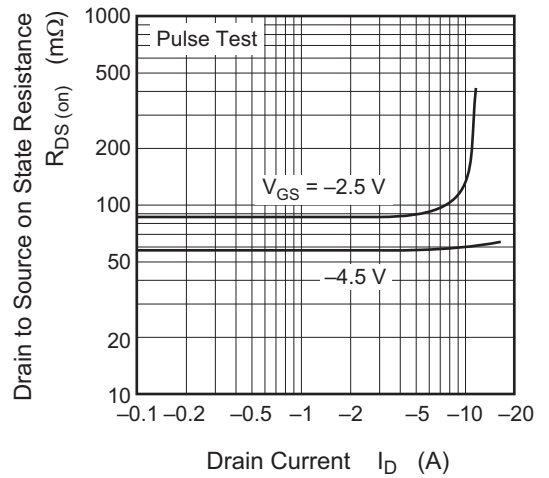
Note 5:
When using the alumina ceramic board
(50 × 50 × 0.7 mm)

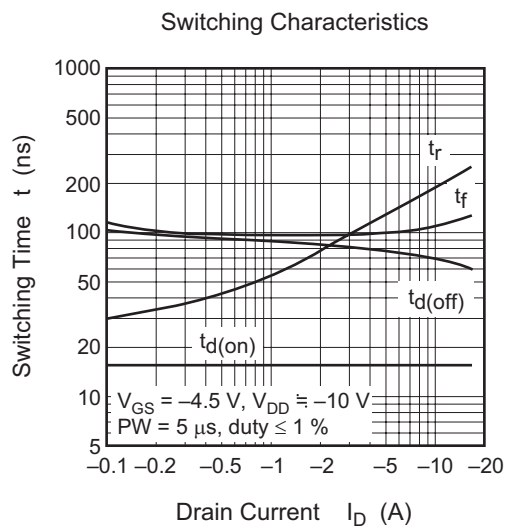
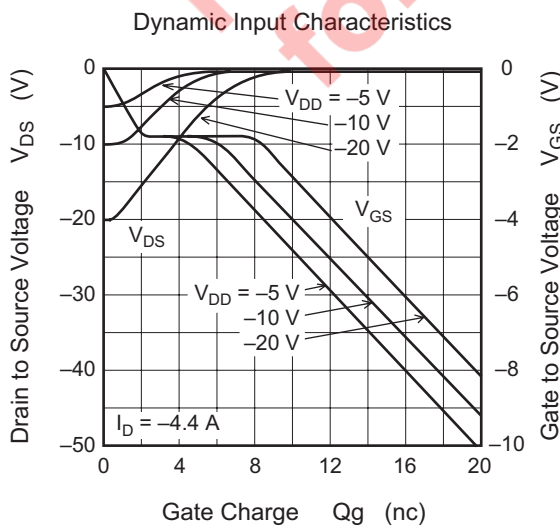
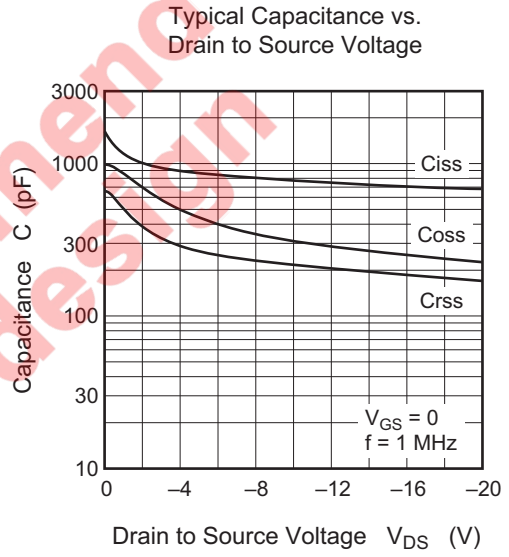
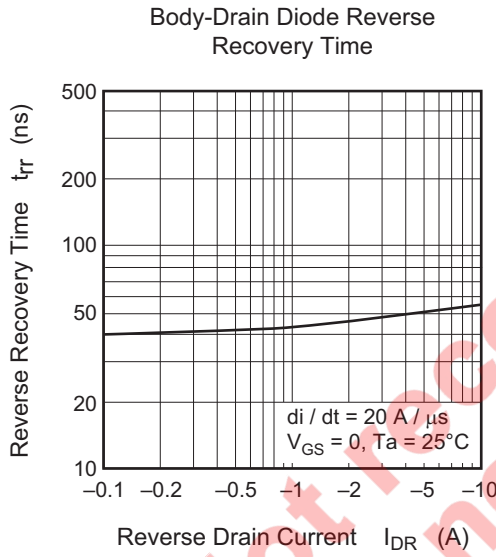
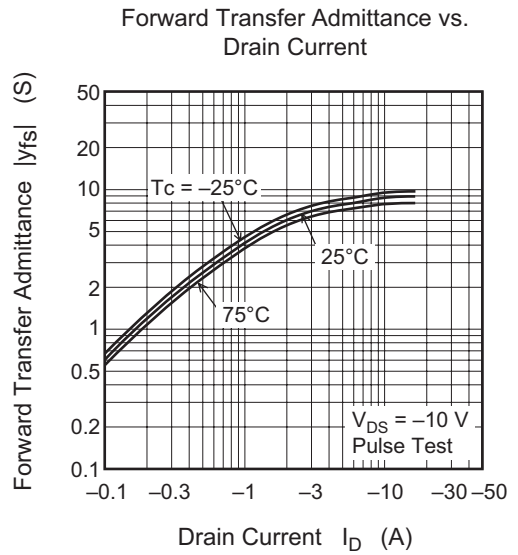
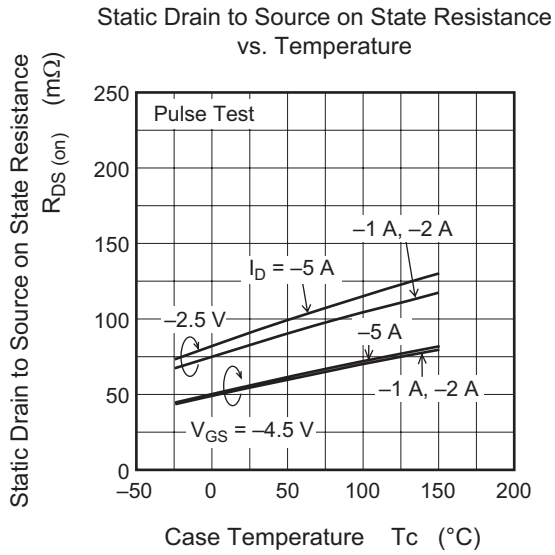


Drain to Source Saturation Voltage vs. Gate to Source Voltage

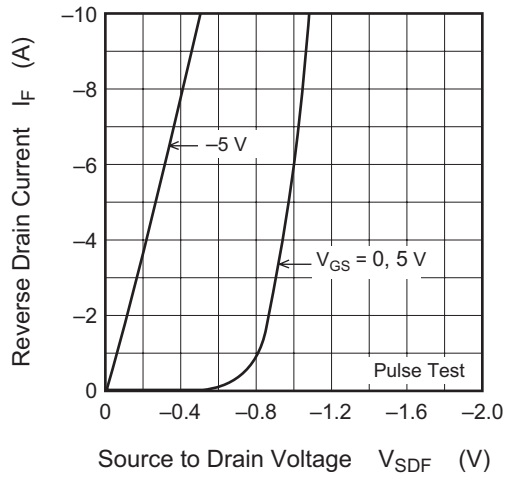


Static Drain to Source on State Resistance vs. Drain Current

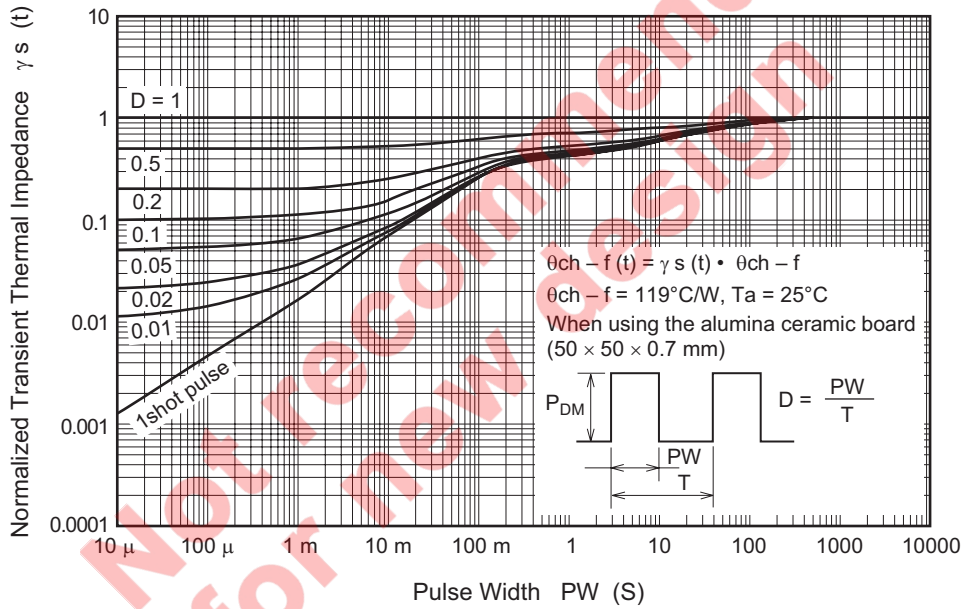




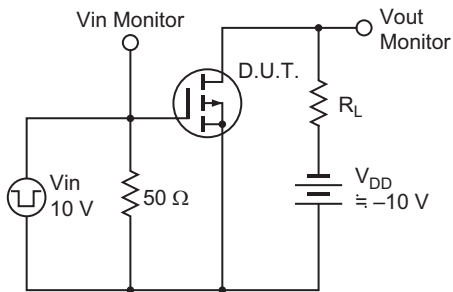
Reverse Drain Current vs. Source to Drain Voltage



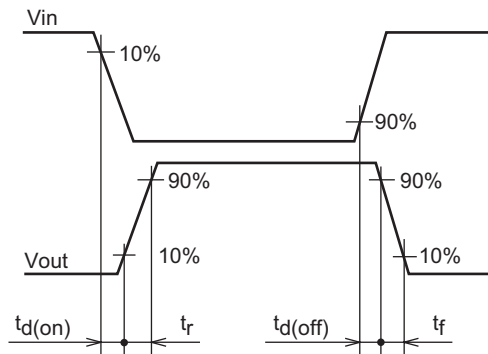
Normalized Transient Thermal Impedance vs. Pulse Width



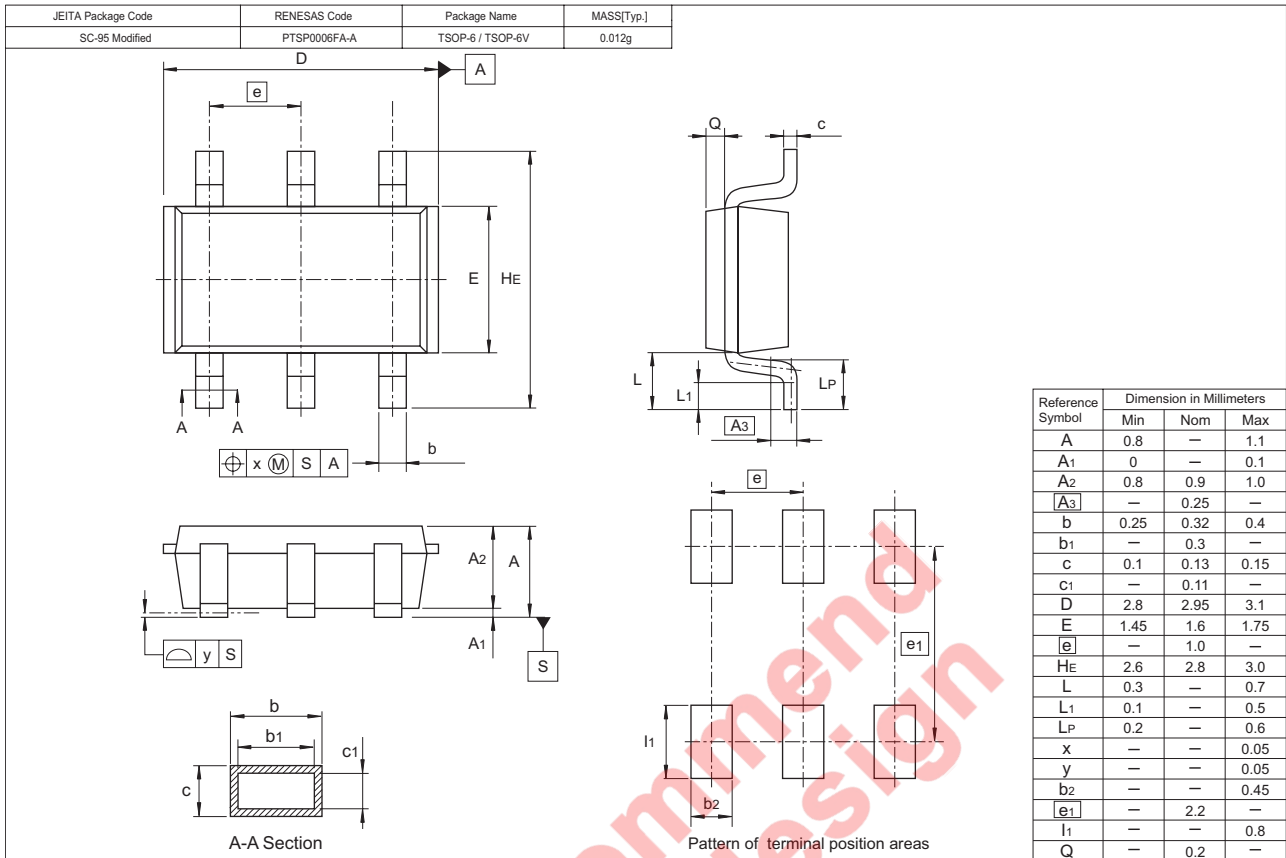
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAT1043M-EL-E	3000 pcs	Taping

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