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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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HAF1001

Silicon P Channel MOS FET Series Power Switching

REJ03G1132-0400
(Previous: ADE-208-583A)
Rev.4.00
Apr 27, 2006

Description

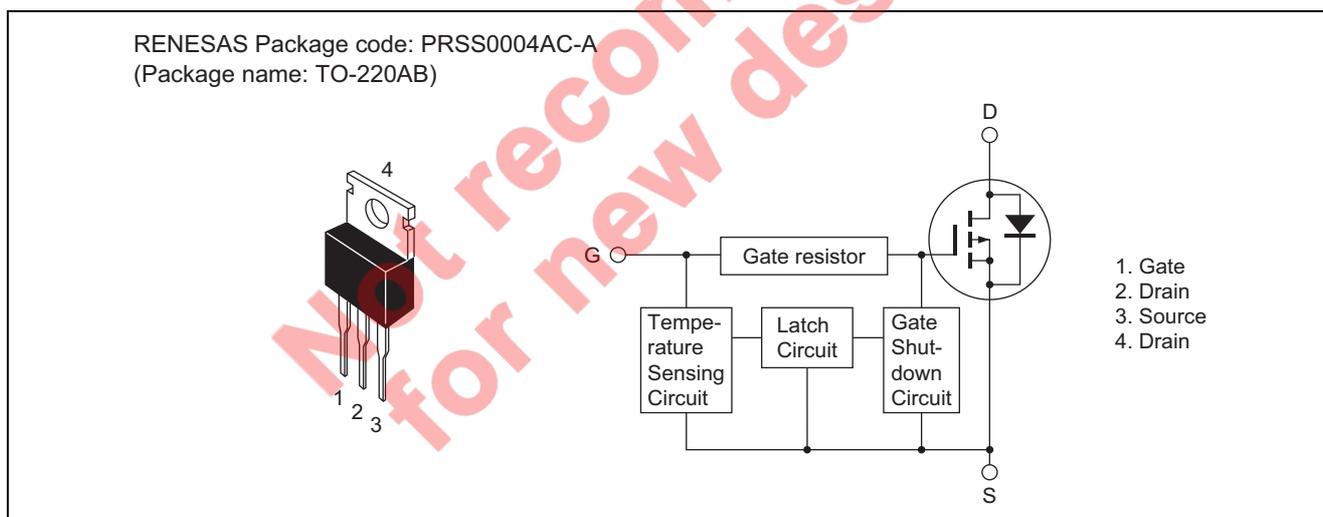
This FET has the over temperature shut-down capability sensing to the junction temperature.

This FET has the built-in over temperature shut-down circuit in the gate area. And this circuit operation to shut-down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

Features

- Logic level operation (-4 to -6 V Gate drive)
- High endurance capability against to the short circuit
- Built-in the over temperature shut-down circuit
- Latch type shut-down operation (Need 0 voltage recovery)

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	-60	V
Gate to source voltage	V _{GSS}	-16	V
	V _{GSS}	3	V
Drain current	I _D	-15	A
Drain peak current	I _{D (pulse)} ^{Note 1}	-30	A
Body-drain diode reverse drain current	I _{DR}	-15	A
Channel dissipation	P _{ch} ^{Note 2}	50	W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%

2. Value at Tc = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V _{IH}	-3.5	—	—	V	
	V _{IL}	—	—	-1.2	V	
Input current (Gate non shut down)	I _{IH1}	—	—	-100	μA	V _i = -8 V, V _{DS} = 0
	I _{IH2}	—	—	-50	μA	V _i = -3.5 V, V _{DS} = 0
	I _{IL}	—	—	-1	μA	V _i = -1.2 V, V _{DS} = 0
Input current (Gate shut down)	I _{IH (sd) 1}	—	-0.8	—	mA	V _i = -8 V, V _{DS} = 0
	I _{IH (sd) 2}	—	-0.35	—	mA	V _i = -3.5 V, V _{DS} = 0
Shut down temperature	T _{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V _{OP}	-3.5	—	-13	V	

Not recommended
for new designs

Electrical Characteristics

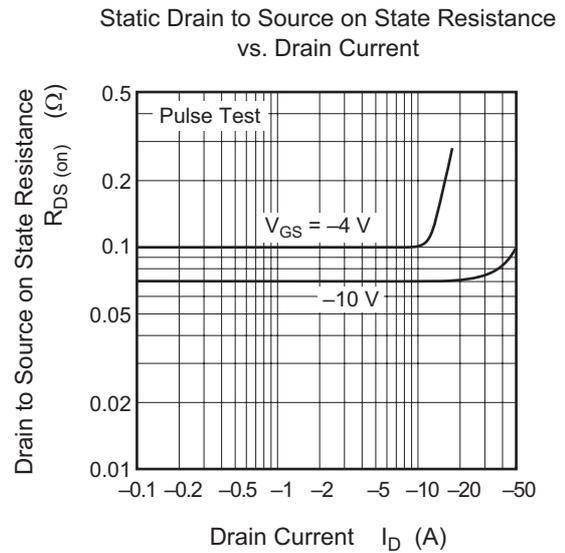
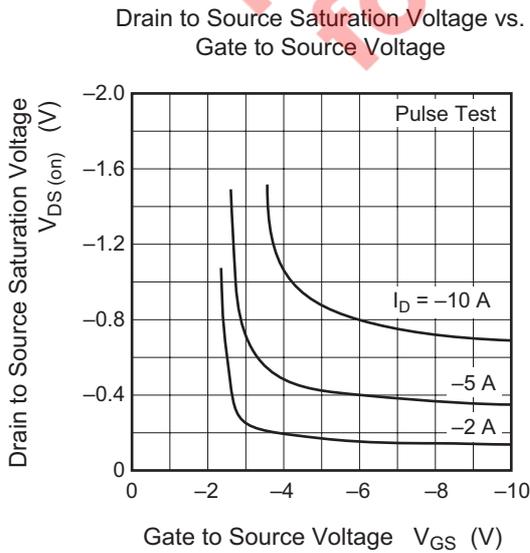
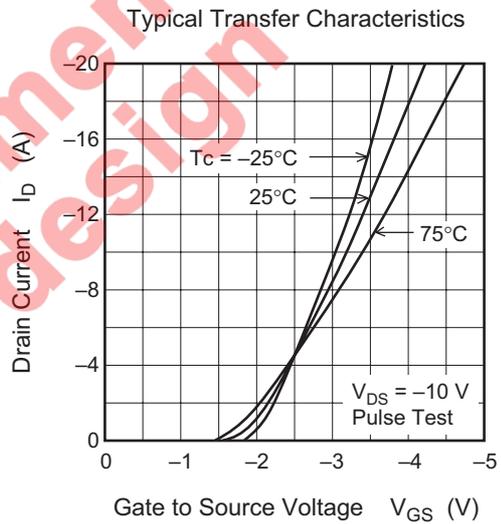
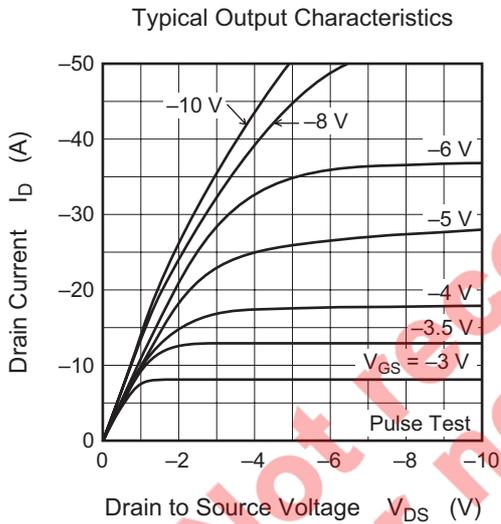
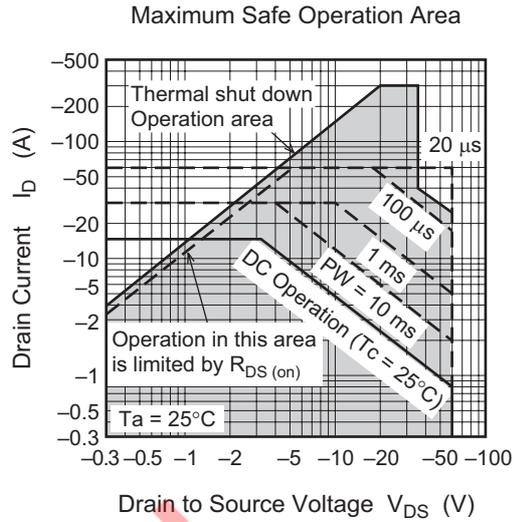
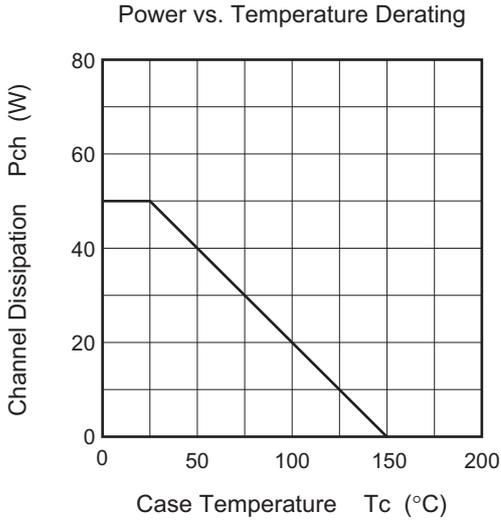
(Ta = 25°C)

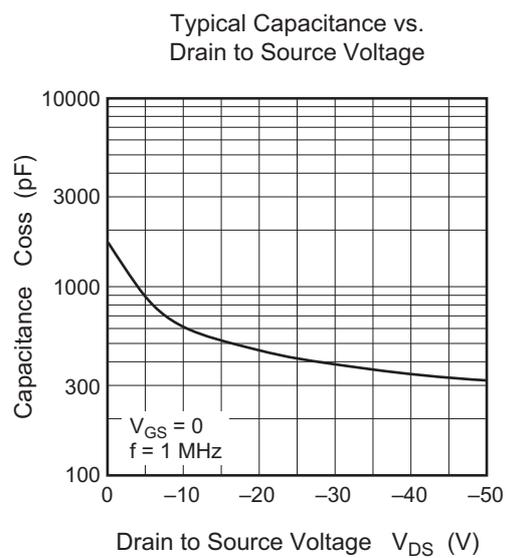
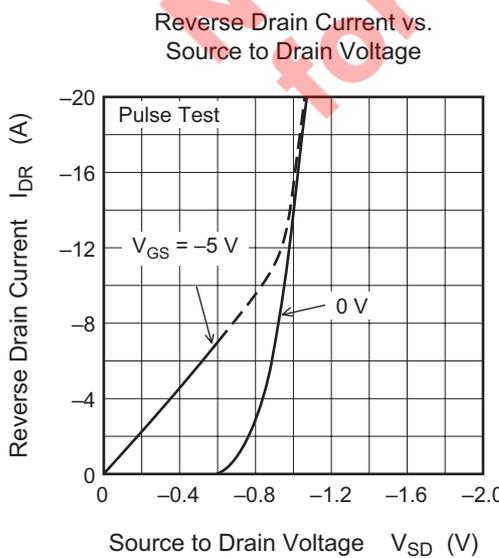
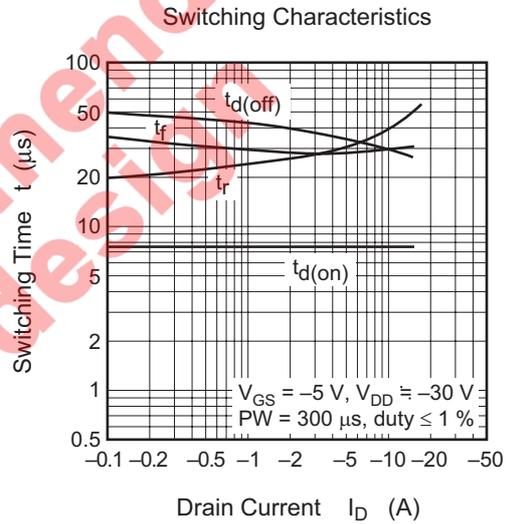
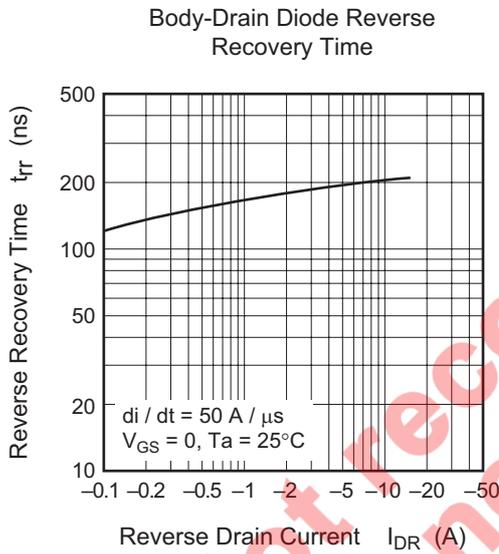
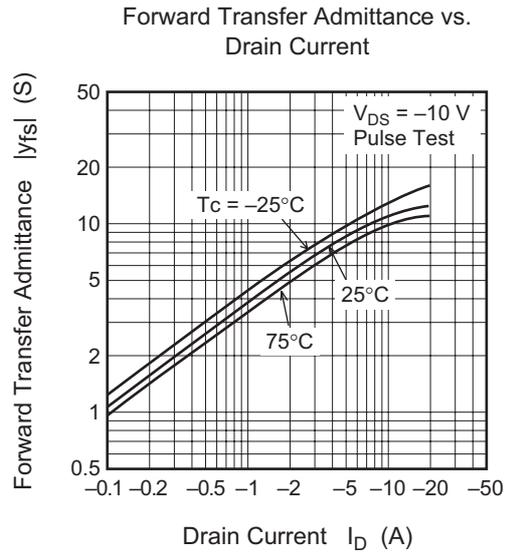
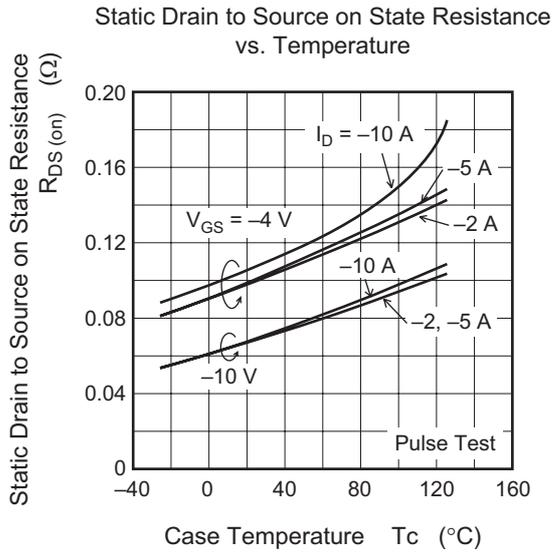
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	-7	—	—	A	$V_{GS} = -3.5\text{ V}, V_{DS} = -2\text{ V}$
	I_{D2}	—	—	-10	mA	$V_{GS} = -1.2\text{ V}, V_{DS} = -2\text{ V}$
Drain to source breakdown voltage	$V_{(BR)DSS}$	-60	—	—	V	$I_D = -10\text{ mA}, V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	-16	—	—	V	$I_G = -100\text{ }\mu\text{A}, V_{DS} = 0$
	$V_{(BR)GSS}$	3	—	—	V	$I_G = 100\text{ }\mu\text{A}, V_{DS} = 0$
Gate to source leak current	I_{GSS1}	—	—	-100	μA	$V_{GS} = -8\text{ V}, V_{DS} = 0$
	I_{GSS2}	—	—	-50	μA	$V_{GS} = -3.5\text{ V}, V_{DS} = 0$
	I_{GSS3}	—	—	-1	μA	$V_{GS} = -1.2\text{ V}, V_{DS} = 0$
	I_{GSS4}	—	—	100	μA	$V_{GS} = 2.4\text{ V}, V_{DS} = 0$
Input current (shut down)	$I_{GS(op)1}$	—	-0.8	—	mA	$V_{GS} = -8\text{ V}, V_{DS} = 0$
	$I_{GS(op)2}$	—	-0.35	—	mA	$V_{GS} = -3.5\text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	-250	μA	$V_{DS} = -50\text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	-1.1	—	-2.25	V	$I_D = -1\text{ mA}, V_{DS} = -10\text{ V}$
Static drain to source on state resistance	$R_{DS(on)}$	—	100	130	m Ω	$I_D = -7.5\text{ A}, V_{GS} = -4\text{ V}$ ^{Note 3}
	$R_{DS(on)}$	—	70	90	m Ω	$I_D = -7.5\text{ A}, V_{GS} = -10\text{ V}$ ^{Note 3}
Forward transfer admittance	$ y_{fs} $	5	10	—	S	$I_D = -7.5\text{ A}, V_{DS} = -10\text{ V}$ ^{Note 3}
Output capacitance	C_{oss}	—	610	—	pF	$V_{DS} = -10\text{ V}, V_{GS} = 0$ $f = 1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	7.5	—	μs	$I_D = -7.5\text{ A}$
Rise time	t_r	—	36	—	μs	$V_{GS} = -5\text{ V}$
Turn-off delay time	$t_{d(off)}$	—	32	—	μs	$R_L = 4\text{ }\Omega$
Fall time	t_f	—	29	—	μs	
Body-drain diode forward voltage	V_{DF}	—	-1.0	—	V	$I_F = -15\text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	200	—	ns	$I_F = -15\text{ A}, V_{GS} = 0$ $di_F/dt = 50\text{ A}/\mu\text{s}$
Over load shut down operation time ^{Note4}	t_{os1}	—	3.7	—	ms	$V_{GS} = -5\text{ V}, V_{DD} = -12\text{ V}$
	t_{os2}	—	1	—	ms	$V_{GS} = -5\text{ V}, V_{DD} = -24\text{ V}$

Notes: 3. Pulse test

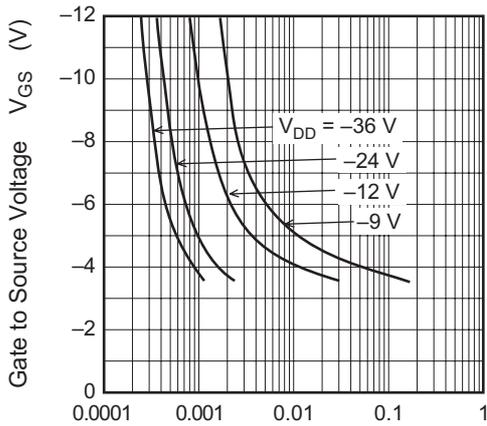
4. Include the time shift based on increasing of channel temperature when operate under over load condition.

Main Characteristics



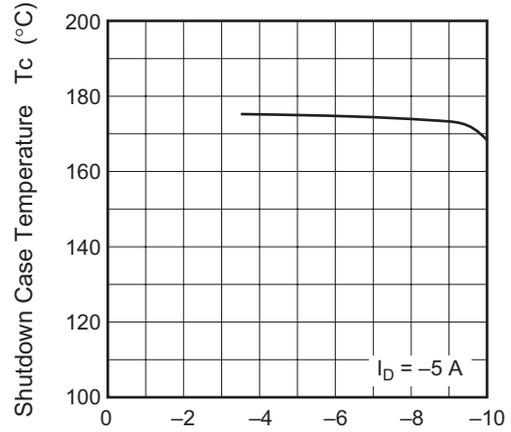


Gate to Source Voltage vs. Shutdown Time of Load-Short Test



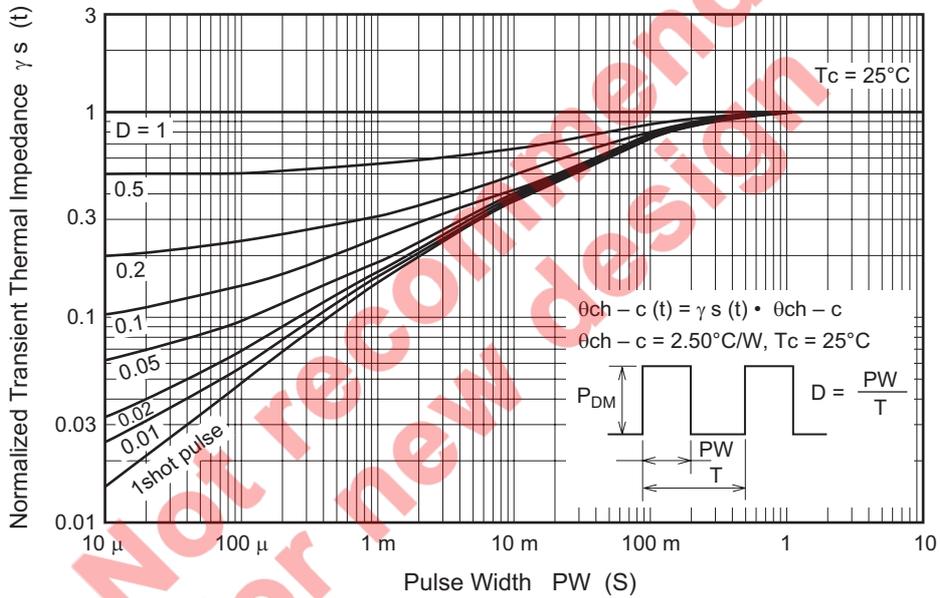
Shutdown Time of Load-Short Test PW (S)

Shutdown Case Temperature vs. Gate to Source Voltage

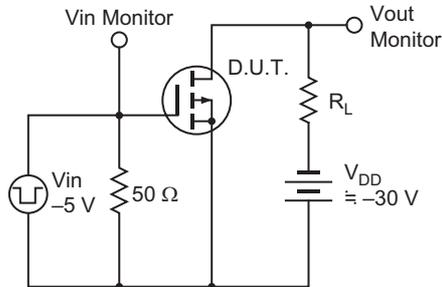


Gate to Source Voltage V_{GS} (V)

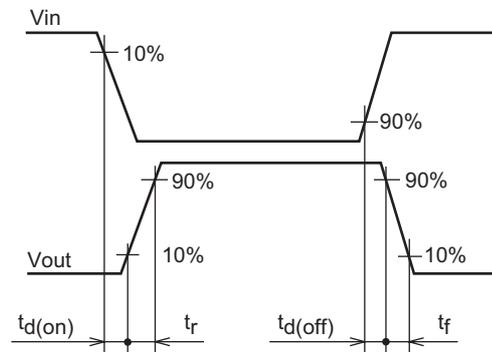
Normalized Transient Thermal Impedance vs. Pulse Width



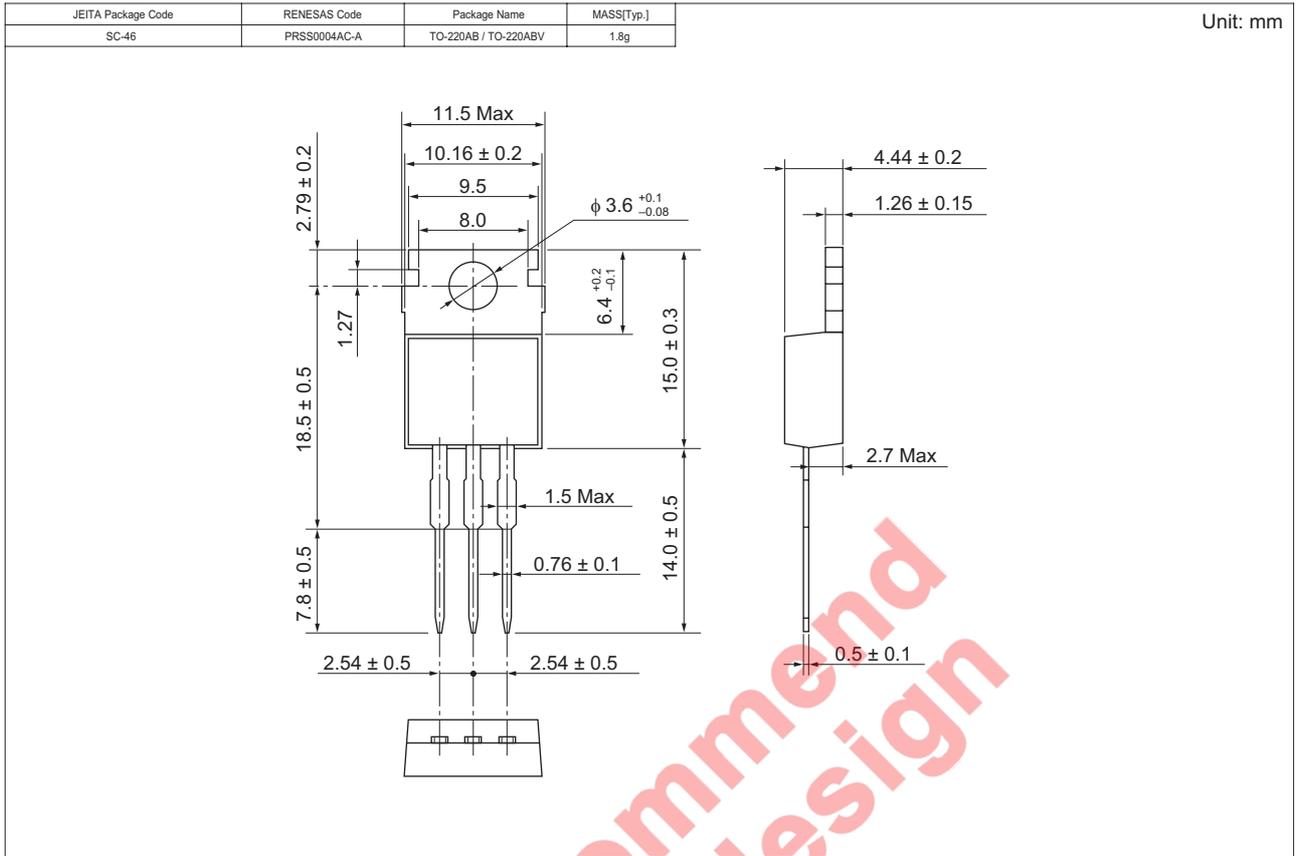
Switching Time Test Circuit



Waveform



Package Dimensions



Ordering Information

Part Name	Quantity	Shipping Container
HAF1001-90	Max: 50 pcs/sack	Sack

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