HA-5033

250MHz Video Buffer

FN2924
Rev 8.00
February 6, 2006

The HA-5033 is a unity gain monolithic IC designed for any application requiring a fast, wideband buffer. Featuring a bandwidth of 250MHz and outstanding differential phase/ gain characteristics, this high performance voltage follower is an excellent choice for video circuit design. Other features, which include a minimum slew rate of 1000V/µs and high output drive capability, make the HA-5033 applicable for line driver and high speed data conversion circuits.

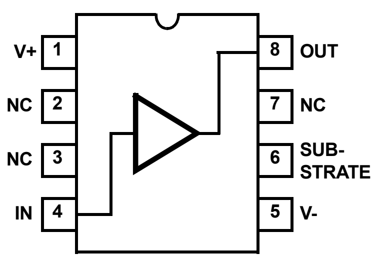
The high performance of this product is a result of the Intersil Dielectric Isolation process. A major feature of this process is that it produces both PNP and NPN high frequency transistors which makes wide bandwidth designs, such as the HA-5033, practical. Alternative process methods typically produce a lower AC performance.

Ordering Information

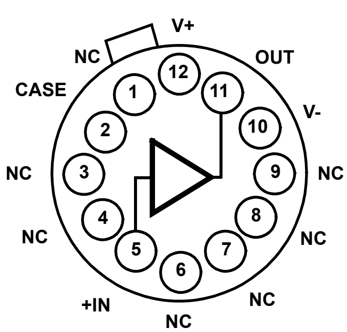
PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA2-5033-2	HA2-5033-2	-55 to 125	12 Pin Metal Can	T12.C
HA3-5033-5	HA3-5033-5	0 to 75	8 Ld PDIP	E8.3

Pinouts

HA-5033 (PDIP)
TOP VIEW



HA-5033 (METAL CAN)
TOP VIEW



Features

- Differential Phase Error . . . . 0.02 Degrees
- Differential Gain Error 0.03%
- High Slew Rate 1100V/µs
- Wide Bandwidth (Small Signal) 250MHz
- Wide Power Bandwidth . . . . DC to 17.5MHz
- Fast Rise Time 3ns
- High Output Drive. . . . . ±10V With 100Ω Load
- Wide Power Supply Range . . . . ±5V to ±16V
- Replace Costly Hybrids

Applications

- Video Buffer
- High Frequency Buffer
- Isolation Buffer
- High Speed Line Driver
- Impedance Matching
- Current Boosters
- High Speed A/D Input Buffers
- Related Literature
  - AN548, Designer's Guide for HA-5033

Absolute Maximum Ratings

Voltage Between V+ and V- Pins. 40V
DC Input Voltage . . . . V+ to V-
Output Current (Peak) (50ms On/1 Second Off) . . . . ±200mA
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) 2000V

Operating Conditions

Temperature Ranges (Note 3)
HA-5033-2 . . . . -55°C to 125°C
HA-5033-5 . . . . 0°C to 75°C

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
Metal Can Package	65	34
PDIP Package	120	N/A

Maximum Junction Temperature (Note 1) . . . . 175°C
Maximum Junction Temperature (Plastic Packages) . . . . 150°C
Maximum Storage Temperature Range . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . 300°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including load conditions, must be designed to maintain the maximum junction temperature below 175°C for the metal can package, and below 150°C for the plastic packages (See Figure 5.).
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. The maximum operating temperature may have to be derated depending on the output load condition. See Figure 5 for more information.

Electrical Specifications

V_{SUPPLY} = ±12V, R_S = 50Ω, R_L = 100Ω, C_L = 10pF, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5033-2			HA-5033-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS									
Offset Voltage		25	-	5	15	-	5	15	mV
		Full	-	6	25	-	6	25	mV
Average Offset Voltage Drift		Full	-	33	-	-	33	-	μV/°C
Bias Current		25	-	20	35	-	20	35	μA
		Full	-	30	50	-	30	50	μA
Input Resistance		25	-	3	-	-	3	-	MΩ
Input Capacitance		25	-	1.6	-	-	1.6	-	pF
Input Noise Voltage	10Hz to 100MHz	25	-	20	-	-	20	-	μV_{P-P}
TRANSFER CHARACTERISTICS									
Voltage Gain	R_L = 100Ω	25	0.93	-	-	0.93	-	-	V/V
	R_L = 1kΩ	25	0.93	0.99	-	0.93	0.99	-	V/V
	R_L = 100Ω	Full	0.92	-	-	0.92	-	-	V/V
-3dB Bandwidth		25	-	250	-	-	250	-	MHz
OUTPUT CHARACTERISTICS									
Output Voltage Swing	R_L = 100Ω	Full	±8	±10	-	±8	±10	-	V
	R_L = 1kΩ, V_S = ±15V	Full	±11	±12	-	±11	±12	-	V
Output Current		25	±80	±100	-	±80	±100	-	mA
Output Resistance		25	-	8	-	-	8	-	Ω
Full Power Bandwidth	V_{OUT} = $1V_{RMS}$, R_L = 1kΩ	25	-	146	-	-	146	-	MHz
Full Power Bandwidth (Note 4)		25	15.9	17.5	-	15.9	17.5	-	MHz
TRANSIENT RESPONSE									
Rise Time	V_{OUT} = 500mV	25	-	4.6	-	-	4.6	-	ns
Propagation Delay		25	-	1	-	-	1	-	ns

Electrical Specifications V_{SUPPLY} = ±12V, R_S = 50Ω, R_L = 100Ω, C_L = 10pF, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (°C)	HA-5033-2			HA-5033-5			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Overshoot		25	-	3	-	-	3	-	%
Slew Rate (Note 4)		25	1	1.1	-	1	1.1	-	V/ns
Settling Time to 0.1%		25	-	50	-	-	50	-	ns
Differential Phase Error (Note 5)		25	-	0.02	-	-	0.02	-	Degree
Differential Gain Error (Note 5)		25	-	0.03	-	-	0.03	-	%
POWER SUPPLY CHARACTERISTICS									
Supply Current		25	-	21	25	-	21	25	mA
		Full	-	21	30	-	21	30	mA
Power Supply Rejection Ratio		Full	54	-	-	54	-	-	dB
Harmonic Distortion	V_{IN} = 1V_{RMS} at 100kHz	25	-	<0.1	-	-	<0.1	-	%

NOTES:

4. V_{SUPPLY} = ±15V, V_{OUT} = ±10V, R_L = 1kΩ.
5. Differential gain and phase error are nonlinear signal distortions found in video systems and are defined as follows: Differential gain error is defined as the change in amplitude at the color subcarrier frequency as the picture signal is varied from blanking to white level. Differential phase error is defined as the change in the phase of the color subcarrier as the picture signal is varied from blanking to white level. R_L = 300Ω.

Test Circuits and Waveforms

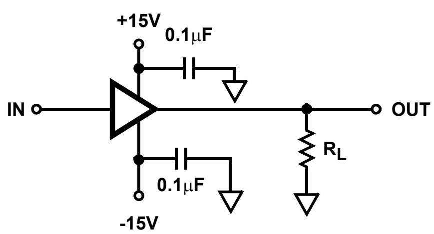


FIGURE 1. SLEW RATE AND SETTLING TIME

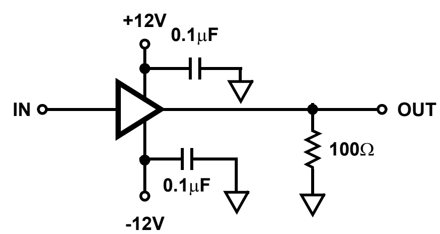


FIGURE 2. TRANSIENT RESPONSE

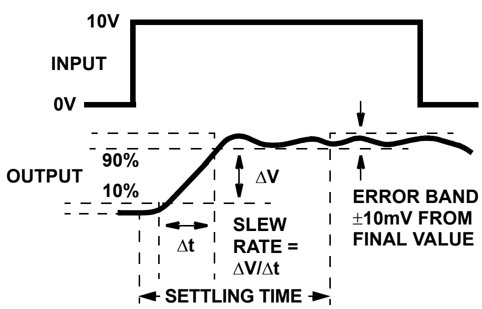


FIGURE 3. SETTLING TIME AND SLEW RATE

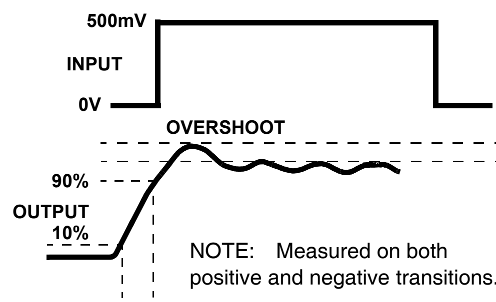
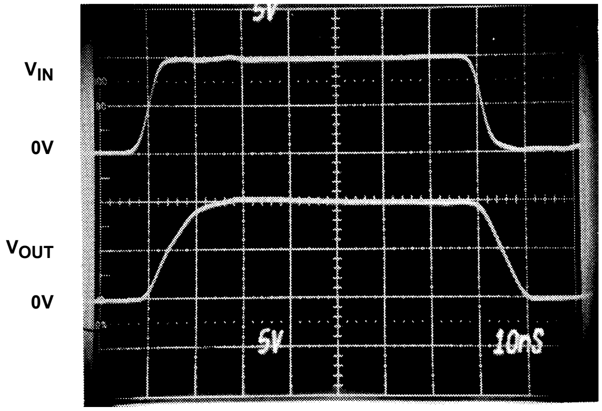


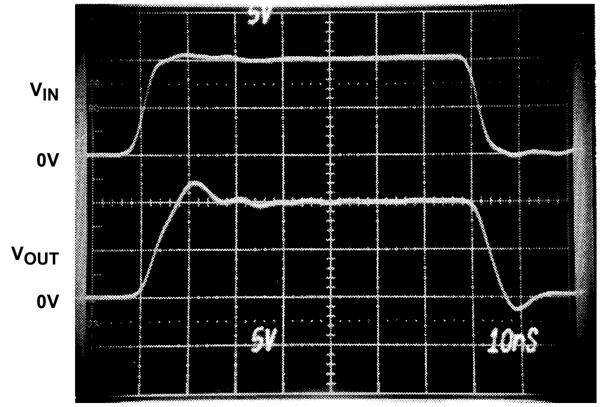
FIGURE 4. RISE TIME AND OVERSHOOT

Test Circuits and Waveforms (Continued)



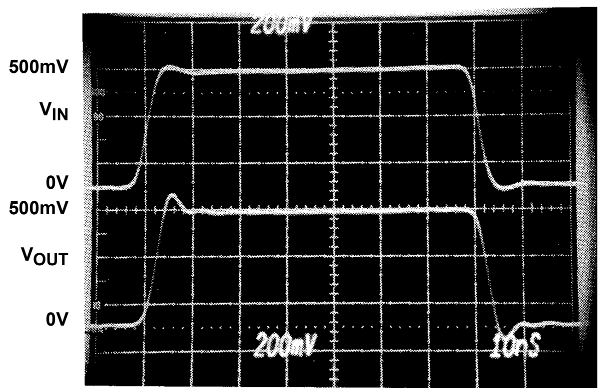
T_A = 25°C, R_S = 50Ω, R_L = 100Ω

+10V RESPONSE



T_A = 25°C, R_S = 50Ω, R_L = 1kΩ

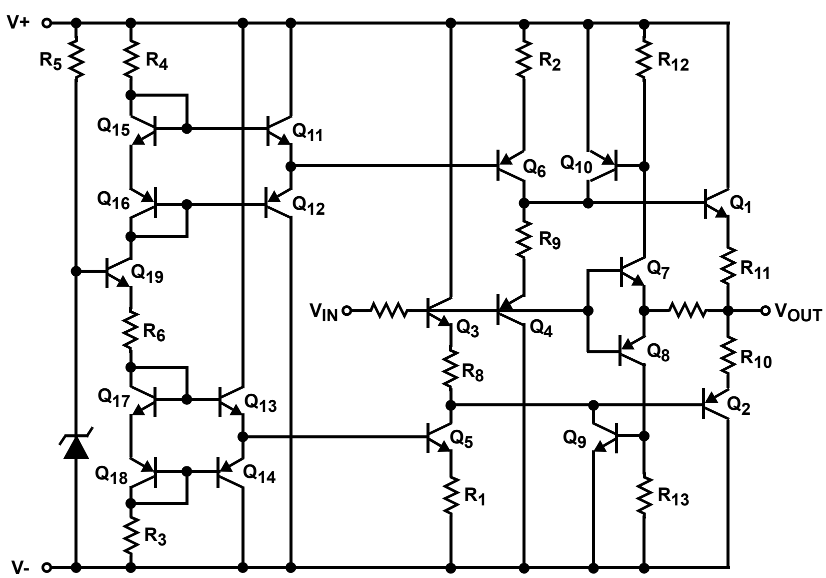
+10V RESPONSE



T_A = 25°C, R_S = 50Ω, R_L = 100Ω

PULSE RESPONSE

Schematic Diagram



Application Information

Layout Considerations

The wide bandwidth of the HA-5033 necessitates that high frequency circuit layout procedures be followed. Failure to follow these guidelines can result in marginal performance.

Probably the most crucial of the RF/video layout rules is the use of a ground plane. A ground plane provides isolation and minimizes distributed circuit capacitance and inductance which will degrade high frequency performance. IC sockets contribute inter-lead capacitance which limits device bandwidth and should be avoided.

Pin 6 can be tied to either supply, grounded, or simply not used. But to optimize device performance and improve isolation, it is recommended that this pin be grounded.

Other considerations are proper power supply bypassing and keeping the input and output connections as short as possible which minimizes distributed capacitance and reduces board space.

Power Supply Decoupling

For optimum device performance, it is recommended that the positive and negative power supplies be bypassed with capacitors to ground. Ceramic capacitors ranging in value from 0.01µF to 0.1µF will minimize high frequency variations in supply voltage. Solid tantalum capacitors 1µF or larger will optimize low frequency performance.

It is also recommended that the bypass capacitors be connected close to the HA-5033 (preferably directly to the supply pins).

Figure 5 is based on:

$$P_{DMAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

Where: T_{JMAX} = Maximum Junction Temperature of the Device
T_A = Ambient Temperature

θ_{JA} = Junction to Ambient Thermal Resistance

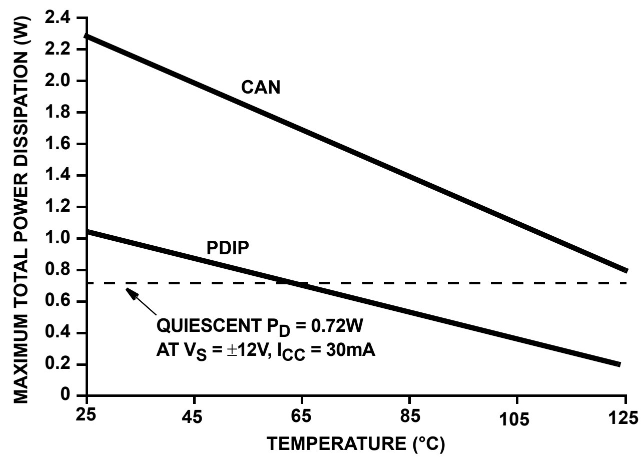


FIGURE 5. MAXIMUM POWER DISSIPATION vs TEMPERATURE

Typical Applications (Also see Application Note AN548)

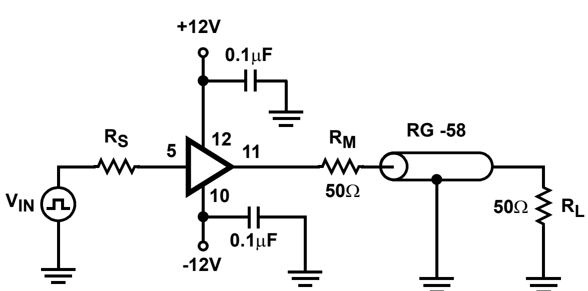


FIGURE 6. VIDEO COAXIAL LINE DRIVER 50Ω SYSTEM

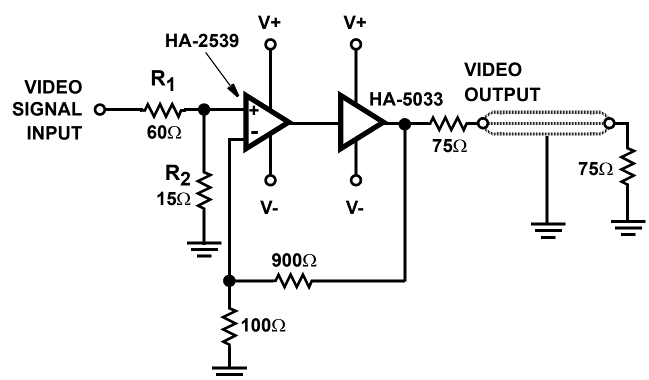
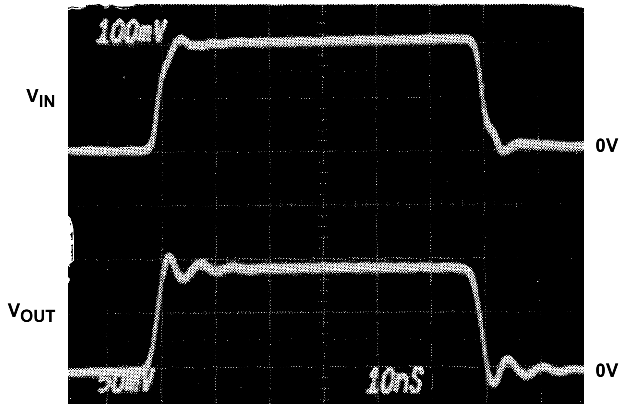


FIGURE 7. VIDEO GAIN BLOCK

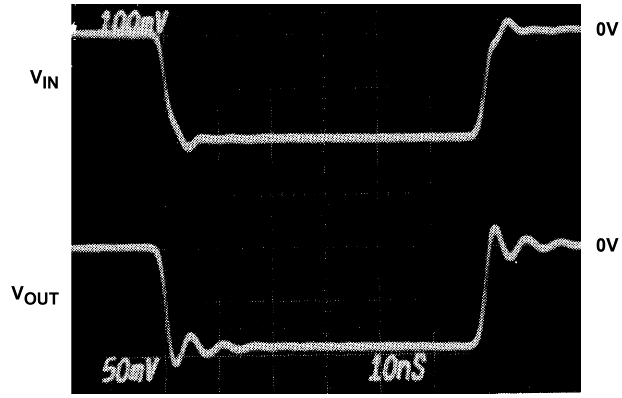
Typical Applications (Also see Application Note AN548) **(Continued)**



$T_A = 25°C, R_S = 50\Omega, R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left[\frac{R_L}{R_L + R_M}\right] = \left[\frac{1}{2}\right]V_{IN}$$

POSITIVE PULSE RESPONSE



$T_A = 25°C, R_S = 50\Omega, R_M = R_L = 50\Omega$

$$V_O = V_{IN}\left[\frac{R_L}{R_L + R_M}\right] = \left[\frac{1}{2}\right]V_{IN}$$

NEGATIVE PULSE RESPONSE

Typical Performance Curves

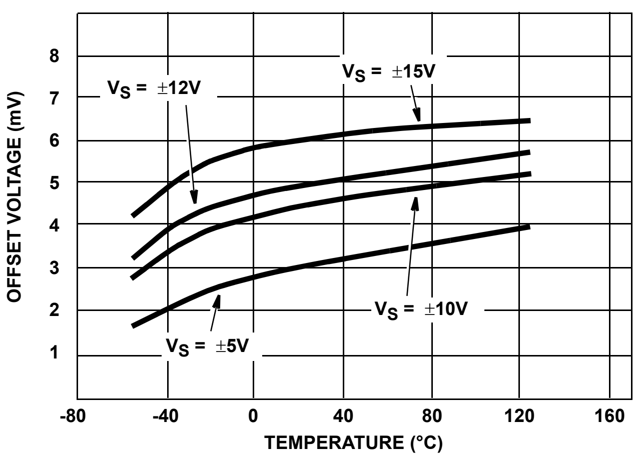


FIGURE 8. INPUT OFFSET VOLTAGE vs TEMPERATURE

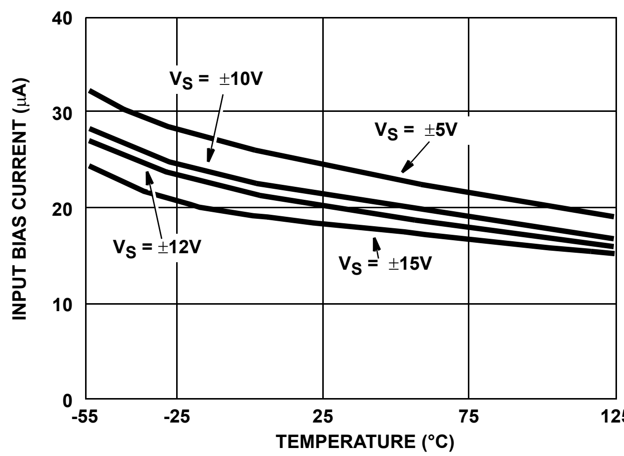


FIGURE 9. INPUT BIAS CURRENT vs TEMPERATURE

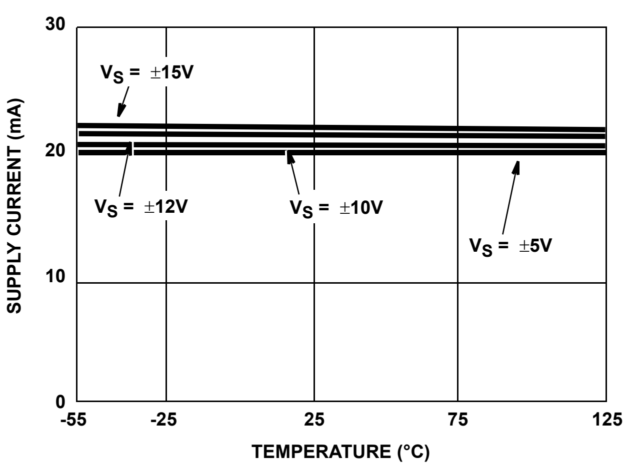


FIGURE 10. SUPPLY CURRENT vs TEMPERATURE

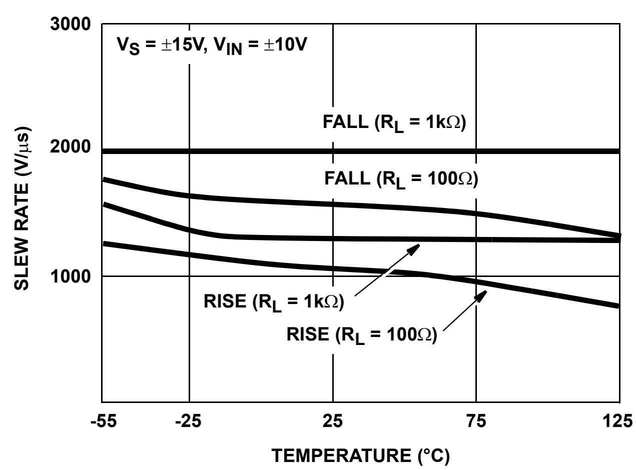


FIGURE 11. SLEW RATE vs TEMPERATURE

Typical Performance Curves (Continued)

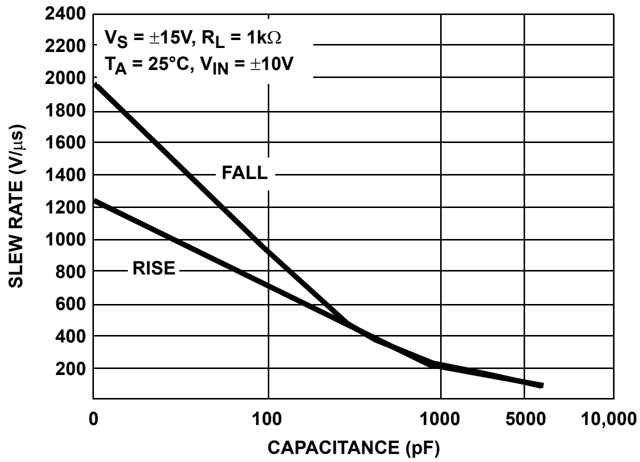


FIGURE 12. SLEW RATE vs LOAD CAPACITANCE

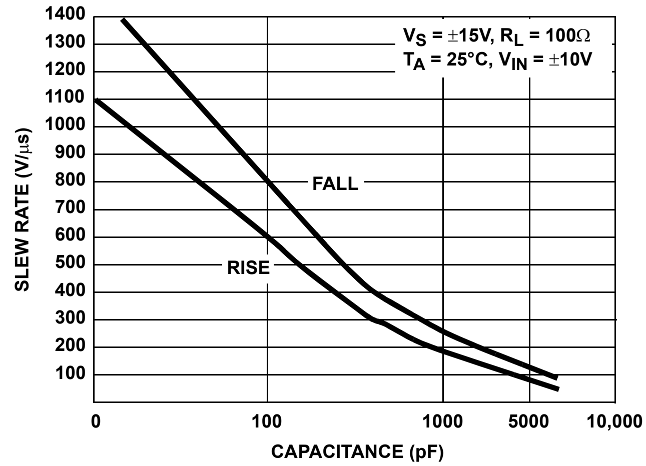


FIGURE 13. SLEW RATE vs LOAD CAPACITANCE

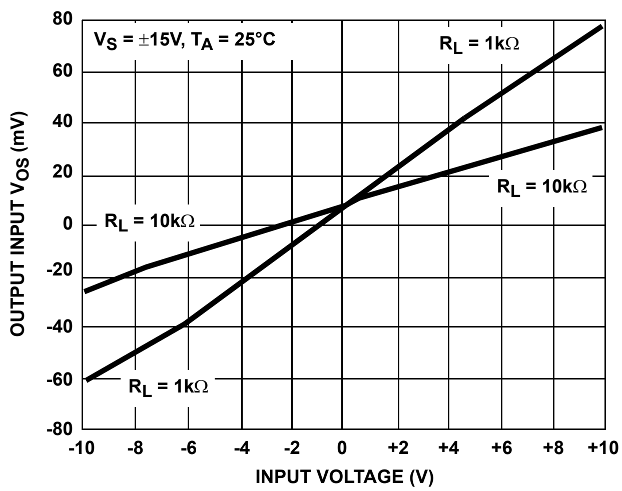


FIGURE 14. GAIN ERROR vs INPUT VOLTAGE

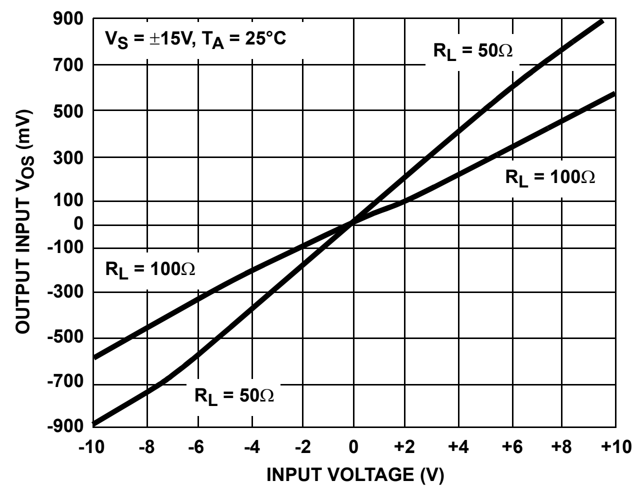


FIGURE 15. GAIN ERROR vs INPUT VOLTAGE

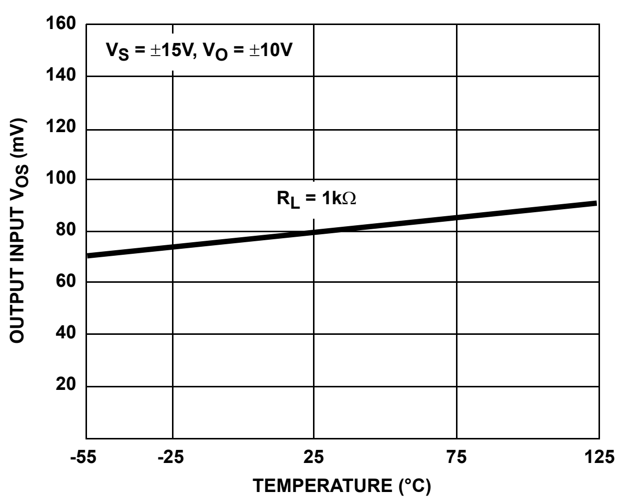


FIGURE 16. GAIN ERROR vs TEMPERATURE

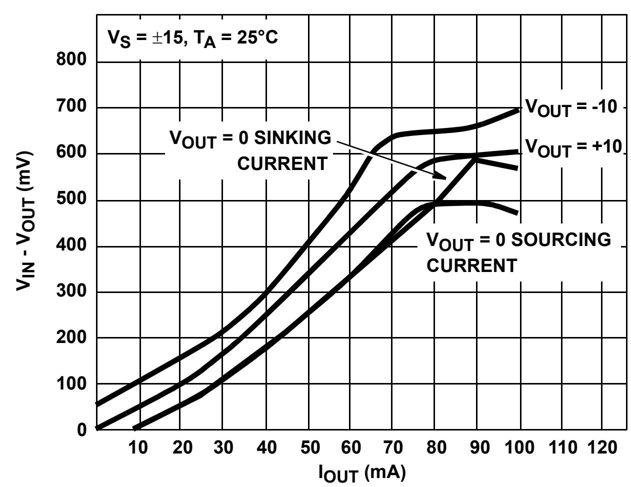


FIGURE 17. V_{IN} - V_{OUT} vs I_{OUT}

Typical Performance Curves (Continued)

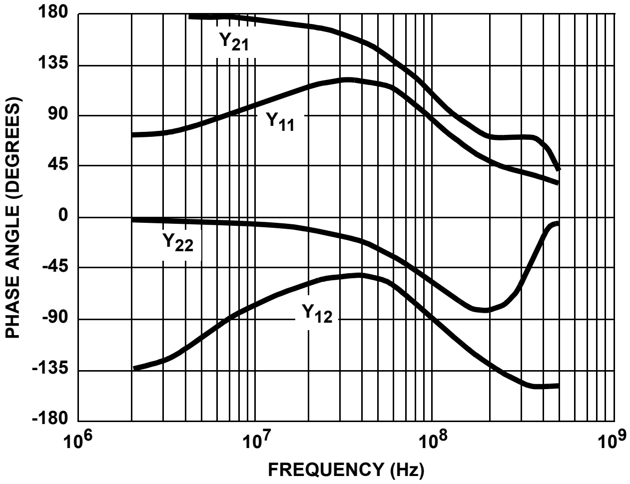


FIGURE 18. Y - PARAMETERS PHASE vs FREQUENCY

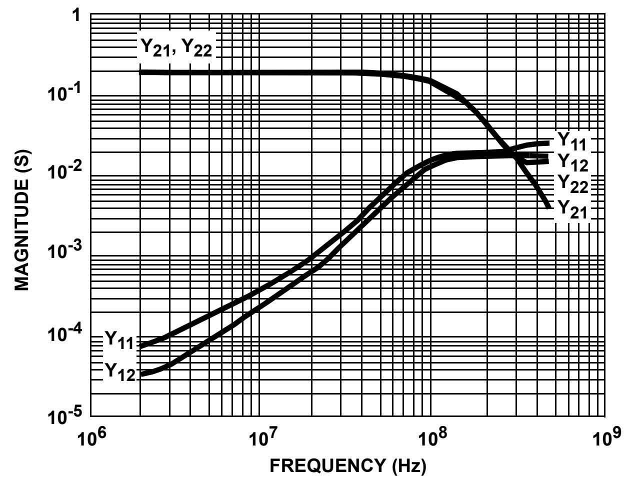


FIGURE 19. Y - PARAMETER MAGNITUDE vs FREQUENCY

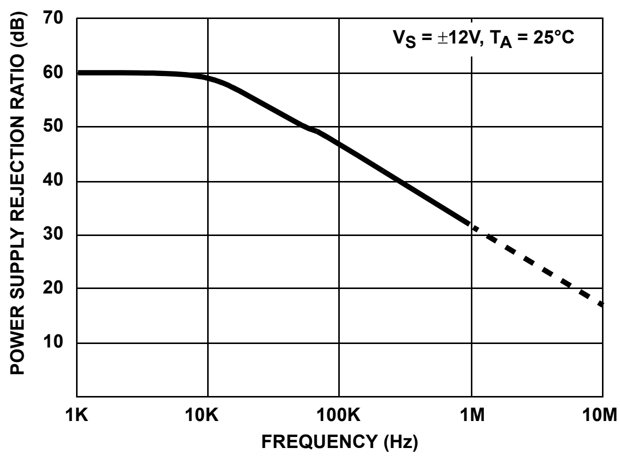


FIGURE 20. POWER SUPPLY REJECTION RATIO vs FREQUENCY

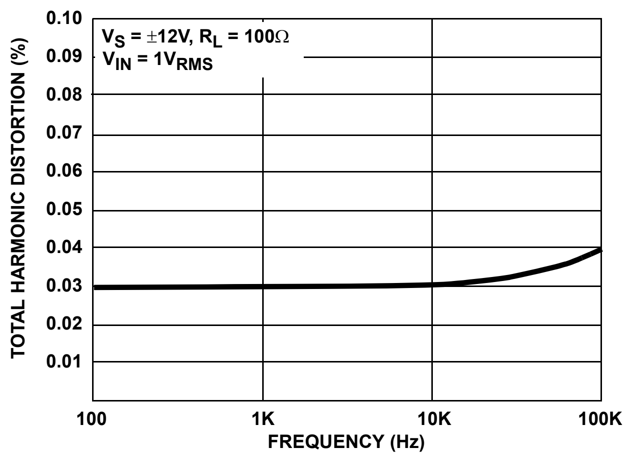


FIGURE 21. TOTAL HARMONIC DISTORTION vs FREQUENCY

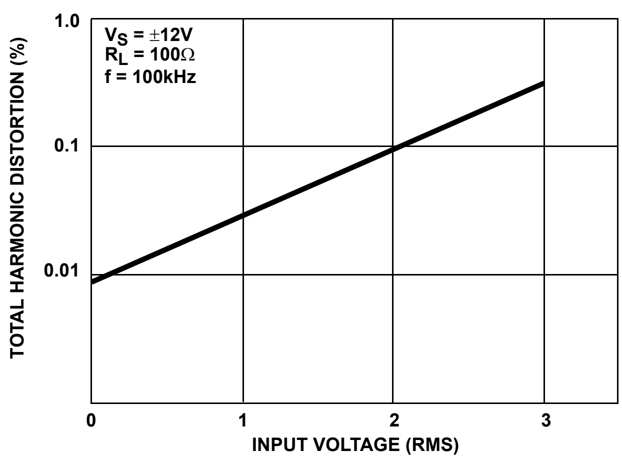


FIGURE 22. TOTAL HARMONIC DISTORTION vs INPUT VOLTAGE

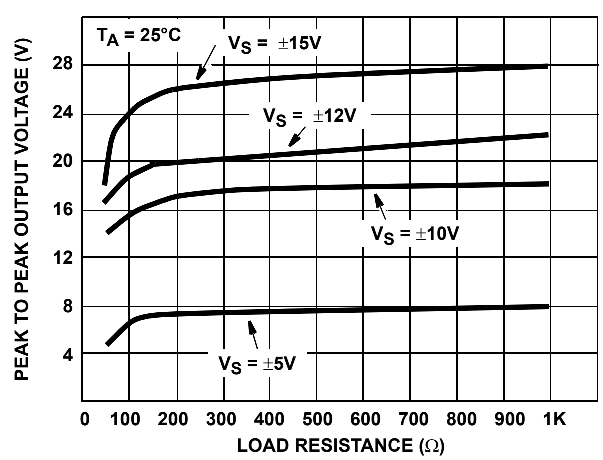


FIGURE 23. OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

Typical Performance Curves (Continued)

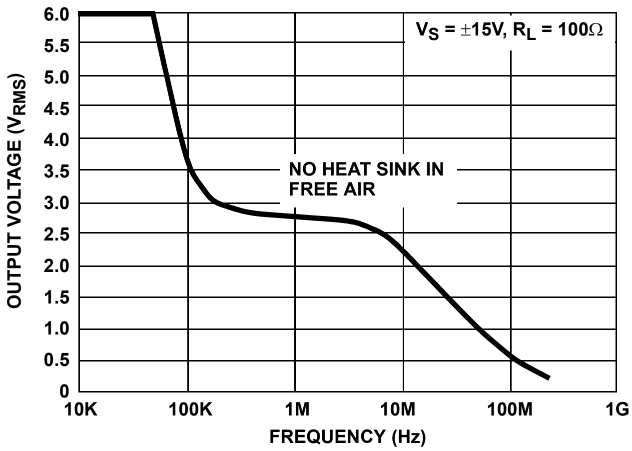


FIGURE 24. OUTPUT SWING vs FREQUENCY (NOTE)

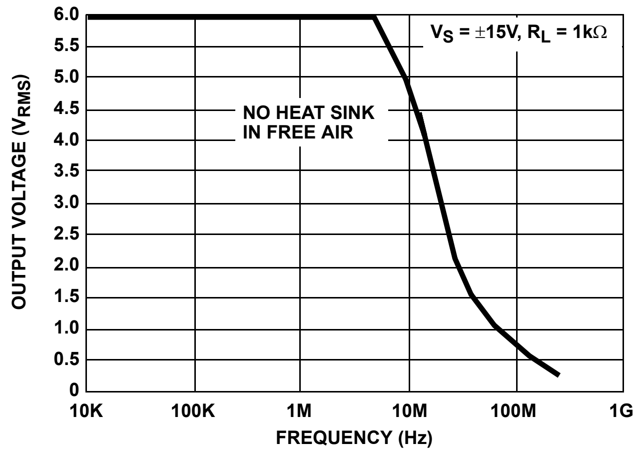


FIGURE 25. OUTPUT SWING vs FREQUENCY (NOTE)

NOTE:

This curve was obtained by noting the output voltage necessary to produce an observable distortion for a given frequency. If higher distortion is acceptable, then a higher output voltage for a given frequency can be obtained. However, operating the HA-5033 with increased distortion (to the right of curve shown), will also be accompanied by an increase in supply current. The resulting increase in chip temperature must be considered and heat sinking will be necessary to prevent thermal runaway. This characteristic is the result of the output transistor operation. If the signal amplitude or signal frequency or both are increased beyond the curve shown, the NPN, PNP output transistors will approach a condition of being simultaneously on. Under this condition, thermal runaway can occur.

Die Characteristics

SUBSTRATE POTENTIAL (POWERED UP):

Unbiased

TRANSISTOR COUNT:

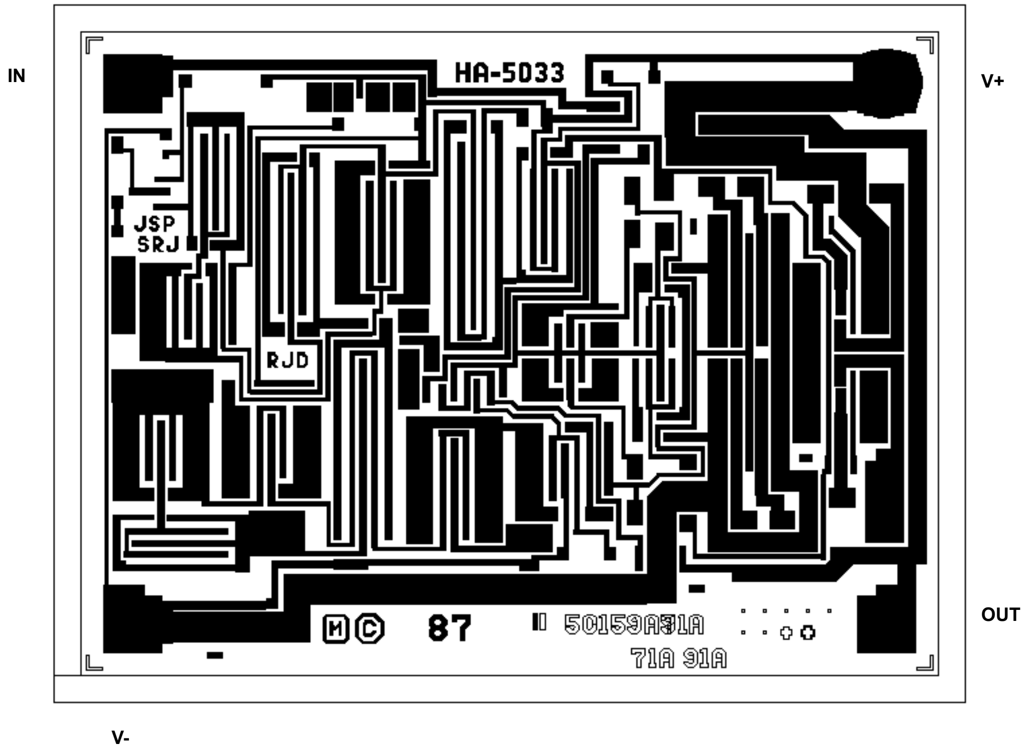
20

PROCESS:

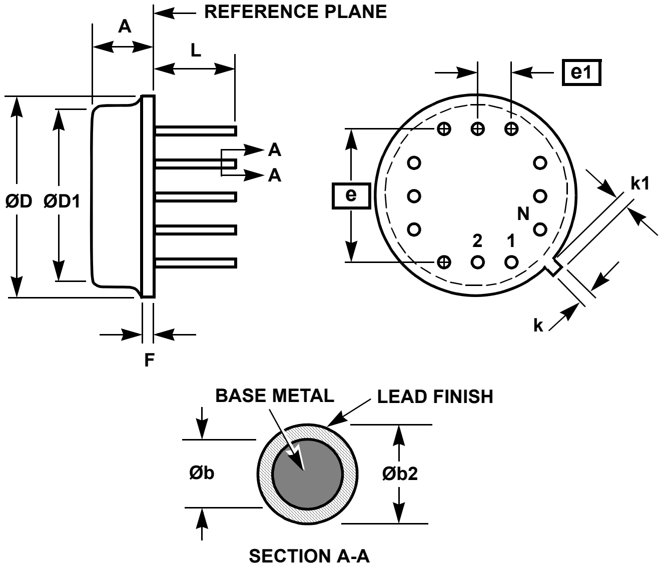
Bipolar Dielectric Isolation

Metallization Mask Layout

HA-5033



Metal Can Packages (Can)



T12.C
12 LEAD METAL CAN PACKAGE

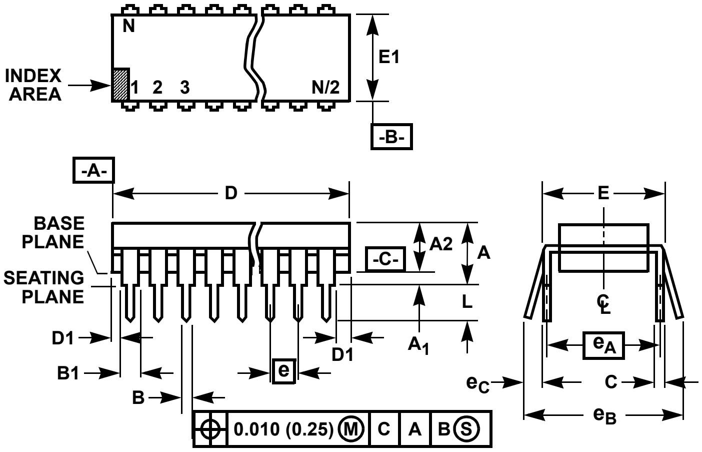
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.130	0.150	3.30	3.81	-
Øb	0.016	0.019	0.41	0.48	-
Øb2	0.016	0.021	0.41	0.53	-
ØD	0.585	0.615	14.86	15.62	-
ØD1	0.540	0.560	13.72	14.22	-
e	0.400 BSC		10.16 BSC		-
e1	0.100 BSC		2.54 BSC		-
F	0.020	0.040	0.51	1.02	-
k	0.027	0.034	0.69	0.86	-
k1	0.027	0.045	0.69	1.14	2
L	0.500	0.560	12.70	14.22	-
N	12		12		3

Rev. 0 5/18/94

NOTES:

1. The reference, base, and seating planes are the same for this variation.
2. Measured from maximum diameter of the product.
3. N is the maximum number of terminal positions.
4. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
5. Controlling dimension: INCH.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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