

Multi-Input Switched Capacitor Converter

General Description

DA9353 is a high voltage, bi-directional multi-input capacitive current and voltage multiplier suitable for applications supplied by 20 V wireless input, 20 V wireless input +1 V modulation, or any USB input voltage between 4 V and 21 V in current multiplier (voltage divider) configuration. In capacitive voltage multiplier (current divider) configuration, input is supported by a dual (2S) Li-Ion or Li-Polymer battery pack or any input voltage between 3.5 V and 12 V.

The power voltage converter (PVC) operates with conversion efficiency exceeding 98 %. Low profile external components and a minimum PCB footprint allow small circuit implementation in compact applications. As the pass devices are fully integrated, no external power switches are needed. Power conversion and the operational modes are controlled via an I²C compatible interface.

DA9353 supports voltage detection with autonomous wake-up and programmable soft-start to limit inrush current from the power node. It also implements integrated over-temperature and over-current protection for increased system reliability without the need for external sensing components.

Enable supervision and nIRQ signals are available, supporting different power up or power cycle scenarios.

Key Features

- Input voltage V_{V2X} (Forward mode)
4 V to 21 V
- Input voltage V_{V1X} (Reverse mode)
3.5 V to 12 V
- Output voltage
 $V_{V1X} = \frac{1}{2} * V_{V2X}$ (Forward mode)
- Output voltage
 $V_{V2X} = 2 * V_{V1X}$ (Reverse mode)
- 4.5 A output current (Divide mode)
- 3 A output current (Bypass mode)
- 2 A output current (Multiply mode)
- Typical 30 μ A quiescent current (POWERDOWN)
- Multi-input power muxing capability
- Integrated power switches
- Autonomous soft start
- Automatic on/off bypass power switch (VPSOUT), VBUS2, and V2X
- ENB pin to control PVC operation
- I²C compatible control interface
- Voltage, current, and temperature supervision
- -40 °C to +125 °C junction temperature range
- 54 ball WLCSP 3.27 mm x 2.82 mm (0.40 mm pitch) middle three rows staggered bumps
- 1 mm max. external components height

Applications

- Smartphones
- Tablets
- Notebook computers
- DSLR and mirrorless cameras
- VR / AR Headsets
- Game consoles
- Drones
- Other 1S or 2S battery powered applications

Multi-Input Switched Capacitor Converter

System Diagram

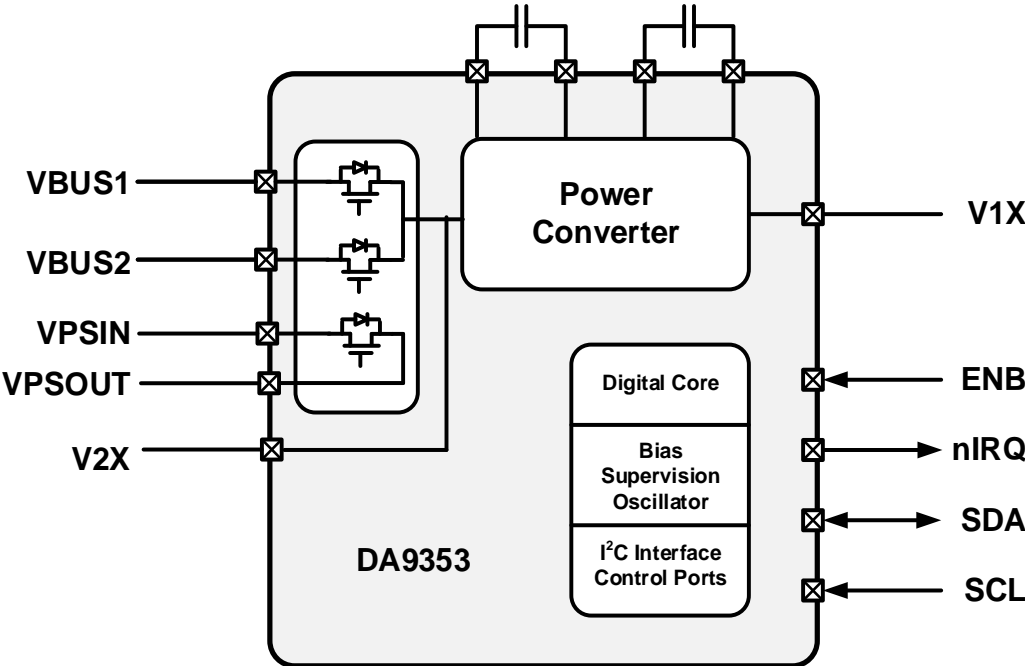


Figure 1: System Diagram

Multi-Input Switched Capacitor Converter

Contents

General Description	1
Key Features	1
Applications	1
System Diagram	2
1 Terms and Definitions	6
2 References	6
3 Block Diagram	7
4 Pinout	8
5 Characteristics	10
5.1 Absolute Maximum Ratings	10
5.2 Recommended Operating Conditions.....	10
5.3 Electrostatic Discharge Ratings	11
5.4 Electrical Characteristics.....	11
5.4.1 Power Voltage Converter	12
5.4.2 Power-on-Reset and Current Supervision.....	15
5.4.3 Protections and Monitoring.....	15
5.4.4 Digital I/O Characteristics	18
5.4.5 I ² C Timing Characteristics	19
6 Functional Description	20
6.1 System Architecture	20
6.1.1 Power Voltage Converter	21
6.1.2 PVC Output Voltage	21
6.1.3 PVC Start-Up	21
6.1.4 DA9353 Power States	22
6.1.5 NO POWER State	22
6.1.6 POWERDOWN State	23
6.1.7 STANDBY State	23
6.1.8 FAULT TIME and FAULT RECOVERY States.....	23
6.1.9 ACTIVE	23
6.1.10 Power Mux and Power Switch Start-Up Scenarios	24
6.1.11 Power Switch Control	24
6.1.12 Power Mux Control	25
6.2 Monitoring and Protections	25
6.2.1 Input Voltage Protection	25
6.2.2 Power Good Protection and Fault Generation	26
6.2.3 Over-Current Protection.....	26
6.2.4 CFLY Short Protection.....	26
6.2.5 CBOOT_OK Monitoring.....	27
6.2.6 QVPS_OK and QVBUSx_OK Monitoring	27
6.2.7 Over-Temperature Protection.....	27
6.2.8 PVC Timer Fault	27
6.2.9 Watchdog Timer	27
6.2.10 nIRQ Fault	28
6.2.11 AVDD Internal Voltage Regulator.....	29

Multi-Input Switched Capacitor Converter

6.2.12	Low Power Operation	29
7	Control Interface.....	30
7.1	I ² C Communication	30
7.2	I ² C Control Bus Protocol	30
8	Register Definitions	32
8.1	Register Map.....	32
9	Package Information	45
9.1	Package Outline.....	45
9.2	Moisture Sensitivity Level.....	46
9.3	WLCSP Handling	46
9.4	Soldering Information	46
10	Ordering Information	47
11	Application Information	47
11.1	Recommended External Components	47
11.1.1	Capacitor Selection.....	47

Figures

Figure 1:	System Diagram.....	2
Figure 2:	Block Diagram.....	7
Figure 3:	WLCSP Pinout Diagram (Top View)	8
Figure 4:	DA9353 Divide Mode Efficiency vs. Load Current, V2X	14
Figure 5:	DA9353 Multiply Mode Efficiency vs. Load Current, V1X.....	14
Figure 6:	Interface Timing.....	19
Figure 7:	DA9353 Charging System Diagram 1	20
Figure 8:	DA9353 Charging System Diagram 2	20
Figure 9:	DA9353 Charging System Diagram 3	20
Figure 10:	Power Voltage Converter Diagram	21
Figure 11:	DA9353 Power States Flow Diagram	22
Figure 12:	Timing of I ² C START and STOP Condition.....	30
Figure 13:	I ² C Byte Write (SDA Line)	31
Figure 14:	I ² C Byte Read (SDA Line).....	31
Figure 15:	WLCSP Package Outline Drawing.....	45

Tables

Table 1:	Pin Description	8
Table 2:	Pin Type Definition	9
Table 3:	Absolute Maximum Ratings.....	10
Table 4:	Recommended Operating Conditions	10
Table 5:	Electrostatic Discharge Ratings	11
Table 6:	Power Voltage Converter	12
Table 7:	Power-on-Reset and Current Supervision	15
Table 8:	Comparator Thresholds.....	15
Table 9:	Digital I/O Characteristics.....	18
Table 10:	I ² C Timing Characteristics	19
Table 11:	PVC Operation Modes	24
Table 12:	Start-Up Scenarios	24
Table 13:	QVPS Power Switch Control	25
Table 14:	QVBUS1 and QVBUS2 Power Mux Control (VPSOUT_PRIORITY = 0)	25
Table 15:	QVBUS2 Only Power Mux Control (VPSOUT_PRIORITY = 1)	25

Multi-Input Switched Capacitor Converter

Table 16: Input Selection for Under-Voltage and Over-Voltage Protection Comparators	26
Table 17: Register Map	32
Table 18: STATUS_B (0x0002).....	32
Table 19: REV_ID (0x0003)	33
Table 20: VENDOR_ID (0x0004)	33
Table 21: CONFIG_ID (0x0005).....	33
Table 22: ONKEY_CONFIG_1 (0x000B)	33
Table 23: SYS_CONFIG_1 (0x000D)	34
Table 24: SYS_CONFIG_2 (0x000E).....	34
Table 25: MASK_FAULT_CONFIG (0x0013).....	34
Table 26: MASK_FAULT_CONFIG_B (0x0014)	35
Table 27: DISABLE_FAULT_CONFIG (0x0015).....	35
Table 28: DISABLE_FAULT_CONFIG_B (0x0016)	36
Table 29: PVC_CONFIG (0x0017).....	36
Table 30: SYS_CTRL_1 (0x0018).....	36
Table 31: PVC_CTRL_1 (0x001C).....	37
Table 32: PVC_CTRL_2 (0x001D).....	37
Table 33: SYS_STATUS (0x001F).....	38
Table 34: PVC_EVENT (0x0022).....	38
Table 35: PVC_EVENT_B (0x0023)	38
Table 36: PVC_STATUS (0x0024).....	39
Table 37: PVC_STATUS_B (0x0025)	40
Table 38: PVC_STATUS_C (0x0026)	40
Table 39: EVENT_LOG (0x0027).....	41
Table 40: I2C_SLAVE_ADDR (0x0039).....	41
Table 41: ANABIAS4 (0x0113).....	41
Table 42: ANABIAS5 (0x0114).....	42
Table 43: PROTECTION1 (0x0210).....	42
Table 44: PROTECTION10 (0x0311).....	42
Table 45: PROTECTION11 (0x0312).....	43
Table 46: PMUX2 (0x0511)	43
Table 47: PMUX3 (0x0512)	43
Table 48: MSL Classification	46
Table 49: Ordering Information	47
Table 50: Recommended External Capacitors.....	47

Multi-Input Switched Capacitor Converter

1 Terms and Definitions

FSM	Finite-state machine
HV	High voltage
Li-Ion	Lithium-ion
nIRQ	Active low interrupt request
OTG	On-the-go
OTP	One-time programmable memory
OVP	Over voltage protection
PCB	Printed circuit board
PD	Power delivery
PPS	Programmable power supply
PVC	Power voltage converter
QVBUS1	Power mux on VBUS1
QVBUS2	Power mux on VBUS2
QVPS	Bypass power switch
R _{DS_ON}	Drain-source on resistance
RX	Receiver
SCL	Serial clock
SDA	Serial data
SIDO	Single input dual output
SISO	Single input single output
SMBus	System management bus
TA	Travel adapter
TX	Transmitter
USB	Universal serial bus

2 References

- [1] NXP Semiconductors N.V., UM10204 I²C-Bus Specification and User Manual, Revision 6, 201

Multi-Input Switched Capacitor Converter

3 Block Diagram

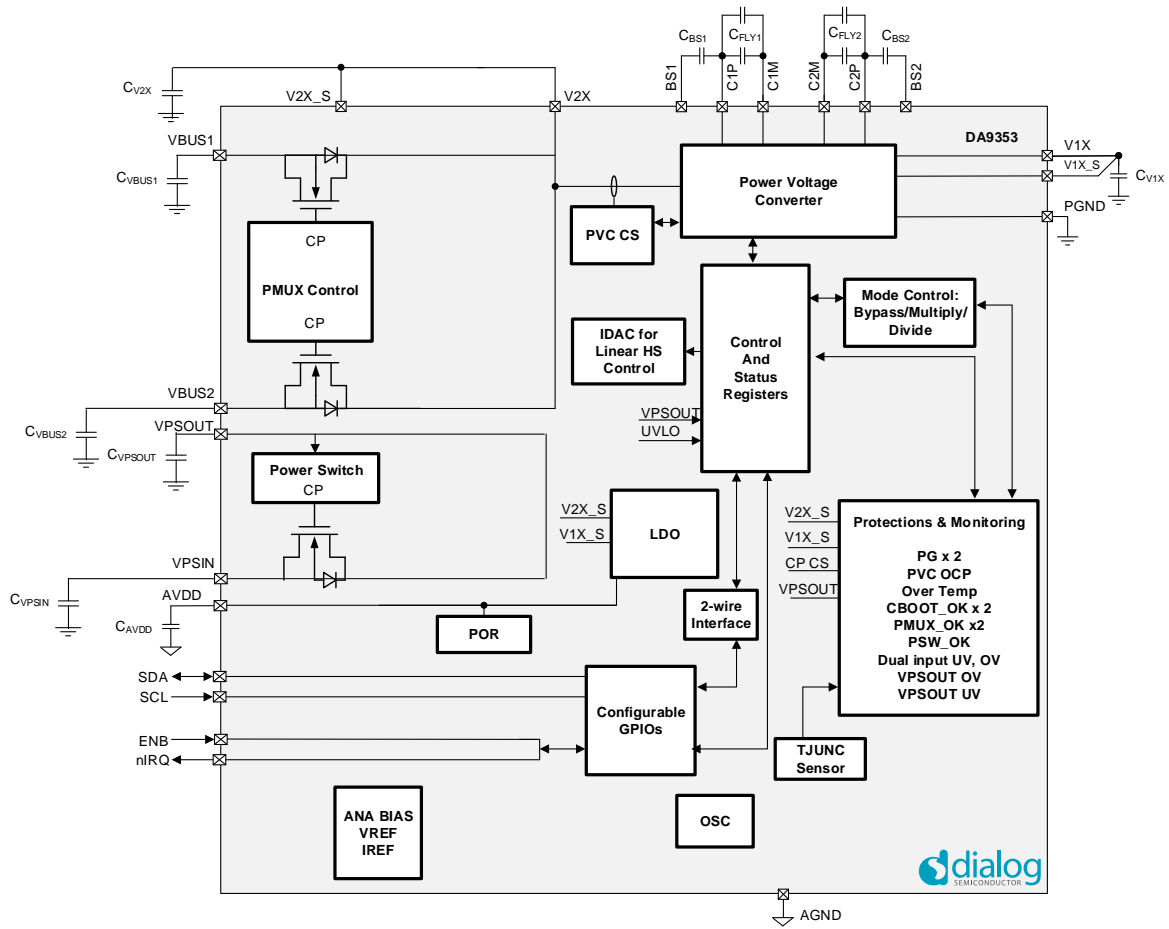


Figure 2: Block Diagram

Multi-Input Switched Capacitor Converter

Pinout

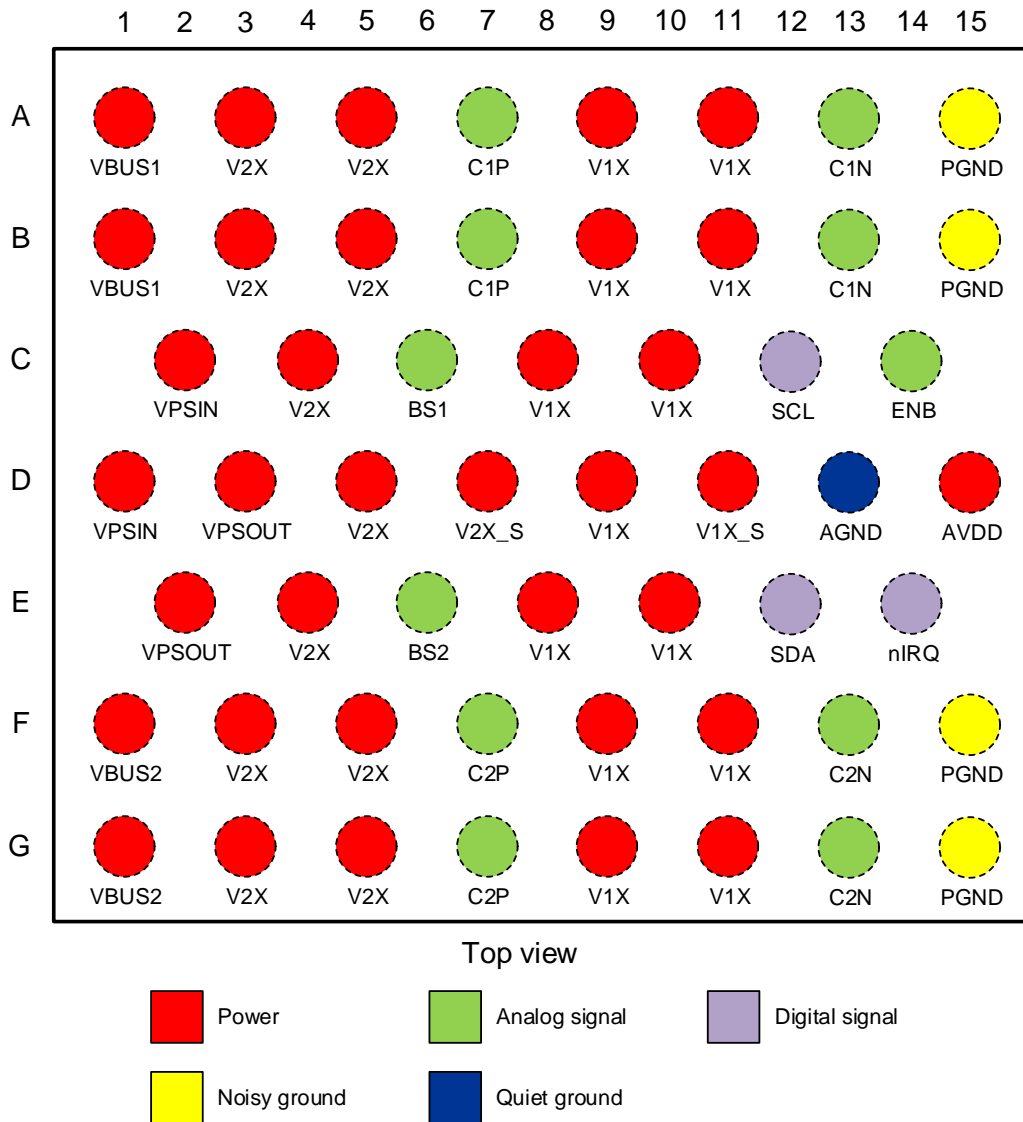


Figure 3: WLCSP Pinout Diagram (Top View)

Table 1: Pin Description

WLCSP Pin #	Pin Name	Type (Table 2)	Description
A1, B1	VBUS1	PWR	Power mux. input/output 1
F1, G1	VBUS2	PWR	Power mux. input/output 2
D3, E2	VPSOUT	PWR	Power switch output
C2, D1	VPSIN	PWR	Power switch input
A3, A5, B3, B5, C4, D5, E4, F3, F5, G3, G5	V2X	PWR	Power supply
A7, B7	C1P	PWR	Flying capacitor 1 positive terminal

Multi-Input Switched Capacitor Converter

WLCSP Pin #	Pin Name	Type (Table 2)	Description
A13, B13	C1N	PWR	Flying capacitor 1 negative terminal
C6	BS1	DI	Bootstrap capacitor 1 positive terminal
C14	ENB	AIO	Enable (active low)
A9, A11, B9, B11, C8, C10, D9, E8, E10, F9, F11, G9, G11	V1X	PWR	Output voltage / power supply
E12	SDA	DIO	I ² C data
E14	nIRQ	DO	nIRQ interrupt GPO
D7	V2X_S	AI	Power supply / output voltage sense
D11	V1X_S	AI	Output voltage / power supply sense
F7, G7	C2P	PWR	Flying capacitor 2 positive terminal
C12	SCL	DI	I ² C clock
D15	AVDD	PWR	Power supply for internal logic and control
F13, G13	C2N	PWR	Flying capacitor 2 negative terminal
E6	BS2	PWR	Bootstrap capacitor 2 positive terminal
D13	AGND	GND	Analog quiet ground
A15, B15, F15, G15	PGND	GND	Power ground

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	PWR	Power
DIO	Digital input/output	GND	Ground

Multi-Input Switched Capacitor Converter

4 Characteristics

4.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T _{STG}	Storage temperature		-65	150	°C
T _J	Junction temperature		-40	150	°C
V _{VBUS2_LIM}	Limiting voltage on VBUS2	Ramp < 0.1 V/μs	-0.3	24	V
V _{VBUS1_LIM}	Limiting voltage on VBUS1	Ramp < 0.1 V/μs	-0.3	24	V
V _{VPSOUT_LIM}	Limiting voltage on VPSOUT	Ramp < 0.1 V/μs	-0.3	24	V
V _{VPSIN_LIM}	Limiting voltage on VPSIN	Ramp < 0.1 V/μs	-0.3	24	V
V _{V2X_LIM}	Limiting voltage on V2X	Ramp < 0.1 V/μs	-0.3	24	V
V _{V1X_LIM}	Limiting voltage on V1X	Ramp < 0.1 V/μs	-0.3	16	V
V _{CFLY_DIFF}	Flying capacitor differential voltage across C _{FLY1} and C _{FLY2}		-0.3	12	V
V _{CBS_LIM}	Limiting bootstrap voltage across C _{BS1} and C _{BS2}		-0.3	5.5	V
V _{AVDD_LIM}	Limiting core voltage on AVDD		-0.3	5.5	V
V _{PIN}	Limiting voltage on all pins except above		-0.3	V _{AVDD} + 0.3	V

4.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T _J	Junction temperature		-40		+125	°C
T _A	Ambient temperature		-40		+85	°C
V _{DD_HI}	Input supply voltage range for the higher voltage rails	V2X, VBUS1 and VBUS2 in SWITCHING (Divide mode)	8		21	V
		V2X, VBUS1, and VBUS2 in BYPASS (Forward mode)	4		12	V
V _{DD_LO}	Input supply voltage range for the lower voltage rails	V1X in BYPASS (Reverse mode)	3.5		12	V
		V1X in SWITCHING (Multiply mode)	3.5		10.5	V

Multi-Input Switched Capacitor Converter

I _{VPS_MAX}	Maximum continuous current on power switch				3	A
I _{V2X_MAX_BYP}	Maximum continuous current on V2X	BYPASS (Forward and Reverse modes)			3	A
I _{V2X_MAX_MULT}	Maximum continuous current on V2X	SWITCHING (Multiply mode)			2	A
I _{V2X_MAX_DIV}	Maximum continuous current on V2X	SWITCHING (Divide mode)			2.5	A
I _{V1X_MAX_BYP}	Maximum continuous current on V1X	BYPASS (Forward and Reverse modes)			3	A
I _{V1X_MAX_MULT}	Maximum continuous current on V1X	SWITCHING (Multiply mode)			4	A
I _{V1X_MAX_DIV}	Maximum continuous current on V1X	SWITCHING (Divide modes)			4.5	A
I _{VBUSx_MAX_BYP}	Maximum continuous current on VBUSx	BYPASS (Forward and Reverse modes)			3	A
I _{VBUSx_MAX_MULT}	Maximum continuous current on VBUSx	SWITCHING (Multiply mode)			2	A
I _{VBUSx_MAX_DIV}	Maximum continuous current on VBUSx	SWITCHING (Divide mode)			2.25	A

4.3 Electrostatic Discharge Ratings

Table 5: Electrostatic Discharge Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
ESD _{HBM}	Maximum ESD protection	Human body model (HBM) All exposed pins	2000			V
ESD _{CDM}	Maximum ESD protection	Charged device model (CDM)	500			V

4.4 Electrical Characteristics

Unless otherwise noted, the following is valid for $T_A = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ and $V_{V2X} = 16\text{ V}$ (SWITCHING state) or $V_{V2X} = 5\text{ V}$ (BYPASS state). Refer to [Table 50](#) for recommended external components.

Multi-Input Switched Capacitor Converter

4.4.1 Power Voltage Converter

Table 6: Power Voltage Converter

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V _{DD_HI_BYP}	Input supply voltage range for the higher supply voltage rails	V _{2X} , V _{BUS1} , V _{BUS2} in BYPASS state (Forward mode)	4		12	V
V _{DD_HI_SW}	Input supply voltage range for the higher supply voltage rails	V _{2X} , V _{BUS1} , and V _{BUS2} in SWITCHING state (Divide mode)	8		21	V
V _{DD_LO_RBYP}	Input supply voltage range for the lower voltage rail	V _{1X} in BYPASS state (Reverse mode)	3.5		12	V
V _{DD_LO_SW}	Input supply voltage range for the lower voltage rail	V _{1X} in SWITCHING state (Multiply mode)	3.5		10.5	V
I _{Q_PWR_DWN}	Quiescent current in POWERDOWN	ENB = high V _{V1X} = 5 V		30		μA
I _{Q_STANDBY}	Current consumption STANDBY	ENB = low V _{V2X} = 5 V PVC_EN = 0x0		100		μA
I _{Q_BYP}	Quiescent current in BYPASS	ENB = low PVC_EN = 0x1 V _{V2X} = 5 V = V _{V1X} = 5 V		2		mA
I _{Q_RBYP}	Quiescent current in BYPASS state (Reverse mode)	ENB = low V _{V2X} = V _{V1X} = 5 V PVC_EN = 0x1		2		mA
I _{Q_ACT}	Quiescent current in SWITCHING state	ENB = low PVC_EN = 0x1 FSW = 0x2 (300 kHz) No load		6		mA
t _{MULT_STARTUP}	Start-up time in Multiply mode	Time measured from PVC_EN = 0x1 to SYS_STATUS = 0xF and DIRECTION_STATUS = 0x1. No load on V _{BUSx}		4		ms
t _{DIV_STARTUP}	Start-up time in Divide mode	Time measured from PVC_EN = 0x1 to SYS_STATUS = 0xF and DIRECTION_STATUS = 0x0. No load on V _{1X}		1		ms
t _{BYP_STARTUP}	Start-up time in Forward Bypass mode	Time measured from PVC_EN = 0x1 to SYS_STATUS = 0x5 and DIRECTION_STATUS = 0x0. No load on V _{1X}		2		ms

Multi-Input Switched Capacitor Converter

Parameter	Description	Conditions	Min	Typ	Max	Unit
t _{RBYP_STARTUP}	Start-up time for Reverse Bypass mode	Time measured from PVC_EN = 0x1 to SYS_STATUS = 0x5 and DIRECTION_STATUS = 0x1. No load on VBUSx		0.5		ms
t _{PS_STARTUP}	Start-up time for Power Switch	Time measured from EN_QVPS = 0x1 to QVPS_ON = 0x1		6		ms
t _{QVBUS1_STARTUP}	Start-up time for Power Switch	Time measured from EN_QVBUS1 = 0x1 to QVBUS1_ON = 0x1		6		ms
t _{QVBUS2_STARTUP}	Start-up time for Power Switch	Time measured from EN_QVBUS2 = 0x1 to QVBUS2_ON = 0x1		6		ms
f _{SW}	PVC switching frequency	Fixed frequency mode	50		1000	kHz
f _{SW_EMI}	Spread spectrum modulation frequency range	Configurable via SPREAD_WIDTH	-16		16	%
η_{DIV_20V}	Efficiency in SWITCHING state (Divide mode)	VBUS1 or VBUS2 = 20 V C _{FLY} = 2 x 22 μ F (0603, 16V) C _{V1X} = 4.7 μ F Load = 4 A		97.9		%
η_{DIV_16V}	Efficiency in SWITCHING state (Divide mode)	VBUS1 or VBUS2 = 16 V C _{FLY} = 2 x 22 μ F (0603, 16V) C _{V1X} = 4.7 μ F Load = 4 A		97.7		%
η_{MULT_10V}	Efficiency in SWITCHING state (Multiply mode)	V _{V1X} = 10 V C _{FLY} = 2 x 22 μ F (0603, 16V) C _{V2X} = 4.7 μ F Load = 2 A (on VBUS1 or VBUS2)		97.9		%
η_{MULT_8V}	Efficiency in SWITCHING state (Multiply mode)	V _{V1X} = 8 V C _{FLY} = 2 x 22 μ F (0603, 16V) C _{V2X} = 4.7 μ F Load = 2 A (on VBUS1 or VBUS2)		97.7		%
R _{ON_BYP_V2X}	Total R _{ON} in BYPASS state (Forward or Reverse modes), measured between V2X and V1X	V _{V2X} = V _{V1X} = 10 V		30		m Ω
R _{ON_QVBUS1}	On resistance of QVBUS1			30	45	m Ω
R _{ON_QVBUS2}	On resistance of QVBUS2			30	45	m Ω
R _{ON_QVPS}	On resistance of QVPS			22	33	m Ω

Multi-Input Switched Capacitor Converter

4.4.1.1 Efficiency Characteristics

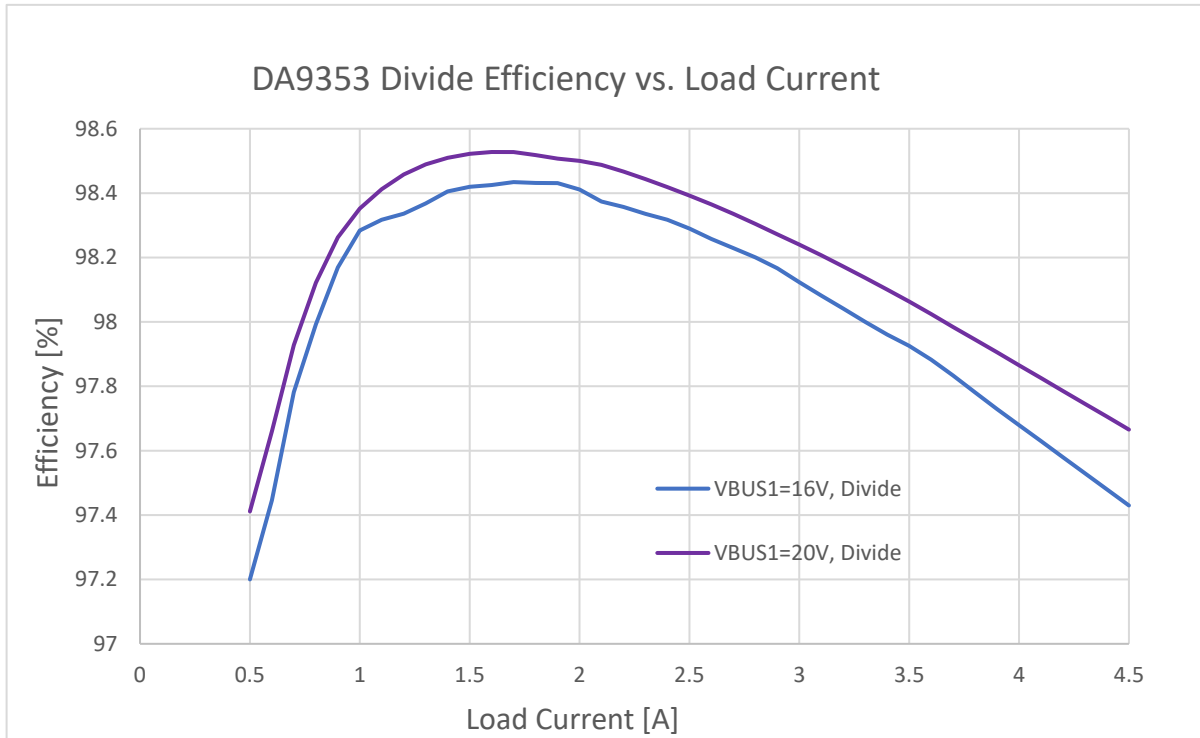


Figure 4: DA9353 Divide Mode Efficiency vs. Load Current, V2X

Conditions: $C_{FLY1} = C_{FLY2} = 2 \times 22 \mu\text{F}$, $C_{V1X} = 1 \times 4.7 \mu\text{F}$, $f_{sw} = 300 \text{ kHz}$

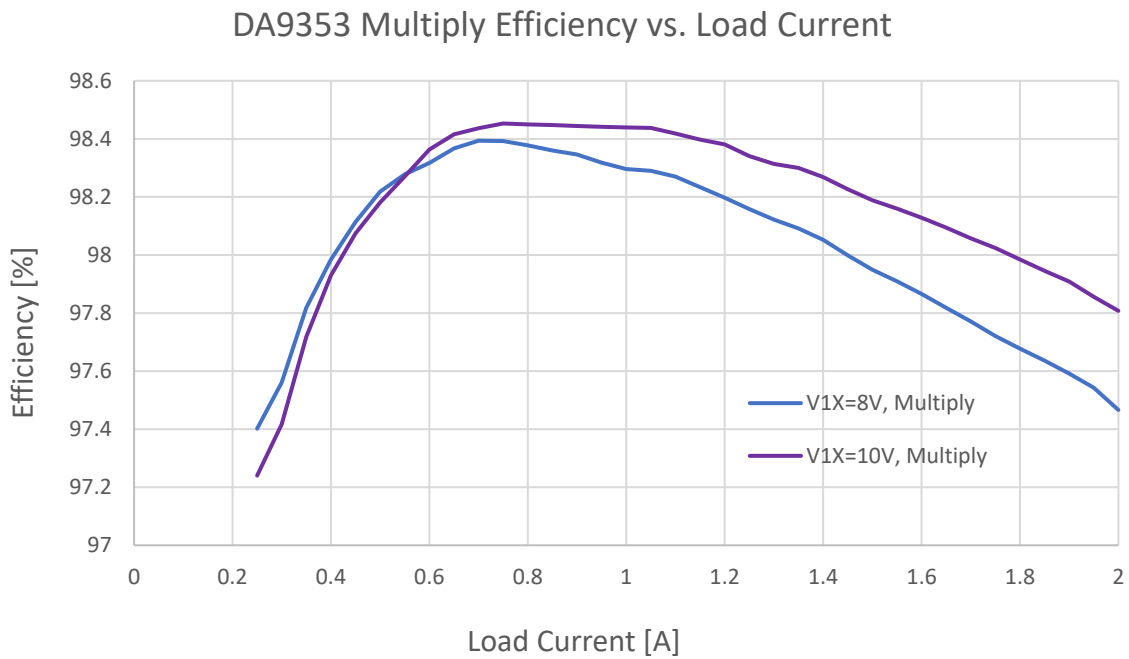


Figure 5: DA9353 Multiply Mode Efficiency vs. Load Current, V1X

Conditions: $C_{FLY1} = C_{FLY2} = 2 \times 22 \mu\text{F}$, $C_{V2X} = 1 \times 4.7 \mu\text{F}$, $f_{sw} = 300 \text{ kHz}$

Multi-Input Switched Capacitor Converter

4.4.2 Power-on-Reset and Current Supervision

Table 7: Power-on-Reset and Current Supervision

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V _{THR_LWR_POR}	Power-on-reset lower threshold	Measured @ AVDD V _{V2X} / V _{V1X} decreasing	2.1		2.7	V
V _{THR_UPPER_POR}	Power-on-reset upper threshold	Measured @ AVDD V _{V2X} / V _{V1X} increasing			2.8	V
I _{V2X_POS_OCP_BYP}	Positive peak current protection programmable range in BYPASS state (Forward mode)	Maximum current on V2X programmable via SEL_OCP_BYPASS (3.25, 3.5, 3.75, 4.0) A	3.25		4	A
I _{V2X_POS_OCP_SW}	Positive peak current protection programmable range in SWITCHING state	Maximum current on V2X programmable via SEL_OCP (1.625, 2.125, 2.625, 3.125) A	1.625		3.125	A
I _{V2X_NEG_OCP_BYP}	Negative peak current protection programmable range in BYPASS state (Reverse mode)	Maximum current on V2X programmable via SEL_OCP_BYPASS (-3.25, -3.5, -3.75, -4.0) A	-4		-3.25	A
I _{V2X_NEG_OCP_SW}	Negative peak current protection programmable range in SWITCHING state	Maximum current on V2X programmable via SEL_OCP (-1.625, -2.125, -2.625, -3.125) A	-3.125		-1.625	A
I _{V2X_OCP_ACC}	Accuracy of current protection on HV rail	V _{V2X} = 8 V OCP setting = 0x0 (3.25 A in BYPASS) OCP setting = 0x3 (3.125 A in SWITCHING)	-15		15	%

4.4.3 Protections and Monitoring

Table 8: Comparator Thresholds

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V _{PSOUT_OV}	Power switch over-voltage threshold limit on VPSOUT.	2-bit programmable via SEL_VPSOUT_OV (12, 13, 13.5, 14) V	12		14	V
V _{PSOUT_UV}	Power switch under-voltage threshold limit on VPSOUT.	2-bit programmable via SEL_VPSOUT_UV (3.2, 3.6, 4.0, 4.4) V	3.2		4.4	V

Multi-Input Switched Capacitor Converter

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{IN_OV_BYP_V}$ BUSx	V_{IN} over-voltage programmable range on VBUS1/VBUS2 (indirect protection through V2X) or V1X in BYPASS state	2-bit programmable via SEL_OVP (12, 13, 13.5, 14) V	12		14	V
$V_{IN_OV_BYP}$	V_{IN} over-voltage programmable range on V2X or V1X in BYPASS state	2-bit programmable via SEL_OVP (12, 13, 13.5, 14) V	12		14	V
$V_{IN_OV_MUL}$	V_{IN} over-voltage programmable range on V1X in SWITCHING (Multiply mode)	2-bit programmable via SEL_OVP_MULT (9.5, 10, 10.5, 11) V	9.5		11	V
$V_{IN_OV_DIV_V}$ BUSx	V_{IN} over-voltage programmable range on VBUS1/VBUS2 (indirect protection through V2X) in SWITCHING (Divide mode)	2-bit programmable via SEL_OVP (19, 20, 21, 22) V	19		22	V
$V_{IN_OV_DIV}$	V_{IN} over-voltage programmable range on V2X in SWITCHING (Divide mode)	2-bit programmable via SEL_OVP (19, 20, 21, 22) V	19		22	V
$V_{IN_OV_HYS}$	Input over-voltage hysteresis in SWITCHING	Falling hysteresis		750		mV
$V_{IN_OV_HYS_B}$ YP	Input over-voltage hysteresis in BYPASS	Falling hysteresis		950		mV
$V_{IN_OV_DIV_B}$ YP_ACC	Input over-voltage accuracy in SWITCHING (Divide mode) or BYPASS state	2-bit programmable via SEL_OVP	-3		3	%
$V_{IN_OV_MUL_A}$ CC	Input over-voltage accuracy in SWITCHING (Multiply mode)	2-bit programmable via SEL_OVP_MULT	-6		6	%
$V_{IN_UV_BYP_M}$ UL	V_{IN} under-voltage on V2X in BYPASS state or V1X in SWITCHING (Multiply mode)	2-bit programmable via SEL_UV (3.2, 3.6, 4.0, 4.4) V, input voltage rising	3.2		4.4	V
$V_{IN_UV_BYP_M}$ UL_VBUSx	V_{IN} under-voltage on VBUS1/VBUS2 in BYPASS state (indirect protection through V2X) or V1X in SWITCHING state (Multiply mode)	2-bit programmable via SEL_UV (3.2, 3.6, 4.0, 4.4) V, input voltage rising	3.2		4.4	V
$V_{IN_UV_DIV}$	V_{IN} under-voltage on V2X in SWITCHING state (Divide mode)	2-bit programmable (7, 8, 9, 10) V, input voltage rising	7		10	V
$V_{IN_UV_DIV_V}$ BUSx	V_{IN} under-voltage on VBUSx in SWITCHING state (Divide mode)	2-bit programmable (7, 8, 9, 10) V, input voltage rising	7		10	V

Multi-Input Switched Capacitor Converter

Parameter	Description	Conditions	Min	Typ	Max	Unit
V _{IN_UV_HYS}	Input under-voltage hysteresis in SWITCHING (Divide mode)	Falling hysteresis		130		mV
V _{IN_UV_HYS_M} UL_BYP	Input under-voltage hysteresis in Multiply mode or BYPASS	Falling hysteresis		200		mV
V _{IN_UV_ACC}	Input under-voltage accuracy in SWITCHING (Divide or Multiply mode) and BYPASS state	2-bit programmable via SEL_UV	-3		3	%
V _{PG_NEG_SW}	Power good negative switching programmable range Maximum allowed V _{1X} - V _{2X} /2 during SWITCHING state (Divide mode or Multiply mode)	V _{V1X} = 8 V. 3 bit programmable via SELPG2. PVC in SWITCHING state (Multiply mode)	100		450	mV
V _{PG_POS_SW}	Power good positive switching programmable range Maximum allowed V _{2X} /2 - V _{1X} during SWITCHING state (Divide or Multiply mode)	V _{V2X} = 16 V. 3 bit programmable via SELPG1. PVC in SWITCHING state (Divide mode)	100		450	mV
V _{PG_NEG_BYP}	Power good negative bypass programmable range Maximum allowed V _{1X} - V _{2X} during BYPASS (Forward or Reverse mode)	V _{V1X} = V _{V2X} = 5 V. 3 bit programmable via SELPG2. PVC in BYPASS state (Reverse mode)	100		450	mV
V _{PG_POS_BYP}	Power good positive bypass programmable range Maximum allowed V _{2X} - V _{1X} during BYPASS (Forward or Reverse mode)	V _{V2X} = V _{V1X} = 5 V. 3-bit programmable with SELPG1 PVC in BYPASS state (Forward mode)	100		450	mV
T _{OT}	Die over-temperature protection		140	145	150	°C
T _{OT_HYS}	Die over-temperature protection hysteresis			10		°C
V _{CBBOOT_OK}	Voltage on bootstrap cap is OK to drive the power FET gate. Only used in non-switching states. In SWITCHING states this is automatically considered as OK.	BYPASS operation	2.7	3	3.6	V
V _{QV_{BUSx}_OK}	Voltage RCP FET is OK to drive the power FET gate.	Valid input detection for Power Mux operation	2.7	3	3.6	V
V _{QV_{PS}_OK}	Voltage on QVPS FET is OK to drive the power FET gate	Valid input detection for Power Mux operation	2.7	3	3.6	V

Multi-Input Switched Capacitor Converter

4.4.4 Digital I/O Characteristics

Table 9: Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
ENB Pin						
V_{IH}	Input high voltage		1.2			V
V_{IL}	Input low voltage				0.4	V
V_{HYS}	Hysteresis	Falling	-100			mV
R_{PD_ENB}	Internal pull down			100		k Ω
SDA or SCL Pin						
$V_{IH_SDA_SCL}$	Input high voltage SDA or SCL	Note 1	1.2			V
$V_{IL_SDA_SCL}$	Input low voltage SDA or SCL	Note 1			0.4	V
SDA Pin						
V_{OL_SDA}	Output low voltage SDA	Open drain $I_{OUT_SDA} = 3 \text{ mA}$			0.24	V
nIRQ Pin						
V_{OL_nIRQ}	Output low voltage nIRQ	External pull-up resistor = 22 k Ω			0.24	V

Note 1 Input range compatible with 1.8 V and 3.3 V logic.

Multi-Input Switched Capacitor Converter

4.4.5 I²C Timing Characteristics

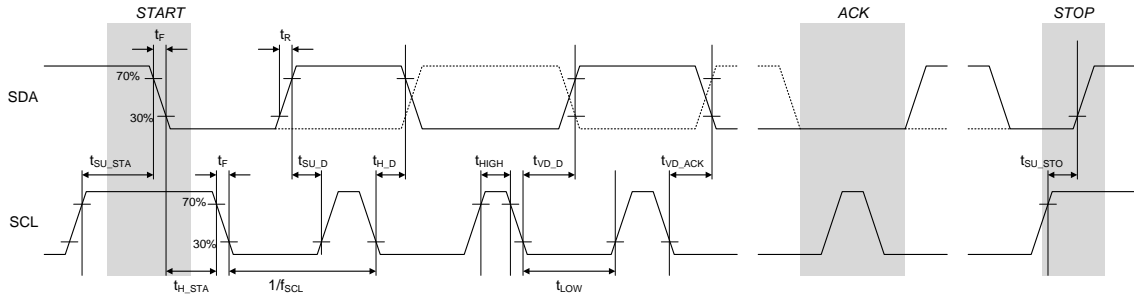


Figure 6: Interface Timing

Table 10: I2C Timing Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
t _{BUF}	Bus free time STOP to START		0.5			μs
C _{BUS}	Bus line capacitive load				150	pF
f _{SCL}			0		1000	kHz
t _{SETUP_START}	Start condition set-up time		0.26			μs
t _{HOLD_START}	Start condition hold time		0.26			μs
t _{LO_SCL}	SCL low time		0.5			μs
t _{HI_SCL}	SCL high time		0.26			μs
t _{RISE}	I ² C SCL and SDA rise time	(input requirement)			300	ns
t _{FALL}	I ² C SCL and SDA fall time	(input requirement)			300	ns
t _{SETUP_DATA}	Data set-up time		50			ns
t _{HOLD_DATA}	Data hold time		0			ns
t _{VAL_DATA}	Data valid time				0.45	μs
t _{VAL_DATA_ACK}	Data valid time acknowledge				0.45	μs
t _{SETUP_STOP}	Stop condition set-up time		0.26			μs

Multi-Input Switched Capacitor Converter

5 Functional Description

5.1 System Architecture

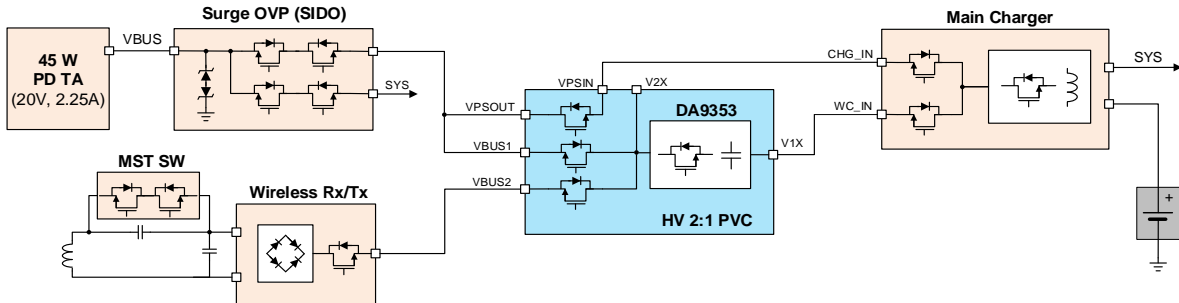


Figure 7: DA9353 Charging System Diagram 1

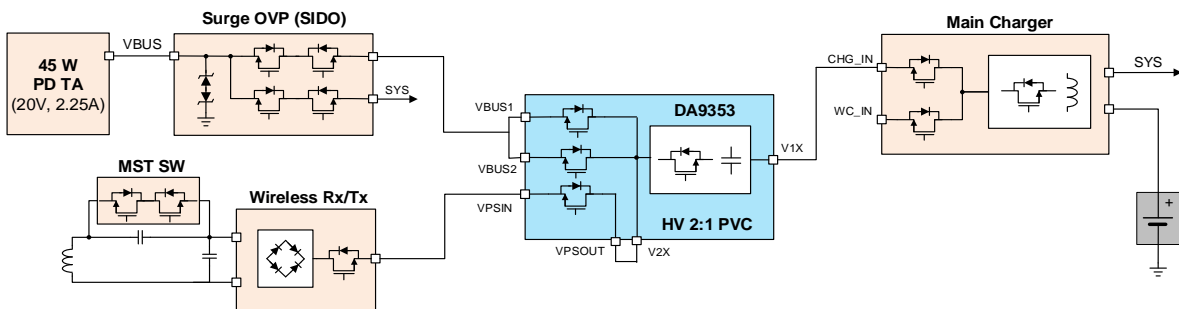


Figure 8: DA9353 Charging System Diagram 2

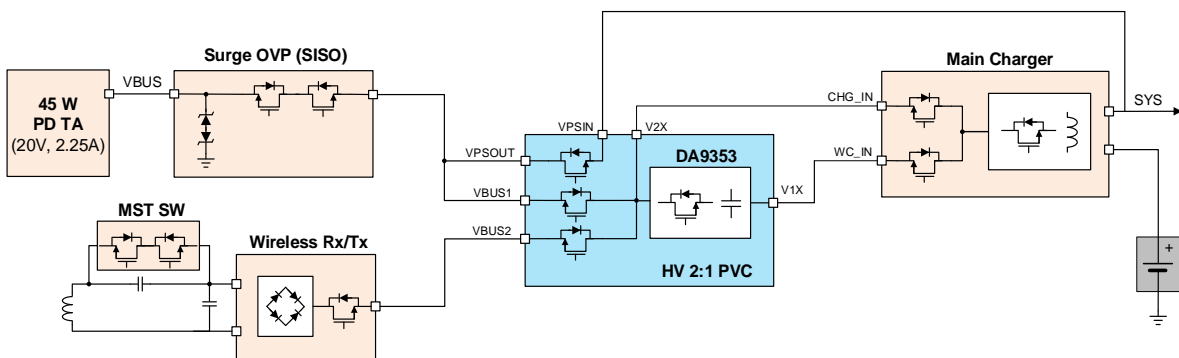


Figure 9: DA9353 Charging System Diagram 3

The system diagrams above illustrate configurations for the high voltage PVC with the inclusion of three internal power switches. These configurations enable the PVC to support a wide range of use cases depending on the application. Some use cases that the PVC is capable of supporting are:

- Dual power sharing: USB OTG (5 V) and wireless RX/TX; Charging System Diagram 1, see [Figure 7](#).
- USB PD PPS TA (reduced R_{DS_ON} with parallel power switches) and HV TX; Charging System Diagram 2, see [Figure 8](#).
- Bypass to SYS test mode support (no need for SIDO OVP); Charging System Diagram 3, see [Figure 9](#).
- QVPS switch for providing power to gaming accessories

Multi-Input Switched Capacitor Converter

5.1.1 Power Voltage Converter

The high voltage, high efficiency 2S to 1S PVC is capable of supplying multiple 1S voltage rails with up to 4.5 A output current, see Figure 10. The dual phase interleaved operation ensures an almost constant input current, resulting in improved immunity to noise.

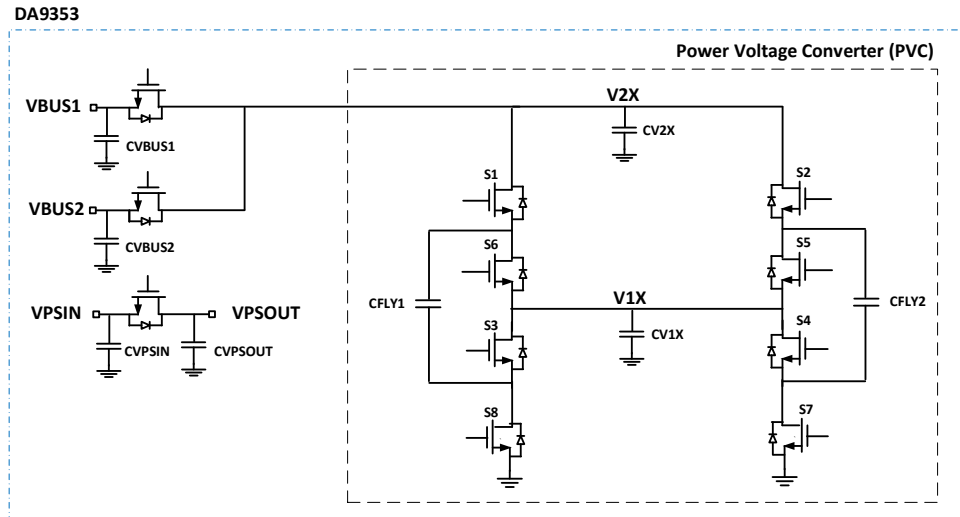


Figure 10: Power Voltage Converter Diagram

5.1.2 PVC Output Voltage

The PVC operates with a fixed duty cycle. Under no-load condition, the output voltage is half of the input voltage. When a current, I_{V1X} , is drawn at the V1X node and the PVC is switching at frequency of f_{SW} , the output voltage is determined as:

$$V_{V1X} = \frac{V_{V2X}}{2} - R_{EQ} \cdot I_{V1X}$$

Where:

- REQ is a function of the sum of all resistances in the input/output power path (including the power device's on-resistance and the PCB routing resistance) as well as the switching frequency, CFLY, and PCB parasitics

The voltage ripple at V_{OUT} can be first order approximated as the voltage drop due to the discharge of the CFLY capacitor in half of the period at an f_{SW} switching frequency, plus the discharge voltage of the output capacitor during a typical 20 ns short dead time for phase switch.

5.1.3 PVC Start-Up

DA9353 supports a PVC start-up into biased power rails (input and output). The PVC operation starts in current limited ramp up until the voltage between the high voltage port (V2X) and the low voltage port (V1X) is considered safe by the PVC's state machine, based on Power Good (PG) comparators. The duration of PVC start-up depends on the total effective capacitance connected to the PVC (flying capacitors and capacitance connected to the high and low voltage power ports) and the initial voltage deviation from the target ratio of 2:1 or 1:1. During PVC start-up, the PVC does not switch and the flying capacitors CFLY are connected in parallel to the output capacitor C_{V1X} .

NOTE

To avoid overheating with thermal power cycling during PVC start-up it is the responsibility of the external application to limit load current from any of the power ports in correspondence to the OTP setting of the start-up current limit until PVC_STATE is BYPASS or SWITCHING. At the end of the start-up phase the normal operation (BYPASS or SWITCHING) of the PVC is restored.

Multi-Input Switched Capacitor Converter

5.1.4 DA9353 Power States

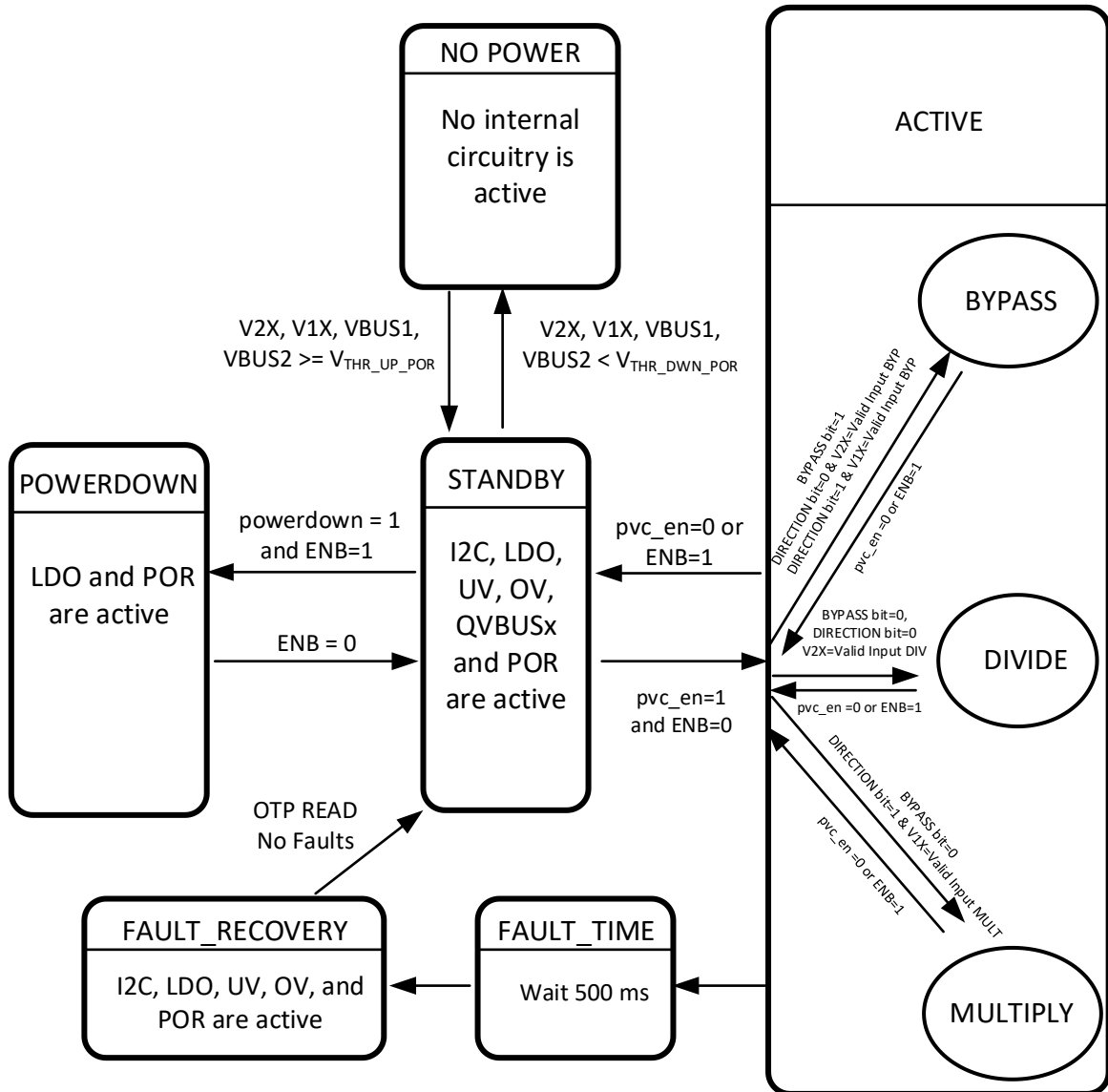


Figure 11: DA9353 Power States Flow Diagram

Note 1 Valid input BYPASS (Forward mode) = $VIN_UV_BYP_MUL < V2X < VIN_OV_BYP$
 Valid input BYPASS (Reverse mode) = $VIN_UV_BYP_MUL < V1X < VIN_OV_BYP$
 Valid input SWITCHING (Divide mode) = $VIN_UV_DIV < V2X < VIN_OV_DIV$
 Valid input SWITCHING (Multiply mode) = Same conditions as BYPASS

5.1.5 NO POWER State

DA9353 is in NO POWER state when the input supply (V2X, V1X, VBUS1, VBUS2) is below the $V_{THR_LWR_POR}$ threshold. During the NO POWER state, the supply voltage is too low for operation of the PVC and the Power-On Reset (POR) circuitry waits for sufficient input voltage.

When input supply $\geq V_{THR_UPPER_POR}$ DA9353 transitions from NO POWER state into OTP load followed by ACTIVE or POWERDOWN state, depending on PVC_EN setting.

Multi-Input Switched Capacitor Converter

5.1.6 POWERDOWN State

The POWERDOWN state is the lowest quiescent current operating state with a valid input supply. It activates the internal AVDD LDO, POR and ENB supervision circuitry. During POWERDOWN state the PVC is off and the flying capacitors are discharged. DA9353 transitions from POWERDOWN to STANDBY if the voltage level at ENB changes from high to low.

5.1.7 STANDBY State

In STANDBY state the PVC is off and other blocks are operational. The 6 MHz main oscillator can be on during this state and I²C is functional. Other circuitry available includes OV and UV protection comparators on both V2X and VPSOUT, nIRQ, event handler, and enabling of the power mux FETs.

STANDBY is also used to support application low power modes with lower quiescent current. This state can be entered into and exited with PVC_EN register write or by driving ENB pin.

5.1.8 FAULT TIME and FAULT RECOVERY States

When a fault turns off the PVC, DA9353 transitions from ACTIVE through FAULT TIME (500 ms) to FAULT RECOVERY.

Fault events are captured in the PVC_EVENT (0x0022) and PVC_EVENT_B (0x0023) registers for host interrogation and generate maskable interrupt events. FAULT RECOVERY is a temporary state and is automatically entered and exited depending on fault condition presence.

The device waits for a FAULT TIME after the PVC is disabled. DA9353 automatically exits FAULT RECOVERY state when the fault condition has expired. The PVC_EVENT and PVC_EVENT_B registers can be reset by a register write of 1 to the appropriate register bit.

5.1.9 ACTIVE

ACTIVE is the main operating state of DA9353. In this state, the PVC is on and operates in SWITCHING state (Divide or Multiply mode) or BYPASS state (Forward or Reverse mode). DA9353 exits out of the ACTIVE state in any of the following circumstances:

- the PVC is disabled (PVC_EN = 0) or ENB = high
- the input supply is outside the supported range
- the junction temperature exceeds the critical threshold
- a fault has occurred

5.1.9.1 SWITCHING State (Divide or Multiply Mode)

During SWITCHING state, any two of the PVC switches in one branch are turned fully on (for example S1 and S3) while the other two switches (in this case S6 and S8) are off, see [Figure 10](#). This configuration occurs during one phase operation of the PVC. In the second phase, the polarity of these switches is reversed.

The PVC is switching between these two phases to place the flying capacitor in series or parallel to the V1X capacitor. The act of charging the capacitor in one phase and redistributing the charge to the V1X capacitor in the other phase enables the doubling or halving operation.

This is dependent on the direction of the configured PVC and input voltage applied (VBUSx or V1X). The PVC operates with two branches interleaved to reduce switching ripple and improve efficiency performance, see [Figure 10](#).

There are two modes of operation in SWITCHING state (Divide or Multiply). The configuration of either of these modes is dependent on a valid input supply being applied (VBUSx or V1X) and the settings of the BYPASS and CHARGE_DIRECTION register bits, see [Table 11](#).

5.1.9.2 BYPASS State (Forward or Reverse Mode)

In BYPASS, the PVC turns on the four switches (S1, S2, S5, and S6) on the high side and S7, S8 on the low side. V1X ≈ V2X and both PG comparators are expected to be high.

Multi-Input Switched Capacitor Converter

The PVC will remain in Forward mode if the BYPASS register bit is asserted and CHARGE_DIRECTION bit is de-asserted, see [Table 11](#).

To operate in Reverse mode (when input voltage supply is applied on V1X), BYPASS and CHARGE_DIRECTION bits should be set high.

Table 11: PVC Operation Modes

Input Voltage Supply	BYPASS Bit	CHARGE_DIRECTION Bit	Operating Modes
VBUSx	0	0	Divide
V1X	0	1	Multiply
VBUSx	1	0	Forward
V1X	1	1	Reverse

5.1.10 Power Mux and Power Switch Start-Up Scenarios

DA9353 supports autonomous startup on VBUS2, VPSOUT, and V2X. For the start-up configuration for each mode of operation see [Table 12](#).

Table 12: Start-Up Scenarios

Power Supply	Autonomous Start	Soft-Start Divide	Soft-Start BYPASS	Soft-Start Multiply
VBUS1	No	Yes (to V1X, not to V2X)	Yes (to V1X)	N/A
VBUS2	Yes	Yes (to V1X, not to V2X)	Yes (to V1X)	N/A
VPSOUT	Yes (BYPASS both modes)	N/A	Yes (to VPSIN)	N/A
VPSIN	No	N/A	Yes (diode to VPSOUT)	N/A
V2X	Yes (Forward mode only)	Yes	Yes	N/A
V1X	No	N/A	Yes (to VBUSx, not to V2X)	Yes (to VBUSx, V2X)

5.1.11 Power Switch Control

The bypass power switch connected between VPSOUT and VPSIN (QVPS) will turn on autonomously when a valid voltage is present on VPSOUT. Likewise, QVPS will turn off when there is no valid voltage on VPSOUT, an over-temperature fault condition, or when EN_QVPS is set to 0. A valid voltage on VPSOUT represents a voltage greater than V_{PSOUT_UV} and less than V_{PSOUT_OV} . The state of QVPS (Off, On, or Linear) is summarized in [Table 13](#).

The QVPS power switch is activated when V_{PSOUT_UV} (comparator output) is set to 0 (the voltage level of VPSOUT is greater than the V_{PSOUT_UV} threshold). If this condition is met and EN_QVPS is 1, then QVPS will be operating in either Linear or On state.

The condition of the state depends on whether QVPS_SS_TIMER (QVPS soft-switching timer) has expired or not. QVPS_SS_TIMER starts when all valid conditions are met to activate QVPS. If QVPS_SS_TIMER has not expired and EN_QVPS is 1, then QVPS will be in the Linear state. Otherwise, QVPS will be operating in the On state once the timer has expired. The timer settings for QVPS can be adjusted from QVPS_SS_TIMER 2-bit register. It has programmable timer settings of 1 ms, 5 ms, 10 ms, and 20 ms, see [Table 13](#).

Multi-Input Switched Capacitor Converter

NOTE

If QVPS is not required for the application then set EN_QVPS = 0x0; in addition, connect VPSOUT and VPSIN to the ground planes on the PCB.

Table 13: QVPS Power Switch Control

VPSOUT_UV	EN_QVPS	QVPS_SS_TIMER Expired	QVPS State
X	0	N/A	Off
1	1	N/A	Off
0	1	No	Linear
0	1	Yes	On

5.1.12 Power Mux Control

Table 14: QVBUS1 and QVBUS2 Power Mux Control (VPSOUT_PRIORITY = 0)

EN_QVBUSx	QVBUSx_SS_TIMER Expired	QVBUSx FET State
0	N/A	Off
1	No	Linear
1	Yes	On

Table 15 : QVBUS2 Only Power Mux Control (VPSOUT_PRIORITY = 1)

EN_QVBUS2	VPSOUT_UV	QVBUS2_SS_TIMER Expired	QVBUS2 FET State
0	1	N/A	Off
1	1	No	Linear
1	1	Yes	On
X	0	N/A	Off

The state of QVBUSx (power mux FET) is governed by EN_QVBUSx and QVBUSx_SS_TIMER expiration when VPSOUT_PRIORITY = 0, see [Table 14](#). If VPSOUT_PRIORITY = 1, then QVBUS2 FET will not turn on if VPSOUT has a valid voltage present. This selection logic is available in DA9353 to enable autonomous turn-on for QVBUS2 and prevent the conduction of both switches (QVPS and QVBUS2) from turning on at the same time when a valid voltage is present on VPSOUT. In this scenario, QVPS will have the priority to turn on.

The condition for activating QVBUS2 FET with VPSOUT_PRIORITY = 1, is dependent on EN_QVBUS2, VPSOUT_UV, and QVBUS2_SS_TIMER expiration, see [Table 15](#).

QVBUS2 FET timer settings are programmable from a 2-bit register, VBUSx_SS_TIMER, with settings of 1 ms, 5 ms, 10 ms, and 20 ms.

5.2 Monitoring and Protections

Monitoring and Protections is a matrix of comparators for protecting the circuit from functioning in hazardous conditions and for controlling the state transitions.

5.2.1 Input Voltage Protection

Input voltage protection is used for detecting the presence of an input supply, VIN, and for disabling the PVC when VIN rises too high. The PVC is only operational when VIN (V2X or V1X) is within the range defined by [VIN_UV_BYP_MUL or VIN_UV_DIV] and [VIN_OV_BYP, VIN_OV_MUL, or VIN_OV_DIV].

Multi-Input Switched Capacitor Converter

VIN over-voltage conditions will disable the PVC and will trigger OV_FAULT_EVENT. Resuming normal operation is allowed after all fault conditions are gone.

Similarly, under-voltage conditions will disable the PVC and will trigger UV_FAULT_EVENT. Resuming normal operation is allowed after all fault conditions are gone.

In DA9353, the feedback for the under-voltage and over-voltage comparators depends on the state and functional mode setting (CHARGE_DIRECTION and BYPASS register bits) of the PVC. The feedback may either be taken on the V2X_S or V1X_S pin. Configuration for the feedback of these protection comparators is shown in Table 16.

Table 16: Input Selection for Under-Voltage and Over-Voltage Protection Comparators

CHARGE_DIRECTION Bit	BYPASS Bit	UV and OV Input	UV and OV Settings
0	1	V2X_S	BYPASS (Forward mode)
0	0	V2X_S	Divide
1	X	V1X_S	BYPASS (Reverse mode) / Multiply

Note 1 If PVC is on, any change in CHARGE_DIRECTION or BYPASS bits will not be registered until PVC turns off.

5.2.2 Power Good Protection and Fault Generation

The purpose of the power good (PG) protection is to detect when the input-to-output voltage is within a safe operating window, defined by V_{PG_NEG} and V_{PG_POS} thresholds, see conditions for PG comparators (V_{PG_NEG_SW}, V_{PG_POS_SW}, V_{PG_NEG_BYP}, V_{PG_POS_BYP}) in .

DA9353 has two sets of PG comparators:

- PG_NEG with V1X_S positive input and V2X_S negative input
- PG_POS with V2X_S positive input and V1X_S negative input

Both comparators are used to detect a PG fault or to assist with start-up during the state transitions. Each comparator has OTP configuration settings and trimming capabilities.

The PG_NEG and PG_POS comparators output a 1 if the operating conditions on V2X_S and V1X_S are considered within safe limits for the PVC (ratio is less than the PG comparator threshold).

A PG fault is generated if at least one of the comparators outputs a 0 while the PVC is in BYPASS or SWITCHING state.

5.2.3 Over-Current Protection

DA9353 features bi-directional current protection for protecting over-current in both forward and reverse direction. If a high current is sensed the OCP comparator will trigger a fault condition. The OCP comparator has 3-bit programmability for over-current selection for SWITCHING state, via bits SEL_OCP, and another 3-bit setting for BYPASS state, via bits SEL_OCP_BYPASS.

NOTE

Do not configure SEL_OCP_BYPASS setting higher than 0x1. Settings above this value will exceed recommended current capability of the PVC.

5.2.4 CFLY Short Protection

In addition to over-current protection, the PVC has a safety feature to protect the flying capacitors from being shorted. This generates a PG fault or OC fault.

Multi-Input Switched Capacitor Converter

5.2.5 CBOOT_OK Monitoring

During certain states (such as BYPASS) of the PVC's FSM, the bootstrap capacitors are being charged using an internal charge pump. The CBOOT_OK comparators (1 and 2) are monitoring the voltage on the bootstrap capacitor. If enough voltage (3 V) is developed across the bootstrap capacitor, the comparator will set CBOOT_OK = 1. The CBOOT_OK signal ensures that high side power FETs are turned on with enough voltage gate drive.

A CBOOT_OK fault is generated if CBOOT_OK = 0 while the PVC is in BYPASS state. CBOOT_OK fault will not be generated in any other PVC state, regardless of the CBOOT_OK output.

5.2.6 QVPS_OK and QVBUSx_OK Monitoring

When any of the three power FETs in the power mux are in the On or Linear state, the gate drive is charged using an internal charge pump. The QVPS_OK and QVBUSx_OK comparators monitor the gate-to-source voltages on these power FETs. If sufficient voltage is developed on the gate (3 V), the comparators will output a 1. These signals ensure that the power FETs are turned on with sufficient gate-source voltages.

A QVPS_OK or QVBUSx_OK fault is generated if the corresponding comparator = 0 while the power FET state is On. The fault will not be generated in any other power FET states (Off or Linear), regardless of the output of the comparator.

5.2.7 Over-Temperature Protection

DA9353 is protected from damage due to excessive power dissipation through thermal shutdown. There are two thresholds concerning thermal protection: thermal critical and thermal re-enable. When T_J is more than T_{OT} (thermal critical or over-temperature threshold), DA9353 enters FAULT state until T_J has dropped below $T_{OT} - T_{OT_HYS}$ (thermal re-enable threshold).

Due to the slow changing nature of T_J , a single comparator with an input hysteresis, T_{OT_HYS} , is included. To reduce current consumption, the comparator is turned off during NO POWER and POWERDOWN states.

5.2.8 PVC Timer Fault

This is a fault generated by the PVC's state machine whenever a transitional state timer expires before the condition to exit from that state. This will force the PVC to turn off instead of proceeding to the next state.

5.2.9 Watchdog Timer

DA9353 features a watchdog timer which monitors the host during its operation and disables the PVC if a timeout event occurs.

The watchdog timer is enabled, via I²C, through WD_TIMER_EN. If enabled, the timer is active in STANDBY (when both QVBUS1 and QVBUS2 are enabled) and in ACTIVE.

When enabled, the watchdog timer is loaded with a pre-programmed timeout period and starts decrementing. The timeout period value is selected, via I²C, in WD_TIMER_SEL.

When the watchdog timer is on, the host is expected to issue an I²C transaction to DA9353 before the end of the timeout period. The I²C transaction re-starts the watchdog timer by over-writing a new value to WD_TIMER_SEL.

However, if the host does not issue the transaction within the timeout period, and DISABLE_WD_TO_EVENT is not set:

1. A timeout event occurs.
2. WD_TO_EVENT is asserted, unless masked by MASK_WD_TO_EVENT.
3. If the system is in ACTIVE state, the PVC is disabled and the system transitions to STANDBY.
4. In the system is in STANDBY state, QVBUS1 and QVBUS2 are disabled.
5. A watchdog timer fault is indicated by the WD_TO_STATUS bit.

Multi-Input Switched Capacitor Converter

NOTE

The registers bits WD_TIMER_SEL and WD_TIMER_EN are password protected. I²C access is required to unlock these bits. Write 0x3D to address 0xB541.

5.2.10 nIRQ Fault

nIRQ is an active low, open drain output signal that indicates an interrupt has occurred. The related event and status information, such as warnings about temperature and voltages, over-current fault conditions, or status changes is available in the EVENT and STATUS registers.

The EVENT registers hold information about the events that have occurred. The conditions that are triggering the events are described in the individual event bit descriptions within the EVENT register tables, see [Table 34](#) and [Table 35](#). When an event bit is set the nIRQ signal is asserted, unless this event is masked by the appropriate MASK register.

The masked bits only mask the nIRQ assertion, and do not suppress the event generation. The nIRQ is not released until all event bits are cleared by writing a 1 to the appropriate EVENT register bits.

The assertion of the following conditions results in an nIRQ generation:

- VPSOUT_UV_OK
- QVBUS1_FAULT
- QVBUS2_FAULT
- QVPS_FAULT
- VPSOUT_OV_FAULT
- VPSOUT_UV_FAULT
- PG_FAULT
- CBOOT_FAULT
- OC_FAULT
- OV_FAULT
- UV_FAULT
- OT_FAULT
- CFLY_SHORT_FAULT
- CP_TIMER_FAULT
- SYS_RESET
- WD_TO_EVENT

The following status or events prevent the PVC from turning on (in STANDBY state):

- QVBUS1_FAULT_STATUS
- QVBUS2_FAULT_STATUS
- UV_STATUS
- WD_TO_STATUS
- OV_STATUS
- OT_STATUS
- AUTO_FAULT_RECOVERY

The following faults disable the PVC (in ACTIVE state):

- QVBUS1_FAULT_STATUS
- QVBUS2_FAULT_STATUS
- UV_STATUS
- OC_STATUS
- OV_STATUS
- WD_TO_STATUS
- OT_STATUS
- PG_FAULT_STATUS
- CBOOT_FAULT_STATUS
- CFLY_SHORT_FAULT_STATUS
- CP_TIMER_FAULT_STATUS

The following faults disable the QVBUSx FETs (in STANDBY or ACTIVE state):

- OV_FAULT_STATUS
- WD_TO_STATUS

The following faults prevent QVPS FET from turning on:

- VPSOUT_UV_FAULT_STATUS
- VPSOUT_OV_FAULT_STATUS
- OT_FAULT_STATUS

Multi-Input Switched Capacitor Converter

5.2.11 AVDD Internal Voltage Regulator

The AVDD supply is a 4 V rail internally generated by DA9353 for the internal analog and digital supply. It is always enabled except in NO POWER state.

AVDD is the only regulator with an external bypass capacitor at port AVDD. Power supplied for AVDD is derived from two possible power ports (V2X or V1X) via ports V2X_S and V1X_S. Depending on which voltage is higher, supply to the regulator rail is automatically switched. If the highest available voltage supplied for AVDD does not exceed $V_{THR_UPPER_POR}$, DA9353 remains in a NO POWER state and no internal circuitry is active.

For $V1X < 4.2$ V and $AVDD > V_{THR_LWR_POR}$, the LDO operates in dropout mode, to minimize quiescent current.

5.2.12 Low Power Operation

Low quiescent current operating modes are available in DA9353 for POWERDOWN, BYPASS (Forward and Reverse), and STANDBY states.

NOTE
When configuring the PVC for low quiescent current conditions, it is the responsibility of the application to ensure that the discharge FETs are not activated when the power mux or power switches are disabled.

Once activated, the PVC will draw additional current if there is a valid input voltage present at the travel adapter or wireless power input. If voltage is applied at V1X instead, there is no additional current drawn and the PVC operates in the low quiescent current setting. The conditions for activating a discharge FET is based on the power mux/switch being de-asserted, system is ready (STANDBY or ACTIVE state), and the discharge register bits are enabled. The register bits for controlling the appropriate discharge FETs are defined in PVC_CTRL_2 register, see [Table 32](#).

In addition to controlling the discharge FETs, the gate pulldowns on VBUS1 and VBUS2 must be set appropriately via PMUX3 register. If the gate pulldowns are enabled in POWERDOWN, the quiescent current will be high. To avoid this, the pulldowns must be disabled ($DIS_GATESTRPD_VBUS1$ and $DIS_GATESTRPD_VBUS2 = 0x1$) in POWERDOWN and enabled ($DIS_GATESTRPD_VBUS1$ and $DIS_GATESTRPD_VBUS2 = 0x0$) in any state other than POWERDOWN.

Multi-Input Switched Capacitor Converter

6 Control Interface

I²C is always enabled in ACTIVE or STANDBY and IOs run on AVDD.

DA9353 can be software controlled through an I²C serial control interface. Data are shifted into or out of DA9353 under the control of the host processor that also provides the serial clock. In a normal application case the interface is only configured once from OTP values, which are loaded during the initial start-up of DA9353. In this phase the I²C slave address is loaded from OTP.

6.1 I²C Communication

DA9353 has an OTP configurable 7-bit I²C slave address (default: 0x70) which can be configured in the register field I2C_SLAVE_ADDRESS.

The SCL port functions as the I²C clock and the SDA port carries the bi-directional I²C data.

The I²C interface is open drain supporting multiple devices on a single line. The bus lines have to be pulled high by external pull-up resistors (2 kΩ to 20 kΩ range). The devices connected to the I²C SDA can only drive the bus line low to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. The highest frequency of the bus is 1000 kHz. With asserted control I2C_TIMEOUT_EN an automatic interface RESET can be triggered when the SDA and SCL signal ceases to toggle for > 35 ms (compatible with SMBus t_{TIMEOUT}).

The interface supports an operation compatible with Standard-mode, Fast-mode, and Fast-mode Plus protocols, see I²C-Bus Specification Rev 6, [1].

The communication on the I²C bus always takes place between two devices, one acting as the master and the other as the slave. The DA9353 will only operate as a slave.

6.2 I²C Control Bus Protocol

Data are transmitted over the I²C bus in groups of eight bits. To send a bit the SDA line is driven to the intended state while the SCL is low (for example, a low on SDA indicates a zero bit). Once the SDA has settled the SCL line is brought high and then low. This pulse on SCL clocks the SDA bit into the receivers shift register.

DA9353 uses a 3-byte serial protocol which contains two bytes for the address and one byte for data. Data and address transfer is based on the MSB transmitted first for both read and write operations. All transmission begins with the START condition from the master as long as the bus is in IDLE state (the bus is free). The START condition is defined as a high to low transition at the SDA line while the SCL is high. The STOP condition is defined as a low to high transition at the SDA line while the SCL is high.

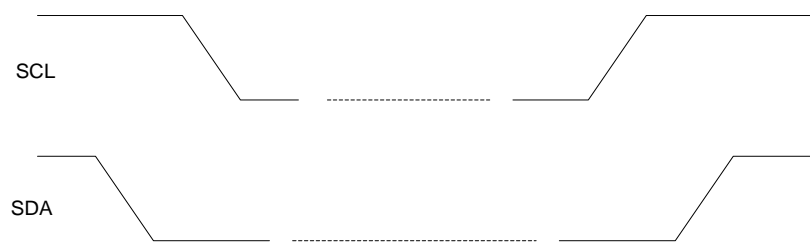


Figure 12: Timing of I²C START and STOP Condition

The I²C bus will be monitored by DA9353 for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. This acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 13 and Figure 14).

The protocol for a register write from master to slave consists of a START condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes responded to by DA9353 with Acknowledge):

Multi-Input Switched Capacitor Converter

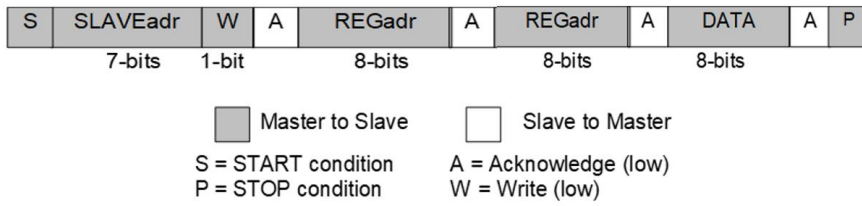


Figure 13: I²C Byte Write (SDA Line)

When the host reads data from a register it first has to write access DA9353 with the target register address and then read access DA9353 with a Repeated START or alternatively a second START condition. After receiving the data, the host sends No Acknowledge and terminates the transmission with a STOP condition:

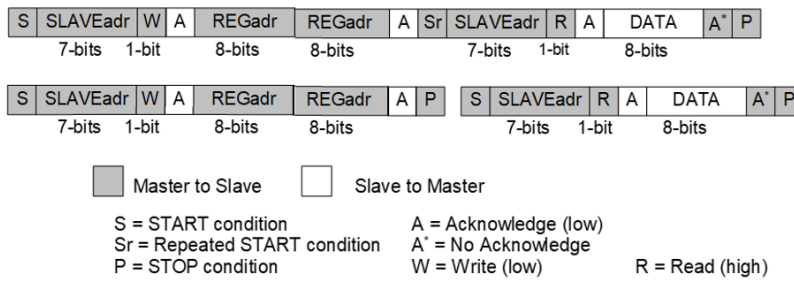


Figure 14: I²C Byte Read (SDA Line)

Multi-Input Switched Capacitor Converter

7 Register Definitions

7.1 Register Map

Table 17: Register Map

Address	Register	Description
0x0002	STATUS_B	FSM and HW/SW modes
0x0003	REV_ID	Revision code
0x0004	VENDOR_ID	Specific vendor ID
0x0005	CONFIG_ID	Target application ID
0x000B	ONKEY_CONFIG_1	Auto fault recovery
0x000D	SYS_CONFIG_1	System configuration byte 1
0x000E	SYS_CONFIG_2	System configuration byte 2
0x0013	MASK_FAULT_CONFIG	Mask fault configuration byte 1
0x0014	MASK_FAULT_CONFIG_B	Mask fault configuration byte 2
0x0015	DISABLE_FAULT_CONFIG	Protection disable byte 1
0x0016	DISABLE_FAULT_CONFIG_B	Protection disable byte 2
0x0017	PVC_CONFIG	PVC configuration
0x0018	SYS_CTRL_1	System control byte 1
0x001C	PVC_CTRL_1	PVC control byte 1
0x001D	PVC_CTRL_2	PVC control byte 2
0x001F	SYS_STATUS	System Status byte 1
0x0022	PVC_EVENT	PVC event byte 1
0x0023	PVC_EVENT_B	PVC event byte 2
0x0024	PVC_STATUS	PVC status byte 1
0x0025	PVC_STATUS_B	PVC status byte 2
0x0026	PVC_STATUS_C	PVC status byte 3
0x0027	EVENT_LOG	Event logger
0x0039	I2C_SLAVE_ADDRESS	I2C communication slave address
0x0113	ANABIAS4	Analog bias byte 1
0x0114	ANABIAS5	Analog bias byte 2
0x0210	PROTECTION1	Protections byte 1
0x0311	PROTECTION10	Protections byte 2
0x0312	PROTECTION11	Protections byte 3
0x0511	PMUX2	Power mux. threshold settings for VPS switch
0x0512	PMUX3	Power mux gates disable settings

Table 18: STATUS_B (0x0002)

Bit	Mode	Symbol	Description	Reset
7:6	RO	RESERVED		0x0

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
5:2	RO	SYS_CTRL_STATE_READBACK	Readback Sys Ctrl FSM States 0: POWERDOWN 1: ACTIVE 2: FAULT_TIME 3: FAULT_RECOVERY 4:5 RESERVED 6: STANDBY 7:15 RESERVED	0x0
1:0	RO	RESERVED		0x0

Table 19: REV_ID (0x0003)

Bit	Mode	Symbol	Description	Reset
7:4	RO	MAJREV	Major revision code	0xA
3:0	RO	MINREV	Minor revision code	0xD

Table 20: VENDOR_ID (0x0004)

Bit	Mode	Symbol	Description	Reset
7:0	RO OTP	VENDOR_ID	Specific Vendor ID	0x0

Table 21: CONFIG_ID (0x0005)

Bit	Mode	Symbol	Description	Reset
7:2	R/W OTP	CONFIG_ID	ID for customer and target application platform, written during production of variant (OTP variant)	0x0
1:0	R/W OTP	VARIANT_ID	Variant_ID (DA part number)	0x0

Table 22: ONKEY_CONFIG_1 (0x000B)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	RESERVED		0x1
6	R/W OTP	AUTO_FAULT_RECOVERY	This bit determines the auto start of the PVC in case of previous faults. 0x0: The host needs to clear all asserted events to allow the device to go back into ACTIVE state 0x1: No host intervention is required. The device will re-enable itself if the faults go away. The events are still held.	0x1
5:4	R/W OTP	RESERVED		0x1
3:0	R/W OTP	RESERVED		0xD

Multi-Input Switched Capacitor Converter

Table 23: SYS_CONFIG_1 (0x000D)

Bit	Mode	Symbol	Description	Reset
7:4	R/W OTP	RESERVED		0x1
3:1	R/W OTP	RESERVED		0x4
0	R/W OTP	VPSOUT_PRIORITY	This bit determines if autonomous startup on QVBUS2 is needed 0x0: No autonomous startup on QVBUS2 0x1: Autonomous startup enable on QVBUS2. QVBUS2 can enable when VPSOUT_UV is high. When VPSOUT_UV goes low, QVBUS2 disables	0x0

Table 24: SYS_CONFIG_2 (0x000E)

Bit	Mode	Symbol	Description	Reset
7:6	R/W OTP	SPREAD_WIDTH	Spreading of oscillator frequency during spread spectrum 0x0: $\pm 2\%$ 0x1: $\pm 4\%$ 0x2: $\pm 8\%$ 0x3: $\pm 16\%$	0x3
5	R/W OTP	SPREAD_EN	Spread spectrum enable 0x0: Off 0x1: On	0x0
4:3	R/W OTP	RESERVED		0x0
1:2	R/WC OTP	WD_TIMER_SEL	Watchdog timer timeout period value 0x0: 5 s 0x1: 9 s 0x2: 17 s 0x3: 33 s	0x3
0	R/WC OTP	WD_TIMER_EN	Watchdog timer enable 0x0: Disabled 0x1: Enabled	0x0

Table 25: MASK_FAULT_CONFIG (0x0013)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	MASK_OV_FAULT	Mask the over-voltage fault 0x0: Mask disabled 0x1: Mask enabled	0x0
6	R/W OTP	MASK_UV_FAULT	Mask the under-voltage fault 0x0: Mask disabled 0x1: Mask OV fault enabled	0x0
5	R/W OTP	MASK_OT_FAULT	Mask the over-temperature fault 0x0: Mask disabled 0x1: Mask OT fault enabled	0x0
4	R/W	MASK_OC_FAULT	Mask the over-current fault	0x0

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
	OTP		0x0: Mask disabled 0x1: Mask OC fault enabled	
3	R/W OTP	MASK_CBOOT_FAULT	Mask the CBOOT fault 0x0: Mask disabled 0x1: Mask CBOOT fault enabled	0x0
2	R/W OTP	MASK_QVBUS1_FAULT	Mask the QVBUS1 fault 0x0: Mask disabled 0x1: Mask QVBUS1 fault enabled	0x0
1	R/W OTP	MASK_QVBUS2_FAULT	Mask the QVBUS2 fault 0x0: Mask disabled 0x1: Mask QVBUS2 fault enabled	0x0
0	R/W OTP	MASK_QVPS_OK	Mask the QVPS fault 0x0: Mask disabled 0x1: Mask QVPS fault enabled	0x0

Table 26: MASK_FAULT_CONFIG_B (0x0014)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	MASK_WD_TO_EVENT	Mask watchdog timeout event	0x0
6	R/W OTP	MASK_SYS_RESET_EVENT	Mask SYS_RESET event	0x0
5	R/W OTP	MASK_VPSOUT_UV_OK	Mask VPSOUT_UV_OK condition 0x0: Mask disabled 0x1: Mask VPSOUT_UV_OK event enabled	0x0
4	R/W OTP	MASK_VPSOUT_UV_FAULT	Mask VPSOUT_UV fault condition 0x0: Mask disabled 0x1: Mask VPSOUT_UV fault enabled	0x0
3	R/W OTP	MASK_VPSOUT_OV_FAULT	Mask VPSOUT_OV fault 0x0: Mask disabled 0x1: Mask VPSOUT_OV fault enabled	0x0
2:1	R/W OTP	RESERVED		0x0
0	R/W OTP	MASK_PG_FAULT	Mask PG fault 0x0: Mask disabled 0x1: Mask PG fault enabled	0x0

Table 27: DISABLE_FAULT_CONFIG (0x0015)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	DISABLE_OV_FAULT	Disable OV fault	0x0
6	R/W OTP	DISABLE_UV_FAULT	Disable UV fault	0x0
5	R/W OTP	DISABLE_OT_FAULT	Disable OT fault	0x0
4	R/W OTP	DISABLE_OC_FAULT	Disable OC fault	0x0
3	R/W OTP	DISABLE_CBOOT_FAULT	Disable CBOOT fault	0x0
2	R/W OTP	DISABLE_QVBUS1_FAULT	Disable QVBUS1 fault	0x0
1	R/W OTP	DISABLE_QVBUS2_FAULT	Disable QVBUS2 fault	0x0
0	R/W OTP	DISABLE_QVPS_FAULT	Disable QVPS fault	0x0

Multi-Input Switched Capacitor Converter

Table 28: DISABLE_FAULT_CONFIG_B (0x0016)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	DISABLE_WD_TO_EVENT	Disable watchdog timeout fault	0x0
6:5	R/W OTP	RESERVED		0x0
4	R/W OTP	DISABLE_VPSOUT_OV_FAULT	Disable VPSOUT_OV fault	0x0
3	R/W OTP	DISABLE_VPSOUT_UV_FAULT	Disable VPSOUT_UV fault	0x0
2:1	R/W OTP	RESERVED		0x1
0	R/W OTP	DISABLE_PG_FAULT	Disable PG fault	0x0

Table 29: PVC_CONFIG (0x0017)

Bit	Mode	Symbol	Description	Reset
7:6	R/W OTP	RESERVED		0x3
5	R/W OTP	BYPASS	PVC BYPASS state 0x0: BYPASS state disabled 0x1: BYPASS state enabled	0x0
4	R/W OTP	PVC_EN	Enable or disable the PVC. 0x0: PVC disabled 0x1: PVC enabled	0x0
3:1	R/W OTP	FSW	Set the PVC switching frequency 0x0: 50 kHz 0x1: 200 kHz 0x2: 300 kHz 0x3: 375 kHz 0x4: 430 kHz 0x5: 600 kHz 0x6: 750 kHz 0x7: 1 MHz	0x2
0	R/W OTP	CHARGE_DIRECTION	0x0: Forward mode 0x1: Reverse mode	0x0

Table 30: SYS_CTRL_1 (0x0018)

Bit	Mode	Symbol	Description	Reset
7:2	R/W	RESERVED		0x0
1	R/W	POWERDOWN	Forced POWERDOWN state when asserted from I ² C write. Automatically cleared from wake-up 0x0: POWERDOWN enabled 0x1: POWERDOWN not enabled	0x0
0	R/W	SOFT_RESET	When asserted, triggers a power cycle and a reset of all internal registers, followed by an OTP download. Note: When the PVC is in Multiply mode (CHARGE_DIRECTION = Reverse mode and BYPASS = Disabled), DISABLE_OV_FAULT setting should be set to 0x1 before SOFT_RESET is asserted. 0x0: Not enabled 0x1: Enabled	0x0

Multi-Input Switched Capacitor Converter

Table 31: PVC_CTRL_1 (0x001C)

Bit	Mode	Symbol	Description	Reset
7:6	R/W OTP	QVPS_SS_TIMER	Power switch soft start timer 0x0: 1 ms 0x1: 6 ms 0x2: 12 ms 0x3: 24 ms	0x1
5:4	R/W OTP	QVBUS1_SS_TIMER	PMUX soft start timer on QVBUS1 0x0: 1 ms 0x1: 6 ms 0x2: 12 ms 0x3: 24 ms	0x1
3:2	R/W OTP	QVBUS2_SS_TIMER	PMUX soft start timer on QVBUS2 0x0: 1 ms 0x1: 6 ms 0x2: 12 ms 0x3: 24 ms	0x1
1	R/W OTP	EN_VPSOUT_UV	This bit will enable the VPSOUT under-voltage comparator 0x0: Disabled 0x1: Enabled	0x1
0	R/W OTP	EN_VPSOUT_OV	This bit will enable the VPSOUT over-voltage comparator 0x0: Disabled 0x1: Enabled	0x1

Table 32: PVC_CTRL_2 (0x001D)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	EN_QVPS	Enable for VPS power switch 0x0: Disabled 0x1: Enabled	0x0
6	R/W OTP	EN_QVBUS1	Enable for VBUS1 power switch 0x0: Disabled 0x1: Enabled	0x0
5	R/W OTP	EN_QVBUS2	Enable for VBUS2 power switch 0x0: Disabled 0x1: Enabled	0x0
4	R/W OTP	VPSIN_DISCH	VPSIN discharge 0x0: Disabled 0x1: Enabled	0x0
3	R/W OTP	RESERVED		0x0
2	R/W OTP	RESERVED		0x0
1	R/W OTP	V1X_DISCH_OVR_VALUE	V1X discharge override value. This bit is active when bit [0] is high 0x0: Disabled 0x1: Enabled	0x0

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
0	R/W OTP	V1X_DISCH_OVR_EN	V1X discharge override enable 0x0: Disabled 0x1: Enabled	0x0

Table 33: SYS_STATUS (0x001F)

Bit	Mode	Symbol	Description	Reset
7:4	RO	RESERVED		0x0
3:0	RO	PVC_STATE	Monitors the state of the PVC 0x0: PVC OFF 0x5: BYPASS 0xF: SWITCHING	0x0

Table 34: PVC_EVENT (0x0022)

Bit	Mode	Symbol	Description	Reset
7	RW1C	OV_FAULT_EVENT	Over-voltage event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
6	RW1C	UV_FAULT_EVENT	Under-voltage event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
5	RW1C	OT_FAULT_EVENT	Over-temperature event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
4	RW1C	OC_FAULT_EVENT	Over-current event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
3	RW1C	CBOOT_FAULT_EVENT	V _{CBSx} voltage is not high enough to drive power FET gate 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
2	RW1C	QVBUS1_FAULT_EVENT	VBUS1 Power switch is not ready 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
1	RW1C	QVBUS2_FAULT_EVENT	VBUS2 Power switch is not ready 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
0	RW1C	QVPS_FAULT_EVENT	VPS power switch is not ready 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0

Table 35: PVC_EVENT_B (0x0023)

Bit	Mode	Symbol	Description	Reset
7	RW1C	WD_TO_EVENT	Event to indicate that the watchdog timer has expired. This is a fault. Write a 1 to clear.	0x0

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
6	RW1C	SYS_RESET_EVENT	Event to indicate that the system has undergone a reset (POR or I2C triggered). This is not a fault. 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
5	RW1C	VPSOUT_UV_OK_EVENT	Event to indicate VPSOUT voltage is valid 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
4	RW1C	VPSOUT_UV_FAULT_EVENT	VPSOUT under-voltage event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
3	RW1C	VPSOUT_OV_FAULT_EVENT	VPSOUT over-voltage event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
2	RW1C	CP_TIMER_FAULT_EVENT	Indicates a charge pump timer fault event 0x0: No event has occurred 0x1: Event has occurred. Write a 1 to clear	0x0
1	RW1C	RESERVED		0x0
0	RW1C	PG_FAULT_EVENT	Power good signal fault in SWITCHING state (Multiply and Divide modes) or BYPASS state (Forward and Reverse modes). Write 0x1 to clear. 0x0: No event has occurred 0x1: Event has occurred	0x0

Table 36: PVC_STATUS (0x0024)

Bit	Mode	Symbol	Description	Reset
7	RO	OC_FAULT_STATUS	0x0: No fault 0x1: Indicates an over-current condition	0x0
6	RO	OV_FAULT_STATUS	0x0: No fault 0x1: Indicates an over-voltage condition	0x0
5	RO	UV_FAULT_STATUS	0x0: No fault 0x1: Indicates an under-voltage condition	0x0
4	RO	OT_FAULT_STATUS	0x0: No fault 0x1: Indicates an over-temperature condition	0x0
3	RO	CBOOT_FAULT_STATUS	0x0: No fault 0x1: Indicates CBOOT fault is active	0x0
2	RO	QVBUS1_FAULT_STATUS	0x0: No fault 0x1: Indicates QVBUS1 fault is active	0x0
1	RO	QVBUS2_FAULT_STATUS	0x0: No fault 0x1: Indicates QVBUS2 fault is active	0x0
0	RO	QVPS_FAULT_STATUS	0x0: No fault 0x1: Indicates QVPS fault is active	0x0

Multi-Input Switched Capacitor Converter

Table 37: PVC_STATUS_B (0x0025)

Bit	Mode	Symbol	Description	Reset
7	RO	WD_TO_STATUS	A 1 on this indicates a VPSOUT under-voltage condition. This can be considered as a fault.	0x0
6:5	RO	RESERVED		0x0
4	RO	VPSOUT_UV_FAULT_STATUS	Indicates a VPSOUT under-voltage fault 0x0: No fault 0x1: Fault	0x0
3	RO	VPSOUT_OV_FAULT_STATUS	Indicates a VPSOUT over-voltage fault 0x0: No fault 0x1: Fault	0x0
2	RO	CP_TIMER_FAULT_STATUS	Indicates a PVC timeout fault 0x0: No fault 0x1: Fault	0x0
1	RO	RESERVED		0x0
0	RO	PG_FAULT_STATUS	Indicates a fault when the PVC is in SWITCHING state or in BYPASS state and at least one of the comparators is de-asserted. 0x0: No fault 0x1: Fault	0x0

Table 38: PVC_STATUS_C (0x0026)

Bit	Mode	Symbol	Description	Reset
7	RO	NIRQ	Reflects the status of the nIRQ pin (active low). 0x0: IRQ is on 0x1: IRQ is off	0x0
6	RO	RESERVED		0x0
5	RO	PVC_EN_STATUS	PVC enable (final control going to PVC) 0x0: PVC not enabled 0x1: PVC enabled	0x0
4	RO	SWITCHING_STATUS	Indicates if PVC is in 2:1 or 1:1 mode 0x0: BYPASS state 0x1: SWITCHING state (1:2 or 2:1)	0x0
3	RO	DIRECTION_STATUS	Indicates the direction of operation 0x0: Forward mode 0x1: Reverse mode	0x0
2	RO	QVPS_ON	Read out of raw analog signal 0x0: QVPS is not fully on 0x1: QVPS is on	0x0
1	RO	QVBUS1_ON	Read out of raw analog signal 0x0: QVBUS1 is not fully on 0x1: QVBUS1 is on	0x0
0	RO	QVBUS2_ON	Read out of raw analog signal	0x0

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
			0x0: QVBUS2 is not fully on 0x1: QVBUS2 is on	

Table 39: EVENT_LOG (0x0027)

Bit	Mode	Symbol	Description	Reset
7:4	RO	RESERVED		0x0
3:0	RO	FIRST_EVENT_LOG	First event logger 0x0: N/A 0x1: CP_TIMER_EVENT 0x2: CFLY_SHORT_EVENT 0x3: OT_FAULT_EVENT 0x4: UV_FAULT_EVENT 0x5: OV_FAULT_EVENT 0x6: OC_FAULT_EVENT 0x7: CBOOT_OK_FAULT_EVENT 0x8: PG_FAULT_EVENT 0x9: VPSOUT_UV_FAULT_EVENT 0x10: VPSOUT_OV_FAULT_EVENT 0x11: QVPS_FAULT_EVENT 0x12: QVBUS2_FAULT_EVENT 0x13: QVBUS1_FAULT_EVENT 0x14: WD_TIMEOUT_FAULT_EVENT 0x15: N/A	0x0

Table 40: I2C_SLAVE_ADDR (0x0039)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	I2C_TIMEOUT_EN	Enable automatic reset of I2C interface (if SCL stays low for greater than 35 ms) 0x0: I2C timeout disabled 0x1: I2C timeout enabled	0x0
6:0	R/W OTP	I2C_SLAVE_ADDR	7-bit I2C slave address. Default is 7'h70. If user wants to change I2C slave ID, overwrite the I2C Slave ID as last register to program before OTP program so that other registers are not affected.	0x70

Table 41: ANABIAS4 (0x0113)

Bit	Mode	Symbol	Description	Reset
7:5	R/W OTP	SEL_OCP	V2X over-current protection comparator threshold in SWITCHING state. 0x0: 1625 mA 0x1: 2125 mA 0x2: 2625 mA 0x3: 3125 mA 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	0x3

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
4:3	R/W OTP	RESERVED		0x2
2:0	R/W OTP	RESERVED		0x2

Table 42: ANABIAS5 (0x0114)

Bit	Mode	Symbol	Description	Reset
7:3	R/W OTP	RESERVED		0x0
2:0	R/W OTP	SEL_OCP_BYPASS	V2X over-current protection comparator threshold in BYPASS state. 0x0: 3250 mA 0x1: 3500 mA 0x2: 3750 mA 0x3: 4000 mA 0x4: Reserved 0x5: Reserved 0x6: Reserved 0x7: Reserved	0x0

Table 43: PROTECTION1 (0x0210)

Bit	Mode	Symbol	Description	Reset
7:5	R/W OTP	SELPG1	SELPG1 upper threshold selection (mV) 0x0: 100 0x1: 150 0x2: 200 0x3: 250 0x4: 300 0x5: 350 0x6: 400 0x7: 450	0x4
4:2	R/W OTP	SELPG2	SELPG2 lower threshold selection (mV) 0x0: 100 0x1: 150 0x2: 200 0x3: 250 0x4: 300 0x5: 350 0x6: 400 0x7: 450	0x4
1:0	R/W OTP	RESERVED		0x3

Table 44: PROTECTION10 (0x0311)

Bit	Mode	Symbol	Description	Reset
7:6	R/W OTP	SEL_UV	Modifies the VREF2X threshold selection 0x0: V2X UVP = 7 V, V1X UVP = 3.2 V, BYPASS UVP = 3.2 V	0x0

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
			0x1: V2X UVP = 8 V, V1X UVP = 3.6 V, BYPASS UVP = 3.6 V 0x2: V2X UVP = 9 V, V1X UVP = 4 V, BYPASS UVP = 4 V 0x3: V2X UVP = 10 V, V1X UVP = 4.4 V, BYPASS UVP = 4.4 V	
5:0	R/W OTP	RESERVED		0x0

Table 45: PROTECTION11 (0x0312)

Bit	Mode	Symbol	Description	Reset
7	R/W OTP	RESERVED		0x0
6:5	R/W OTP	SEL_OVP_MULT	Sets a voltage input level for the comparator in reverse direction 0x0: V1X OVP = 9.5 V 0x1: V1X OVP = 10 V 0x2: V1X OVP = 10.5 V 0x3: V1X OVP = 11 V	0x3
4:3	R/W OTP	SEL_OVP	Sets a voltage input level for the comparator in forward direction 0x0: V2X OVP = 19 V, V1X OVP = 12 V, BYPASS OVP = 12 V 0x1: V2X OVP = 20 V, V1X OVP = 13 V, BYPASS OVP = 13 V 0x2: V2X OVP = 21 V, V1X OVP = 13.5 V, BYPASS OVP = 13.5 V 0x3: V2X OVP = 22 V, V1X OVP = 14 V, BYPASS OVP = 14 V	0x3
2:0	R/W OTP	RESERVED		0x0

Table 46: PMUX2 (0x0511)

Bit	Mode	Symbol	Description	Reset
7:4	R/W OTP	RESERVED		0x0
3:2	R/W OTP	SEL_VPSOUT_OV	Selects OV level for VPSOUT (V) 0: 12 1: 13 2: 13.5 3: 14	0x0
1:0	R/W OTP	SEL_VPSOUT_UV	Selects UV level for VPSOUT (V) 0: 3.2 1: 3.6 2: 4 3: 4.4	0x0

Table 47: PMUX3 (0x0512)

Bit	Mode	Symbol	Description	Reset
7:4	R/W OTP	RESERVED		0x0

Multi-Input Switched Capacitor Converter

Bit	Mode	Symbol	Description	Reset
3	R/W OTP	DIS_GATESTRPD_VBUS1	Gate pull down control on VBUS1 0: Pull down is on 1: Pull down is off	0x0
2	R/W OTP	DIS_GATESTRPD_VBUS2	Gate pull down control on VBUS2 0: Pull down is on 1: Pull down is off	0x0
1:0	R/W OTP	RESERVED		0x0

Multi-Input Switched Capacitor Converter

8 Package Information

8.1 Package Outline

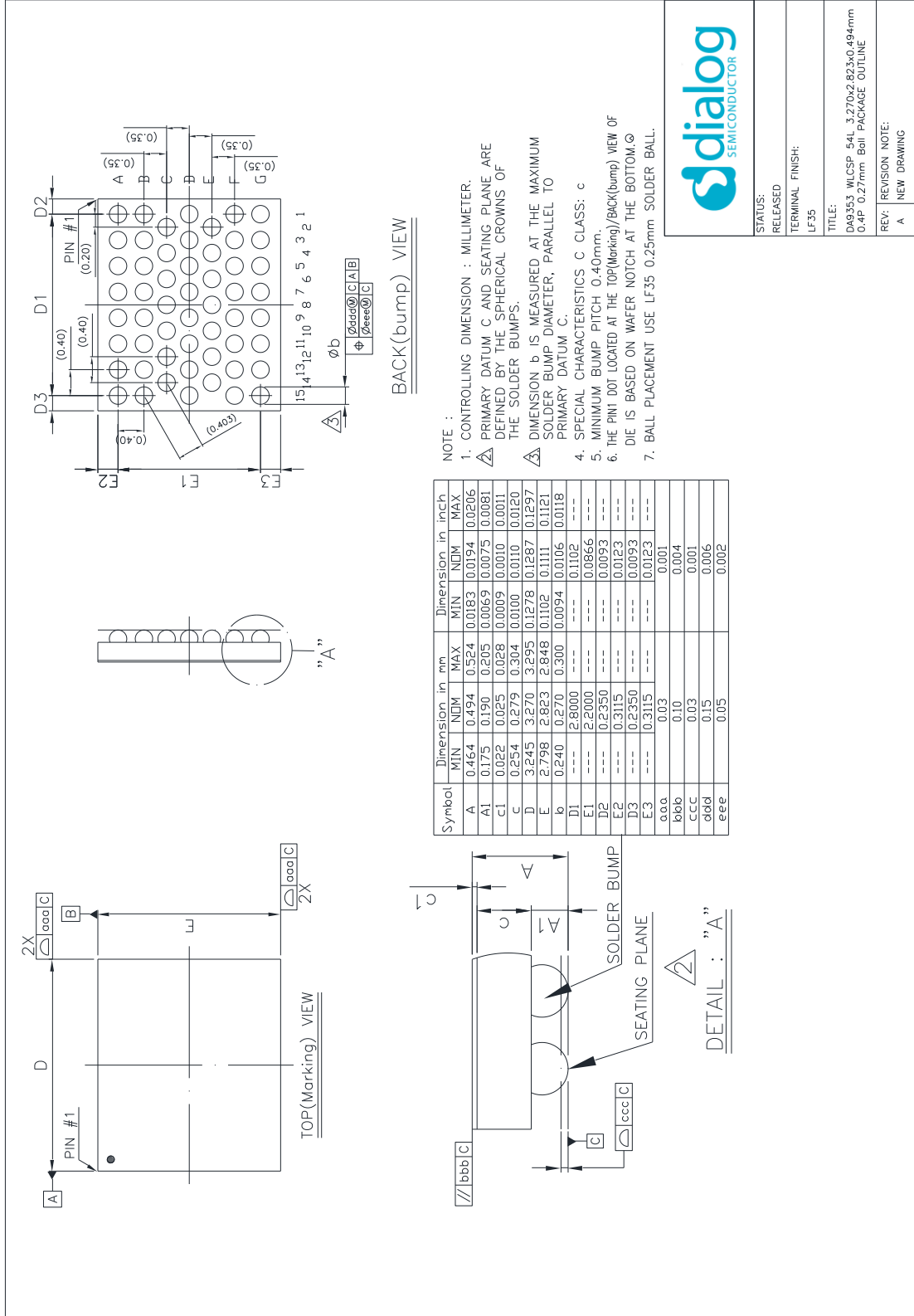


Figure 15: WLCSP Package Outline Drawing

Multi-Input Switched Capacitor Converter

8.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in [Table 48](#).

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from <http://www.jedec.org>.

The WLCSP package is qualified for MSL 1.

Table 48: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

8.3 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore, a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

8.4 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from <http://www.jedec.org>.

Multi-Input Switched Capacitor Converter

9 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas [local sales representative](#).

Table 49: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
DA9353-xxOV2	WLCSP54	3.270 x 2.823 x 0.494	Tape and reel	7500

Part Number Legend:

DA9353-xxOV2

xx: OTP variant

10 Application Information

10.1 Recommended External Components

10.1.1 Capacitor Selection

Use ceramic capacitors as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, take the DC bias characteristic into account.

Table 50: Recommended External Capacitors

Application	Value	Size	Tol (%)	Rated Voltage (V)	Type
C _{FLY1} , C _{FLY2}	2 x 22 μ F	0603	\pm 20	16	Samsung CL10A226MO7JZNC
C _{V2X}	4.7 μ F	0603	\pm 10	35	Murata GRM188R6YA475KE15
C _{V1X}	4.7 μ F	0603	\pm 10	25	TDK C1608X5R1E475K080AC
Alternative C _{V1X}	4.7 μ F	0603	\pm 20	16	Murata GRM188R61C475ME11
C _{VBUS1} , C _{VBUS2} , C _{VPSOUT} , C _{VPSIN}	1 μ F	0402	\pm 10	35	Murata GRM155R6YA105KE11
C _{BS1} , C _{BS2}	100 nF	0201	\pm 10	16	Murata GRM033R61C104KE14D
C _{AVDD}	2.2 μ F	0402	\pm 10	6.3	Murata GRM155R61C225KE11D

Multi-Input Switched Capacitor Converter

Status Definitions

Revision	Datasheet Status	Product Status	Definition
1.<n>	Target	Development	This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.
2.<n>	Preliminary	Qualification	This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design.
3.<n>	Final	Production	This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing, and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via http://www.renesas.com/ .
4.<n>	Obsolete	Archived	This datasheet contains the specifications for discontinued products. The information is provided for reference only.

RoHS Compliance

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

Multi-Input Switched Capacitor Converter

Important Notice and Disclaimer

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

© 2023 Renesas Electronics Corporation. All rights reserved.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu

Koto-ku, Tokyo 135-0061, Japan

www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:

<https://www.renesas.com/contact/>

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.