

# DA9213, DA9214, and DA9215

Multi-Phase 5 A/Phase DC-DC Buck Converter

DA9213, DA9214, and DA9215 are PMUs optimized for the supply of CPUs, GPUs, and DDR memory rails in smartphones, tablets and other portable applications. The fast transient response (10 A/ $\mu$ s) and load regulation are optimized for the latest generation of multi core application processors.

DA9213 operates as a single four-phase buck converter delivering up to 20 A output current.

DA9214 integrates two dual-phase buck converters, capable of delivering 2 x 10 A output current.

DA9215 integrates a three-phase buck converter capable of delivering 15 A and a single-phase buck converter delivering 5 A output current.

Each buck regulates a programmable output voltage in the range 0.3 V to 1.57 V. With an external resistor divider, the output voltage can be set to any voltage between 1.57 V and 4.3 V. The input voltage range of 2.8 V to 5.5 V makes it suited for a wide variety of low voltage systems, including all Li-Ion battery powered applications.

To guarantee the highest accuracy and to support multiple PCB routing scenarios without loss of performance, a remote sensing capability is implemented in DA9213, DA9214, and DA9215.

The power devices are fully integrated, so no external FETs or Schottky diodes are needed.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and secures a slope-controlled activation of the rail.

The Dynamic Voltage Control (DVC) supports adaptive adjustment of the supply voltage depending on the processor load, either via direct register writes through the communication interface (I<sup>2</sup>C or SPI compatible) or via an input pin.

DA9213, DA9214, and DA9215 feature integrated over-temperature and over-current protection for increased system reliability without the need for external sensing components. The safety feature set is completed by a VDDIO under-voltage lockout.

The configurable I<sup>2</sup>C address selection via GPI allows multiple instances of DA9213, DA9214, and DA9215 or both to be placed in the application sharing the same communication interface with different addresses.

# **Key Features**

- 2.8 V to 5.5 V input voltage
- 0.3 V to 1.57 V output voltage
- 1.57 V to 4.3 V with resistor divider
- 20 A DA9213
- 2 x 10 A DA9214
- 1 x 15 A + 1 x 5 A DA9215
- 3 MHz nominal switching frequency (allows use of low profile [1 mm] inductors)
- ±1% accuracy (static)
- ±3% accuracy (dynamic) Feature
- Dynamic voltage control
- Automatic phase shedding
- Integrated power switches
- Remote sensing at point of load
- I<sup>2</sup>C/SPI compatible interface
- Adjustable soft start
- -40 °C to +85 °C temperature range
- Package 66 WL-CSP 0.4 mm pitch or 66 VFBGA 0.5 mm pitch

# **Applications**

- TV/media players
- Smartphones
- Tablet PCs
- Ultrabooks
- Mobile computing

# **System Diagrams**

Table 1 shows how the phases of the device are used for different device configurations. It should be noted in particular that the third phase of DA9215 BuckA is phase B2. Phase B1 is used for the single phase BuckB.

Table 1. Buck Allocations for Each Phase per Device

Device	Phase A1	Phase A2	Phase B1	Phase B2
DA9213	BuckA	BuckA	BuckA	BuckA
DA9214	BuckA	BuckA	BuckB	BuckB
DA9215	BuckA	BuckA	BuckB	BuckA

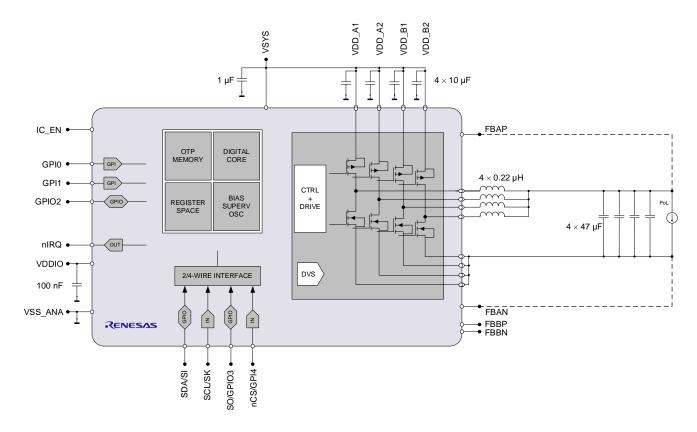


Figure 1. DA9213 System Diagram

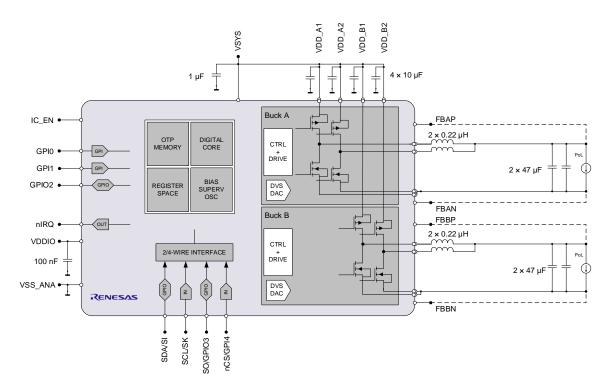


Figure 2. DA9214 System Diagram

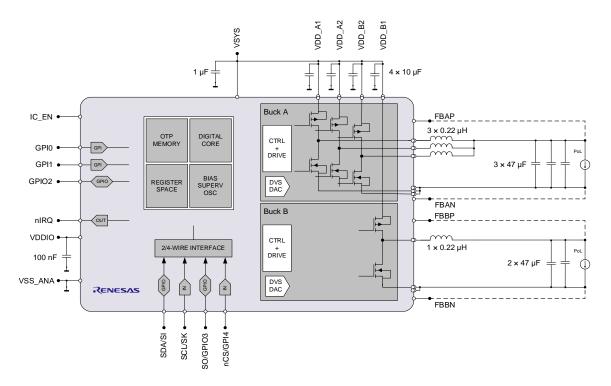


Figure 3. DA9215 System Diagram

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# 1. Terms and Definitions

AP Application processor
CPU Central processing unit

DDR Double data rate (type of SDRAM memory for PCs)

DVC Dynamic voltage control GPU Graphic processing unit

IC Integrated circuit

OTP One-time programmable memory

PCB Printed circuit board

PMIC Power management integrated circuit

POL Point of load

SDRAM Synchronous dynamic random-access memory

# 2. Pin Information

# 2.1 Pin Assignments

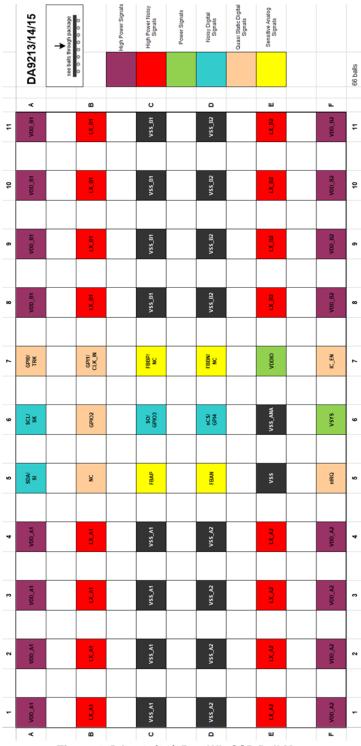


Figure 4. DA9213/14/15 66 WL-CSP Ball Map

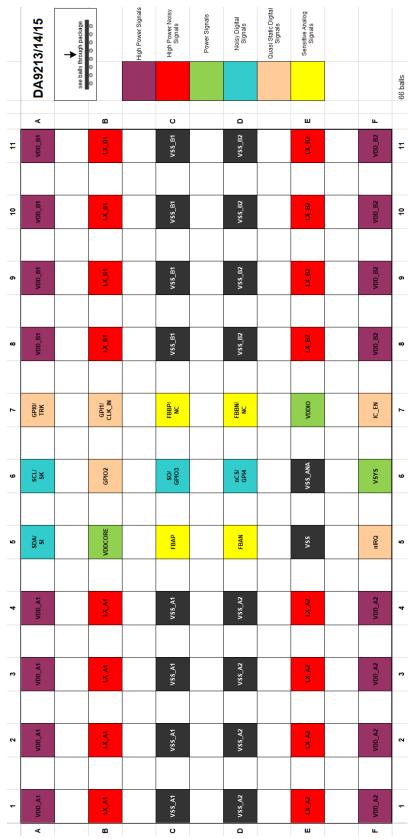


Figure 5. DA9213/14/15 66 VFBGA Ball Map

# 2.2 Pin Descriptions

Table 2. Pin Description

Pin Name	Signal Name	Second Function	Type (Table 3)	Description
B1, B2, B3, B4	LX_A1		AO	Switching node for Buck A phase 1
E1, E2, E3, E4	LX_A2		AO	Switching node for Buck A phase 2
B8, B9, B10, B11	LX_B1		AO	Switching node for Buck B phase 1
E8, E9, E10, E11	LX_B2		AO	Switching node for Buck B phase 2
A1, A2, A3, A4	VDD_A1		PS	Supply voltage for Buck A phase 1 To be connected to VSYS
F1, F2, F3, F4	VDD_A2		PS	Supply voltage for Buck A phase 2 To be connected to VSYS
A8, A9, A10, A11	VDD_B1		PS	Supply voltage for Buck B phase 1 To be connected to VSYS
F8, F9, F10, F11	VDD_B2		PS	Supply voltage for Buck B phase 2 To be connected to VSYS
F7	IC_EN		DI	Integrated Circuit (IC) Enable Signal
F5	nIRQ		DO	Interrupt line towards the host
E7	VDDIO		PS	I/O Voltage Rail
C5	FBAP		Al	Positive sense node for Buck A
D5	FBAN		Al	Negative sense node for Buck A
C7	FBBP		Al	Positive sense node for Buck B of DA9214 or DA9215
	NC		AO	Do not connect for DA9213
D7	FBBN		Al	Negative sense node for Buck B of DA9214 or DA9215
	NC		AO	Do not connect for DA9213
A7	GPI0	TRK	DI/AI	General purpose input, input track
B7	GPI1		DI	General purpose input
B6	GPIO2		DIO	General purpose input/output
A5	SDA	SI	DIO	2-WIRE data, 4-WIRE data input/output
A6	SCL	SK	DI	2-WIRE clock, 4-WIRE clock
D6	nCS	GPI4	DI	4-WIRE chip select, general purpose input
C6	SO	GPIO3	DIO	4-WIRE data output, general purpose input/output
B5	NC		AO	Do not connect and leave floating. This pin is used for the supply of internal circuits.
	VDDCORE		AO	Regulated supply (typical 2.5 V) for internal circuitry. On VFBGA package, decouple with 150 nF (or 220 nF).
F6	VSYS		PS	Supply for IC and input for voltage supervision
E5	VSS		VSS	
E6	VSS_ANA		VSS	
C1, C2, C3, C4, D1, D2, D3, D4, C8, C9, C10, C11, D8, D9, D10, D11	VSS_A1, VSS_A2 VSS_B1 VSS_B2		VSS	Connect together

## Table 3. Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital Input	Al	Analog Input
DO	Digital Output	AO	Analog Output
DIO	Digital Input/Output	AIO	Analog Input/Output
PS	Power Supply	VSS	Ground

# 3. Specifications

# 3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

**CAUTION**: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

**Table 4. Absolute Maximum Ratings** 

Parameter	Description	Conditions (Note 1)	Min	Max	Unit
T <sub>STG</sub>	Storage temperature		-65	+150	°C
TJ	Junction temperature		-40	+150	°C
V <sub>DD_LIM</sub>	Limiting supply voltage		-0.3	6.0	V
VPIN	Limiting voltage at all pins except above		-0.3	V <sub>DD</sub> + 0.3 (max 6.0)	V
V <sub>ESD_HBM</sub>	Electrostatic discharge voltage	Human Body Model		2	kV

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# 3.2 Recommended Operating Conditions

Table 5. Recommended Operating Conditions (Note 1)

Parameter	Description	Conditions	Min	Тур	Max	Unit
V <sub>DD</sub>	Supply voltage		2.8		5.5	V
T <sub>J_OP</sub>	Operating junction temperature				125	°C
T <sub>A</sub>	Ambient temperature		-40		85	°C
V <sub>DDIO</sub>	Input/output supply voltage		1.2		3.6 Note 2	
Ртот	Total power dissipation Note 3	66 WL-CSP Derating factor above T <sub>A</sub> = 70 °C: 37 mW/°C		2035		mW
Ртот	Total power dissipation Note 3	66 VFBGA Derating factor above T <sub>A</sub> = 70 °C: 34.8 mW/°C		1920		mW

- Note 1 Within the specified limits, a lifetime of 10 years is guaranteed.
- **Note 2**  $V_{DDIO}$  is not allowed to be higher than  $V_{DD}$ .
- Note 3 Obtained from simulation on a 2S2P 4L JEDEC Board (EIA/JESD51-2). Influenced by PCB technology and layout.

# 3.3 Electrical Specifications

Electrical characteristics table limits are guaranteed by production testing, design, or correlation using standard statistical quality control methods unless otherwise stated. Typical (Typ) specifications are mean or average values at  $T_A = 25^{\circ}$ C and are not guaranteed.

Unless otherwise noted, the following is valid for  $T_J$  = -40 °C to +125 °C,  $V_{DD}$  = 2.8 V to 5.5 V,  $C_{OUT}$  = 47  $\mu F$  per phase, local sensing.

**Table 6. Buck Converters Characteristics** 

Parameter	Description	Conditions	Min	Тур	Max	Unit
External Co	mponent Electrical Conditions	•				
C <sub>OUT</sub>	Output capacitance (per phase)	Including voltage and temperature coefficient	23	47	62	μF
ESR <sub>COUT</sub>	Equivalent series resistance (per phase)	f > 100 kHz			10	mΩ
LPHASE	Inductance (per phase)	Including current and temperature dependence	0.11	0.22	0.29	μΗ
DCR <sub>LPHASE</sub>	Inductor resistance				100	mΩ
Electrical CI	haracteristics					
V <sub>DD</sub>	Supply voltage	VDD_x = VSYS	2.8		5.5	V
Vвиск	Buck output voltage Note 1	Io = 0 to Io_max	0.3		1.57	V
Voacc	Output voltage accuracy PWM mode	Incl. static line/load reg and voltage ripple V <sub>BUCK</sub> ≥ 1 V	-2.0		+2.0	%
		Incl. static line/load reg and voltage ripple VBUCK < 1 V		±20		mV
		$V_{BUCK} = 1 \text{ V}$ $V_{DD} = 3.8 \text{ V}$ no load	-1.0		+1.0	%
		$V_{BUCK} = 1 V$ $V_{DD} = 3.8 V$ no load $T_{A} = 27  ^{\circ}C$	-0.5		+0.5	%
Vtr_load	Load regulation transient voltage Note 2	DA9213 Io = 0 to 5 A, t <sub>R</sub> = 500 ns PWM 4-phase V <sub>BUCK</sub> ≥ 1 V V <sub>BUCK</sub> < 1 V	-2 -20 mV		+2 +20 mV	%
		DA9213 $I_0 = 0$ to 5 A, $t_R = 500$ ns auto mode, ph shedding $V_{BUCK} = 1 \text{ V}$	-3.5		+3.5	%
		DA9214  Io = 0 to 5 A, t <sub>R</sub> = 500 ns  PWM 2-phase  V <sub>BUCK</sub> = 1 V		±3.5		%
		DA9215 Buck A		±2.5		%

Parameter	Description	Conditions	Min	Тур	Max	Unit
		$I_O$ = 0 to 5 A, $t_R$ = 500 ns PWM 3-phase VBUCK = 1 V				
		DA9215 Buck B $I_O = 0$ to 2.5 A, $t_R = 200$ ns PWM, 2 x 47 $\mu$ F $V_{BUCK} = 1$ V		±2.5		%
VTR_LINE	Line regulation transient voltage	$V_{DD} = 3.0 \text{ to } 3.6 \text{ V}$ $dt = 10  \mu \text{s}$ $I_{O} = I_{O(MAX)}/2$		15		mV
I <sub>O_MAX</sub>	Maximum output current	Per phase	5000			mA
ILIM_MIN	Minimum current limit per phase (programmable)	BUCKA_ILIM = 0000 BUCKB_ILIM = 0000 Note 3	-20%	4000	20%	mA
ILIM_MAX	Maximum current limit per phase (programmable)	BUCKA_ILIM = 1111 BUCKB_ILIM = 1111 Note 3	-20%	7000	20%	mA
IQ_PWM	Quiescent current at synchronous rectification mode	Per phase No load V <sub>DD</sub> = 3.7 V		17		mA
f <sub>SW</sub>	Switching frequency			3		MHz
tstup	Start-up time	VOUT = 1.0 V BUCKA_UP_CTRL = 100 BUCKB_UP_CTRL = 100		50 Note 4		μs
Ro_PD	Output pull-down resistance	For each phase at the LX node at 0.5 V, (see BUCKx_PD_DIS)		150	200	Ω
Ron_pmos	PMOS on-resistance	66 WL-CSP incl. pin and routing VDD = 3.7 V per phase		26		mΩ
		66 VFBGA incl. pin and routing VDD = 3.7 V per phase		27		mΩ
Ron_nmos	NMOS on-resistance	66 WL-CSP incl. pin and routing VDD = 3.7 V per phase		18		mΩ
		66 VFBGA incl. pin and routing VDD = 3.7 V per phase		19		mΩ

#### **DA9213, DA9214, DA9215 Datasheet**

Parameter	Description	Conditions	Min	Тур	Max	Unit
PFM Mode		•	·			
V <sub>BUCK_PFM</sub>	Buck output voltage in PFM	$I_0 = 0$ mA to $I_{0\_MAX}$	0.3		1.57	V
IMIN_PFM	Minimum output current in PFM	Static output voltage, no DVC	2			mA
IQ_PFM_A2	DA9214 quiescent current Buck A enabled	No switching $V_{DD} = 3.7 \text{ V}$ Note 5		58		μА
IQ_PFM_A4	DA9213 quiescent current Buck enabled	No switching V <sub>DD</sub> = 3.7 V Note 5		72		μA
IQ_PFM_A2B2	DA9214 quiescent current Buck A enabled Buck B enabled	No switching VDD = 3.7 V Note 5		106		μA
IQ_PFM_A3B1	DA9215 quiescent current Buck A enabled Buck B enabled	No switching VDD = 3.7 V Note 5		130		μА

- Note 1 Programmable in 10 mV increments.
- **Note 2** Additional to the dc accuracy. The value is intended to be measured directly at C<sub>OUT(EXT)</sub>. In case of remote sensing, parasitics of PCB and external components may affect this value.
- Note 3 On-time > 50 ns.
- **Note 4** Time from beginning to end of the voltage ramp. Additional 10 µs typical delay, plus internal sync to the enable port.
- Note 5 For the total quiescent current of the IC, the  $I_{DD\_ON}$  should be added.

Table 7. IC Performance and Supervision

Parameter	Description	Conditions	Min	Тур	Max	Unit
IDD_OFF	Off state supply current	IC_EN = 0 T <sub>A</sub> = 27 °C		0.1	1	μA
I <sub>DD_ON</sub>	On state supply current	IC_EN = 1 Buck A/B off T <sub>A</sub> = 27 °C		14		μА
V <sub>TH_PG</sub>	Power good threshold voltage	Referred to V <sub>BUCK</sub>		-50		mV
VHYS_PG	Power good hysteresis voltage			50		mV
VTH_UVLO_VDD	Under-voltage lockout threshold at V <sub>DD</sub>	66 WL-CSP		2.0		V
	Under-voltage lockout threshold at VDD	66 VFBGA BUCK_EN = 0		2.0		V
		66 VFBGA BUCK_EN = 1		2.55		V
VTH_UVLO_IO	Under-voltage lockout threshold at V <sub>DDIO</sub>		1.35	1.45	1.55	V
V <sub>HYS_UVLO_IO</sub>	Under-voltage lockout hysteresis at VDDIO			70		mV
T <sub>TH_WARN</sub>	Thermal warning threshold temperature		110	125	140	°C
T <sub>TH_CRIT</sub>	Thermal critical threshold temperature		125	140	155	°C
T <sub>TH_POR</sub>	Thermal power on reset threshold temperature		135	150	165	°C
fosc	Internal oscillator frequency		-7%	6.0	+7%	MHz

Unless otherwise noted, the following is valid for  $T_A = -40$  °C to +85 °C

Table 8. Digital I/O Characteristics

Parameter	Description	Conditions	Min	Тур	Max	Unit
V <sub>IH_EN</sub>	HIGH level input voltage	At pin IC_EN	1.1			V
V <sub>IL_EN</sub>	LOW level input voltage	At pin IC_EN			0.35	V
t <sub>EN</sub>	Enable time	I/F operating		750		μs
Ro_Pu_GPO	Pull up resistor at GPO	V <sub>DDIO</sub> = 1.8 V V <sub>GPO</sub> = 0 V		100		kΩ
R <sub>I_PD_GPI</sub>	Pull down resistor at GPI	V <sub>DDIO</sub> = 1.8 V V <sub>GPO</sub> = 0 V		150		kΩ
V <sub>IH</sub>	GPI0-4, SCL, SDA, (2-WIRE mode) HIGH level input voltage	VDDCORE mode VDDIO mode	1.75 0.7 * V <sub>DDIO</sub>			V
VIL	GPI0-4, SCL, SDA, (2-WIRE mode) LOW level input voltage	VDDCORE mode VDDIO mode			0.75 0.3 * V <sub>DDIO</sub>	V
V <sub>IH_4</sub> WIRE	SK, nCS, SI		0.7* V <sub>DDIO</sub>			V

Parameter	Description	Conditions	Min	Тур	Max	Unit
	(4-WIRE Mode) HIGH level input voltage					
VIL_4WIRE	SK, nCS, SI (4-WIRE Mode) LOW level input voltage				0.3*V <sub>DDIO</sub>	V
V <sub>OH</sub>	GPO2-3, SO (4-WIRE mode) HIGH level output voltage	Push-pull mode at 1 mA V <sub>DDIO</sub> ≥ 1.5 V	0.8*V <sub>DDIO</sub>			V
V <sub>OL1</sub>	GPO2-3, SDA (2-WIRE mode) SO (4-WIRE mode) LOW level output voltage at lo <sub>L</sub> = 1 mA				0.3	V
V <sub>OL3</sub>	SDA (2-WIRE Mode)  LOW level output voltage at loL = 3 mA				0.24	V
V <sub>OL20</sub>	SDA (2-WIRE Mode)  LOW level output voltage at loL = 20 mA				0.4	V
Cin	CLK, SDA (2-WIRE Mode) input capacitance			2.5	10	pF
tsp	CLK, SDA (2-WIRE Mode) spike suppression pulse width	Fast/Fast+ mode High Speed mode	0		50 10	ns
t <sub>fDA</sub>	Fall time of SDA signal (2-WIRE Mode)	Fast at $C_B < 550$ pF HS at $10 < C_B < 100$ pF HS at $C_B < 400$ pF	20+0.1C <sub>B</sub> 10 20		120 80 160	ns

Unless otherwise noted, the following is valid for  $T_A$  = -40 °C to +85 °C

Table 9. 2-WIRE Control Bus Characteristics

Parameter	Description	Conditions	Min	Тур	Max	Unit
t <sub>BUF</sub>	Bus free time from STOP to START condition		0.5			μs
Св	Bus line capacitive load				150	pF
Standard/Fa	st/Fast+ Mode					
f <sub>SCL</sub>	Clock frequency	At pin SCL	0 Note 1		1000	kHz
tsu_sta	START condition set-up time		0.26			μs
t <sub>H_STA</sub>	START condition hold time		0.26			μs
tw_cL	Clock LOW duration		0.5			μs
tw_ch	Clock HIGH duration		0.26			μs
t <sub>R</sub>	Rise time	Input requirement. At pin CLK and DATA			1000	ns
t <sub>F</sub>	Fall time	Input requirement. At pin CLK and DATA			300	ns

Parameter	Description	Conditions	Min	Тур	Max	Unit
tsu_D	Data set-up time		50			ns
t <sub>H_D</sub>	Data hold time		0			ns
High Speed	Mode					
fscl_Hs	Clock frequency	At pin SCL	0 Note 1		3400	kHz
tsu_sta_hs	START condition set-up time		160			ns
th_sta_hs	START condition hold time		160			ns
tw_cl_Hs	Clock LOW duration		160			ns
tw_ch_hs	Clock HIGH duration		60			ns
t <sub>R_HS</sub>	Rise time	Input requirement. At pin CLK and DATA			160	ns
t <sub>F_HS</sub>	Fall time	Input requirement. At pin CLK and DATA			160	ns
tsu_d_Hs	Data set-up time		10			ns
t <sub>H_D_Hs</sub>	Data hold time		0			ns
tsu_sto_hs	STOP condition set-up time		160			ns

Note 1 Minimum clock frequency is 10 kHz if 2WIRE\_TO is enabled

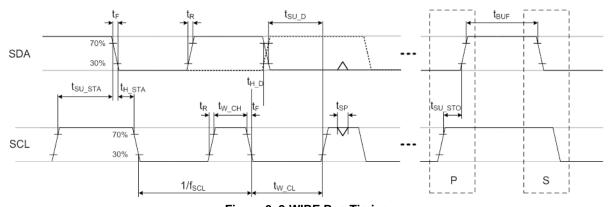


Figure 6. 2-WIRE Bus Timing

Unless otherwise noted, the following is valid for  $T_A = -40$  °C to +85 °C

**Table 10. 4-WIRE Control Bus Characteristics** 

Parameter	Description	Conditions	Min	Тур	Max	Unit
Св	Bus line capacitive load				100	pF
tc	Cycle time	1	70			ns
tsu_cs	Chip select setup time	2, from CS active to first SK edge	20			ns
t <sub>H_CS</sub>	Chip select hold time	3, from last SK edge to CS idle	20			ns
tw_cL	Clock LOW duration	4	0.4 x t <sub>C</sub>			ns
tw_ch	Clock HIGH duration	5	0.4 x tc			ns
t <sub>SU_SI</sub>	Data input setup time	6	10			ns
t <sub>H_SI</sub>	Data input hold time	7	10			ns
t <sub>V_SO</sub>	Data output valid time	8			22	ns
t <sub>H_SO</sub>	Data output hold time	9	6			ns

Parameter	Description	Conditions	Min	Тур	Max	Unit
tw_cs	Chip select HIGH duration	10	20			ns

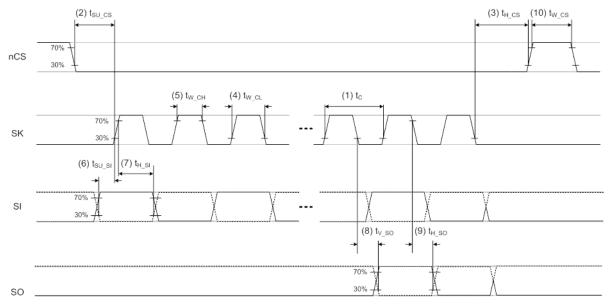
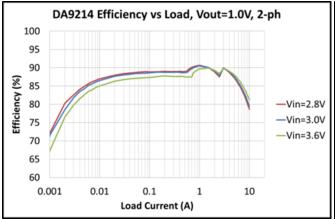


Figure 7. 4-WIRE Bus Timing

# 4. Typical Performance Graphs

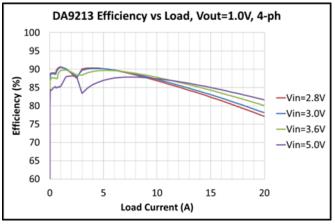
Note: 66 WL-CSP, phase shedding is enabled.



DA9214 Efficiency vs Load, Vin=3.6V, 2-ph 100 95 90 85 80 Vout=0.8V -Vout=1.0V 75 -Vout=1.2V 65 60 0.01 0.1 10 0.001 Load Current (A)

Figure 8. 2 Phase Auto-Mode, 0 A to 10 A

Figure 9. 2 Phase Auto-Mode, 0 A to 10 A



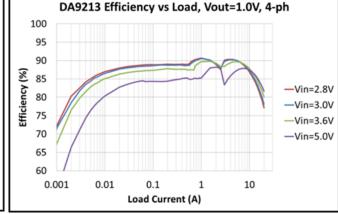
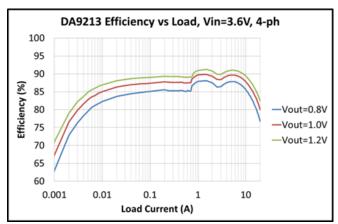


Figure 10. 4 Phase Auto-Mode, 0 A to 20 A (Linear)

Figure 11. 4 Phase Auto-Mode, 0 A to 20 A (Logarithmic)





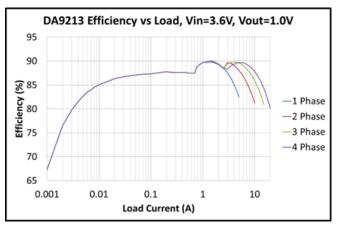


Figure 13. 1, 2, 3, and 4 Phase Modes

# 5. Functional Description

Flexible configurability and the availability of different control schemes make both DA9213, DA9214, and D A9215 the ideal single/dual buck companion ICs to expand the existing capabilities of a master PMIC.

Due to the advanced compatibility between both DA9213, DA9214, and DA9215 and the DA9063, they offer several advantages when they are operated together. These advantages include:

- DA9213, DA9214, and DA9215 can be enabled and controlled by DA9063 during the power up sequence, thanks to DA9063's dedicated output signals during power up, and compatible input controls in both DA9213, DA9214, and DA9215.
- DA9213, DA9214, and DA9215 can be used in a completely transparent way for the host processor and can share the same Control Interface (same SPI chip select or I<sup>2</sup>C address), thanks to the compatible registers map. DA9213, DA9214, and DA9215 have a dedicated register space for configuration and control which does not conflict with DA9063.
- DA9213, DA9214, and DA9215 support a power good configurable port for enhanced communication to the host processor and improved power up sequencing.
- DA9213, DA9214, and DA9215 can share the same interrupt line with DA9063.

In addition, the 2-WIRE / 4-WIRE interfaces allow DA9213, DA9214, and DA9215 to fit many standard PMU parts and power applications.

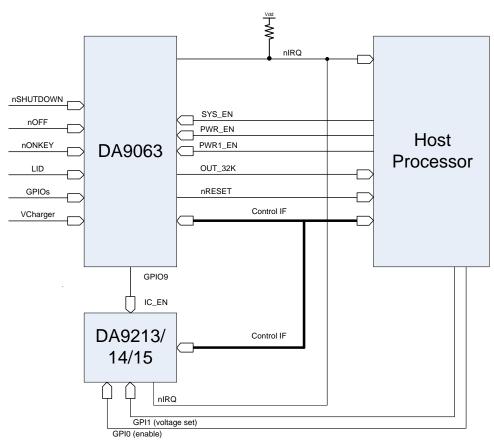


Figure 14. Interface of DA9213/14/15 with DA9063 and the Host Processor

As shown in Figure 14, a typical application case includes a host processor, a Main PMIC (for example, DA9063) and DA9213, DA9214, and DA9215 used as companion IC for the high-power core supply.

The easiest way of controlling DA9213, DA9214, and DA9215 is through the Control Interface. The master initiating the communication must always be the host processor that reads and writes to the main PMIC, and to the DA9213, DA9214, and DA9215 registers. To poll the status of DA9213 or DA9214, the host processor must access the dedicated register area through the Control Interface. DA9213, DA9214, and DA9215 can be additionally controlled by means of hardware inputs.

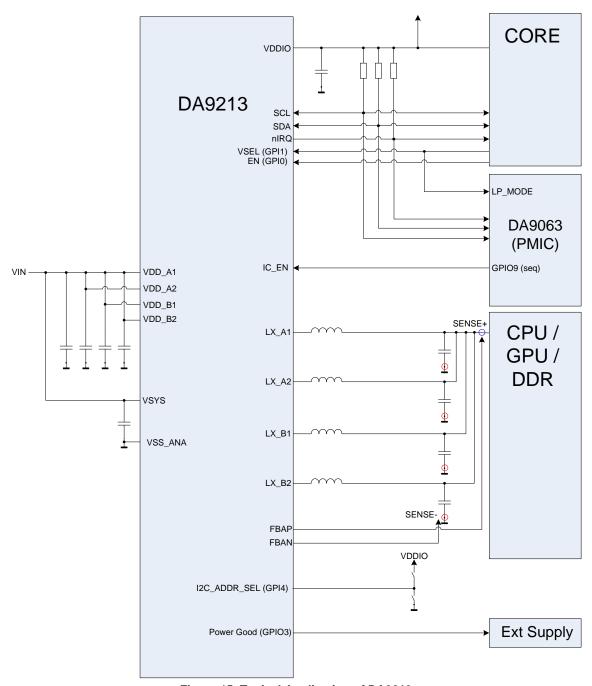


Figure 15. Typical Application of DA9213

Figure 15 shows a typical use case of DA9213 for the supply of CPU, GPU, or DDR rails. The IC is enabled and disabled by the main PMIC via IC\_EN port as part of its sequencer. Once the IC is enabled, the CORE application processor enables the buck converter with the EN1 signal and manages the output voltage selection with the VSEL signal.

The VSEL signal can be shared between the main PMIC and the DA9213. Three GPI/GPIOs embedded in DA9213 are used in this case:

- GPIO2 signals the insertion of an external charger in the application (through interrupt to the host processor)
- GPIO3 indicates a power good condition, either to proceed with the power up sequence or to enable an external supply connected to the port
- GPI4 is used for the I<sup>2</sup>C interface address hardware selection

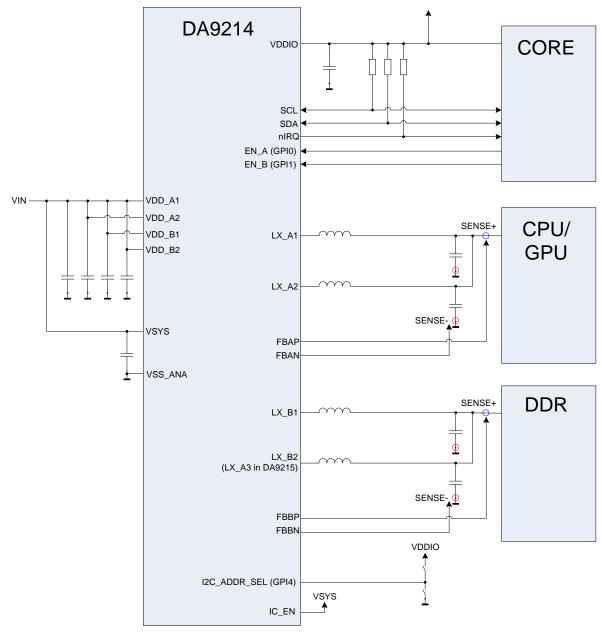


Figure 16. Typical Application of DA9214

Figure 16 shows a typical use case of DA9214 for the simultaneous supply of a CPU and a GPU rail. The IC is always enabled because IC\_EN is shorted to the battery voltage. The CORE application processor enables and disables the CPU/GPU and the DDR individually via dedicated ports on DA9214.

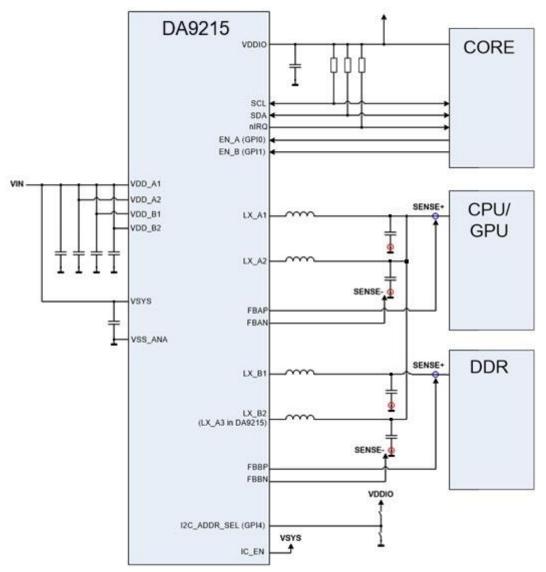


Figure 17. Typical Application of DA9215

Figure 17 shows a typical use case of DA9215 for the simultaneous supply of a CPU and a GPU rail. The IC is always enabled because IC\_EN is shorted to the battery voltage. The CORE application processor enables and disables the CPU/GPU and the DDR individually via dedicated ports on DA9215.

Table 11. Buck Allocations for each Phase per Device

Device	Phase A1	Phase A2	Phase B1	Phase B2
DA9213	BuckA	BuckA	BuckA	BuckA
DA9214	BuckA	BuckA	BuckB	BuckB
DA9215	BuckA	BuckA	BuckB	BuckA

Table 11 shows how the phases of the device are used for different device configurations. It should be noted in particular that the third phase of DA9215 BuckA is phase B2. Phase B1 is used for the single phase BuckB.

## 5.1 DC\_DC Buck Converter

DA9213 is a four-phase 20 A high efficiency synchronous step-down DVC regulator, operating at a high frequency of typically 3 MHz. It supplies an output voltage of typically 1.0 V for a CPU rail, configurable in the range 0.3 V to 1.57 V, with high accuracy in steps of 10 mV.

DA9214 contains two buck converters, Buck A and Buck B, each capable of delivering 10 A.

DA9215 contains also two buck converters, Buck A capable of 15 A and Buck B capable of 5 A.

To improve the accuracy of the delivered voltage, each buck converter is able to support a differential sensing of the configured voltage directly at the point of load via dedicated positive and negative sense pins.

Both Buck A and Buck B have two voltage registers each. One defines the normal output voltage, while the other offers an alternative retention voltage. In this way different application power modes can easily be supported. The voltage selection can be operated either via GPI or via control interface to guarantee the maximum flexibility according to the specific host processor status in the application.

When a buck is enabled, its output voltage is monitored, and a power good signal indicates that the buck output voltage has reached a level higher than the V<sub>TH(PG)</sub> threshold. The power good is lost when the voltage drops below V<sub>TH(PG)</sub> - V<sub>HYS(PG)</sub>, which is the level at which the signal is de-asserted. The power good signaling should not be used in conjunction with fast start up rates, configured in BUCKx\_UP\_CTRL register fields and can be individually masked during DVC transitions using the PGA\_DVC\_MASK and PGB\_DVC\_MASK bits. For each of the buck converters the status of the power good indicator can be read back via I²C from the PWRGOOD\_A and PWRGOOD\_B status bits. It can be also individually assigned to either GPIO2 or GPIO3 using BUCKA\_PG\_SEL and BUCKB\_PG\_SEL. For correct functionality, the GPIO ports need to be configured as output. An I²C write in GPIOx\_MODE can overwrite the internal configuration so that a new update will be automatically done only when the internal power good indicator changes status.

The buck converters are capable of supporting DVC transitions that occur:

- When the active and selected A-voltage or B-voltage is updated to a new target value.
- When the voltage selection is changed from the A-voltage to the B-voltage (or B-voltage to the A voltage) using VBUCKA SEL and VBUCKB SEL.

The DVC controller operates in Pulse Width Modulation (PWM) mode with synchronous rectification. When the host processor changes the output voltage, the voltage transition of each buck converter can be individually signaled with a READY signal routed to either GPIO2 or GPIO3. The port has to be configured as GPO and selected for the functionality via READYA\_CONF or READYB\_CONF. In contrast to the power good signal, the READY only informs the host processor about the completion of the digital DVC ramp without confirming that the target voltage has actually been reached.

The slew rate of the DVC transition is individually programmed for each buck converter at 10 mV per (4, 2, 1, or 0.5) µs via control bit SLEW\_RATE\_A and SLEW\_RATE\_B.

The typical supply current is in the order of 17 mA per phase (quiescent current and charge/discharge current) and drops to  $<1 \mu$ A when the buck is turned off.

When the buck is disabled, a pull down resistor (typically 150  $\Omega$ ) for each phase is activated depending of the value stored in register bits BUCKA\_PD\_DIS and BUCKB\_PD\_DIS. Phases disabled using PHASE\_SEL\_A and PHASE\_SEL\_B will not have any pull down. The pull-down resistor is always disabled at all phases when DA9213, DA9214, and DA9215 are OFF.

#### 5.1.1 Switching Frequency

The switching frequency is chosen to be high enough to allow the use of a small 0.22 µH inductor (see a complete list of coils in the Application Information, section 6). The buck switching frequency can be tuned using register bit OSC\_TUNE. The internal 6 MHz oscillator frequency is tuned in steps of 180 kHz. This impacts the buck converter frequency in steps of 90 kHz and helps to mitigate possible disturbances to other HF systems in the application.

### 5.1.2 Operation Modes and Phase Selection

The buck converters can operate in synchronous PWM mode and PFM mode. The operating mode is selected using register bits BUCKA\_MODE and BUCKB\_MODE.

An automatic phase shedding can be enabled for each buck converter in PWM mode via PH\_SH\_EN\_A, PH\_SH\_EN\_B, thereby automatically reducing or increasing the number of active phases depending on the output load current. For DA9214 the phase shedding will automatically change between 1-phase and 2-phase operation at a typical current of 2.0 A. For DA9213 the phase shedding will automatically change between 1-phase and 4-phase operation at a typical current of 2.5 A. The PHASE\_SEL\_A and PHASE\_SEL\_B register fields limit the maximum number of active phases under any conditions.

If the automatic operation mode is selected on BUCKA\_MODE or BUCKB\_MODE, the buck converters will automatically change between synchronous PWM mode and PFM depending on the load current. This improves the efficiency of the converters across the whole range of output load currents.

# 5.1.3 Output Voltage Selection

The switching converter can be configured using either a 2-WIRE or a 4-WIRE interface. For security reasons, the re-programming of registers that can cause damage when wrongly programmed (for example, the voltage settings) can be disabled by asserting the control V\_LOCK. When V\_LOCK is asserted, reprogramming the registers 0xD0 to 0x14F from control interfaces is disabled.

For each buck converter two output voltages can be pre-configured inside registers VBUCKA\_A and VBUCKB\_A, and registers VBUCKA\_B and VBUCKB\_B. The output voltage can be selected by either toggling register bits VBUCKA\_SEL and VBUCKB\_SEL or by re-programming the selected voltage control register. Both changes will result into ramped voltage transitions, during which the READY signal is asserted. After being enabled, the buck converter will by default use the register settings in VBUCKA\_A and VBUCKB\_A unless the output voltage selection is configured via the GPI port.

If "00" has been selected in BUCKA\_MODE or BUCKB\_MODE, A-/B- voltage selection registers VBUCKx\_x control the operation of the PWM and PFM modes.

Regardless of the values programmed in the VBUCKx\_A and VBUCKx\_B registers, the registers VBUCKA\_MAX, VBUCKB\_MAX will individually limit the output voltage that can be set for each of the buck converters.

The buck converter provides an optional hardware enable/disable via selectable GPI, and configured via control register bits BUCKA\_GPI and BUCKB\_GPI. A change of the output voltage from the state of a GPI is enabled via control register bits VBUCKA\_GPI and VBUCKB\_GPI. After detecting a rising or falling edge at the related GPIs, DA9213, DA9214, and DA9215 will configure the buck converters according to their status.

In addition to selecting between the A/B voltages, a track mode can be activated for Buck A to set the output voltage. In the DA9213, the track mode is applied to the 4-phase buck converter. This feature can be enabled on GPI0 via GPI0\_PIN. The output voltage will be configured to follow the value applied at a selected GPI pin. The voltage applied at GPI0 must be in the same range as the nominal output voltage selectable for the buck rail (see VBUCKA A and VBUCKA B registers). In Track Mode, only single ended remote sensing is possible.

In Track Mode, the content of the VBUCKA\_SEL bit is ignored, as well as VBUCKA\_A and VBUCKA\_B bits. They will become active again once the voltage track mode is disabled. The GPI0 does not generate any event in this case.

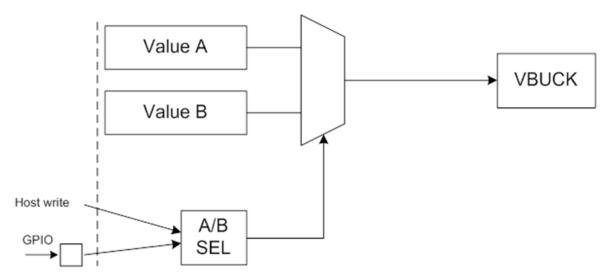


Figure 18. Concept of Control of the Buck's Output Voltage

## 5.1.4 Soft Start-Up

To limit in-rush current from VSYS, the buck converters can perform a soft start after being enabled. The start-up behavior is a compromise between acceptable inrush current from the battery and turn on time. In DA9213, DA9214, and DA9215, different ramp times can be individually configured for each buck converter on register BUCKA\_UP\_CTRL and BUCKB\_UP\_CTRL. Rates higher than 20 mV/µs may produce overshoot during the start-up phase, so they should be considered carefully.

A ramped power down can be selected on register bits BUCKA\_DOWN\_CTRL and BUCKB\_DOWN\_CTRL. When no ramp is selected, the output node will be discharged only by the pull down resistor, if enabled via BUCKA\_PD\_DIS and BUCKB\_PD\_DIS.

#### 5.1.5 Current Limit

The integrated current limit is meant to protect DA9213, DA9214, and DA9215's power stages and the external coil from excessive current. The bucks' current limit should be configured to be at least 40% higher than the required maximum continuous output current.

When reaching the current limit, each buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using the OCx\_MASK controls. These OCA\_MASK and OCB\_MASK control bits can be used to mask the generation of over current events during DVC transitions. An extra masking time as defined in OCx\_MASK will be automatically added to the DVC interval after the DVC has finished in order to ensure that the possible high current levels needed for DVC do not influence the event generation.

#### 5.1.6 Variable VOUT above 1.57 V

The whole product family is also available with an adjustable output voltage up to 4.3 V. A resistive divider from VOUT to FBAN (or FBBN) can be used to set the output voltage higher than 1.57 V, see Figure 19.

The value of the output voltage  $V_{OUT}$  is set by the selection of the resistive divider shown in equation 1. The total resistance of the divider resistors (R1+R2) should be less than 40 k $\Omega$ .

$$VOUT = \left(1 + \frac{R1}{R2}\right) \cdot VREF \tag{1}$$

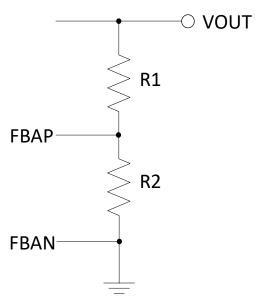


Figure 19. Resistive Divider from VOUT to FBAN

For example, to program the output voltage VOUT to 1.8 V, with VREF set to 1.2 V, suggest 10 k $\Omega$  on R1 and 20 k $\Omega$  on R2.

**Note:** The resistors need to be properly selected since the output voltage accuracy will be directly affected by any errors on the resistors. The voltage across FBAP and FBAN (VREF) is guaranteed, but not the output voltage accuracy.

#### CAUTION

The followings are important notes that need to be considered before using resistive divider on DA9213, DA9214, and DA9215:

- 1. Please contact your region's Renesas representative when adopting the resistive divider technique. Renesas need to prepare a special OTP because incorrect OTP settings may result in a different output voltage than expected.
- 2. The voltage difference between input voltage and output voltage needs to be: above 1.2 V, VIN VOUT > 1.2 V.
- 3. The total resistance (R1 + R2) is less than 40 k $\Omega$ .
- 4. It is recommended that the device is operated in PWM mode only.

## 5.2 Ports Description

This section describes the functionality of each input / output port.

### 5.2.1 VDDIO

VDDIO is an independent IO supply rail input to DA9213, DA9214, and DA9215 that can be assigned to the power manager interface and to the GPIOs (see control PM\_IF\_V and GPI\_V). The rail assignment determines the IO voltage levels and logical thresholds (see also the Digital I/O Characteristics in Table 8).

An integrated under-voltage lockout circuit for the VDDIO prevents internal errors by disabling the I<sup>2</sup>C communication when the voltage drops below V<sub>ULO\_IO</sub>. In that case the buck converters are also disabled and cannot be re-enabled (even via input port) until the VDDIO under-voltage condition has been resolved. At the exit of the VDDIO under-voltage condition an event E\_UVLO\_IO is generated and the nIRQ line is driven active if the event is not masked.

The VDDIO under-voltage circuit monitors voltages relative to a nominal voltage of 1.8 V. If a different rail voltage is being used, the under-voltage circuit can be disabled via UVLO\_IO\_DIS.

Note that the maximum speed at 4-WIRE interface is only available if the selected supply rail is greater than 1.6 V.

## 5.2.2 IC\_EN

IC\_EN is a general enable signal for DA9213, DA9214, and DA9215, turning on and off the internal circuitry (for example, the reference, the digital core, and so on.). Correct control of this port has a direct impact on the quiescent current of the whole application. A low level of IC\_EN allows the device to reach the minimum quiescent current. The voltage at this pin is continuously sensed by a dedicated analog circuit.

The host processor will be allowed to start the communication with DA9213, DA9214, and DA9215 through the Control Interface and, for example to turn on the buck converters, a delay time of t<sub>EN</sub> after assertion of the IC\_EN pin. If the bucks are enabled via OTP (see BUCKA\_EN and BUCKB\_EN controls), they will start up automatically after assertion of IC\_EN.

The IC\_EN activation threshold is defined with a built-in hysteresis to avoid glitching transitions that take place with unstable rising or falling edges.

#### 5.2.3 nIRQ

The nIRQ port indicates that an interrupt causing event has occurred and that the event/status information is available in the related registers. The nIRQ is an output signal that can either be push pull or open drain (selected via IRQ\_TYPE). If an active high IRQ signal is required, it can be achieved by asserting control IRQ\_LEVEL (recommended for push-pull mode).

Examples of this type of information can be critical temperature and voltage, fault conditions, status changes at GPI ports, and so forth. The event registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set, the nIRQ signal is asserted unless this interrupt is masked by a bit in the IRQ mask register. The nIRQ will not be released until all event registers with asserted bits have been read and cleared. New events that occur during reading an event register are held until the event register has been cleared, ensuring that the host processor does not miss them.

#### 5.2.4 GPIO Extender

DA9213, DA9214, and DA9215 include a GPIO extender that offers up to five 5 V-tolerant general purpose input/output ports. Each port is controlled via registers from the host processor.

The GPIO3 and GPI4 ports are pin-shared with the 4-WIRE Control Interface. For instance, if GPIO3\_PIN = 01, GPI4\_PIN = 01 (Interface selected), the GPIO3 and GPI4 ports will be exclusively dedicated to output and chip select signaling for 4-WIRE purposes. If the alternative function is selected, all GPIOs configuration as per registers 0x58 to 0x5A and 0x145 will be ignored.

GPIs are supplied from the internal rail VDDCORE or VDDIO (selected via GPI\_V) and can be configured to be active high or active low (selected via GPIOx\_TYPE). The input signals can be debounced or directly change the state of the assigned status register GPIx to high or low, according to the setting of GPIOx\_MODE. The debouncing time is configurable via control DEBOUNCE (10 ms default).

Whenever the status has changed to its configured active state (edge sensitive), the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked, see also Figure 20).

Whenever DA9213, DA9214, and DA9215 is enabled and enters ON mode (also when enabled changing the setting of GPIOx\_PIN) the GPI status bits are initiated towards their configured passive state. This ensures that already active signals are detected, and that they create an event immediately after the GPI comparators are enabled.

The buck enable signal (BUCKx\_EN) can be controlled directly via a GPI, if so configured in the BUCKA\_GPI and BUCKB\_GPI registers. If it is required that GPI ports do not generate an event when configured for the HW control of the switching regulator, the relative mask bit should be set.

GPIs can alternatively be selected to toggle the VBUCKA\_SEL and VBUCKB\_SEL from rising and falling edges at these inputs. Apart from changing the regulator output voltage this also provides hardware control of the regulator mode (normal/low power mode) from the settings of BUCKA\_SL\_A, BUCKA\_SL\_B, BUCKB\_SL\_A, and BUCKB\_SL\_B (enabled if BUCKA\_MODE or BUCKB\_MODE = 00).

All GPI ports have the additional option of activating a 100 k $\Omega$  pull-down resistor via GPIOx\_PUPD, which ensures a well-defined level in case the input is not actively driven.

If enabled via ADDR\_SEL\_CONF, the I<sup>2</sup>C address selection can be assigned to a specific GPI. An active voltage level at the selected GPI configures the slave address of DA9213, DA9214, and DA9215 to IF\_BASE\_ADDR1 while a passive voltage level configures the slave address to IF\_BASE\_ADDR2. If no GPI is selected then the IF\_BASE\_ADDR1 is automatically used.

If defined as an output, GPIOs can be configured to be open-drain or push-pull. If configured as push pull, the supply rail is VDDIO. By disabling the internal 120 k $\Omega$  pull-up resistor in open-drain mode, the GPO can also be supplied from an external rail. The output state will be assigned as configured by the GPIO register bit GPIOx MODE.

A specific power good port for each of the buck converters can be configured via BUCKA\_PG\_SEL and BUCKB\_PG\_SEL. The respective port must be configured as GPO for correct operation. If assigned to the same GPO, it is necessary that the power good indicators for Buck A and Buck B are both active (supply voltages in range) to assert the overall power good. The signal will be released as soon as one of the single power good signals is not active (that is, at least one supply is out of range).

The power good signaling should not be used in conjunction with fast start up rates, configured in BUCKx\_UP\_CTRL register fields.

Once enabled via RELOAD\_FUNC\_EN the GPIO0 can be used as input port to operate a partial OTP download. When the input level is changed to active, the registers 0x5D, 0x5E, 0xD1 to 0xDA are updated to their OTP default. This allows a complete buck re-configuration that resets all the changes done to those registers previously (soft reset). If the buck should be kept on during the soft reset, the OTP values for the enable bits should be asserted because they are also part of the re-load.

Whenever the GPIO unit is off (POR or OFF Mode) all ports are configured as open drain active high (pass device switched off, high impedance state). When leaving POR the pull-up or pull-down resistors will be configured from register GPIOx\_PUPD.

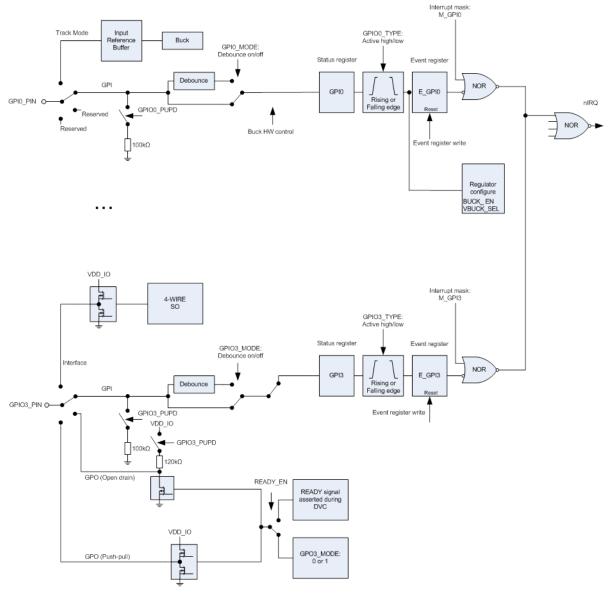


Figure 20. GPIO Principle of Operation (Example Paths)

## 5.3 Operating Modes

#### 5.3.1 ON Mode

DA9213, DA9214, and DA9215 are in ON Mode when the IC\_EN port is higher than EN\_ON and the supply voltage is higher than  $V_{TH(UVLO)(VDD)}$ . Once enabled, the host processor can start the communication with DA9213, DA9214, and DA9215 via Control Interface after the  $t_{EN}$  delay needed for internal circuit start up.

If BUCKA\_EN or BUCKB\_EN is asserted when DA9213, DA9214, and DA9215 is in ON Mode the power up of the related buck converter is initiated. If the bucks are controlled via GPI, the level of the controlling ports is checked when entering ON mode, so that an active level will immediately have effect on the buck. If BUCKA\_EN or BUCKB\_EN are not asserted and all controlling GPI ports are inactive, the buck converter will stay off with the output pull down resistor enabled/disabled according to the setting of BUCKA\_PD\_DIS and BUCKB\_PD\_DIS.

#### 5.3.2 OFF Mode

DA9213, DA9214, and DA9215 are in OFF Mode when the IC\_EN port is lower than EN\_OFF. In OFF Mode, the bucks are always disabled and the output pull down resistors are disabled independently of BUCKA\_PD\_DIS and BUCKB\_PD\_DIS. All I/O ports of DA9213, DA9214, and DA9215 are configured as high impedance.

#### 5.4 Control Interfaces

All the features of DA9213, DA9214, and DA9215 can be controlled by SW through a serial control interfaces. The communication is selectable to be either a 2-WIRE (I²C compliant) or a 4-WIRE connection (SPI compliant) via control IF\_TYPE, which will be selected during the initial OTP read. If 4-WIRE is selected, the GPIO3 and GPI4 are automatically configured as interface pins. Data is shifted into or out of DA9213, DA9214, and DA9215 under the control of the host processor, which also provides the serial clock. In a normal application case, the interface is only configured once from OTP values, which are loaded during the initial start-up of DA9213, DA9214, and DA9215.

DA9213, DA9214, and DA9215 reacts only on read/write commands where the transmitted register address (using the actual page bits as a MSB address range extensions) is within 0x50 to 0x67, 0xD0 to DF, 0x140 to 0x14F and (read only) 0x200 to 0x27F. Host access to registers outside these ranges will be ignored. This means there will be no acknowledge after receiving the register address in 2-WIRE Mode, and SO stays HI-Z in 4-WIRE Mode. During debug and production modes write access is available to page 4 (0x200 to 0x27F). DA9213, DA9214, and DA9215 will react only on write commands where the transmitted register address is 0x00, 0x80, 0x100 to0x106. The host processor must read the content of those registers before writing, thereby changing only the bit fields that are not marked as reserved (the content of the read back comes from the compatible PMIC, for example DA9063).

If the STAND\_ALONE bit is asserted (OTP bit), DA9213, DA9214, and DA9215 will also react to read commands.

#### 5.4.1 4-WIRE Communication

In 4-WIRE Mode the interface uses a chip-select line (nCS/nSS), a clock line (SK), data input (SI) and data output line (SO).

The DA9213, DA9214, and DA9215 register map is split into four pages that each contain up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after turn on includes registers 0x50 to 0x6F. Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting bit REVERT. Unless the REVERT bit was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

All registers outside the DA9213, DA9214, and DA9215 range are write only, that is, the DA9213, DA9214, and DA9215 will not answer to a read command and the data bus is tristate (they are implicitly directed to DA9063). In particular the information contained in registers 0x105 and 0x106 is used by DA9213, DA9214, and DA9215 to configure the control interface. They must be the same as the main PMIC (DA9063), so that a write to those registers configures both the main PMIC and DA9213, DA9214, and DA9215 at the same time. The default OTP settings also need to be identical for a correct operation of the system.

The 4-WIRE interface features a half-duplex operation, that is, data can be transmitted and received within a single 16-bit frame at enhanced clock speed (up to 14 MHz). It operates at the clock frequencies provided by the host.

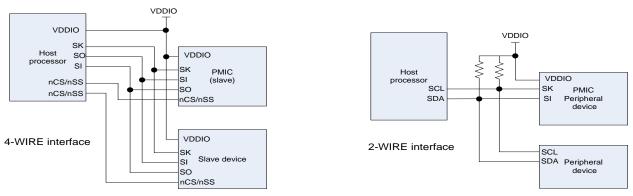


Figure 21. Schematic of 4-WIRE and 2-WIRE Power Manager Bus

A transmission begins when initiated by the host. Reading and writing is accomplished by the use of an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first seven bits specify the register address (0x01 to 0x07) that will be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with an R/W bit, which together with the control bit R/W\_POL specifies the direction of the following data exchange. During register writing the host continues sending out data during the following eight SK clocks. For reading, the host stops transmitting and the 8-bit register is clocked out of DA9213, DA9214, and DA9215 during the consecutive eight SK clocks of the frame. Address and data are transmitted with MSB first. The polarity (active state) of nCS is defined by control bit nCS\_POL. nCS resets the interface when inactive and it has to be released between successive cycles.

The SO output from DA9213, DA9214, and DA9215 is normally in high-impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed at the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

CPHA Clock Polarity	CPOL Clock Phase	Output Data is Updated at SK Edge	Input Data is Registered at SK Edge
0 (idle low)	0	Falling	Rising
0 (idle low)	1	Rising	Falling
1 (idle high)	0	Rising	Falling
1 (idle high)	1	Falling	Rising

DA9213, DA9214, and DA9215's 4-WIRE interface offers two further configuration bits. Clock polarity (CPOL) and clock phase (CPHA) define when the interface will latch the serial data bits. CPOL determines whether SK idles high (CPOL = 1) or low (CPOL = 0). CPHA determines on which SK edge data is shifted in and out. With CPOL = 0 and CPHA = 0, DA9213, DA9214, and DA9215 latch data on the SK rising edge. If the CPHA is set to 1 the data is latched on the SK falling edge. CPOL and CPHA states allow four different combinations of clock polarity and phase. Each setting is incompatible with the other three. The host and DA9213, DA9214, and DA9215 must be set to the same CPOL and CPHA states to communicate with each other.

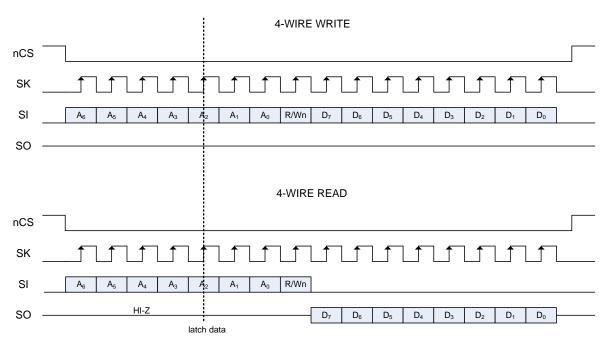


Figure 22. 4-WIRE Host Write and Read Timing (nCS\_POL = 0, CPOL = 0, CPHA = 0)

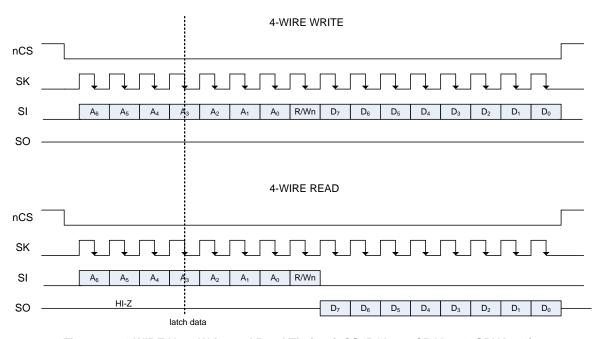


Figure 23. 4-WIRE Host Write and Read Timing (nCS\_POL= 0, CPOL = 0, CPHA = 1)

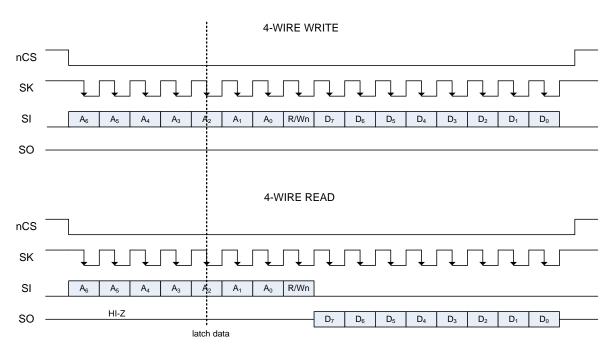


Figure 24. 4-WIRE Host Write and Read Timing (nCS\_POL = 0, CPOL = 1, CPHA = 0)

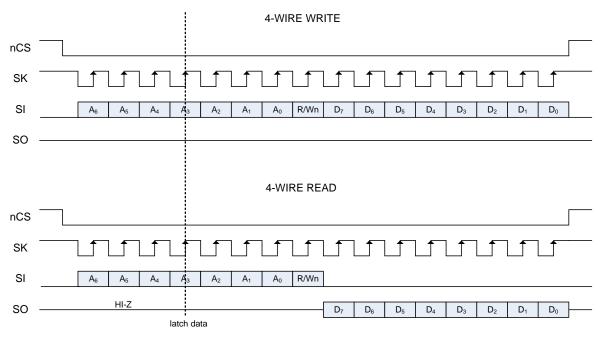


Figure 25. 4-WIRE Host Write and Read Timing (nCS\_POL = 0, CPOL = 1, CPHA = 1)

Table 13. 4-WIRE Interface Summary

Parameters				
Signal lines	nCS	Chip select		
	SI Serial input data	Master out Slave in		
	SO Serial output data	Master in Slave out		
	SK	Transmission clock		
Interface	Push-pull with tristate			
Supply voltage	Selected from VDDIO	1.6 V to 3.3 V		
Data rate	Effective read/write data	Up to 7 Mbps		

Parameters				
Transmission	Half-duplex	MSB first		
	16-bit cycles	7-bit address, 1-bit read/write, 8-bit data		
Configuration	CPOL	Clock polarity		
	СРНА	Clock phase		
	nCS_POL	nCS is active low/high		

**Note 1** Reading the same register at high clock rates directly after writing it does not guarantee a correct value. It is recommended to keep a delay of one frame until re-accessing a register that has just been written (for example, by writing/reading another register address in-between).

#### 5.4.2 2-WIRE Communication

The IF\_TYPE bit in the INTERFACE2 register can be used to configure the DA9213, DA9214, and DA9215 control interface as a 2-WIRE serial data interface. In this case the GPIO3 and GPI4 are free for regular input/output functions. DA9213, DA9214, and DA9215 has a configurable device write address (default: 0xD0) and a configurable device read address (default: 0xD1). See control IF\_BASE\_ADDR1 for details of configurable addresses. The ADDR\_SEL\_CONF bit is used to configure the device address as IF\_BASE\_ADDR1 or IF\_BASE\_ADDR2 depending on the voltage level applied at a configurable GPI port (see section 5.2.4).

The SK port functions as the 2-WIRE clock and the SI port carries all the power manager bidirectional 2-WIRE data. The 2-WIRE interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (in the  $2~k\Omega$  to  $20~k\Omega$  range). The attached devices only drive the bus lines LOW by connecting them to ground. As a result, two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9213, DA9214, and DA9215 internal clock signals. DA9213, DA9214, and DA9215 will follow the host clock speed within the described limitations, and does not initiate any clock arbitration or slow down. An automatic interface reset can be triggered using control  $2WIRE\_TO$  if the clock signal stops to toggle for more than 35~ms.

The interface supports operation compatible to Standard, Fast, Fast-Plus and High-Speed mode of the I<sup>2</sup>C-bus specification Rev 4. Operation in high-speed mode at 3.4 MHz requires mode changing in order to set spike suppression and slope control characteristics to be compatible with the I<sup>2</sup>C-bus specification. The high-speed mode can be enabled on a transfer-by-transfer basis by sending the master code (0000 1XXX) at the beginning of the transfer. DA9213, DA9214, and DA9215 do not make use of clock stretching, and deliver read data without additional delay up to 3.4 MHz.

Alternatively, PM\_IF\_HSM configures the interface to use high speed mode continuously. In this case, the master code is not required at the beginning of every transfer. This reduces the communication overhead on the bus but limits the slaves attachable to the bus to compatible devices.

The communication on the 2-WIRE bus always takes place between two devices, one acting as the master and the other as the slave. The DA9213, DA9214, and DA9215 will only operate as a SLAVE.

In contrast to the 4-WIRE mode, the 2-WIRE interface has direct access to two pages of the register map (up to 256 addresses). The register at address zero on each page is used as a page control register (with the 2-WIRE bus ignoring the LSB of control REG\_PAGE). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control REVERT. Unless REVERT was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

In 2-WIRE operation DA9213, DA9214, and DA9215 offer an alternative way to access register page 2 and page 3. It removes the need for preceding page selection writes by incrementing the device write/read address by one (default 0xD2/0xD3) for any direct access of page 2 and page 3 (page 0 and 1 access requires the basic write/read device address with the MSB of REG\_PAGE to be 0).

#### 5.4.3 Details of the 2-WIRE Control Bus Protocol

All data is transmitted across the 2-WIRE bus in groups of eight bits. To send a bit the SDA line is driven towards the intended state while the SCL is LOW (a low on SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought HIGH and then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).



Figure 26. Timing of 2-WIRE START and STOP Condition

The 2-WIRE bus is monitored by DA9213, DA9214, and DA9215 for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with A in Figure 27 to Figure 31).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by eight bits of data terminated by a STOP condition. DA9213, DA9214, and DA9215 respond to all bytes with Acknowledge. This is illustrated in Figure 27.

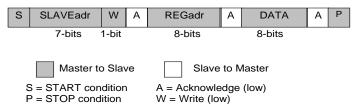


Figure 27. 2-WIRE Byte Write (SDA Line)

When the host reads data from a register it first has to write to DA9213, DA9214, and DA9215 with the target register address and then read from DA9213, DA9214, and DA9215 with a Repeated START or alternatively a second START condition. After receiving the data, the host sends No Acknowledge and terminates the transmission with a STOP condition. This is illustrated in Figure 28.

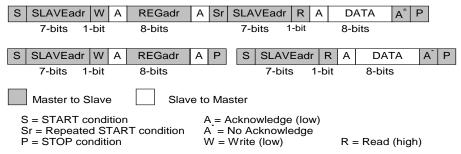


Figure 28. Examples of 2-WIRE Byte Read (SDA Line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not acknowledge after receipt of the data word. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a Not acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent 2-WIRE address is read out, the DA9213, DA9214, and DA9215 will return code zero. This is illustrated in Figure 29.

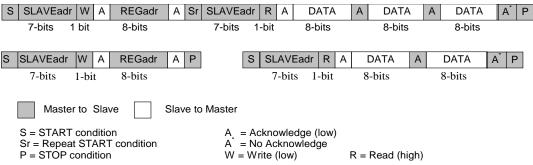


Figure 29. Examples of 2-WIRE Page Read (SDA Line)

Note that the slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the Master sends several data bytes following a slave register address. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address, stores the received data and sends an Acknowledge until the master sends the STOP condition. This is illustrated in Figure 30.

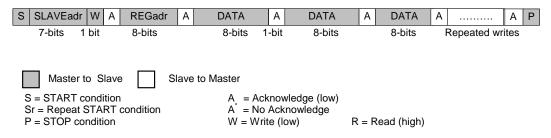


Figure 30. 2-WIRE Page Write (SDA Line)

Via control WRITE\_MODE an alternate write mode can be configured. Register addresses and data are sent in alternation like in Figure 31 to support host repeated write operations that access several non-consecutive registers. Data will be stored at the previously received register address.

An update of WRITE\_MODE cannot be done without interruption within a transmission frame. Thus, if not previously selected or not set as OTP default, the activation of Repeated Write must be done with a regular write on WRITE\_MODE followed by a stop condition. The next frame after a start condition can be written in Repeated Write.

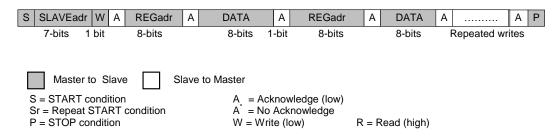


Figure 31. 2-WIRE Repeated Write (SDA Line)

If a new START or STOP condition occurs within a message, the bus will return to IDLE mode.

### 5.5 Internal Temperature Supervision

To protect DA9213, DA9214, and DA9215 from damage due to excessive power dissipation, the internal temperature is continuously monitored. There are three temperature thresholds, as shown in Table 14.

**Table 14. Over-Temperature Thresholds** 

Temperature Threshold	Typical Temperature Setting	Interrupt Event	Status Bit	Masking Bit
TEMP_WARN	125 °C	E_TEMP_WARN	TEMP_WARN	M_TEMP_WARN
TEMP_CRIT	140 °C	E_TEMP_CRIT	TEMP_CRIT	M_TEMP_CRIT
TEMP_POR	150 °C			

When the junction temperature reaches the TEMP\_WARN threshold, DA9213, DA9214, and DA9215 will assert the bit TEMP\_WARN and will generate the event E\_TEMP\_WARN. If not masked using bit M\_TEMP\_WARN, the output port nIRQ will be asserted. The status bit TEMP\_WARN will remain asserted as long as the junction temperature remains higher than TEMP\_WARN.

When the junction temperature increases further to TEMP\_CRIT, DA9213, DA9214, and DA9215 will immediately disable the buck converter, assert the bit TEMP\_CRIT, and will generate the event E\_TEMP\_CRIT. If not masked via bit M\_TEMP\_CRIT, the output port nIRQ will be asserted. The status bit TEMP\_CRIT will remain asserted as long as the junction temperature remains higher than TEMP\_CRIT. The buck converter will be kept disabled as long as the junction temperature is above TEMP\_CRIT. It will not be automatically reenabled even after the temperature drops below the valid threshold (even if the controlling GPI is asserted). A direct write into BUCKA\_EN or BUCKB\_EN, or a toggling of the controlling GPI, is needed to enable the buck converter.

Whenever the junction temperature exceeds TEMP\_POR, a power on reset to the digital core is immediately asserted, which stops all functionalities of DA9213, DA9214, and DA9215. This is needed to prevent possible permanent damage in the case of a rapid temperature increase.

## 6. Application Information

The following recommended components are examples selected from requirements of a typical application.

### 6.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

**Table 15. Recommended Capacitor Types** 

Application	Value	Size	Temp Char	Tol (%)	V-Rate	Туре
VOUT output bypass	47 μF	0603	X5R ±15%	±20	6.3 V	Murata GRM188R60J476ME15
	47 μF	0805	X5R ±15%	±20	10 V	Murata GRM21BR61A476ME15
	22 μF	0603	X5R ±15%	±20	10 V	Murata GRM188R61A226ME15
	22 µF	0402	X5R ±15%	±20	4 V	Semco CL05A226MR5NZNC
VDDx bypass	10 µF	0402	X5R ±15%	±20	10 V	Semco CL05A106MP5NUNC
	10 µF	0603	X5R ±15%	±10	10 V	Murata GRM188R61A105KAAL
VSYS bypass	1 µF	0402	X5R ±15%	±10	10 V	Murata GRM155R61A105KE15
VDDIO bypass	100 nF	01005	X5R ±15%	±10	6.3 V	Semco CL02A104KQ2NNN

#### 6.2 Inductor Selection

Inductors should be selected based upon the following parameters:

- Rated max. current: usually a coil provides two current limits: The Isat specifies the maximum current at which the inductance drops by 30% of the nominal value. The Imax is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance: critical for the converter efficiency and should therefore be minimized.
- The typical recommended output inductance is 0.22 μH per phase. Use of larger output inductance degrades the load transient performance of the buck converter.

**Table 16. Recommended Inductor Types** 

Value (µH)	Size (mm)	Imax(dc) (A)	Isat (A)	Tol (%)	DC Res (mΩ)	Туре
0.47	2.0 x 1.6 x 1.0	4.7	6.2	±20	26	Semco
						CIGT201610EHR47MLE
0.47	2.5 x 2.0 x 0.8	5.5	5.5	±20	15	Semco
						CIGT252008 EHR47MNE
0.24	2.5 x 2.0 x 1.0	5.7	5.7	±20	10	Semco
						CIGT252010 LMR24MNE
0.24	2.5 x 2.0 x 1.2	6.6	6.6	±20	8	Semco
						CIGT252012 LMR24MNE
0.47	2.5 x 2.0 x 1.0	4.1	5.3	±20	28	токо
						DFE252010P-H-R47M
0.47	2.5 x 2.0 x 1.2	4.7	6.1	±20	21	токо
						DFE252012P-H-R47M

### **DA9213, DA9214, DA9215 Datasheet**

Value (µH)	Size (mm)	Imax(dc) (A)	Isat (A)	Tol (%)	DC Res (mΩ)	Туре
0.33	2.5 x 2.0 x 1.0	4.4	5.8	±20	22	TOKO DFE252010P-H-R33M
0.33	2.5 x 2.0 x 1.2	5.0	6.4	±20	18	TOKO DFE252012P-H-R33M
0.47	2.5 x 2.0 x 1.2	4.7	5.2	±20	19	Cyntec HMLE25201B-R47MS
0.22	2.5 x 2.0 x 1.2	7.3	7.0	±20	8	Cyntec PIFE25201B
0.22	2.5 x 2.0 x 1.0	6.6	5.8	±20	10	Cyntec PIFE25201T-R22MS
0.47	4 x 4 x 1.0	9.0	10.5	±20	17	Cyntec PIME041B-R47MS-11
0.47	2.5 x 2.0 x 1.2	3.9	4.8	±20	30	Taiyo Yuden MAMK2520T R47M
0.47	4 x 4 x 1.2	8.7	6.7	±20	14	Coilcraft XFL4012-471ME

# 7. Registers

## 7.1 Register Map

Table 17 displays the register map, where all bits loaded from OTP are marked in bold.

Table 17. Register Map

Addr	Function	7	6	5	4	3	2	1	0	
	Register Page 0									
0×00	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved		F	REG_PAGE		
0×50	STATUS_A	Reserved	Reserved	Reserved	GPI4	GPI3	GPI2	GPI1	GPI0	
0×51	STATUS_B	RAMP_READY_B	RAMP_READY_A	OV_CURR_B	OV_CURR_A	TEMP_CRIT	TEMP_WARN	PWRGOOD_B	PWRGOOD_A	
0×52	EVENT_A	Reserved	E_UVLO_IO	Reserved	E_GPI4	E_GPI3	E_GPI2	E_GPI1	E_GPI0	
0×53	EVENT_B	Reserved	Reserved	E_OV_CURR_B	E_OV_CURR_A	E_TEMP_CRIT	E_TEMP_WARN	E_PWRGOODB	E_PWRGOOD_A	
0×54	MASK_A	Reserved	M_UVLO_IO	Reserved	M_GPI4	M_GPI3	M_GPI2	M_GPI1	M_GPI0	
0×55	MASK_B	Reserved	Reserved	M_OV_CURR_B	M_OV_CURR_A	M_TEMP_CRIT	M_TEMP_WARN	M_PWRGOOD_B	M_PWRGOOD_A	
0×56	CONTROL_A	V_LOCK	SLEW_	RATE_B	SLEW_	RATE_A	TE_A DEBOUNCING			
0×57	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×58	GPIO0-1	GP11_MODE	GPI1_TYPE	GPI1_	PIN	GPI0_MODE	GPI0_TYPE	GPI0_PIN		
0×59	GPIO2-3	GPIO3_MODE	GPIO3_TYPE	GPIO3	_PIN	GPIO2_MODE	GPIO2_TYPE	GPIO2_PIN		
0×5A	GPIO4	Reserved	Reserved	Reser	ved	GPI4_MODE	GPIO4_TYPE	G	PI4_PIN	
0×5B	Reserved	Reserved	Reserved	Reser	ved	Reserved	Reserved	R	eserved	
0×5C	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×5D	BUCKA_CONT	Reserved	VBUC	KA_GPI	VBUCKA_SEL	BUCKA_PD_DIS	BUC	KA_GPI	BUCKA_EN	
0×5E	BUCKB_CONT	Reserved	VBUC	KB_GPI	VBUCKB_SEL	BUCKB_PD_DIS	BUC	KB_GPI	BUCKB_EN	
				Regi	ster Page 1					
0×80	PAGE_CON	REVERT	WRITE_MODE	WRITE_MODE Reserved Reserved				REG_PAGE		
0×D0	BUCK_ILIM		вискв	_ILIM			В	UCKA_ILIM		
0×D1	BUCKA_CONF		BUCKA_DOWN_CTRL			BUCKA_UP_CTRL		BUC	KA_MODE	
0×D2	BUCKB_CONF		BUCKB_DOWN_CTRL			BUCKB_UP_CTRL BUCKB_MODE				

Addr	Function	7	6	5	4	3	2	1	0	
0×D3	BUCK_CONF	Reserved	Reserved	Reserved	PH_SH_EN_B	PH_SH_EN_A	PHASE_SEL_B	PHASE_SEL_B PHASE_SEL_A		
0×D4	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×D5	VBUCKA_MAX	Reserved				VBUCKA_MAX				
0×D6	VBUCKB_MAX	Reserved				VBUCKB_MAX				
0×D7	VBUCKA_A	BUCKA_SL_A				VBUCKA_A				
0×D8	VBUCKA_B	BUCKA_SL_B				VBUCKA_B				
0×D9	VBUCKB_A	BUCKB_SL_A				VBUCKB_A				
0×DA	VBUCKB_B	BUCKB_SL_B				VBUCKB_B				
				Regi	ster Page 2					
0×100	PAGE_CON	REVERT	WRITE_MODE	Reserved	Reserved	Reserved		REG_PAGE		
0×101	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×102	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×103	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×104	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×105	INTERFACE		IF_BASE_	ADDR1		R/W_POL	СРНА	CPOL	nCS_POL	
0×106	INTERFACE2	IF_TYPE	PM_IF_HSM	PM_IF_FMP	PM_IF_V	Reserved	Reserved	Reserved	Reserved	
0×140	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	
0×141	Reserved				Reserv	ed				
0×142	Reserved				Reserv	ed				
0×143	CONFIG_A	Reserved	Reserved	Reserved	2WIRE_TO	GPI_V	Reserved	IRQ_TYPE	IRQ_LEVEL	
0×144	CONFIG_B	UVLO_IO_DIS	PGB_DVC_MASK	PGA_DVC_MASK	OCB_	MASK	OCA	MASK	RELOAD_FUNC_EN	
0×145	CONFIG_C	Reserved	Reserved	Reserved	GPI4_PUPD	GPIO3_PUPD	GPIO2_PUPD	GPI1_PUPD	GPIO_PUPD	
0×146	CONFIG_D	BUCKB	_PG_SEL	BUCKA_P	G_SEL	READY	B_CONF	REA	DYA_CONF	
0×147	CONFIG_E	STAND_ALONE	Reserved	Reserved	Reserved	Reserved		OSC_TUNE		
0×148	CONFIG_F		IF_BASE_	ADDR2		Reserved	Reserved	ADDF	R_SEL_CONF	

### 7.1.1 Register Page Control

Register	Bit	Туре	Label	Description
0x00 PAGE_CON	7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
	6	R/W	WRITE_MODE	2-WIRE multiple write mode (Note 1) 0: Page Write Mode 1: Repeated Write Mode
	5:3	R/W	(reserved)	
	2:0	R/W	REG_PAGE	I <sup>2</sup> C  00x: Selects Register 0x00 to 0xFF  01x: Selects Register 0x100 to 0x17F  SPI  000: Selects Register 0x00 to 0x7F  001: Selects Register 0x80 to 0xFF  010: Selects Register 0x100 to 0x17F  >010: Reserved for production and test

Note 1 Not used for 4-WIRE-IF

## 7.1.2 Register Page 0

#### 7.1.2.1 System Control and Event

The STATUS registers report the current value of the various signals at the time that it is read out.

Register	Bit	Туре	Label	Description
0x50	7:5	R	(reserved)	
STATUS_A	4	R	GPI4	GPI4 level
	3	R	GPI3	GPI3 level
	2	R	GPI2	GPI2 level
	1	R	GPI1	GPI1 level
	0	R	GPI0	GPI0 level

Register	Bit	Туре	Label	Description
0x51	7	R	RAMP_READY_B	De-asserted during Buck A DVC, power up and power down
STATUS_B	6	R	RAMP_READY_A	De-asserted during Buck B DVC, power up and power down
	5	R	OV_CURR_B	Asserted as long as the current limit for Buck B is hit
	4	R	OV_CURR_A	Asserted as long as the current limit for Buck A is hit
	3	R	TEMP_CRIT	Asserted as long as the thermal shutdown threshold is reached
	2	R	TEMP_WARN	Asserted as long as the thermal warning threshold is reached
	1	R	PWRGOOD_B	Asserted as long as the Buck B output voltage is in range
	0	R	PWRGOOD_A	Asserted as long as the Buck A output voltage is in range

The EVENT registers hold information about events that have occurred in DA9213, DA9214, and DA9215. Events are triggered by a change in the status register which contains the status of monitored signals. When an EVENT bit is set in the event register, the IRQ signal is asserted unless the event is masked by a bit in the mask

register. The IRQ triggering event register will be cleared from the host by writing back its read value. New events occurring during clearing will be delayed before they are passed to the event register, ensuring that the host controller does not miss them.

Register	Bit	Туре	Label	Description
0x52	7	R	(reserved)	
EVENT_A	6	R	E_UVLO_IO	UVLO_IO caused event
	5	R	(reserved)	
	4	R	E_GPI4	GPI4 event according to active state setting
	3	R	E_GPI3	GPI3 event according to active state setting
	2	R	E_GPI2	GPI2 event according to active state setting
	1	R	E_GPI1	GPI1 event according to active state setting
	0	R	E_GPI0	GPI0 event according to active state setting

Register	Bit	Туре	Label	Description
0x53	7:6	R	(reserved)	
EVENT_B	5	R	E_OV_CURR_B	OV_CURR Buck B caused event
	4	R	E_OV_CURR_A	OV_CURR Buck A caused event
	3	R	E_TEMP_CRIT	TEMP_CRIT caused event
	2	R	E_TEMP_WARN	TEMP_WARN caused event
	1	R	E_PWRGOOD_B	PWRGOOD loss at Buck B caused event
	0	R	E_PWRGOOD_A	PWRGOOD loss at Buck A caused event

Register	Bit	Туре	Label	Description
0x54	7	R/W	(reserved)	
MASK_A	6	R/W	M_UVLO_IO	Mask UVLO_IO caused nIRQ
	5	R/W	(reserved)	
	4	R/W	M_GPI4	Mask nIRQ interrupt at GPI4
	3	R/W	M_GPI3	Mask nIRQ interrupt at GPI3
	2	R/W	M_GPI2	Mask nIRQ interrupt at GPI2
	1	R/W	M_GPI1	Mask nIRQ interrupt at GPI1
	0	R/W	M_GPI0	Mask nIRQ interrupt at GPI0

Register	Bit	Туре	Label	Description
0x55	7:6	R/W	(reserved)	
MASK_B	5	R/W	M_OV_CURR_B	Mask OV_CURR Buck B caused nIRQ and event
	4	R/W	M_OV_CURR_A	Mask OV_CURR Buck A caused nIRQ and event
	3	R/W	M_TEMP_CRIT	Mask TEMP_CRIT caused nIRQ
	2	R/W	M_TEMP_WARN	Mask TEMP_WARN caused nIRQ
	1	R/W	M_PWRGOOD_B	Mask PWRGOOD Buck B caused nIRQ
	0	R/W	M_PWRGOOD_A	Mask PWRGOOD Buck A caused nIRQ

Register	Bit	Туре	Label	Description
0x56	7	R/W	V_LOCK	0: Allows host writes into registers 0xD0 to 0x14F
CONTROL_A				1: Disables register 0xD0 to 0x14F re-programming from control interfaces
	6:5	R/W	SLEW_RATE_B	Buck B DVC slewing is executed at
				00: 10 mV every 4.0 μs
				01: 10 mV every 2.0 μs
				10: 10 mV every 1.0 μs
				11: 10 mV every 0.5 μs
	4:3	R/W	SLEW_RATE_A	Buck A DVC slewing is executed at
				00: 10 mV every 4.0 μs
				01: 10 mV every 2.0 μs
				10: 10 mV every 1.0 μs
				11: 10 mV every 0.5 μs
	0:2	R/W	DEBOUNCE	Input signals debounce time:
				000: no debounce time
				001: 0.1 ms
				010: 1.0 ms
				011: 10 ms
				100: 50 ms
				101: 250 ms
				110: 500 ms
				111: 1000 ms

### 7.1.2.2 GPIO Control

Register	Bit	Туре	Label	Description
0x58 GPI0-1	7	R/W	GPI1_MODE	0: GPI: debouncing off 1: GPI: debouncing on
	6	R/W	GPI1_TYPE	0: GPI: active low 1: GPI: active high
	5:4	R/W	GPI1_PIN	PIN assigned to:  00: GPI >00: Reserved
	3	R/W	GPI0_MODE	0: GPI: debouncing off 1: GPI: debouncing on
	2	R/W	GPI0_TYPE	0: GPI: active low 1: GPI: active high
	1:0	R/W	GPI0_PIN	PIN assigned to:  00: GPI  01: Track enable  1x: Reserved

Register	Bit	Туре	Label	Description
0x59 GPIO2-3	7	R/W	GPIO3_MODE	0: GPI: debouncing off GPO: Sets output to passive level
	7	R/VV		GPI: debouncing on     GPO: Sets output to active level

Register	Bit	Туре	Label	Description
	6	R/W	GPIO3_TYPE	0: GPI/GPO: active low 1: GPI/GPO: active high
	5:4	R/W	GPIO3_PIN	PIN assigned to:  00: GPI  01: Reserved  10: GPO (Open drain)  11: GPO (Push-pull)
	3	R/W	GPIO2_MODE	O: GPI: debouncing off GPO: Sets output to passive level  1: GPI: debouncing on GPO: Sets output to active level
	2	R/W	GPIO2_TYPE	0: GPI/GPO: active low 1: GPI/GPO: active high
	1:0	R/W	GPIO2_PIN	PIN assigned to:  00: GPI  01: Reserved  10: GPO (Open drain)  11: GPO (Push-pull)

Register	Bit	Туре	Label	Description
0x5A	7:4	R/W	(reserved)	
GPI4	3	R/W	GPI4_MODE	0: GPI: debouncing off 1: GPI: debouncing on
	2	R/W	GPI4_TYPE	0: GPI: active low 1: GPI: active high
	1:0	R/W	GPI4_PIN	PIN assigned to:  00: GPI  01: Reserved  1x: Reserved

## 7.1.2.3 Regulators Control

Register	Bit	Туре	Label	Description
0x5D	7	R/W	(reserved)	
BUCKA_CONT	6:5	R/W	VBUCKA_GPI	Selects the GPI that specifies the target voltage of VBUCKA. This is VBUCKA_A on active to passive transition, VBUCKA_B on passive to active transition.  Active high/low is controlled by GPIx_TYPE.  00: Not controlled by GPIO  01: GPIO1 controlled  10: GPIO2 controlled  11: GPIO4 controlled
	4	R/W	VBUCKA_SEL	Buck A voltage is selected from (ramping):  0: VBUCKA_A  1: VBUCKA_B
	3	R/W	BUCKA_PD_DIS	O: Enable pull-down resistor of Buck A when the buck is disabled  1: Disable pull-down resistor of Buck A when the buck is disabled
	2:1	R/W	BUCKA_GPI	GPIO enables the Buck A on passive to active state transition, disables the Buck A on active to passive state transition  00: Not controlled by GPIO  01: GPIO0 controlled  10: GPIO1 controlled  11: GPIO3 controlled
	0	R/W	BUCKA_EN	0: Buck A disabled 1: Buck A enabled

Register	Bit	Туре	Label	Description
0x5E	7	R/W	(reserved)	
BUCKB_CONT	6:5	R/W	VBUCKB_GPI	Selects the GPI that specifies the target voltage of VBUCKB. This is VBUCKB_A on active to passive transition, VBUCKB_B on passive to active transition.  Active high/low is controlled by GPIx_TYPE.  O0: Not controlled by GPIO  01: GPIO1 controlled  10: GPIO2 controlled  11: GPIO4 controlled
	4	R/W	VBUCKB_SEL	Buck A voltage is selected from (ramping):  0: VBUCKB_A  1: VBUCKB_B
	3	R/W	BUCKB_PD_DIS	O: Enable pull-down resistor of Buck B when the buck is disabled  1: Disable pull-down resistor of Buck B when the buck is disabled
	2:1	R/W	BUCKB_GPI	GPIO enables the Buck B on passive to active state transition, disables the Buck B on active to passive state transition  Oo: Not controlled by GPIO  O1: GPIO0 controlled

Register	Bit	Туре	Label	Description
				10: GPIO1 controlled
				11: GPIO3 controlled
		DAM	DUCKD EN	0: Buck B disabled
	0	R/W	BUCKB_EN	1: Buck B enabled

## 7.1.3 Register Page 1

Register	Bit	Туре	Label	Description
0x80 PAGE_CON	7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
	6	R/W	WRITE_MODE	2-WIRE multiple write mode 0: Page Write Mode 1: Repeated Write Mode
	5:3	R/W	(reserved)	
	2:0	R/W	REG_PAGE	I <sup>2</sup> C  00x: Selects Register 0x00 to 0xFF  01x: Selects Register 0x100 to 0x17F  SPI  000: Selects Register 0x00 to 0x7F  001: Selects Register 0x80 to 0xFF  010: Selects Register 0x100 to 0x17F  >010: Reserved for production and test

## 7.1.3.1 Regulators Settings

Register	Bit	Туре	Label	Description
0xD0				Current limit per phase:
BUCK_ILIM				0000: 4000 mA
				0001: 4200 mA
				0010: 4400 mA
	7:4	R/W	BUCKB_ILIM	Continuing through
				1001: 5800 mA
				to
				1110: 6800 mA
				1111: 7000 mA
				Current limit per phase:
				0000: 4000 mA
				0001: 4200 mA
				0010: 4400 mA
	3:0	R/W	BUCKA_ILIM	Continuing through
				1001: 5800 mA
				to
				4440, 0000 4
				1110: 6800 mA
				1111: 7000 mA

Register	Bit	Туре	Label	Description
0xD1 BUCKA_CONF	7:5	R/W	BUCKA_DOWN_ CTRL	Buck A voltage ramping during power down 000: 1.25 mV/μs 001: 2.5 mV/μs 010: 5 mV/μs 011: 10 mV/μs
				100: 20 mV/μs 101: 30 mV/μs 110: 40 mV/μs 111: no ramped power down
	4:2	R/W	BUCKA_UP_CT RL	Buck A voltage ramping during start up 000: 1.25 mV/μs 001: 2.5 mV/μs 010: 5 mV/μs 011: 10 mV/μs 100: 20 mV/μs (Note 1) 101: 30 mV/μs 110: 40 mV/μs 111: target voltage applied immediately (no soft start)
	1:0	R/W	BUCKA_MODE	00: PFM/PWM mode controlled via voltage A and B registers 01: Automatic mode (1-phase) 10: Buck A always operates in PWM mode 11: Automatic mode

Note 1 Settings higher than 20 mV/µs may cause significant overshoot

Register	Bit	Туре	Label	Description
0xD2				Buck B voltage ramping during power down
BUCKB_CONF				000: 1.25 mV/μs
				001: 2.5 mV/μs
			BUOKE BOWN	010: 5 mV/μs
	7:5	R/W	BUCKB_DOWN_ CTRL	011: 10 mV/μs
			CIKL	100: 20 mV/µs
				101: 30 mV/μs
				110: 40 mV/μs
				111: no ramped power down
			BUCKB_UP_CT RL	Buck B voltage ramping during start up
				000: 1.25 mV/μs
				001: 2.5 mV/μs
				010: 5 mV/μs
	4:2	R/W		011: 10 mV/μs
				100: 20 mV/µs (Note 2)
				101: 30 mV/μs
				110: 40 mV/μs
				111: target voltage applied immediately (no soft start)
				00: PFM/PWM mode controlled via voltage A and B registers
	1:0	R/W	BUCKB_MODE	01: Automatic mode (1-phase)
				10: Buck B always operates in PWM mode
				11: Automatic mode

Note 2 Settings higher than 20 mV/µs may cause significant overshoot

Register	Bit	Туре	Label	Description
0xD3	7:5	R/W	(reserved)	
BUCK_CONF	4	R/W	PH_SH_EN_B	Enable current dependent phase shedding in PWM for Buck B
	3	R/W	PH_SH_EN_A	Enable current dependent phase shedding in PWM for Buck A
	2	R/W	PHASE_SEL_B	Phase selection for Buck B in PWM  0: 1 phase is selected  1: 2 phases are selected
	1:0	R/W	PHASE_SEL_A	Phase selection for Buck A in PWM mode. Settings >01 apply only for DA9213 otherwise the number of phases is limited to max 2 00: 1 phase is selected 01: 2 phases are selected 10: 3 phases are selected (uneven 0/90/180 phase shift)
				11: 4 phases are selected

Register	Bit	Туре	Label	Description
0xD5	7	R/W	(reserved)	
VBUCKA_MAX	6:0	R	VBUCKA_MAX	Sets the maximum voltage allowed for Buck A (OTP programmed, access only in test mode)  0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V  Continuing through 1000110: 1.0 V to  111110: 1.55 V 1111111: 1.57 V
				1000110: 1.0 V to 1111101: 1.55 V

Register	Bit	Туре	Label	Description
0xD6	7	R/W	(reserved)	
VBUCKB_MAX				Sets the maximum voltage allowed for Buck B (OTP programmed, access only in test mode)
				0000000: 0.30 V
	0.0	_	VOLICED MAY	0000001: 0.31 V
	6:0	R	VBUCKB_MAX	0000010: 0.32 V
				Continuing through
				1000110: 1.0 V
				to

Register	Bit	Туре	Label	Description
				1111101: 1.55 V
				1111110: 1.56 V
				1111111: 1.57 V

Register	Bit	Туре	Label	Description
0xD7 VBUCKA_A	7	R/W	DUCKA SI A	0: Configures Buck A to PWM mode whenever selecting A voltage setting
_	,	IN/VV	BUCKA_SL_A	Configures Buck A to automatic mode whenever selecting     A voltage setting
				0000000: 0.30 V
				0000001: 0.31 V
				0000010: 0.32 V
				Continuing through
	6:0	R/W	VBUCKA_A	1000110: 1.0 V
				to
				1111101: 1.55 V
				1111110: 1.56 V
				1111111: 1.57 V

Register	Bit	Туре	Label	Description
0xD8 VBUCKA_B	7	R/W	BUCKA_SL_B	O: Configures Buck A to PWM mode, whenever selecting B voltage setting  1: Configures Buck A to automatic mode, whenever selecting B voltage setting
	6:0	R/W	VBUCKA_B	0000000: 0.30 V 0000001: 0.31 V 0000010: 0.32 V Continuing through 1000110: 1.0 V to 1111101: 1.55 V 1111111: 1.57 V

Register	Bit	Туре	Label	Description
0xD9 VBUCKB_A	_	DAM	BUCKB_SL_A	0: Configures Buck B to PWM mode, whenever selecting A voltage setting
	'	R/W		Configures Buck B to automatic mode, whenever selecting     A voltage setting
				0000000: 0.30 V
6:	6:0	R/W	VBUCKB_A	0000001: 0.31 V
			0000010: 0.32 V	

Register	Bit	Туре	Label	Description
				Continuing through 1000110: 1.0 V to
				1111101: 1.55 V 1111110: 1.56 V 1111111: 1.57 V

Register	Bit	Туре	Label	Description
0xDA VBUCKB_B	7	R/W	BUCKB_SL_B	0: Configures Buck B to PWM mode, whenever selecting B voltage setting
_	'	R/VV	BUCKB_SL_B	1: Configures Buck B to automatic mode, whenever selecting B voltage setting
				0000000: 0.30 V
				0000001: 0.31 V
				0000010: 0.32 V
				Continuing through
	6:0	R/W	VBUCKB B	1000110: 1.0 V
	0.0	IX/VV	VBOOKD_B	to
				1111101: 1.55 V
				1111110: 1.56 V
				1111111: 1.57 V

## 7.1.4 Register Page 2

Register	Bit	Туре	Label	Description
0x100 PAGE_CON	7	R/W	REVERT	Resets REG_PAGE to 000 after read/write access has finished
	6	R/W	WRITE_MODE	2-WIRE multiple write mode  0: Page Write Mode  1: Repeated Write Mode
	5:3	R/W	(reserved)	
	2:0	R/W	REG_PAGE	I <sup>2</sup> C 00x: Selects Register 0x00 to 0xFF 01x: Selects Register 0x100 to 0x17F SPI 000: Selects Register 0x00 to 0x7F 001: Selects Register 0x80 to 0xFF 010: Selects Register 0x100 to 0x17F >010: Reserved for production and test

## 7.1.4.1 Interface and OTP Settings (shared with DA9063)

Register	Bit	Туре	Label	Description
0x105 INTERFACE	7:4	R/W	IF_BASE_ADDR 1	4 MSB of 2-WIRE control interfaces base address XXXX0000  11010000 = 0xD0 write address of PM 2-WIRE interface (page 0 and 1)  11010001 = 0xD1 read address of PM 2-WIRE interface (page 0 and 1)  11010010 = 0xD2 write address of PM-2-WIRE interface (page 2 and 3)  11010011 = 0xD3 read address of PM-2-WIRE interface (page 2 and 3)  Code 0000 is reserved for unprogrammed OTP (triggers start-up with hardware default interface address)
	3	R/W	R/W_POL	4-WIRE: Read/Write bit polarity 0: Host indicates reading access via R/W bit = 0 1: Host indicates reading access via R/W bit = 1
	2	R/W	СРНА	4-WIRE interface clock phase (see Table 12)
	1	R/W	CPOL	4-WIRE interface clock polarity  0: SK is low during idle  1: SK is high during idle
	0	R/W	nCS_POL	4-WIRE chip select polarity 0: nCS is low active 1: nCS is high active

Register	Bit	Туре	Label	Label Description			
0x106 INTERFACE2	7	R/W	IF_TYPE	O: Power manager interface is 4-WIRE. Automatically configures GPIO3 and GPI4 as interface signals. The GPIO configuration is overruled.      Power manager interface is 2-WIRE			
	6	R/W	PM_IF_HSM	Enables continuous high speed mode on 2-WIRE interface if asserted (no master code required)			
	5	R/W	PM_IF_FMP	Enables 2-WIRE interface operating with fast mode+ timings if asserted			
	4	R/W	PM_IF_V	O: Power manager interface in 2-WIRE mode is supplied from VDDCORE (4-WIRE always from VDDIO)  1: Power manager interface in 2-WIRE mode is supplied from VDDIO (4-WIRE always from VDDIO)			
0:3 R/W (I		(reserved)					

## 7.1.4.2 Application Configuration Settings

Register	Bit	Туре	Label	Description
0x143	7:5	R/W	(reserved)	
CONFIG_A	4	R/W	2WIRE_TO	Enables automatic reset of 2-WIRE interface if the clock stays low for >35 ms  0: Disabled  1: Enabled
	3	R/W	GPI_V	GPIs are supplied from:  0: VDDCORE  1: VDDIO

Register	Bit	Туре	Label Description			
	2	R/W	(reserved)			
	1	R/W	IRQ_TYPE	nIRQ output port is: 0: Push-pull 1: Open drain (requires external pull-up resistor)		
	0	R/W	IRQ_LEVEL	nIRQ output port is:  0: Active low  1: Active high		

Register	Bit	Туре	Label	Description
0x144 CONFIG_B	7	R/W	UVLO_IO_DIS	Disable the UVLO for the VDDIO rail and its comparator (suggested for rail voltages different to 1.8 V and to save quiescent current)
	6	R/W	PGB_DVC_MASK	Power-good configuration for Buck B 0: Power-good signal not masked during DVC transitions 1: Power-good signal masked during DVC transitions (keep previous status)
	5	R/W	PGA_DVC_MASK	Power-good configuration for Buck A  0: Power-good signal not masked during DVC transitions  1: Power-good signal masked during DVC transitions (keep previous status)
	4:3	R/W	OCB_MASK	Over Current configuration for Buck B  00: Event generation due to over current hit is always active during DVC transitions of the Buck converter  01: Event generation due to over current hit is masked during DVC transitions of the buck converter + 2 µs extra masking at the end  10: Event generation due to over current hit is masked during DVC transitions of the buck converter + 10 µs extra masking at the end  11: Event generation due to over current hit is masked during DVC transitions of the buck converter + 50 µs
	2:1	R/W	OCA_MASK	extra masking at the end  Over Current configuration for Buck A  O0: Event generation due to over current hit is always active during DVC transitions of the buck converter  O1: Event generation due to over current hit is masked during DVC transitions of the buck converter + 2 μs extra masking at the end  10: Event generation due to over current hit is masked during DVC transitions of the buck converter + 10 μs extra masking at the end  11: Event generation due to over current hit is masked during DVC transitions of the buck converter + 50 μs extra masking at the end
	0	R/W	RELOAD_FUNC_EN	Enable the OTP re-load function for GPIO0 when configured as input port

Register	Bit	Туре	Label	Description
0x145	7:5	R/W	(reserved)	
CONFIG_C	4	R/W	GPI4_PUPD	0: GPI: pull-down resistor disabled 1: GPI: pull-down resistor enabled
	3 R/W GPIO3_PUPD		GPIO3_PUPD	O: GPI: pull-down resistor disabled GPO (open drain): pull up resistor disabled (external pull-up resistor)  1: GPI: pull-down resistor enabled GPO (open drain): pull up resistor
	2 R/W GPIO2_PUPD		GPIO2_PUPD	O: GPI: pull-down resistor disabled GPO (open drain): pull up resistor disabled (external pull-up resistor)  1: GPI: pull-down resistor enabled GPO (open drain): pull up resistor enabled
	1	R/W	GPI1_PUPD	0: GPI: pull-down resistor disabled 1: GPI: pull-down resistor enabled
	0	R/W	GPI0_PUPD	0: GPI: pull-down resistor disabled 1: GPI: pull-down resistor enabled

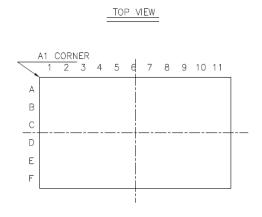
Register	Bit	Туре	Label	Description
0x146 CONFIG_D	7:6	R/W	BUCKB_PG_SEL	Selection of the PG signal for Buck B 00: none 01: GPO2 10: GPO3 11: reserved
	5:4	R/W	BUCKA_PG_SEL	Selection of the PG signal for Buck A 00: none 01: GPO2 10: GPO3 11: reserved
	3:2	R/W	READYB_CONF	Selection of the READY signal for Buck B 00: none 01: GPO2 10: GPO3 11: reserved
	1:0	R/W	READYA_CONF	Selection of the READY signal for Buck A 00: none 01: GPO2 10: GPO3 11: reserved

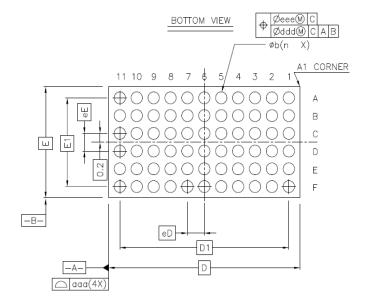
Register	Bit	Туре	Label Description		
0x147 CONFIG_E	7	R/W	STAND_ALONE	0: DA9213, DA9214, and DA9215 is used as companion IC to DA9063 or DA9063-compliant 1: DA9213, DA9214, and DA9215 is standalone or as companion IC with another PMU not DA9063-compliant	
	6:5	R/W	(reserved)		

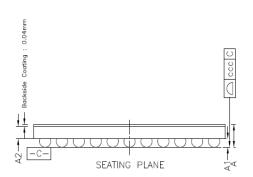
Register	Bit	Туре	Label	Label Description		
	4:3	R/W	(reserved)			
				Tune the main 6 MHz oscillator frequency:		
				000: no tune		
				001: +180 kHz		
				010: +360 kHz		
	2:0	R/W	OSC_TUNE	011: +540 kHz		
				100: +720 kHz		
				101: +900 kHz		
				110: +1080 kHz		
				111: +1260 kHz		

Register	Bit	Туре	Label	Description
0x148 CONFIG_F	7:4	R/W	IF_BASE_ADDR2	If a second I <sup>2</sup> C address is to be selected on ADR_SEL_CONF, this field configures the second address.  4 MSB of 2-WIRE control interfaces base address XXXX0000  11010000 = 0xD0 write address of PM 2-WIRE interface (page 0 and 1)  11010001 = 0xD1 read address of PM 2-WIRE interface (page 0 and 1)  11010010 = 0xD2 write address of PM-2-WIRE interface (page 2 and 3)  11010011 = 0xD3 read address of PM-2-WIRE interface (page 2 and 3)
				Code 0000 is reserved for unprogrammed OTP (triggers start-up with hardware default interface address)
	3:2	R	(reserved)	
				Selects the GPI for the alternative I <sup>2</sup> C address selection:
	4	R/W	ADDD SEL COME	00: none
	1	R/VV	ADDR_SEL_CONF	01: GPI0
				10: GPI1
				11: GPI4

# 8. Package Outline Drawings







	SYMBOL	COMMO	ON DIMEN	ISIONS
	STMBUL	MIN.	NOM.	MAX.
Total Thickness	A	0.471	0.511	0.551
Stand Off	A1	0.177	-	0.205
Wafer Thickness	<b>A</b> 2	0.2	79 <b>±</b> 0	.025
Body Size	D		4.530	BSC
body Size	E		2.509	BSC
Ball Diameter (Size)			0.25	
Ball/Bump Width	Ь	0.255	0.270	0.285
Bell /Burns Bikah	eD		0.4	
Ball/Bump Pitch	еE		0.4	
Ball/Bump Count	n		66	
Edge Bell Center to Center	D1		4.0	BSC
Edge Ball Center to Center	E1		2.0	BSC
Package Edge Tolerance	aaa		0.03	
Coplanarity (whole wafer)	ccc		0.03	
Ball/Bump Offset (Package)	ddd		0.05	
Ball/Bump Offset (Ball)	eee		0.015	

Figure 32. DA9213/14/15 66 WL-CSP Package Outline Drawing

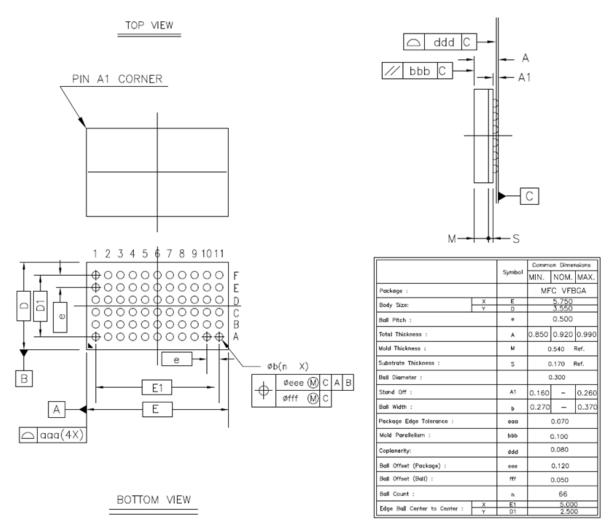


Figure 33. DA9213/14/15 66 VFBGA Package Outline Drawing

## 8.1 Package Marking

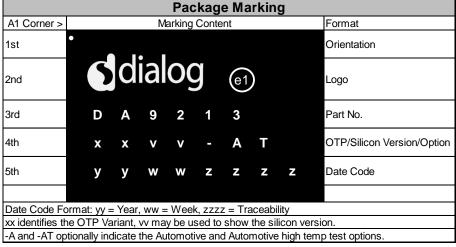


Figure 34. Package Marking

## 9. Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult your Renesas local sales representative.

**Table 18. Ordering Information** 

Part Number	Package	Package & Quantity per	MOQ	Package Outline
DA9213-xxUP2, Note 1	66 WL-CSP	T&R, 4500 pcs	2 reels (9000 pcs)	Figure 32
DA9213-xxUPC	66 WL-CSP	T&R, 4500 pcs	2 reels (9000 pcs)	
DA9213-xxUP6	66 WL-CSP	Tray, 63 pcs	100 trays (6300 pcs)	
DA9214-xxUP2, Note 1	66 WL-CSP	T&R, 4500 pcs	2 reels (9000 pcs)	
DA9214-xxUPC	66 WL-CSP	T&R, 4500 pcs	2 reels (9000 pcs)	
DA9214-xxUP6	66 WL-CSP	Tray, 63 pcs	100 trays (6300 pcs)	
DA9215-xxUP2, Note 1	66 WL-CSP	T&R, 4500 pcs	2 reels (9000 pcs)	
DA9215-xxUPC	66 WL-CSP	T&R, 4500 pcs	2 reels (9000 pcs)	
DA9215-xxUP6	66 WL-CSP	Tray, 63 pcs	100 trays (6300 pcs)	
DA9213-xxFS1BB	66 VFBGA	Tray, 455 pcs	10 trays (4550 pcs)	Figure 33
DA9213-xxFS2BB, Note 1	66 VFBGA	T&R, 5000 pcs	2 reel (10000 pcs)	
DA9213-xxFSCBB	66 VFBGA	T&R, 1100 pcs	4 reels (4400 pcs)	
DA9214-xxFS1BB	66 VFBGA	Tray, 455 pcs	10 trays (4550 pcs)	
DA9214-xxFS2BB, Note 1	66 VFBGA	T&R, 5000 pcs	2 reel (10000 pcs)	
DA9214-xxFSCBB	66 VFBGA	T&R, 1100 pcs	4 reels (4400 pcs)	
DA9215-xxFS1BB	66 VFBGA	Tray, 455 pcs	10 trays (4550 pcs)	
DA9215-xxFS2BB, Note 1	66 VFBGA	T&R, 5000 pcs	2 reel (10000 pcs)	
DA9215-xxFSCBB	66 VFBGA	T&R, 1100 pcs	4 reels (4400 pcs)	

Note 1 Large reel sizes are no longer supported, contact sales for further information

#### **RoHS Compliance**

Renesas Electronics' suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.