

## Datasheet

### 1. General description

DA9211 and DA9212 are PMUs optimised for the supply of CPUs, GPUs, and DDR memory rails in smartphones, tablets and other handheld applications. The fast transient response (10A/μs) and load regulation are optimised for the new generation of multi-core application processors.

DA9212 integrates two dual-phase buck converters, each phase using a small external 0.47  $\mu$ H inductor. Each buck is capable of delivering up to 6 A output current at an output voltage in the range 0.3 - 1.57 V. The input voltage range of 2.8 – 5.5 V makes it suited for a wide variety of low voltage systems, including all Li-Ion battery-powered applications.

DA9211 operates as a single four-phase buck converter delivering up to 12 A output current. To guarantee the highest accuracy and to support multiple PCB routing scenarios without loss of performance, a remote sensing capability is implemented in both DA9211 and DA9212.

The power devices are fully integrated, so no external FETs or Schottky diodes are needed.

A programmable soft start-up can be enabled, which limits the inrush current from the input node and secures a slope-controlled activation of the rail.

The Dynamic Voltage Control (DVC) supports adaptive adjustment of the supply voltage depending on the processor load, either via direct register writes through the communication interface (I2C or SPI compatible) or via an input pin.

A voltage tracking functionality is implemented allowing the buck output voltage to be controlled by an analogue input signal. This feature allows complete control of the buck converter from external signals in the platform.

DA9211 and DA9212 feature integrated over-temperature and over-current protection for increased system reliability without the need for external sensing components. The safety feature set is completed by a  $V_{DDIO}$  under voltage lockout.

The configurable I2C address selection via GPI allows multiple instances of DA9211 and DA9212 or both to be placed in the application sharing the same communication interface with different addresses.

### 2. Key features

- 2.8 V to 5.5 V Input voltage
- 0.3 V to 1.57 V Output voltage
- 12 A Output Current (DA9211)
- 2x 6 A Output Current (DA9212)
- 3 MHz nominal Switching Frequency
- Max Inductor height 1.0 mm
- $\pm 1\%$  Accuracy (static)
- $\pm 3\%$  Accuracy (dynamic)
- Dynamic Voltage Control (DVC)
- Automatic Phase Shedding
- Integrated Power Switches
- Remote Sensing at Point of Load
- I2C/SPI compatible Interface
- Output Voltage Tracking Capability
- Adjustable Soft Start
- -40 to +85 °C Temperature Range
- Package 42 WL-CSP 0.4 mm pitch

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## 3. Applications

- Smartphones, Mobile Phones and Ultra books
- Portable Navigation Devices, TV and Media players
- Tablet PCs, E-Book Readers and Car Infotainment

## 4. System diagrams

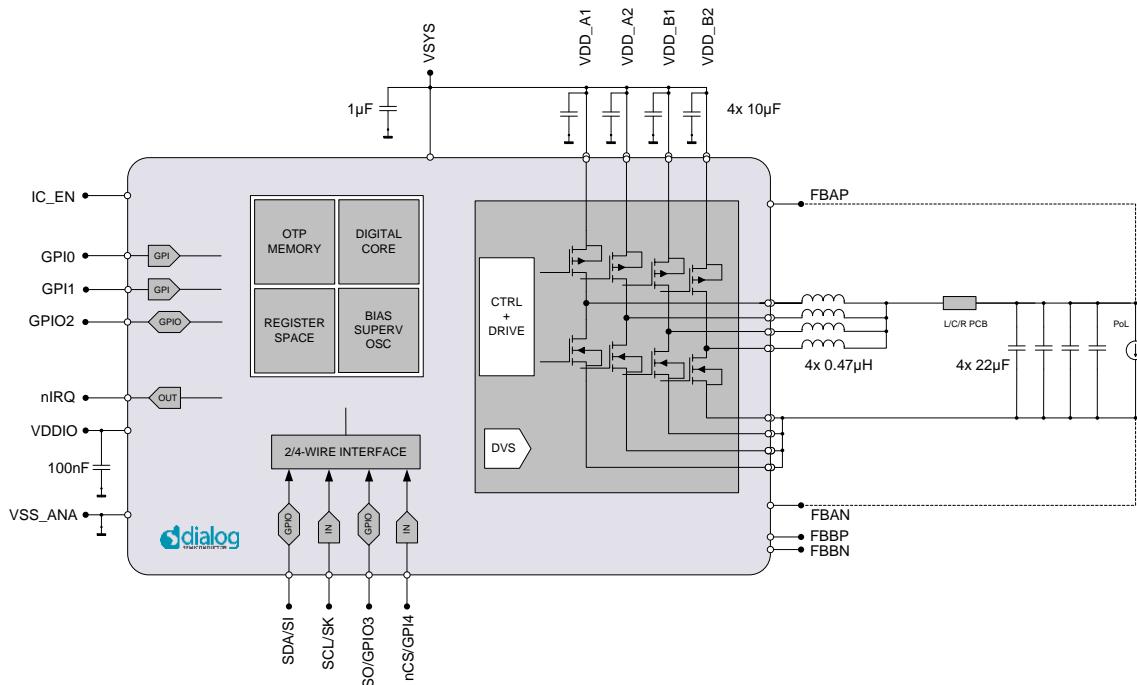


Figure 1: DA9211 System diagram

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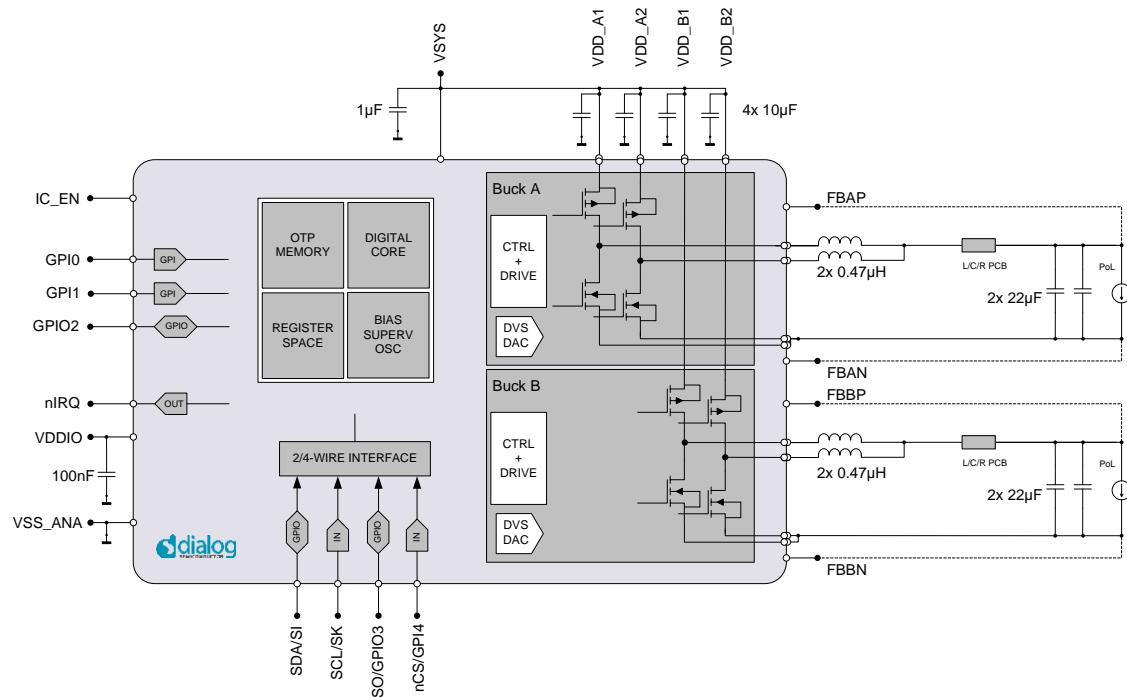


Figure 2: DA9212 System diagram

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### 5. Revision history

| Version | Date          | Description                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|---------|---------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2.0     | Feb 2014      | Initial Release                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 2.1     | July 2014     | Updated transient line<br>Updated UVLO electrical characteristics<br>Swapped GPIO0 and GPIO1<br>Updated IC_EN electrical characteristics<br>Update OSC_TUNE register<br>Updated quiescent current in PFM                                                                                                                                                                                                                                              |
| 2.2     | November 2014 | Updated GPIO-4, SCL, SDA V <sub>IH</sub> and V <sub>IL</sub> specification<br>Updated IC_EN description and timing relation to VDD_IO<br>Updated use case 2-phases<br>Update IQ according to NEROII-34<br>Fixed block diagrams assignment to DA9211 and DA9212<br>Added limitation on use of power good<br>Removed force PFM mode selection<br>Added minimum on time Updated load and line transient performances<br>Updated quiescent current in PWM |
| 3.0     | February 2015 | Added performance plots (to be done)<br>Updated IQ<br>Added Typical Characteristics<br>Updated Application Information<br>Added power dissipation<br>Updated UVLO of VDDIO min value<br>Updated description in selection of A-/B- voltage                                                                                                                                                                                                             |
| 3.1     | December 2020 | Removed confidential markings<br>Updated header, footer and disclaimer pages to latest format.                                                                                                                                                                                                                                                                                                                                                        |

### 6. Terms and definitions

|      |                                                                   |
|------|-------------------------------------------------------------------|
| AP   | Application Processor                                             |
| CPU  | Central Processing Unit                                           |
| DDR  | Double Data Rate SDRAM (Synchronous Dynamic Random Access Memory) |
| DVC  | Dynamic Voltage Control                                           |
| GPU  | Graphic Processing Unit                                           |
| IC   | Integrated Circuit                                                |
| OTP  | One Time Programmable memory                                      |
| PCB  | Printed Circuit Board                                             |
| PMIC | Power Management Integrated Circuit                               |
| POL  | Point Of Load                                                     |

**Datasheet****7. Ordering information**

The order number consists of the part number followed by a suffix indicating the packing method. For details, please consult the [customer portal](#) on the Dialog web site or your local sales representative.

**Table 1: Ordering information**

| Part number  | Package   | Package description | Package outline           |
|--------------|-----------|---------------------|---------------------------|
| DA9211-xxUU2 | 42 WL-CSP | T&R, 5000pcs        | <a href="#">Figure 49</a> |
| DA9211-xxUU6 | 42 WL-CSP | Waffle              |                           |
| DA9212-xxUU2 | 42 WL-CSP | T&R, 5000pcs        |                           |
| DA9212-xxUU6 | 42 WL-CSP | Waffle              |                           |

**8. Pin information****Figure 4: Connection diagram**

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**Table 2: Pin description**

| Pin Name | Signal Name | Second function | Type (See Table 3) | Description                                                  |
|----------|-------------|-----------------|--------------------|--------------------------------------------------------------|
| B1, B2   | LX_A1       |                 | AO                 | Switching node for Buck A phase 1                            |
| E1, E2   | LX_A2       |                 | AO                 | Switching node for Buck A phase 2                            |
| B6, B7   | LX_B1       |                 | AO                 | Switching node for Buck B phase 1                            |
| E6, E7   | LX_B2       |                 | AO                 | Switching node for Buck B phase 2                            |
| A1, A2   | VDD_A1      |                 | PS                 | Supply voltage for Buck A phase 1<br>To be connected to VSYS |
| F1, F2   | VDD_A2      |                 | PS                 | Supply voltage for Buck A phase 2<br>To be connected to VSYS |
| A6, A7   | VDD_B1      |                 | PS                 | Supply voltage for Buck B phase 1<br>To be connected to VSYS |
| F6, F7   | VDD_B2      |                 | PS                 | Supply voltage for Buck B phase 2<br>To be connected to VSYS |
| F5       | IC_EN       |                 | DI                 | Integrated Circuit (IC) Enable Signal                        |
| F3       | nIRQ        |                 | DO                 | Interrupt line towards the host                              |
| E5       | VDDIO       |                 | PS                 | I/O Voltage Rail                                             |
| C3       | FBAP        |                 | AI                 | Positive sense node for the Buck A                           |
| D3       | FBAN        |                 | AI                 | Negative sense node for the Buck A                           |
| C5       | FBBP        |                 | AI                 | Positive sense node for the Buck B for DA9212                |
|          | N/C         |                 | AI                 | For DA9211                                                   |
| D5       | FBBN        |                 | AI                 | Negative sense node for the Buck B for DA9212                |
|          | N/C         |                 | AI                 | For DA9211                                                   |
| A5       | GPIO        | TRK             | DI/AI              | General purpose input, input track                           |
| B5       | GPIO1       |                 | DI                 | General purpose input                                        |
| B4       | GPIO2       |                 | DIO                | General purpose input/output                                 |
| A3       | SDA         | SI              | DIO                | 2-WIRE data, 4-WIRE data input/output                        |
| A4       | SCL         | SK              | DI                 | 2-WIRE clock, 4-WIRE clock                                   |
| D4       | nCS         | GPIO4           | DI                 | 4-WIRE chip select, general purpose input                    |
| C4       | SO          | GPIO3           | DIO                | 4-WIRE data output, general purpose input/output             |
| B3       | NC          |                 |                    | Leave floating                                               |
| F4       | VSYS        |                 | PS                 | Supply for IC and input for voltage supervision              |
| E3       | VSS         |                 | VSS                |                                                              |
| E4       | VSS_ANA     |                 | VSS                |                                                              |

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| Pin Name | Signal Name | Second function | Type (See Table 3) | Description      |
|----------|-------------|-----------------|--------------------|------------------|
| C1, C2   | VSS_A1,     |                 | VSS                | Connect together |
| D1, D2   | VSS_A2      |                 |                    |                  |
| C6, C7   | VSS_B1      |                 |                    |                  |
| D6, D7   | VSS_B2      |                 |                    |                  |

**Table 3: Pin type definition**

| Pin type | Description          | Pin type | Description           |
|----------|----------------------|----------|-----------------------|
| DI       | Digital Input        | AI       | Analogue Input        |
| DO       | Digital Output       | AO       | Analogue Output       |
| DIO      | Digital Input/Output | AIO      | Analogue Input/Output |
| PS       | Power Supply         |          |                       |
| VSS      | Ground               |          |                       |

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### 9. Absolute maximum ratings

Table 4: Absolute maximum ratings (Note 1)

| Symbol               | Parameter                                 | Conditions                                            | Min  | Typ  | Max                             | Unit |
|----------------------|-------------------------------------------|-------------------------------------------------------|------|------|---------------------------------|------|
| T <sub>STG</sub>     | Storage temperature                       |                                                       | -65  |      | +165                            | °C   |
| T <sub>A_LIM</sub>   | Limiting ambient temperature              |                                                       | -40  |      | +85                             | °C   |
| V <sub>DD_LIM</sub>  | Limiting supply voltage                   |                                                       | -0.3 |      | 5.5                             | V    |
| V <sub>PIN</sub>     | Limiting voltage at all pins except above |                                                       | -0.3 |      | V <sub>DD</sub> + 0.3 (max 5.5) | V    |
| P <sub>TOT</sub>     | total power dissipation (Note 2)          | derating factor above T <sub>A</sub> = 70°C: 23 mW/°C | 1265 | 1610 |                                 | mW   |
| V <sub>ESD_HBM</sub> | Electrostatic discharge voltage           | Human Body Model                                      |      |      | 2                               | kV   |

**Note 1** Stresses beyond those listed under 'Absolute maximum ratings' may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Note 2** Obtained from simulation on a 2S2P 4L JEDEC Board (EIA/JESD51-2). Influenced by PCB technology and layout

### 10. Recommended operating conditions

Table 5: Recommended operating conditions (Note 1)

| Symbol            | Parameter                   | Conditions | Min | Typ | Max          | Unit |
|-------------------|-----------------------------|------------|-----|-----|--------------|------|
| V <sub>DD</sub>   | Supply voltage              |            | 2.8 |     | 5.5          | V    |
| V <sub>DDIO</sub> | Input/output supply voltage |            | 1.2 |     | 3.6 (Note 2) | V    |

**Note 1** Within the specified limits, a life time of 10 years is guaranteed

**Note 2** V<sub>DDIO</sub> is not allowed to be higher than V<sub>DD</sub>

**Datasheet****11. Electrical characteristics****Table 6: Buck Converters Characteristics**

Unless otherwise noted, the following is valid for  $T_A = -40$  to  $+85$  °C,  $V_{DD} = 2.8$  V to 5.5 V,  $C_{OUT} = 22$   $\mu$ F /phase, local sensing

| Symbol         | Parameter                                         | Conditions                                                                                                                              | Min            | Typ                    | Max            | Unit      |
|----------------|---------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------|----------------|------------------------|----------------|-----------|
| $V_{DD}$       | Supply voltage                                    | $V_{DD\_x} = V_{SYS}$                                                                                                                   | 2.8            |                        | 5.5            | V         |
| $C_{OUT}$      | Output capacitance (per phase)                    | Including voltage and temperature coefficient                                                                                           | 11             | 22                     | 28.6           | $\mu$ F   |
|                |                                                   |                                                                                                                                         | 23             | 47                     | 61             | $\mu$ F   |
| $ESR_{COUT}$   | Equivalent series resistance (per phase)          | $f > 100$ kHz                                                                                                                           |                |                        | 10             | $m\Omega$ |
| $L_{PHASE047}$ | Inductance (per phase)                            | Including current and temperature dependence                                                                                            | 0.23           | 0.47                   | 0.62           | $\mu$ H   |
| $L_{PHASE022}$ | Inductance (per phase)                            | Including current and temperature dependence                                                                                            | 0.11           | 0.22                   | 0.29           | $\mu$ H   |
| $DCR_{LPHASE}$ | Inductor resistance                               |                                                                                                                                         |                | 30                     | 100            | $m\Omega$ |
| $V_{BUCK}$     | Buck output voltage<br>( <a href="#">Note 1</a> ) | $I_{O} = 0$ to $I_{O\_MAX}$                                                                                                             | 0.3            |                        | 1.57           | V         |
| $V_{OACC}$     | Output voltage accuracy<br>PWM mode               | Incl. static line/load reg and voltage ripple<br>$V_{BUCK} \geq 1$ V                                                                    | -2.0           |                        | +2.0           | %         |
|                |                                                   | Incl. static line/load reg and voltage ripple<br>$V_{BUCK} < 1$ V                                                                       |                | $\pm 20$               |                | $mV$      |
|                |                                                   | $V_{BUCK} = 1$ V<br>$V_{DD} = 3.8$ V<br>no load                                                                                         | -1.0           |                        | +1.0           | %         |
|                |                                                   | $V_{BUCK} = 1$ V<br>$V_{DD} = 3.8$ V<br>no load<br>$T_A = 27$ °C                                                                        | -0.5           |                        | +0.5           | %         |
| $V_{TR\_LOAD}$ | Load regulation transient voltage                 | $I_{O} = 0$ to 5 A, 10 A/ $\mu$ s<br>4-phase operation, PWM<br>$V_{BUCK} \geq 1$ V<br>$0.6$ V $\leq V_{BUCK} < 1$ V                     | -3<br>-30 mV   | <a href="#">Note 2</a> | +3<br>+30 mV   | %         |
|                |                                                   | $I_{O} = 0$ to 5 A, 10 A/ $\mu$ s<br>phase shedding, PWM<br>$V_{DD} \leq 4.2$ V<br>$V_{BUCK} \geq 1$ V<br>$0.6$ V $\leq V_{BUCK} < 1$ V | -3.5<br>-35 mV | <a href="#">Note 2</a> | +3.5<br>+35 mV | %         |

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| Symbol           | Parameter                                          | Conditions                                                                                                                                | Min            | Typ            | Max            | Unit      |
|------------------|----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------|----------------|-----------|
|                  |                                                    | $I_O = 0$ to 5 A, 10 A/ $\mu$ s<br>auto mode, ph shedding<br>$C_{OUT} = 47 \mu F$<br>$V_{BUCK} \geq 1$ V<br>$0.6$ V $\leq V_{BUCK} < 1$ V | -3.5<br>-35 mV | Note 2         | +3.5<br>+35 mV | %         |
| $V_{TR\_LINE}$   | Line regulation transient voltage                  | $V_{DD} = 3$ to 3.6 V<br>$dt = 10 \mu s$<br>$I_O = I_{O(MAX)}/2$                                                                          |                | 8              |                | mV        |
| $R_{RS\_MAX}$    | Maximum remote sensing resistance (Note 3)         | To sense connection at point of load                                                                                                      |                | 10             |                | $m\Omega$ |
| $L_{RS\_MAX}$    | Maximum remote sensing inductance (Note 3)         | To sense connection at point of load                                                                                                      |                | 10             |                | nH        |
| $I_{O\_MAX}$     | Maximum output current                             | Per phase                                                                                                                                 | 3000           |                |                | mA        |
| $I_{LIM\_MIN}$   | Minimum current limit per phase (programmable)     | BUCKA_ILIM<br>BUCKB_ILIM<br>= 0000                                                                                                        | -20%           | 2000           | 20%            | mA        |
| $I_{LIM\_MAX}$   | Maximum current limit per phase (programmable)     | BUCKA_ILIM<br>BUCKB_ILIM<br>= 1111                                                                                                        | -20%           | 5000           | 20%            | mA        |
| $I_{Q\_PWM}$     | Quiescent current @ synchronous rectification mode | Per phase<br>No load<br>$V_{DD} = 3.7$ V                                                                                                  |                | 10             |                | mA        |
| $f_{SW}$         | Switching frequency                                |                                                                                                                                           |                | 3              |                | MHz       |
| $t_{ON\_MIN}$    | minimum on time                                    |                                                                                                                                           |                | 20             |                | ns        |
| $t_{STUP}$       | Start up time                                      | BUCKA_UP_CTRL<br>BUCKB_UP_CTRL<br>= 011                                                                                                   |                | 50<br>(Note 4) |                | $\mu s$   |
| $R_{O\_PD}$      | Output pull-down resistance                        | For each phase at the LX node @ 0.5 V, (see BUCKx_PD_DIS)                                                                                 |                | 150            | 200            | $\Omega$  |
| <b>PFM Mode</b>  |                                                    |                                                                                                                                           |                |                |                |           |
| $V_{BUCK\_PFM}$  | Buck output voltage in PFM                         | $I_O = 0$ mA to $I_{O\_MAX}$                                                                                                              | 0.3            |                | 1.57           | V         |
| $I_{Q\_PFM\_A2}$ | DA9212 quiescent current<br>Buck A enabled         | No load<br>$V_{DD} = 3.7$ V                                                                                                               |                | 56             |                | $\mu A$   |
| $I_{Q\_PFM\_A4}$ | DA9211 quiescent current<br>Buck enabled           | No load<br>$V_{DD} = 3.7$ V                                                                                                               |                | 70             |                | $\mu A$   |

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| Symbol                  | Parameter                                                 | Conditions                         | Min | Typ | Max | Unit |
|-------------------------|-----------------------------------------------------------|------------------------------------|-----|-----|-----|------|
| I <sub>Q_PFM_A2B2</sub> | DA9212 quiescent current<br>Buck A enabled Buck B enabled | No load<br>V <sub>DD</sub> = 3.7 V |     | 104 |     | µA   |

**Note 1** Programmable in 10 mV increments

**Note 2** Additionally to the dc accuracy. The value is intended measured directly at C<sub>OUT(EXT)</sub>. In case of remote sensing, parasitics of PCB and external components may affect this value.

**Note 3** (ca 13 cm) trace routed over a ground plane (approx 1.2 nH/cm)

**Note 4** Time from begin to end of the voltage ramp. Additional 10 µs typical delay, plus internal sync to the enable port

**Datasheet****Table 7: IC Performance and Supervision** $T_A = -40$  to  $+85$  °C

| Symbol              | Parameter                                     | Conditions                                    | Min  | Typ  | Max  | Unit |
|---------------------|-----------------------------------------------|-----------------------------------------------|------|------|------|------|
| $I_{DD\_OFF}$       | Off state supply current @VSYS,VDDx           | $IC\_EN = 0$<br>$T_A = 27$ °C                 |      | 0.1  | 1    | μA   |
| $I_{DD\_ON}$        | On state supply current @VSYS,VDDx            | $IC\_EN = 1$<br>Buck A/B off<br>$T_A = 27$ °C |      | 12   |      | μA   |
| $V_{TH\_PG}$        | Power good threshold voltage                  | referred to $V_{BUCK}$                        |      | -50  |      | mV   |
| $V_{HYS\_PG}$       | Power good hysteresis voltage                 |                                               |      | 50   |      | mV   |
| $V_{TH\_UVLO\_VDD}$ | Under voltage lockout threshold @ $V_{DD}$    |                                               |      | 2.0  |      | V    |
| $V_{TH\_UVLO\_IO}$  | Under voltage lockout threshold @ $V_{DDIO}$  |                                               | 1.33 | 1.45 | 1.55 | V    |
| $V_{HYS\_UVLO\_IO}$ | Under voltage lockout hysteresis @ $V_{DDIO}$ |                                               |      | 70   |      | mV   |
| $T_{TH\_WARN}$      | Thermal warning threshold temperature         |                                               | 110  | 125  | 140  | °C   |
| $T_{TH\_CRIT}$      | Thermal critical threshold temperature        |                                               | 125  | 140  | 155  | °C   |
| $T_{TH\_POR}$       | Thermal power on reset threshold temperature  |                                               | 135  | 150  | 165  | °C   |
| $f_{osc}$           | Internal oscillator frequency                 |                                               | -7%  | 6.0  | +7%  | MHz  |

**Datasheet****Table 8: Digital I/O Characteristics** $T_A = -40$  to  $+85$  °C

| Symbol           | Parameter                                                                                | Conditions                                      | Min                     | Typ | Max                     | Unit |
|------------------|------------------------------------------------------------------------------------------|-------------------------------------------------|-------------------------|-----|-------------------------|------|
| $V_{IH\_EN}$     | HIGH level input voltage @ pin IC_EN                                                     |                                                 | 0.7* $V_{DDIO}$         |     |                         | V    |
| $V_{IL\_EN}$     | LOW level input voltage @ pin IC_EN                                                      |                                                 |                         |     | 0.3* $V_{DDIO}$         | V    |
| $t_{EN}$         | Enable time                                                                              | I/F operating                                   |                         | 750 |                         | μs   |
| $R_{O\_PU\_GPO}$ | Pull up resistor @ GPO                                                                   | $V_{DDIO} = 1.8$ V<br>$V_{GPO} = 0$ V           |                         | 100 |                         | kΩ   |
| $R_{I\_PD\_GPI}$ | Pull down resistor @ GPI                                                                 | $V_{DDIO} = 1.8$ V<br>$V_{GPI} = V_{DDIO}$      |                         | 150 |                         | kΩ   |
| $V_{IH}$         | GPIO-4, SCL, SDA, (2-WIRE mode)<br>HIGH level input voltage                              | $V_{LDOCORE}$ mode<br>$V_{DDIO}$ mode           | 1.75<br>0.7* $V_{DDIO}$ |     |                         | V    |
| $V_{IL}$         | GPIO-4, SCL, SDA, (2-WIRE mode)<br>LOW level input voltage                               | $V_{LDOCORE}$ mode<br>$V_{DDIO}$ mode           |                         |     | 0.75<br>0.3* $V_{DDIO}$ | V    |
| $V_{IH\_4WIRE}$  | SK, nCS, SI (4-WIRE Mode)<br>HIGH level input voltage                                    |                                                 | 0.7* $V_{DDIO}$         |     |                         | V    |
| $V_{IL\_4WIRE}$  | SK, nCS, SI (4-WIRE Mode)<br>LOW level input voltage                                     |                                                 |                         |     | 0.3* $V_{DDIO}$         | V    |
| $V_{OH}$         | GPO2-3, SO (4-WIRE mode)<br>HIGH level output voltage                                    | push-pull mode<br>@1mA<br>$V_{DDIO} \geq 1.5$ V | 0.8* $V_{DDIO}$         |     |                         | V    |
| $V_{OL1}$        | GPO2-3, SDA (2-WIRE mode) SO (4-WIRE mode)<br>LOW level output voltage @ $I_{OL} = 1$ mA |                                                 |                         |     | 0.3                     | V    |
| $V_{OL3}$        | SDA (2-WIRE Mode)<br>LOW level output voltage @ $I_{OL} = 3$ mA                          |                                                 |                         |     | 0.24                    | V    |
| $V_{OL20}$       | SDA (2-WIRE Mode)<br>LOW level output voltage @ $I_{OL} = 20$ mA                         |                                                 |                         |     | 0.4                     | V    |
| $C_{IN}$         | CLK, SDA (2-WIRE Mode)<br>input capacitance                                              |                                                 |                         | 2.5 | 10                      | pF   |

**Datasheet**

| Symbol    | Parameter                                                  | Conditions                                                                                 | Min                      | Typ | Max              | Unit |
|-----------|------------------------------------------------------------|--------------------------------------------------------------------------------------------|--------------------------|-----|------------------|------|
| $t_{SP}$  | CLK, SDA<br>(2-WIRE Mode)<br>spike suppression pulse width | Fast/Fast+ mode<br>High Speed mode                                                         | 0<br>0                   |     | 50<br>10         | ns   |
| $t_{fDA}$ | Fall time of SDA signal<br>(2-WIRE Mode)                   | Fast @ $C_b < 550\text{pF}$<br>HS @ $10 < C_b < 100\text{pF}$<br>HS @ $C_b < 400\text{pF}$ | 20+0.1 $C_b$<br>10<br>20 |     | 120<br>80<br>160 | ns   |

**Table 9: 2-WIRE Control Bus Characteristics** $T_A = -40$  to  $+85^\circ\text{C}$ 

| Symbol                          | Parameter                                  | Conditions        | Min        | Typ | Max  | Unit          |
|---------------------------------|--------------------------------------------|-------------------|------------|-----|------|---------------|
| $t_{BUF}$                       | Bus free time from STOP to START condition |                   | 0.5        |     |      | $\mu\text{s}$ |
| $C_B$                           | Bus line capacitive load                   |                   |            |     | 150  | $\text{pF}$   |
| <b>Standard/Fast/Fast+ Mode</b> |                                            |                   |            |     |      |               |
| $f_{SCL}$                       | Clock frequency @ pin SCL                  |                   | 0 (Note 1) |     | 1000 | $\text{kHz}$  |
| $t_{SU\_STA}$                   | START condition set-up time                |                   | 0.26       |     |      | $\mu\text{s}$ |
| $t_{H\_STA}$                    | START condition hold time                  |                   | 0.26       |     |      | $\mu\text{s}$ |
| $t_{W\_CL}$                     | Clock LOW duration                         |                   | 0.5        |     |      | $\mu\text{s}$ |
| $t_{W\_CH}$                     | Clock HIGH duration                        |                   | 0.26       |     |      | $\mu\text{s}$ |
| $t_R$                           | Rise time @ pin CLK and DATA               | Input requirement |            |     | 1000 | ns            |
| $t_F$                           | Fall time @ pin CLK and DATA               | Input requirement |            |     | 300  | ns            |
| $t_{SU\_D}$                     | Data set-up time                           |                   | 50         |     |      | ns            |
| $t_{H\_D}$                      | Data hold time                             |                   | 0          |     |      | ns            |
| <b>High Speed Mode</b>          |                                            |                   |            |     |      |               |
| $f_{SCL\_HS}$                   | Clock frequency @ pin SCL                  |                   | 0 (Note 1) |     | 3400 | $\text{kHz}$  |
| $t_{SU\_STA\_HS}$               | START condition set-up time                |                   | 160        |     |      | ns            |
| $t_{H\_STA\_HS}$                | START condition hold time                  |                   | 160        |     |      | ns            |
| $t_{W\_CL\_HS}$                 | Clock LOW duration                         |                   | 160        |     |      | ns            |
| $t_{W\_CH\_HS}$                 | Clock HIGH duration                        |                   | 60         |     |      | ns            |
| $t_{R\_HS}$                     | Rise time @ pin CLK and DATA               | Input requirement |            |     | 160  | ns            |

## Datasheet

| Symbol            | Parameter                       | Conditions        | Min | Typ | Max | Unit |
|-------------------|---------------------------------|-------------------|-----|-----|-----|------|
| $t_{F\_HS}$       | Fall time<br>@ pin CLK and DATA | Input requirement |     |     | 160 | ns   |
| $t_{SU\_D\_HS}$   | Data set-up time                |                   | 10  |     |     | ns   |
| $t_{H\_D\_HS}$    | Data hold time                  |                   | 0   |     |     | ns   |
| $t_{SU\_STO\_HS}$ | STOP condition set-up time      |                   | 160 |     |     | ns   |

**Note 1** Minimum clock frequency is 10 kHz if 2WIRE\_TO is enabled

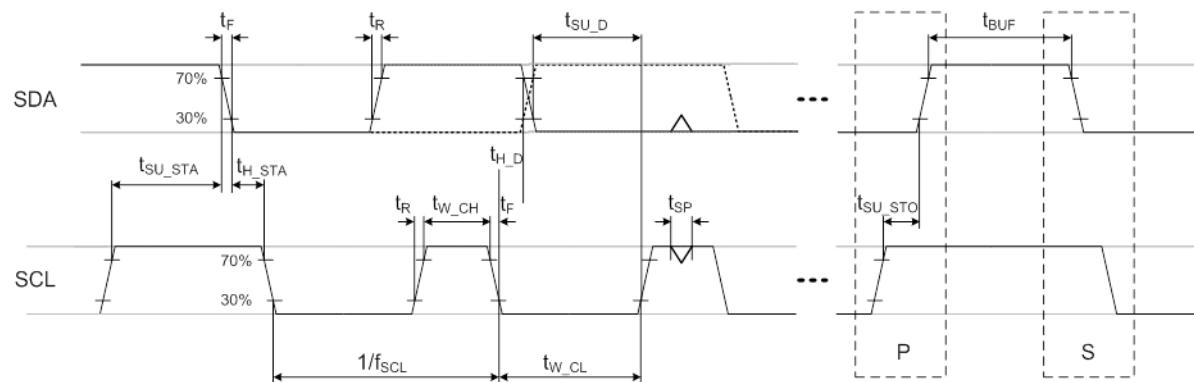


Figure 5: 2-WIRE Bus Timing

## Datasheet

Table 10: 4-WIRE Control Bus Characteristics

 $T_A = -40$  to  $+85$  °C

| Symbol       | Parameter                 | Label in plot                      | Min         | Typ | Max | Unit |
|--------------|---------------------------|------------------------------------|-------------|-----|-----|------|
| $C_B$        | Bus line capacitive load  |                                    |             |     | 100 | pF   |
| $t_c$        | Cycle time                | 1                                  | 70          |     |     | ns   |
| $tsu_{cs}$   | Chip select setup time    | 2, from CS active to first SK edge | 20          |     |     | ns   |
| $t_{H_{CS}}$ | Chip select hold time     | 3, from last SK edge to CS idle    | 20          |     |     | ns   |
| $tw_{CL}$    | Clock LOW duration        | 4                                  | 0.4 x $t_c$ |     |     | ns   |
| $tw_{CH}$    | Clock HIGH duration       | 5                                  | 0.4 x $t_c$ |     |     | ns   |
| $tsu_{SI}$   | Data input setup time     | 6                                  | 10          |     |     | ns   |
| $t_{H_{SI}}$ | Data input hold time      | 7                                  | 10          |     |     | ns   |
| $tv_{SO}$    | Data output valid time    | 8                                  |             |     | 22  | ns   |
| $t_{H_{SO}}$ | Data output hold time     | 9                                  | 6           |     |     | ns   |
| $tw_{CS}$    | Chip select HIGH duration | 10                                 | 20          |     |     | ns   |

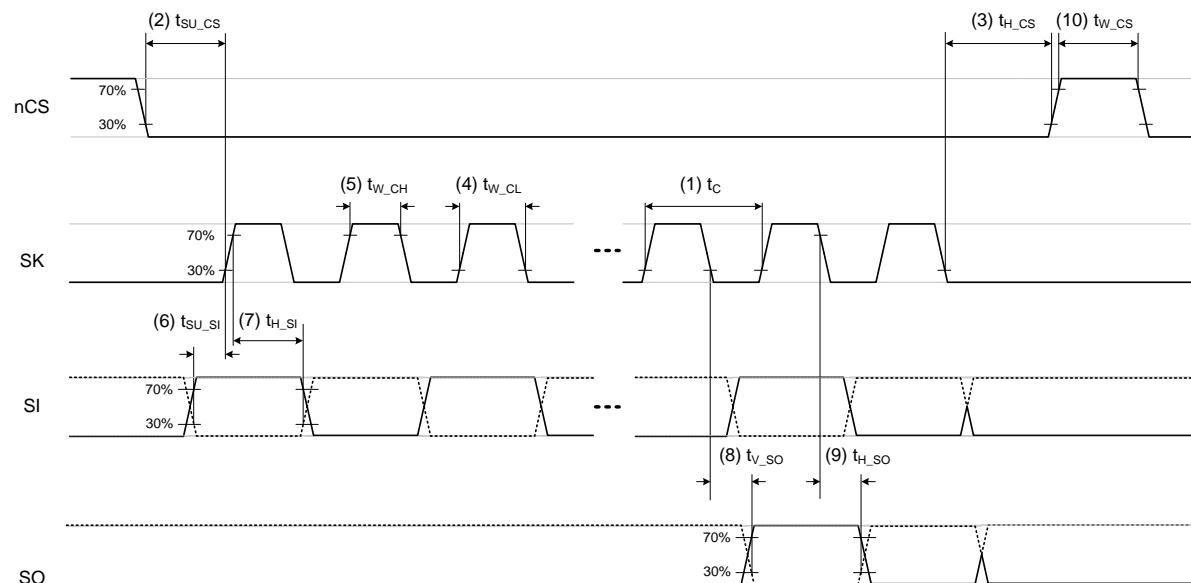


Figure 6: 4-WIRE Bus Timing

**Datasheet****Table 11: Graphs of Typical Characteristics**

| Parameter               | Test Conditions                                                                          | Figure                    |
|-------------------------|------------------------------------------------------------------------------------------|---------------------------|
| Efficiency              | Efficiency vs Output Current, $V_{OUT} = 1.0$ V, 4 phases                                | <a href="#">Figure 7</a>  |
|                         | Efficiency vs Output Current, $V_{OUT} = 1.2$ V, 4 phases                                | <a href="#">Figure 8</a>  |
|                         | Efficiency vs Output Current, $V_{OUT} = 0.9$ V, 4 phases                                | <a href="#">Figure 9</a>  |
|                         | Efficiency vs Output Current, $V_{OUT} = 1.0$ V, 2 phases                                | <a href="#">Figure 10</a> |
|                         | Efficiency vs Output Current, $V_{OUT} = 1.2$ V, 2 phases                                | <a href="#">Figure 11</a> |
|                         | Efficiency vs Output Current, $V_{OUT} = 0.9$ V, 2 phases                                | <a href="#">Figure 12</a> |
|                         | Efficiency vs Input Voltage, $I_{OUT} = 100$ mA                                          | <a href="#">Figure 13</a> |
|                         | Efficiency vs Input Voltage, $I_{OUT} = 2$ A                                             | <a href="#">Figure 14</a> |
|                         | Efficiency vs Input Voltage, $I_{OUT} = 10$ A                                            | <a href="#">Figure 15</a> |
| Start-up                | no load, STARTUP_CTRL=000 (slowest), $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                     | <a href="#">Figure 16</a> |
|                         | no load, STARTUP_CTRL=100 (default), $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                     | <a href="#">Figure 17</a> |
|                         | no load, STARTUP_CTRL=110 (fastest), $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                     | <a href="#">Figure 18</a> |
|                         | 1Ω load, STARTUP_CTRL=000 (slowest), $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                     | <a href="#">Figure 19</a> |
|                         | 1Ω load, STARTUP_CTRL=100 (default), $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                     | <a href="#">Figure 20</a> |
|                         | 1Ω load, STARTUP_CTRL=110 (fastest), $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                     | <a href="#">Figure 21</a> |
|                         | Start up from IC_EN no load, STARTUP_CTRL=100 (default), $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V | <a href="#">Figure 22</a> |
| DVC                     | DVC no load, slowest speed 2.5mV/μs, $V_{DD}=3.7$ V, $V_{OUT}$ 1.2V/0.8V                 | <a href="#">Figure 23</a> |
|                         | DVC no load, default speed 10mV/μs, $V_{DD}=3.7$ V, $V_{OUT}$ 1.2V/0.8V                  | <a href="#">Figure 24</a> |
|                         | DVC no load, fastest speed 20mV/μs, $V_{DD}=3.7$ V, $V_{OUT}$ 1.2V/0.8V                  | <a href="#">Figure 25</a> |
| Switching waveforms     | PWM, no load, $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                                            | <a href="#">Figure 26</a> |
|                         | Voltage and current ripple, PWM, no load, $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                | <a href="#">Figure 27</a> |
|                         | PFM, no load, $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                                            | <a href="#">Figure 28</a> |
| Load Transient response | PWM, 4-phases, 0→5A in 10 A/μs, $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                          | <a href="#">Figure 29</a> |
|                         | PWM, 4-phases, 1→5A in 10 A/μs, $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                          | <a href="#">Figure 30</a> |
|                         | Auto, 4-phases, 10mA→5A in 10 A/μs, $V_{DD}=3.7$ V, $V_{OUT}=1.0$ V                      | <a href="#">Figure 31</a> |

## Datasheet

## 12. Typical Characteristics

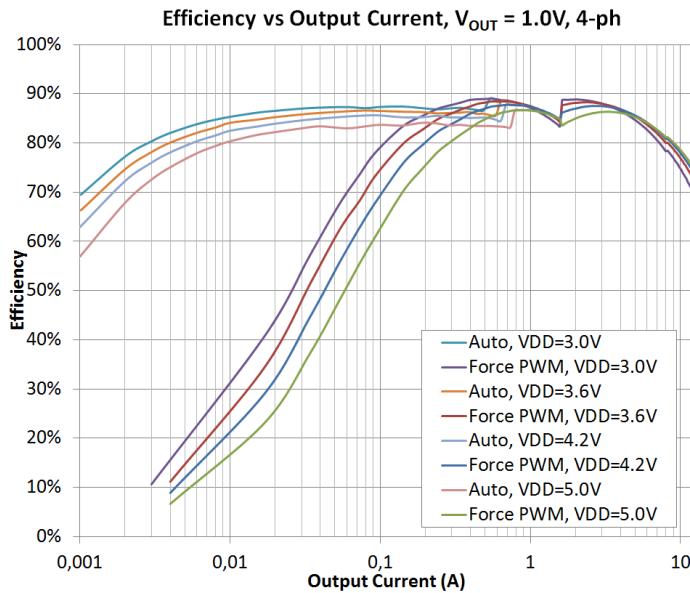


Figure 7

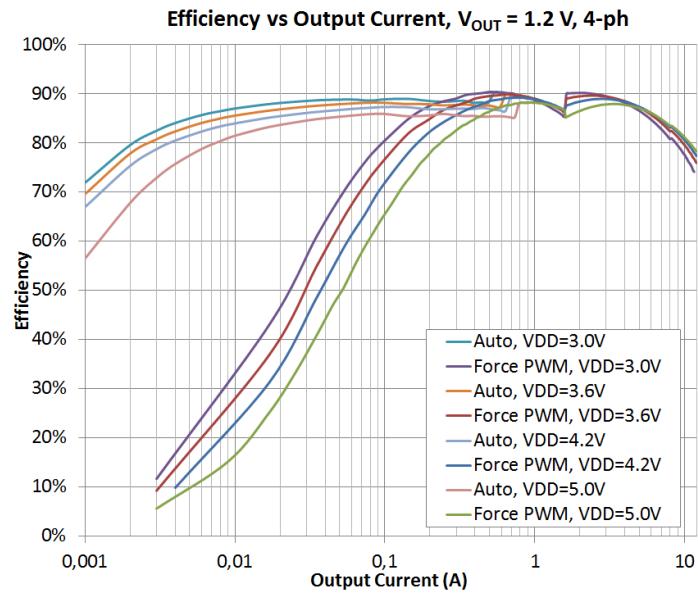


Figure 8

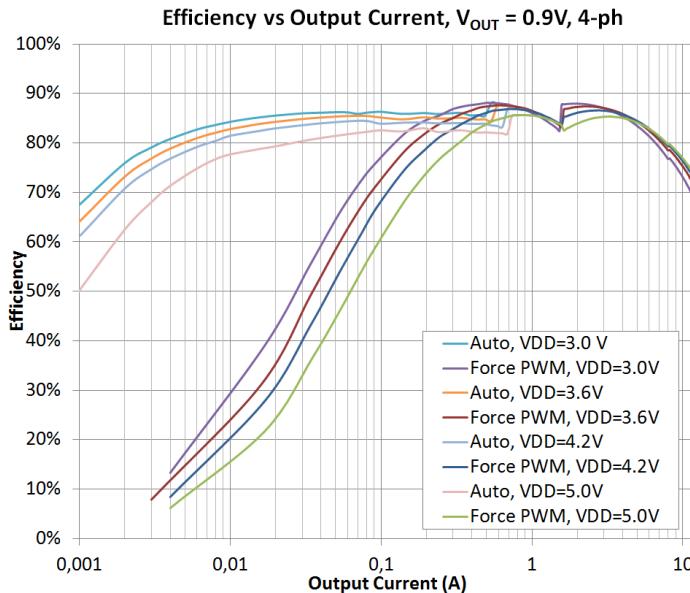


Figure 9

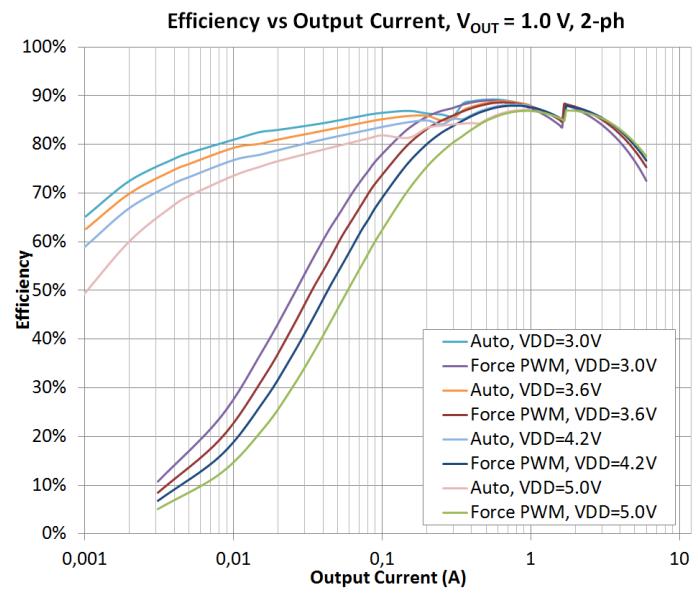
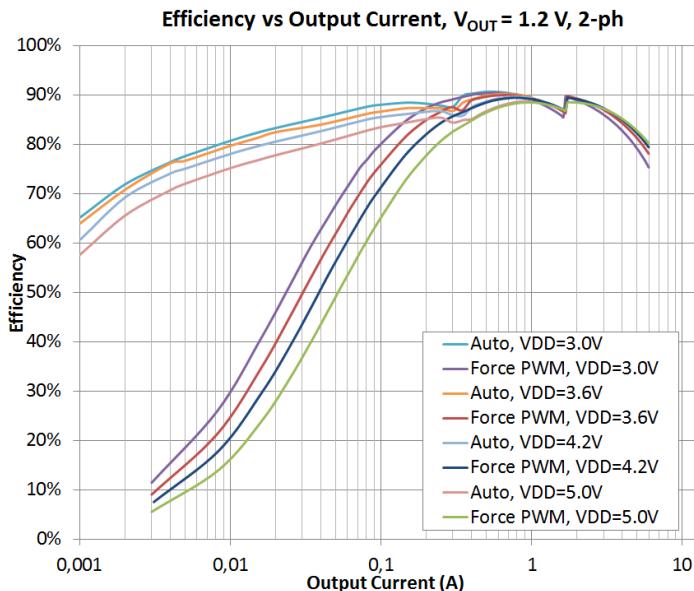
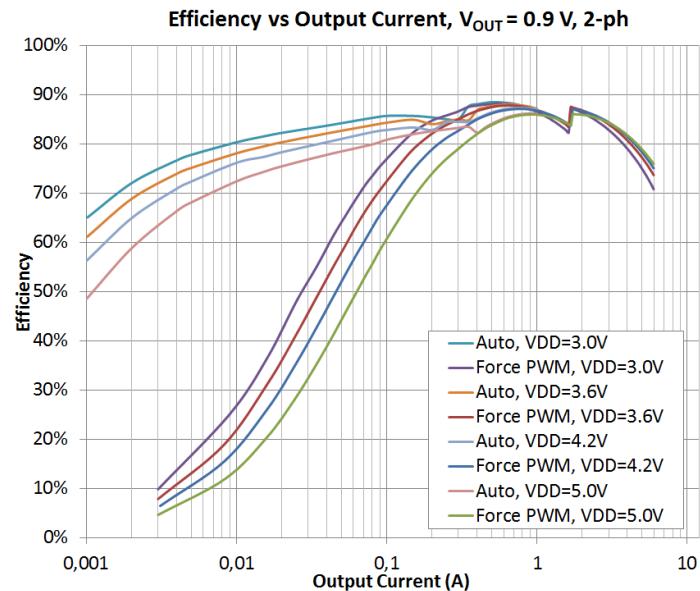
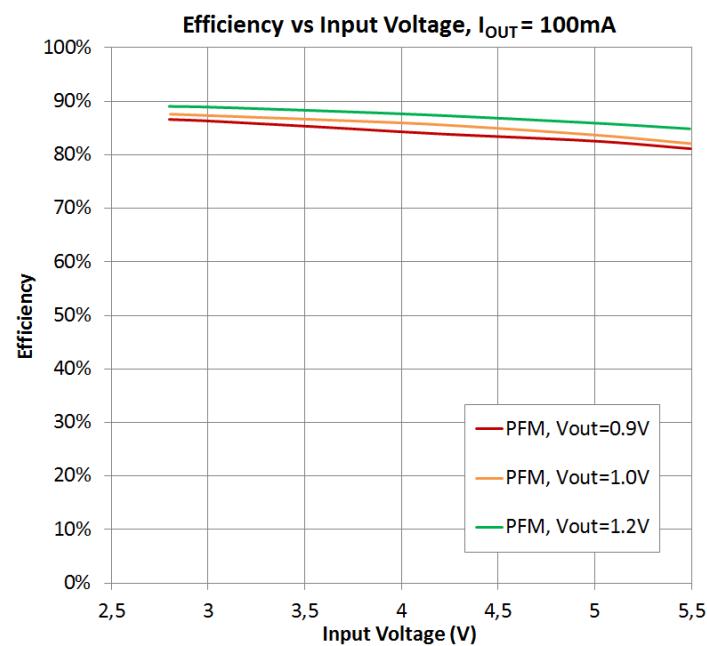
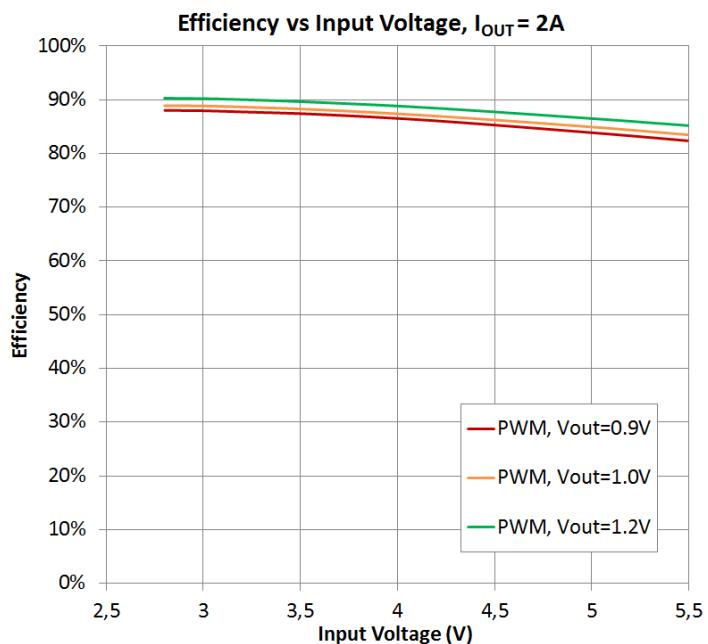


Figure 10

**Datasheet****Figure 11****Figure 12****Figure 13****Figure 14**

## Datasheet

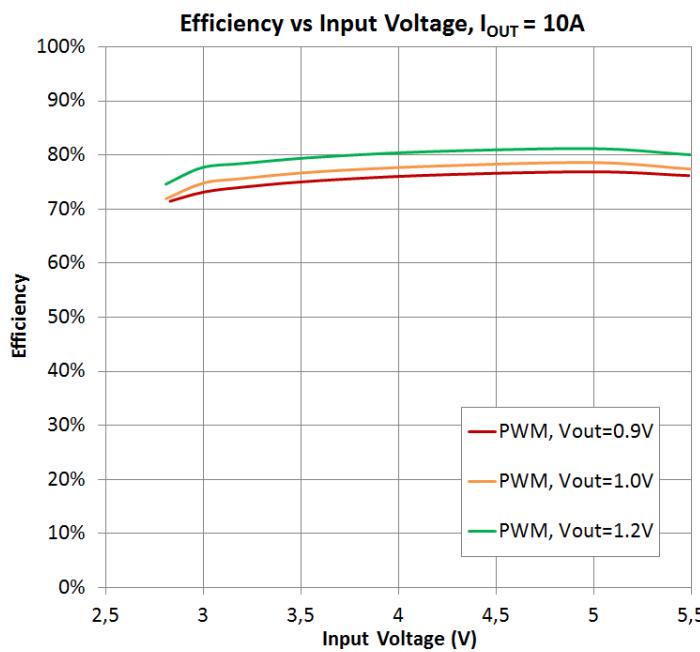


Figure 15

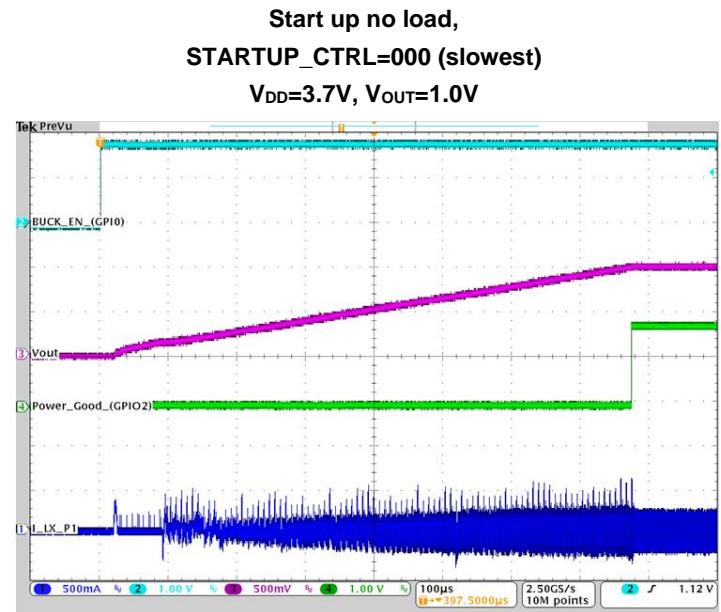


Figure 16

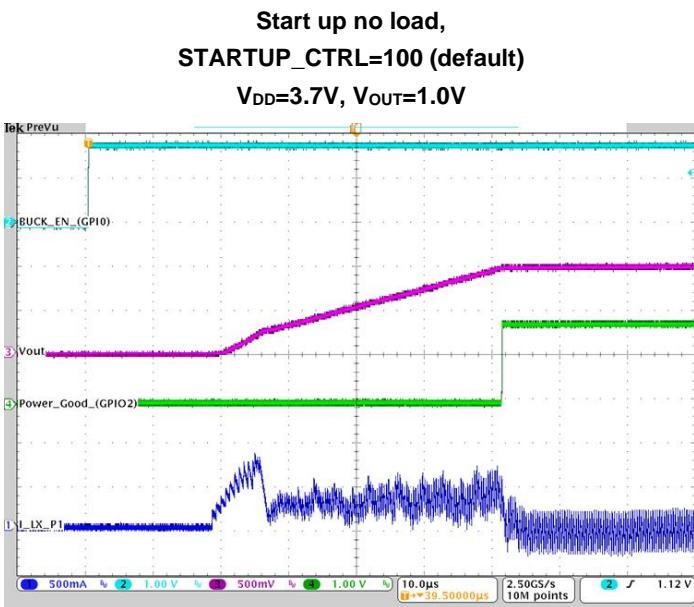


Figure 17

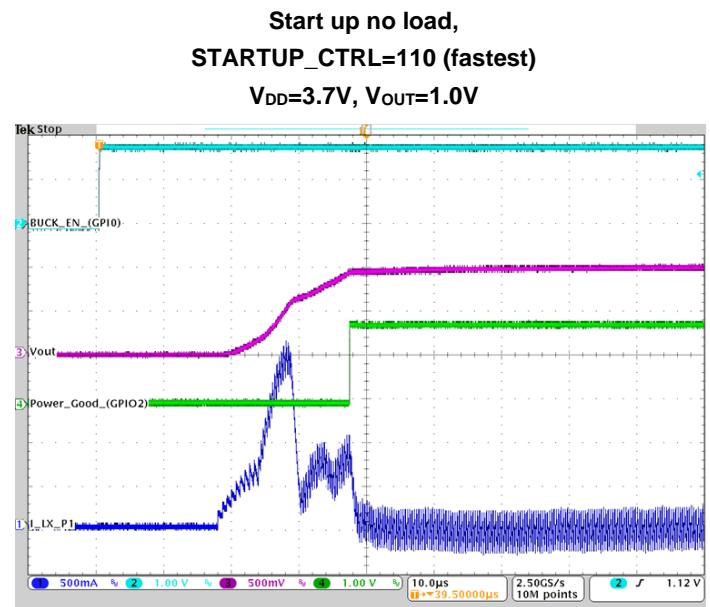


Figure 18

## Datasheet

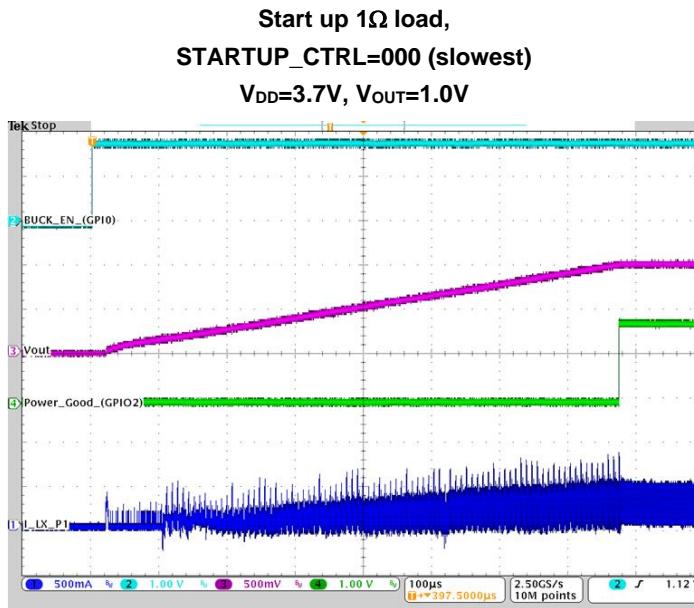


Figure 19

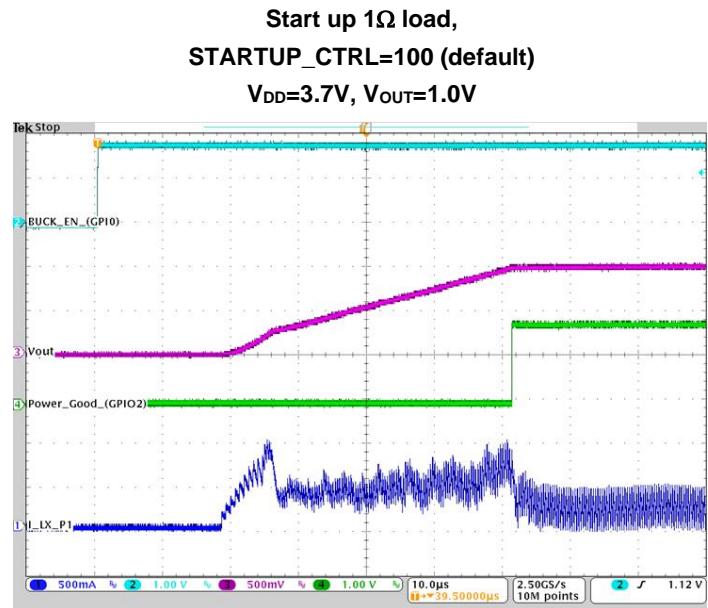


Figure 20

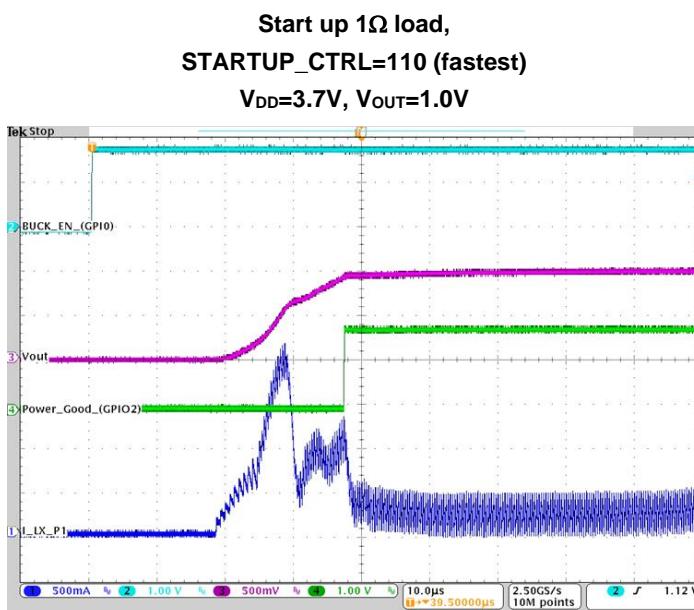


Figure 21

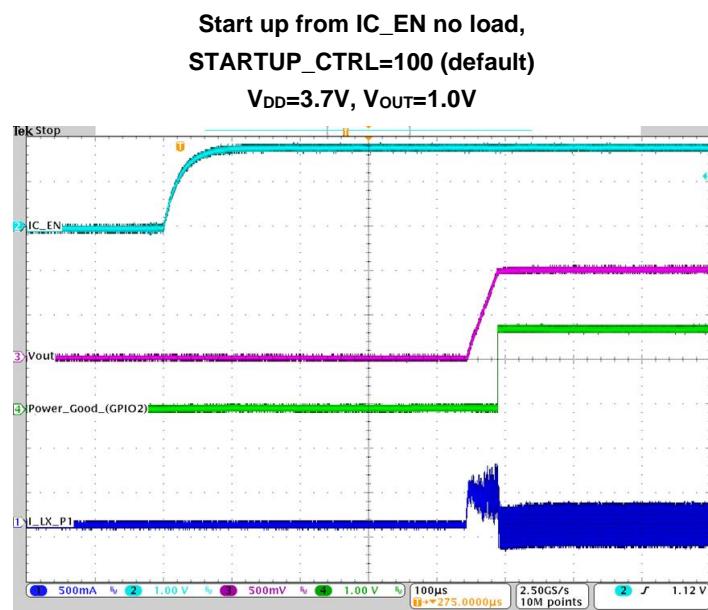
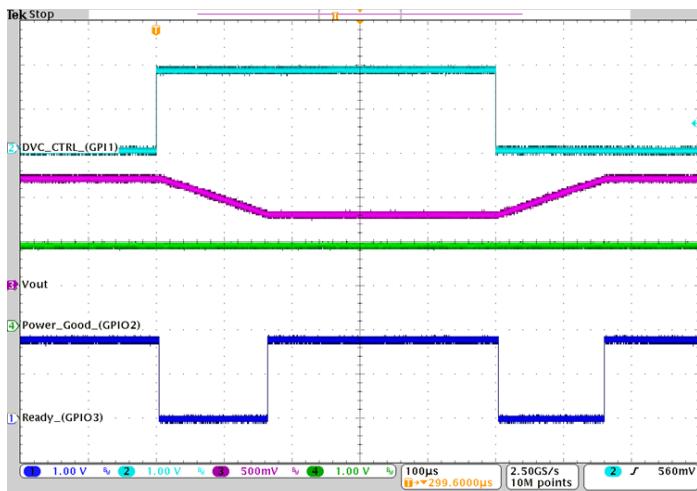


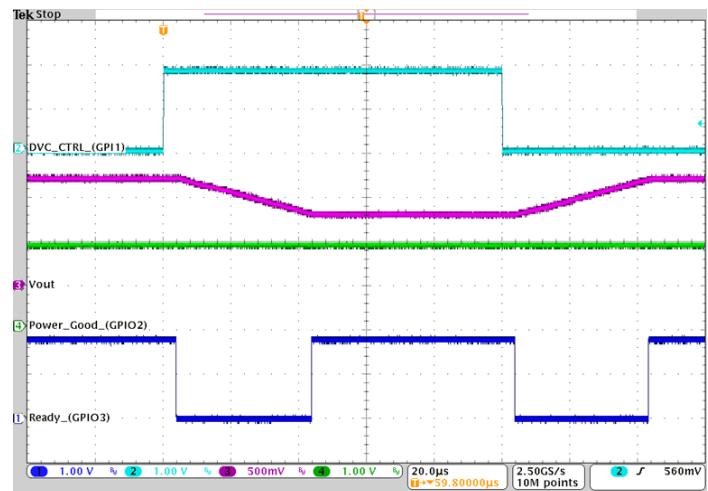
Figure 22

**Datasheet**

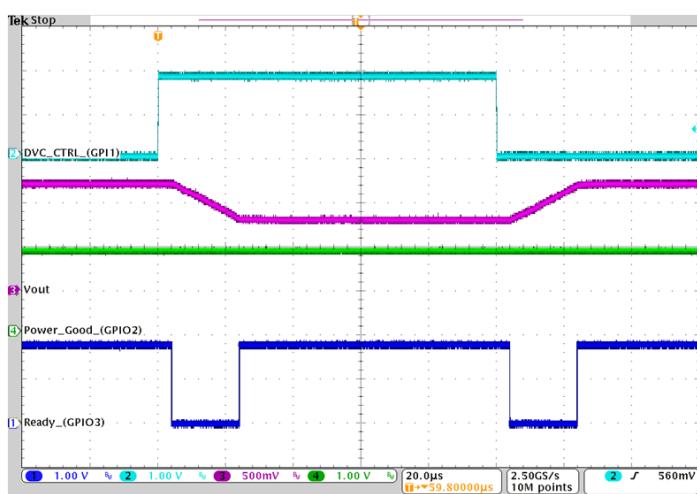
**DVC no load,  
slowest speed 2.5mV/μs  
V<sub>DD</sub>=3.7V, V<sub>OUT</sub> 1.2V/0.8V**


**Figure 23**

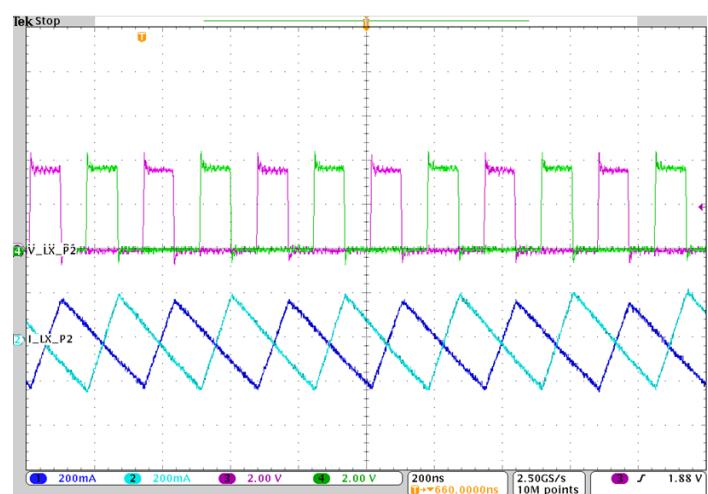
**DVC no load,  
default speed 10mV/μs  
V<sub>DD</sub>=3.7V, V<sub>OUT</sub> 1.2V/0.8V**


**Figure 24**

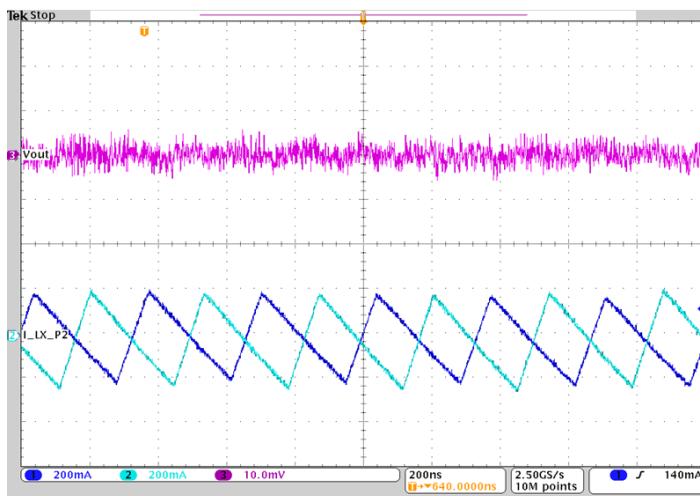
**DVC no load,  
fastest speed 20mV/μs  
V<sub>DD</sub>=3.7V, V<sub>OUT</sub> 1.2V/0.8V**


**Figure 25**

**Switching waveforms,  
PWM, no load  
V<sub>DD</sub>=3.7V, V<sub>OUT</sub>=1.0V**

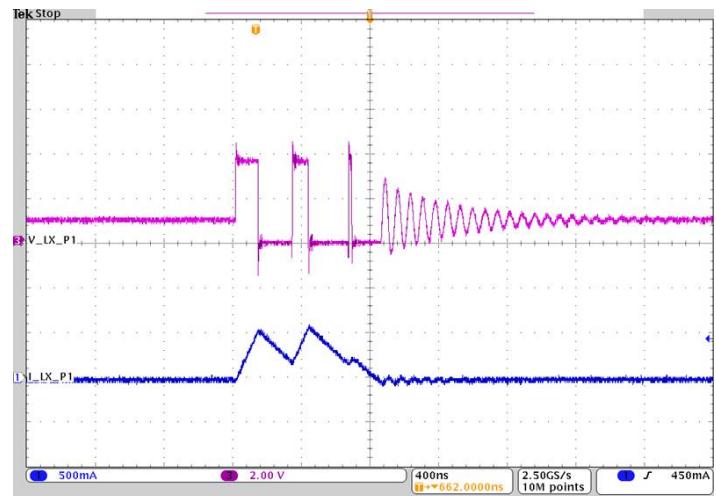

**Figure 26**

**Voltage and current ripple,  
PWM, no load**  
 **$V_{DD}=3.7V$ ,  $V_{OUT}=1.0V$**



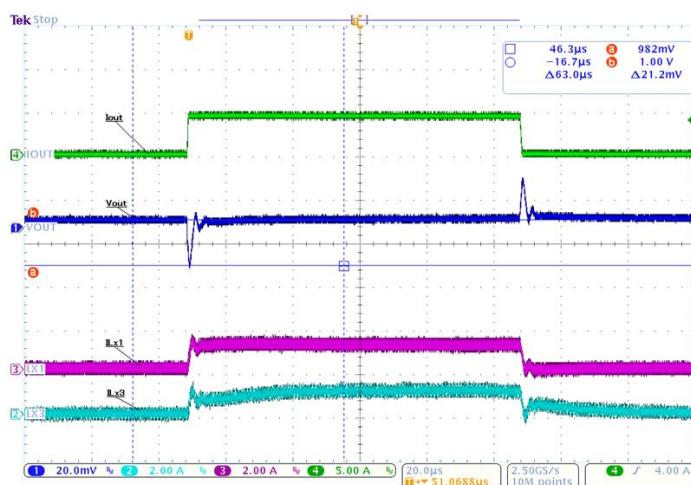
**Figure 27**

**Switching waveforms,  
PFM, no load**  
 **$V_{DD}=3.7V$ ,  $V_{OUT}=1.0V$**



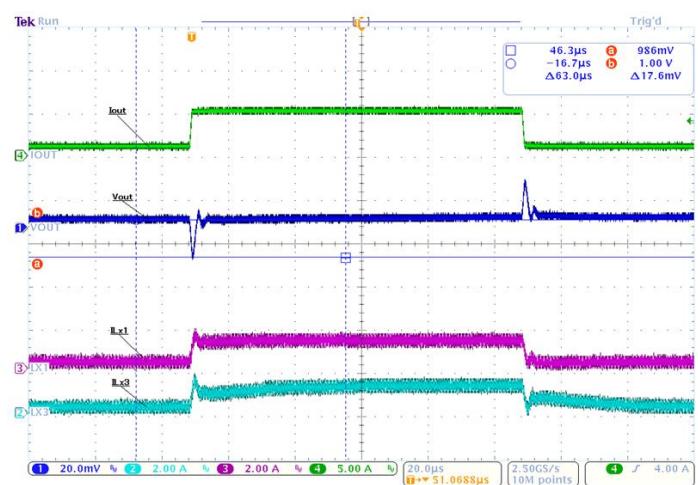
**Figure 28**

**Transient Load , PWM, 4-phases**  
 **$0 \rightarrow 5A$  in  $10A/\mu s$ ,**  
 **$V_{DD}=3.7 V$ ,  $V_{OUT}=1.0 V$**



**Figure 29**

**Transient Load , PWM, 4-phases**  
 **$1 \rightarrow 5A$  in  $10A/\mu s$ ,**  
 **$V_{DD}=3.7 V$ ,  $V_{OUT}=1.0 V$**



**Figure 30**

## Datasheet

## Transient Load , Auto, 4-phases

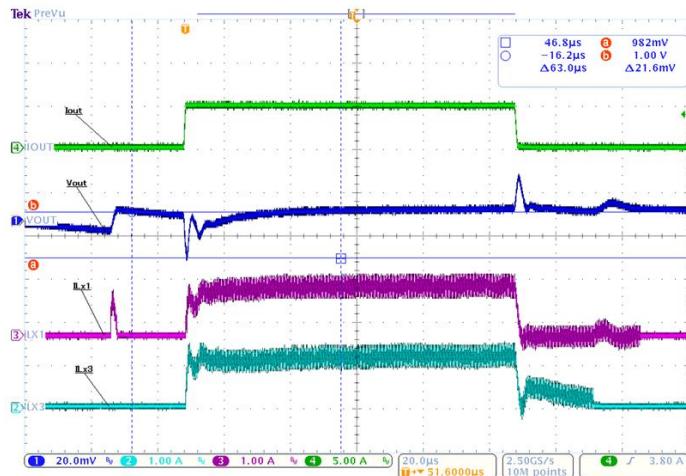
10mA  $\rightarrow$  5A in 10A/ $\mu$ s,V<sub>DD</sub>=3.7 V, V<sub>OUT</sub>=1.0 V

Figure 31

## Datasheet

## 13. Functional description

Flexible configurability and the availability of different control schemes make both DA9211 and DA9212 the ideal single/dual buck companion ICs to expand the existing capabilities of a master PMIC.

Due to the advanced compatibility between both DA9211 and DA9212 and the DA9063, they offer several advantages when they are operated together. These advantages include:

- DA9211 and DA9212 can be enabled and controlled by DA9063 during the power up sequence, thanks to DA9063's dedicated output signals during power-up, and compatible input controls in both DA9211 and DA9212.
- DA9211 and DA9212 can be used in a completely transparent way for the host processor and can share the same Control Interface (same SPI chip select or I2C address), thanks to the compatible registers map. DA9211 and DA9212 has a dedicated register space for configuration and control which doesn't conflict with DA9063.
- DA9211 and DA9212 supports a Power-good configurable port for enhanced communication to the host processor and improved power-up sequencing.
- DA9211 and DA9212 can both share the same interrupt line with DA9063.

In addition, the 2-WIRE / 4-WIRE interfaces allow DA9211 and DA9212 to fit to many standard PMU parts and power applications.

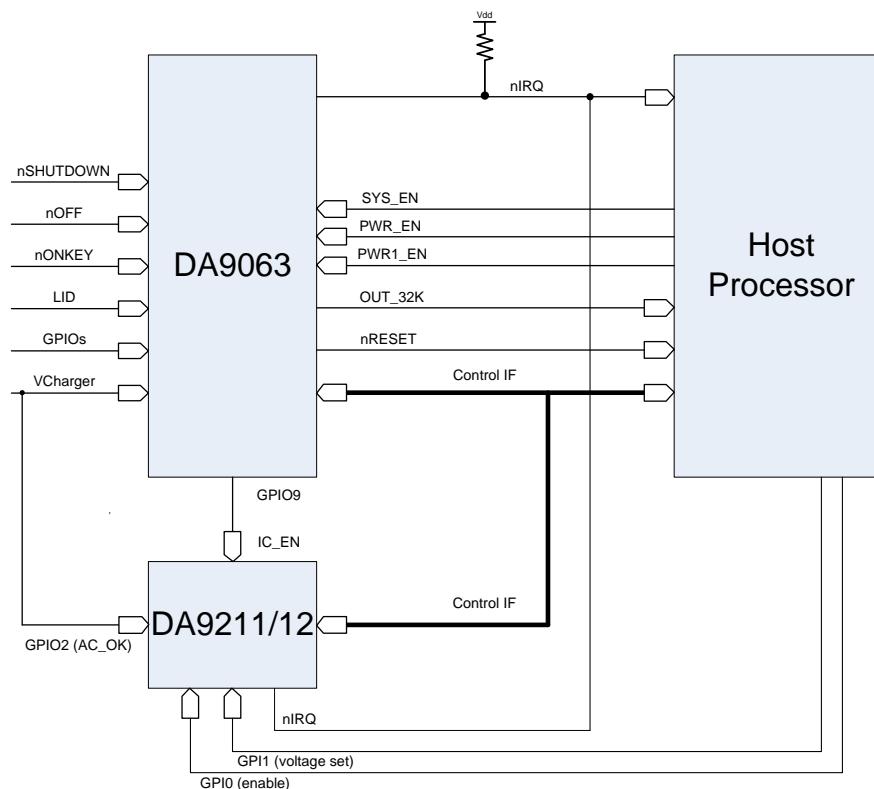
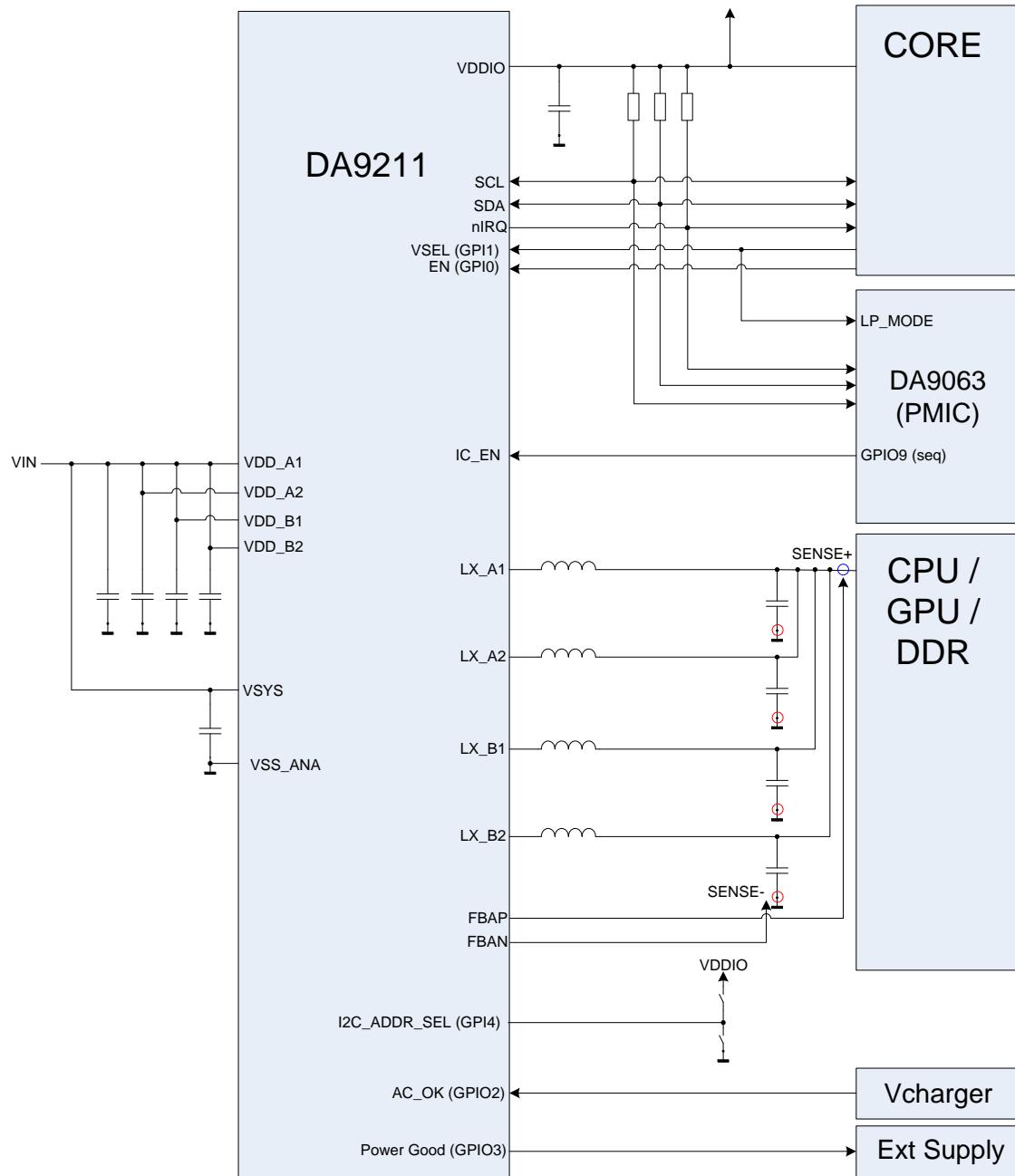


Figure 32: Interface of DA9211/12 with DA9063 and the host processor

**Datasheet**

As shown in [Figure 32](#), a typical application case includes a host processor, a Main PMIC (for example, DA9063) and DA9211 or DA9212 used as companion IC for the high power core supply.

The easiest way of controlling DA9211 and DA9212 is through the Control Interface. The master initiating the communication must always be the host processor that reads and writes to the main PMIC, and to the DA9211 and DA9212 registers. To poll the status of DA9211 or DA9212, the host processor must access the dedicated register area through the Control Interface. DA9211 and DA9212 can be additionally controlled by means of hardware inputs.



**Figure 33: Typical application of DA9211**

## Datasheet

Figure 33 shows a typical use case of DA9211 for the supply of CPU, GPU, or DDR rails. The IC is enabled and disabled by the main PMIC via IC\_EN port as part of its sequencer. Once the IC is enabled, the CORE application processor enables the buck converter with the EN1 signal and manages the output voltage selection with the VSEL signal.

The VSEL signal can be shared between the main PMIC and the DA9211. Three GPI/GPIOs embedded in DA9211 are used in this case:

- GPIO2 signals the insertion of an external charger in the application (through interrupt to the host processor)
- GPIO3 indicates a power-good-condition, either to proceed with the power up sequence or to enable an external supply connected to the port
- GPIO4 is used for the I2C interface address hardware selection

## Datasheet

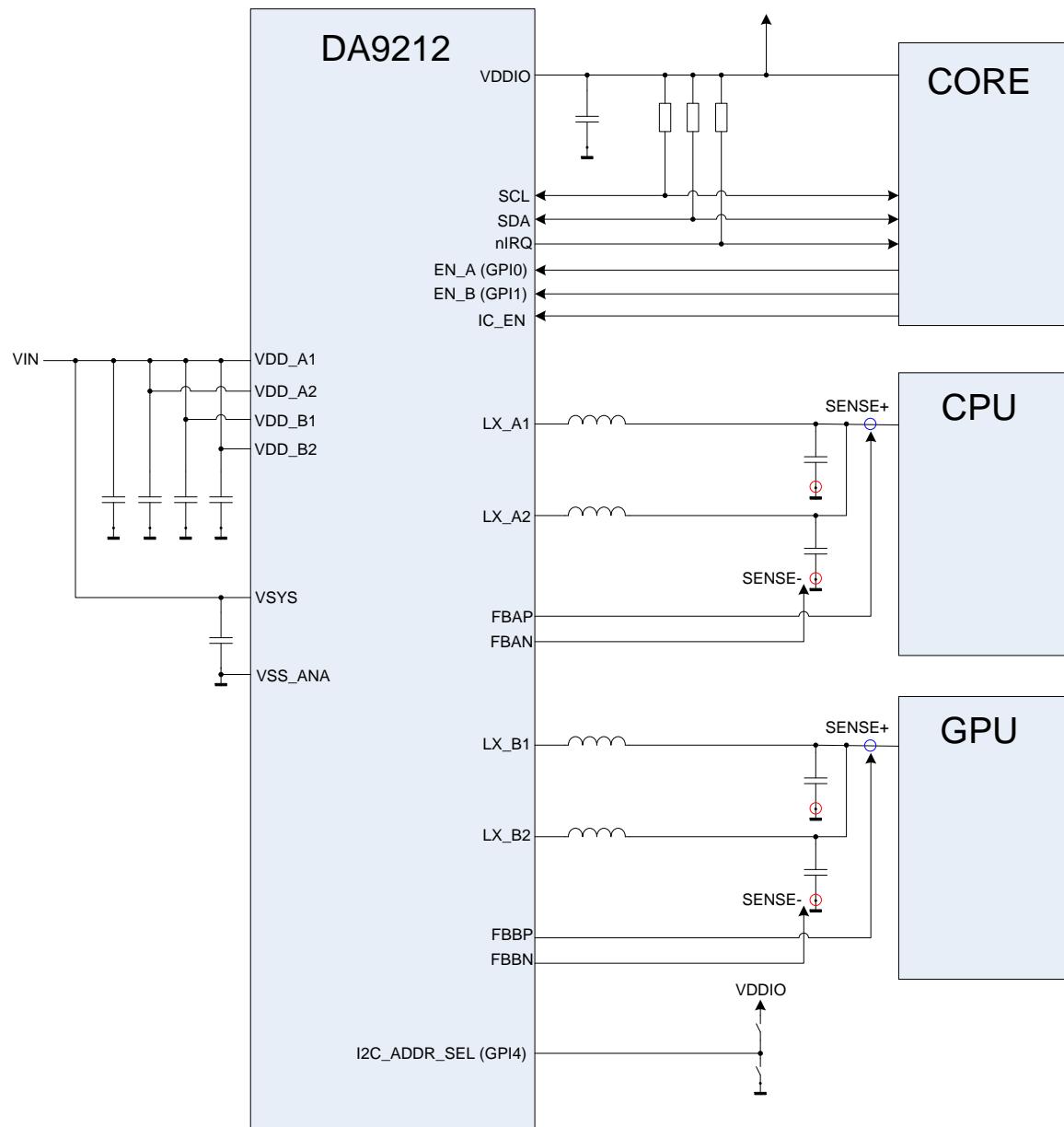


Figure 34: Typical application of DA9212

Figure 34 shows a typical use case of DA9212 for the simultaneous supply of a CPU and a GPU rail. The CORE application processor enables and disables the IC, the CPU and the GPU individually via dedicated ports on DA9212.

## Datasheet

### 13.1 DC-DC Buck Converter

DA9211 is a four-phase 12 A high efficiency synchronous step-down DVC regulator, operating at a high frequency of typically 3 MHz. It supplies an output voltage of typically 1.0 V for a CPU rail, configurable in the range 0.3 – 1.57 V, with high accuracy in steps of 10 mV.

DA9212 contains two buck converters, Buck A and Buck B, each capable of delivering 6 A

To improve the accuracy of the delivered voltage, each buck converter is able to support a differential sensing of the configured voltage directly at the point of load via dedicated positive and negative sense pins.

Both Buck A and Buck B have two voltage registers each. One defines the normal output voltage, while the other offers an alternative retention voltage. In this way different application power modes can easily be supported. The voltage selection can be operated either via GPI or via control interface to guarantee the maximum flexibility according to the specific host processor status in the application.

When a buck is enabled, its output voltage is monitored and a power-good signal indicates that the buck output voltage has reached a level higher than the  $V_{TH(PG)}$  threshold. The power-good is lost when the voltage drops below  $V_{TH(PG)} - V_{HYS(PG)}$ , which is the level at which the signal is de-asserted. The power good signalling should not be used in conjunction with fast start up rates, configured in `BUCKx_UP_CTRL` register fields and can be individually masked during DVC transitions using the `PGA_DVC_MASK` and `PGB_DVC_MASK` bits. For each of the buck converters the status of the power-good indicator can be read back via I2C from the `PWRGOOD_A` and `PWRGOOD_B` status bits. It can be also individually assigned to either GPIO2 or GPIO3 using `BUCKA_PG_SEL` and `BUCKB_PG_SEL`. For correct functionality, the GPIO ports need to be configured as output. An I2C write in `GPIOx_MODE` can overwrite the internal configuration so that a new update will be automatically done only when the internal power-good indicator changes status.

The buck converters are capable of supporting DVC transitions that occur:

- When the active and selected A-voltage or B-voltage is updated to a new target value.
- When the voltage selection is changed from the A-voltage to the B-voltage (or B-voltage to the A-voltage) using `VBUCKA_SEL` and `VBUCKB_SEL`.

The DVC controller operates in Pulse Width Modulation (PWM) mode with synchronous rectification. When the host processor changes the output voltage, the voltage transition of each buck converter can be individually signalled with a READY signal routed to either GPIO2 or GPIO3. The port has to be configured as GPO and selected for the functionality via `READYA_CONF` or `READYB_CONF`. In contrast to the power-good signal, the READY only informs the host processor about the completion of the digital DVC ramp without confirming that the target voltage has actually been reached.

The slew rate of the DVC transition is individually programmed for each buck converter at 10mV per (4, 2, 1 or 0.5  $\mu$ s) via control bit `SLEW_RATE_A` and `SLEW_RATE_B`.

The typical supply current is in the order of 8 mA per phase (quiescent current and charge/discharge current) and drops to <1  $\mu$ A when the buck is turned off.

When the buck is disabled, a pull-down resistor (typically 150  $\Omega$ ) for each phase is activated depending of the value stored in register bits `BUCKA_PD_DIS` and `BUCKB_PD_DIS`. Phases disabled using `PHASE_SEL_A` and `PHASE_SEL_B` will not have any pull-down. The pull-down resistor is always disabled at all phases when DA9211 and DA9212 are OFF.

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### 13.1.1 Switching Frequency

The switching frequency is chosen to be high enough to allow the use of a small 0.47  $\mu$ H inductor (see a complete list of coils in the Application Information section (see section 15). The buck switching frequency can be tuned using register bit **OSC\_TUNE**. The internal 6 MHz oscillator frequency is tuned in steps of 180 kHz. This impacts the buck converter frequency in steps of 90 kHz and helps to mitigate possible disturbances to other HF systems in the application.

### 13.1.2 Operation Modes and Phase Selection

The buck converters can operate in synchronous PWM mode and PFM mode. The operating mode is selected using register bits **BUCKA\_MODE** and **BUCKB\_MODE**.

An automatic phase shedding can be enabled for each buck converter in PWM mode via **PH\_SH\_EN\_A**, **PH\_SH\_EN\_B**, thereby automatically reducing or increasing the number of active phases depending on the output load current. For DA9212 the phase shedding will automatically change between 1-phase and 2-phase operation at a typical current of 1.3 A. For DA9211 the phase shedding will automatically change between 1-phase and 4-phase operation at a typical current of 1.6 A. The **PHASE\_SEL\_A** and **PHASE\_SEL\_B** register fields limit the maximum number of active phases under any conditions.

If the automatic operation mode is selected on **BUCKA\_MODE** or **BUCKB\_MODE**, the buck converters will automatically change between synchronous PWM mode and PFM depending on the load current. This improves the efficiency of the converters across the whole range of output load currents.

### 13.1.3 Output Voltage Selection

The switching converter can be configured using either a 2-WIRE or a 4-WIRE interface. For security reasons, the re-programming of registers that can cause damage when wrongly programmed (for example, the voltage settings) can be disabled by asserting the control **V\_LOCK**. When **V\_LOCK** is asserted, reprogramming the registers 0xD0 to 0x14F from control interfaces is disabled.

For each buck converter two output voltages can be pre-configured inside registers **VBUCKA\_A** and **VBUCKB\_A**, and registers **VBUCKA\_B** and **VBUCKB\_B**. The output voltage can be selected by either toggling register bits **VBUCKA\_SEL** and **VBUCKB\_SEL** or by re-programming the selected voltage control register. Both changes will result into ramped voltage transitions, during which the READY signal is asserted. After being enabled, the buck converter will by default use the register settings in **VBUCKA\_A** and **VBUCKB\_A** unless the output voltage selection is configured via the GPIO port.

Regardless of the values programmed in the **VBUCKx\_A** and **VBUCKx\_B** registers, the registers **VBUCKA\_MAX**, **VBUCKB\_MAX** will individually limit the output voltage that can be set for each of the buck converters .

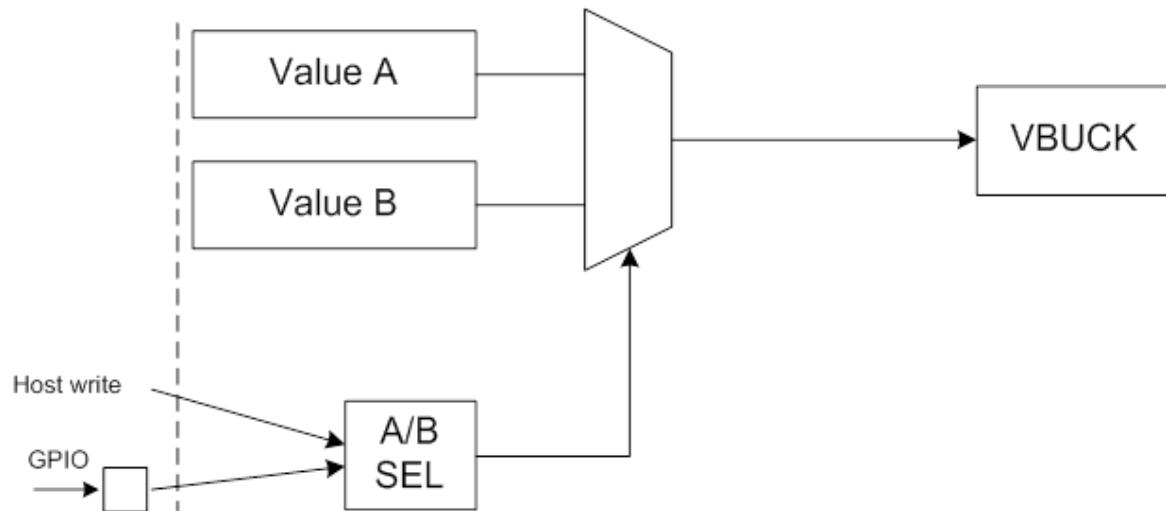
The buck converter provides an optional hardware enable/disable via selectable GPIO, and configured via control register bits **BUCKA\_GPI** and **BUCKB\_GPI**. A change of the output voltage from the state of a GPIO is enabled via control register bits **VBUCKA\_GPI** and **VBUCKB\_GPI**. After detecting a rising or falling edge at the related GPIOs, DA9211 and DA9212 will configure the buck converters according to their status.

In addition to selecting between the A/B voltages, a track mode can be activated for Buck A to set the output voltage. In the DA9211, the track mode is applied to the 4-phase buck converter. This feature can be enabled on GPIO0 via **GPIO0\_PIN**. The output voltage will be configured to follow the value applied at a selected GPIO pin. The voltage applied at GPIO0 must be in the same range as the nominal

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output voltage selectable for the buck rail (see [VBUCKA\\_A](#) and [VBUCKA\\_B](#) registers). In Track Mode, only single ended remote sensing is possible.

In Track Mode, the content of the [VBUCKA\\_SEL](#) bit is ignored, as well as [VBUCKA\\_A](#) and [VBUCKA\\_B](#) bits. They will become active again once the voltage track mode is disabled. The GPIO does not generate any event in this case.



**Figure 35: Concept of control of the buck's output voltage**

### 13.1.4 Soft Start up

To limit in-rush current from VSYS, the buck converters can perform a soft-start after being enabled. The start-up behaviour is a compromise between acceptable inrush current from the battery and turn-on time. In DA9211 and DA9212, different ramp times can be individually configured for each buck converter on register [BUCKA\\_UP\\_CTRL](#) and [BUCKB\\_UP\\_CTRL](#). Rates higher than 20 mV/μs may produce overshoot during the start-up phase, so they should be considered carefully.

A ramped power-down can be selected on register bits [BUCKA\\_DOWN\\_CTRL](#) and [BUCKB\\_DOWN\\_CTRL](#). When no ramp is selected, the output node will be discharged only by the pull-down resistor, if enabled via [BUCKA\\_PD\\_DIS](#) and [BUCKB\\_PD\\_DIS](#).

### 13.1.5 Current Limit

The integrated current limit is meant to protect DA9211 and DA9212's power stages and the external coil from excessive current. The bucks' current limit should be configured to be at least 40% higher than the required maximum continuous output current (see table below).

When reaching the current limit, each buck converter generates an event and an interrupt to the host processor unless the interrupt has been masked using the [OCx\\_MASK](#) controls. These [OCA\\_MASK](#) and [OCB\\_MASK](#) control bits can be used to mask the generation of over-current events during DVC transitions. An extra masking time as defined in [OCx\\_MASK](#) will be automatically added to the DVC interval after the DVC has finished in order to ensure that the possible high current levels needed for DVC do not influence the event generation.

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**Table 12: Selection of the buck current limit from the coil parameters**

| Min ISAT (mA) | Frequency (MHz) | Buck current limit (mA) | Average current (mA) |
|---------------|-----------------|-------------------------|----------------------|
| 5060          | 3               | 4600                    | 3300                 |
| 4180          | 3               | 3800                    | 2700                 |
| 3080          | 3               | 2800                    | 2000                 |
| 1760          | 3               | 1600                    | 1100                 |

## 13.2 Ports Description

This section describes the functionality of each input / output port.

### 13.2.1 VDDIO

VDDIO is an independent IO supply rail input to DA9211 and DA9212 that can be assigned to the power manager interface and to the GPIOs (see control [PM\\_IF\\_V](#) and [GPI\\_V](#)). The rail assignment determines the IO voltage levels and logical thresholds (see also the Digital I/O Characteristics in [Table 8](#)).

An integrated under voltage lockout circuit for the VDDIO prevents internal errors by disabling the I2C communication when the voltage drops below  $V_{ULO\_IO}$ . In that case the buck converters are also disabled and can not be re-enabled (even via input port) until the VDDIO under-voltage condition has been resolved. At the exit of the VDDIO under voltage condition an event [E\\_UVLO\\_IO](#) is generated and the nIRQ line is driven active if the event is not masked.

The VDDIO under-voltage circuit monitors voltages relative to a nominal voltage of 1.8V. If a different rail voltage is being used, the under-voltage circuit can be disabled via [UVLO\\_IO\\_DIS](#).

Note that the maximum speed at 4-WIRE interface is only available if the selected supply rail is greater than 1.6 V.

### 13.2.2 IC\_EN

IC\_EN is a general enable signal for DA9211 and DA9212, turning on and off the internal circuitry (for example, the reference, the digital core, etc). Correct control of this port has a direct impact on the quiescent current of the whole application. A low level of IC\_EN allows the device to reach the minimum quiescent current. The voltage at this pin is continuously sensed by a dedicated analogue circuit.

The host processor will be allowed to start the communication with DA9211 and DA9212 through the Control Interface and, for example to turn on the buck converters, a delay time of  $t_{EN}$  after assertion of the IC\_EN pin. If the bucks are enabled via OTP (see [BUCKA\\_EN](#) and [BUCKB\\_EN](#) controls), they will start up automatically after assertion of IC\_EN.

The IC\_EN signal shall be asserted and deasserted only when the VDD\_IO supply is available and its level is above the undervoltage threshold level  $V_{TH\_UVLO\_IO}$ .

### 13.2.3 nIRQ

The nIRQ port indicates that an interrupt-causing event has occurred and that the event/status information is available in the related registers. The nIRQ is an output signal that can either be

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push-pull or open drain (selected via [IRQ\\_TYPE](#)). If an active high IRQ signal is required, it can be achieved by asserting control [IRQ\\_LEVEL](#) (recommended for push-pull mode).

Examples of this type of information can be critical temperature and voltage, fault conditions, status changes at GPI ports, and so forth. The event registers hold information about the events that have occurred. Events are triggered by a status change at the monitored signals. When an event bit is set, the nIRQ signal is asserted unless this interrupt is masked by a bit in the IRQ mask register. The nIRQ will not be released until all event registers with asserted bits have been read and cleared. New events that occur during reading an event register are held until the event register has been cleared, ensuring that the host processor does not miss them.

### 13.2.4 GPIO Extender

DA9211 and DA9212 includes a GPIO extender that offers up to five 5 V-tolerant general purpose input/output ports. Each port is controlled via registers from the host processor.

The GPIO3 and GPIO4 ports are pin-shared with the 4-WIRE Control Interface. For instance, if [GPIO3\\_PIN](#) = 01, [GPIO4\\_PIN](#) = 01 (Interface selected), the GPIO3 and GPIO4 ports will be exclusively dedicated to output and chip-select signaling for 4-WIRE purposes. If the alternative function is selected, all GPIOs configuration as per registers 0x58 to 0x5A and 0x145 will be ignored.

GPIs are supplied from the internal rail VDDCORE or VDDIO (selected via [GPIO\\_V](#)) and can be configured to be active high or active low (selected via [GPIOx\\_TYPE](#)). The input signals can be debounced or directly change the state of the assigned status register GPIOx to high or low, according to the setting of [GPIOx\\_MODE](#). The debouncing time is configurable via control [DEBOUNCE](#) (10 ms default).

When ever the status has changed to its configured active state (edge sensitive), the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked, see also [Figure 36](#)).

Whenever DA9211 and DA9212 is enabled and enters ON mode (also when enabled changing the setting of [GPIOx\\_PIN](#)) the GPI status bits are initiated towards their configured passive state. This ensures that already active signals are detected, and that they create an event immediately after the GPI comparators are enabled.

The buck enable signal (BUCKx\_EN) can be controlled directly via a GPI, if so configured in the [BUCKA\\_GPI](#) and [BUCKB\\_GPI](#) registers. If it is required that GPI ports do not generate an event when configured for the HW control of the switching regulator, the relative mask bit should be set.

GPIs can alternatively be selected to toggle the [VBUCKA\\_SEL](#) and [VBUCKB\\_SEL](#) from rising and falling edges at this inputs.

All GPI ports have the additional option of activating a 100 kΩ pull-down resistor via [GPIOx\\_PUPD](#), which ensures a well defined level in case the input is not actively driven.

If enabled via [ADDR\\_SEL\\_CONF](#), the I2C address selection can be assigned to a specific GPI. An active voltage level at the selected GPI configures the slave address of DA9211 and DA9212 to [IF\\_BASE\\_ADDR1](#) while a passive voltage level configures the slave address to [IF\\_BASE\\_ADDR2](#). If no GPI is selected then the [IF\\_BASE\\_ADDR1](#) is automatically used.

If defined as an output, GPIOs can be configured to be open-drain or push-pull. If configured as push-pull, the supply rail is VDDIO. By disabling the internal 120 kΩ pull-up resistor in open-drain mode, the GPO can also be supplied from an external rail. The output state will be assigned as configured by the GPIO register bit [GPIOx\\_MODE](#).

A specific power-good port for each of the buck converters can be configured via [BUCKA\\_PG\\_SEL](#) and [BUCKB\\_PG\\_SEL](#). The respective port must be configured as GPO for correct operation. If assigned to the same GPO, it is necessary that the power-good indicators for Buck A and Buck B are

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both active (supply voltages in range) to assert the overall power-good. The signal will be released as soon as one of the single power-good signals is not active (that is, at least one supply is out of range).

The power good signalling should not be used in conjunction with fast start up rates, configured in BUCKx\_UP\_CTRL register fields.

Whenever the GPIO unit is off (POR or OFF Mode) all ports are configured as open drain active high (pass device switched off, high impedance state). When leaving POR the pull-up or pull-down resistors will be configured from register GPIOx\_PUPD.

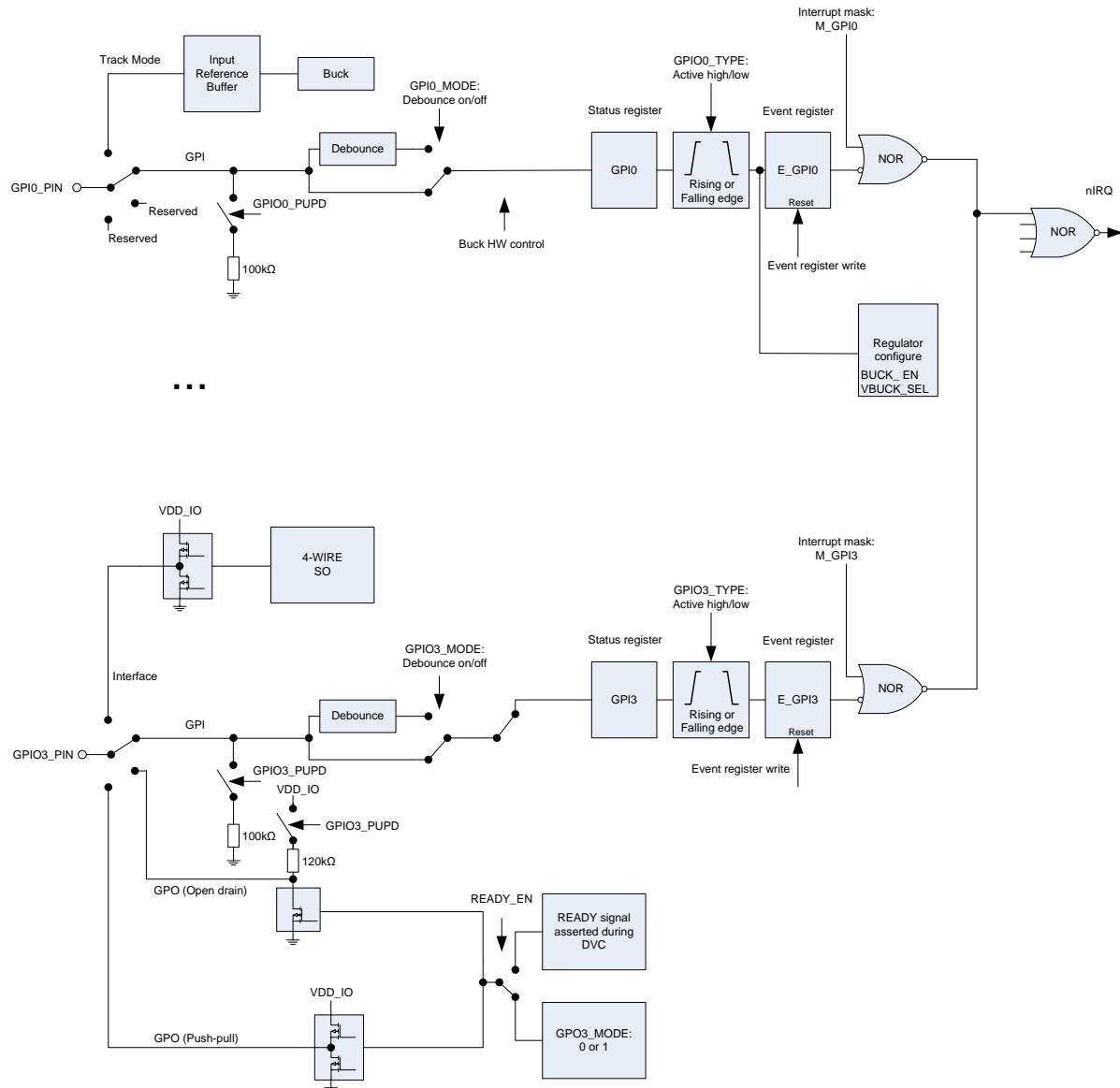


Figure 36: GPIO principle of operation (example paths)

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### 13.3 Operating Modes

#### 13.3.1 ON Mode

DA9211 and DA9212 is in ON Mode when the IC\_EN port is higher than EN\_ON and the supply voltage is higher than  $V_{TH(UVLO)}(VDD)$ . Once enabled, the host processor can start the communication with DA9211 and DA9212 via Control Interface after the  $t_{EN}$  delay needed for internal circuit start up.

If **BUCKA\_EN** or **BUCKB\_EN** is asserted when DA9211 and DA9212 is in ON Mode the power up of the related buck converter is initiated. If the bucks are controlled via GPI, the level of the controlling ports is checked when entering ON mode, so that an active level will immediately have effect on the buck. If **BUCKA\_EN** or **BUCKB\_EN** are not asserted and all controlling GPI ports are inactive, the buck converter will stay off with the output pull-down resistor enabled/disabled according to the setting of **BUCKA\_PD\_DIS** and **BUCKB\_PD\_DIS**.

#### 13.3.2 OFF Mode

DA9211 and DA9212 is in OFF Mode when the IC\_EN port is lower than EN\_OFF. In OFF Mode, the bucks are always disabled and the output pull-down resistors are disabled independently of **BUCKA\_PD\_DIS** and **BUCKB\_PD\_DIS**. All I/O ports of DA9211 and DA9212 are configured as high impedance.

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### 13.4 Control Interfaces

All the features of DA9211 and DA9212 can be controlled by SW through a serial control interfaces. The communication is selectable to be either a 2-WIRE (I2C compliant) or a 4-WIRE connection (SPI compliant) via control **IF\_TYPE**, which will be selected during the initial OTP read. If 4-WIRE is selected, the GPIO3 and GPI4 are automatically configured as interface pins. Data is shifted into or out of DA9211 and DA9212 under the control of the host processor, which also provides the serial clock. In a normal application case the interface is only configured once from OTP values, which are loaded during the initial start-up of DA9211 and DA9212.

DA9211 and DA9212 reacts only on read/write commands where the transmitted register address (using the actual page bits as a MSB address range extensions) is within 0x50 to 0x67, 0xD0 to DF, 0x140 to 0x14F and (read only) 0x200 to 0x27F. Host access to registers outside these ranges will be ignored. This means there will be no acknowledge after receiving the register address in 2-WIRE Mode, and SO stays HI-Z in 4-WIRE Mode. During debug and production modes write access is available to page 4 (0x200 to 0x27F). DA9211 and DA9212 will react only on write commands where the transmitted register address is 0x00, 0x80, 0x100 to 0x106. The host processor must read the content of those registers before writing, thereby changing only the bit fields that are not marked as reserved (the content of the read back comes from the compatible PMIC, for example DA9063).

If the **STAND\_ALONE** bit is asserted (OTP bit), DA9211 and DA9212 will also react to read commands.

#### 13.4.1 4-WIRE Communication

In 4-WIRE Mode the interface uses a chip-select line (nCS/nSS), a clock line (SK), data input (SI) and data output line (SO).

The DA9211 and DA9212 register map is split into four pages that each contain up to 128 registers. The register at address zero on each page is used as a page control register. The default active page after turn-on includes registers 0x50 to 0x6F. Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting bit **REVERT**. Unless the **REVERT** bit was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

All registers outside the DA9211 and DA9212 range are write only, that is, the DA9211 and DA9212 will not answer to a read command and the data bus is tri-state (they are implicitly directed to DA9063). In particular the information contained in registers 0x105 and 0x106 is used by DA9211 and DA9212 to configure the control interface. They must be the same as the main PMIC (DA9063), so that a write to those registers configures both the main PMIC and DA9211 and DA9212 at the same time. The default OTP settings also need to be identical for a correct operation of the system.

The 4-WIRE interface features a half-duplex operation, that is, data can be transmitted and received within a single 16-bit frame at enhanced clock speed (up to 14 MHz). It operates at the clock frequencies provided by the host.

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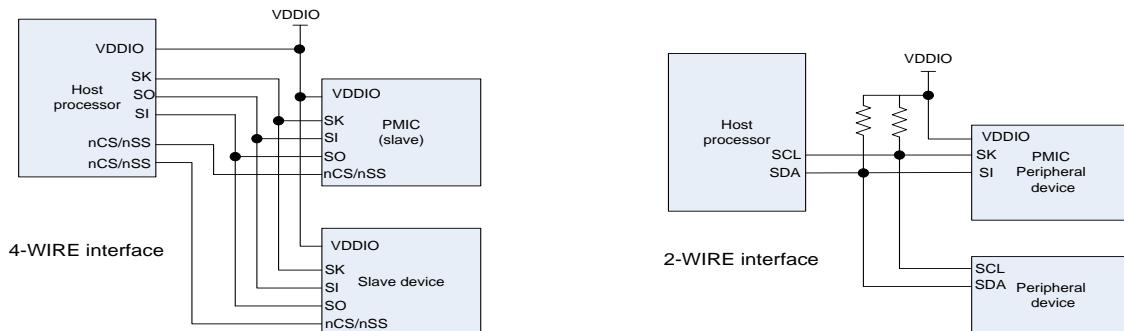


Figure 37: Schematic of 4-WIRE and 2-WIRE Power Manager Bus

A transmission begins when initiated by the host. Reading and writing is accomplished by the use of an 8-bit command, which is sent by the host prior to the exchanged 8-bit data. The byte from the host begins shifting in on the SI pin under the control of the serial clock SK provided from the host. The first seven bits specify the register address (0x01 to 0x07) that will be written or read by the host. The register address is automatically decoded after receiving the seventh address bit. The command word ends with an R/W bit, which together with the control bit **R/W\_POL** specifies the direction of the following data exchange. During register writing the host continues sending out data during the following eight SK clocks. For reading, the host stops transmitting and the 8-bit register is clocked out of DA9211 and DA9212 during the consecutive eight SK clocks of the frame. Address and data are transmitted with MSB first. The polarity (active state) of nCS is defined by control bit **nCS\_POL**. nCS resets the interface when inactive and it has to be released between successive cycles.

The SO output from DA9211 and DA9212 is normally in high-impedance state and active only during the second half of read cycles. A pull-up or pull-down resistor may be needed at the SO line if a floating logic signal can cause unintended current consumption inside other circuits.

Table 13: 4-WIRE Clock Configurations

| Configurations      |                  |                                   |                                     |
|---------------------|------------------|-----------------------------------|-------------------------------------|
| CPHA clock polarity | CPOL clock phase | Output data is updated at SK edge | Input data is registered at SK edge |
| 0 (idle low)        | 0                | Falling                           | Rising                              |
| 0 (idle low)        | 1                | Rising                            | Falling                             |
| 1 (idle high)       | 0                | Rising                            | Falling                             |
| 1 (idle high)       | 1                | Falling                           | Rising                              |

DA9211 and DA9212's 4-WIRE interface offers two further configuration bits. Clock polarity (**CPOL**) and clock phase (**CPHA**) define when the interface will latch the serial data bits. **CPOL** determines whether SK idles high (**CPOL** = 1) or low (**CPOL** = 0). **CPHA** determines on which SK edge data is shifted in and out. With **CPOL** = 0 and **CPHA** = 0, DA9211 and DA9212 latch data on the SK rising edge. If the **CPHA** is set to 1 the data is latched on the SK falling edge. **CPOL** and **CPHA** states allow four different combinations of clock polarity and phase. Each setting is incompatible with the other three. The host and DA9211 and DA9212 must be set to the same **CPOL** and **CPHA** states to communicate with each other.

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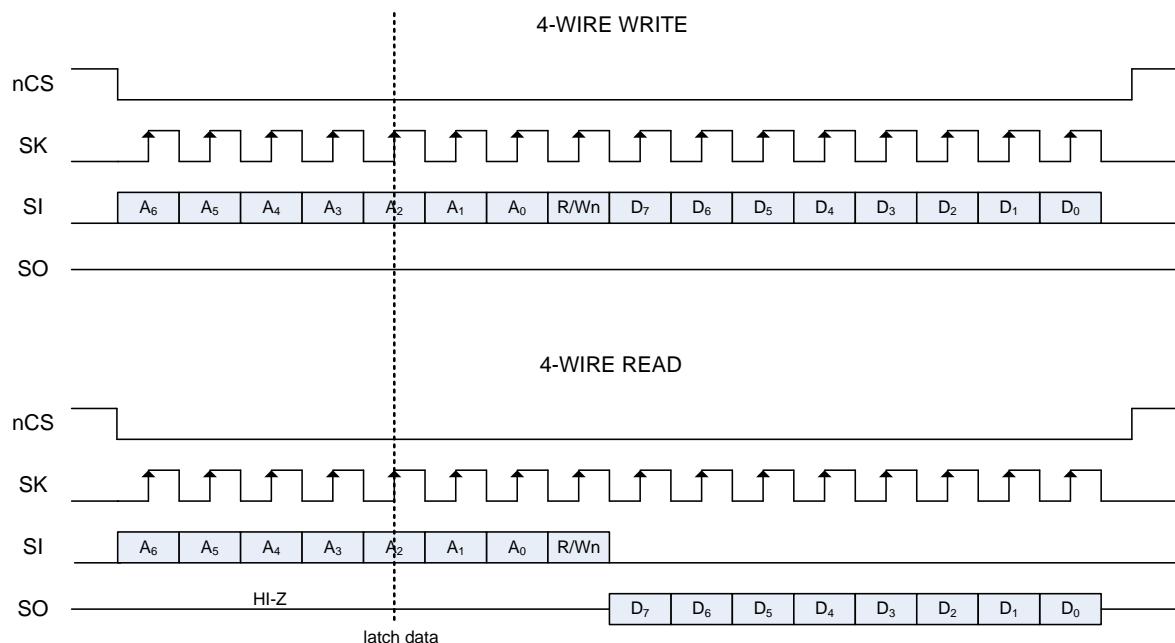


Figure 38: 4-WIRE Host Write and Read Timing (nCS\_POL = '0', CPOL = '0', CPHA = '0')

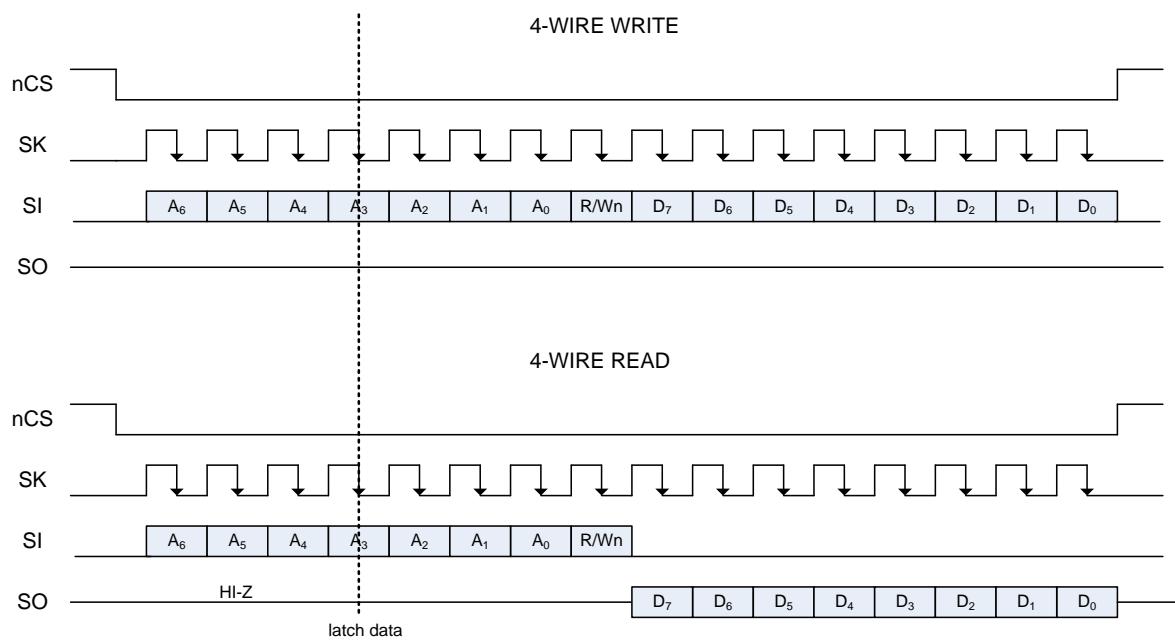


Figure 39: 4-WIRE Host Write and Read Timing (nCS\_POL= '0', CPOL = '0', CPHA = '1')

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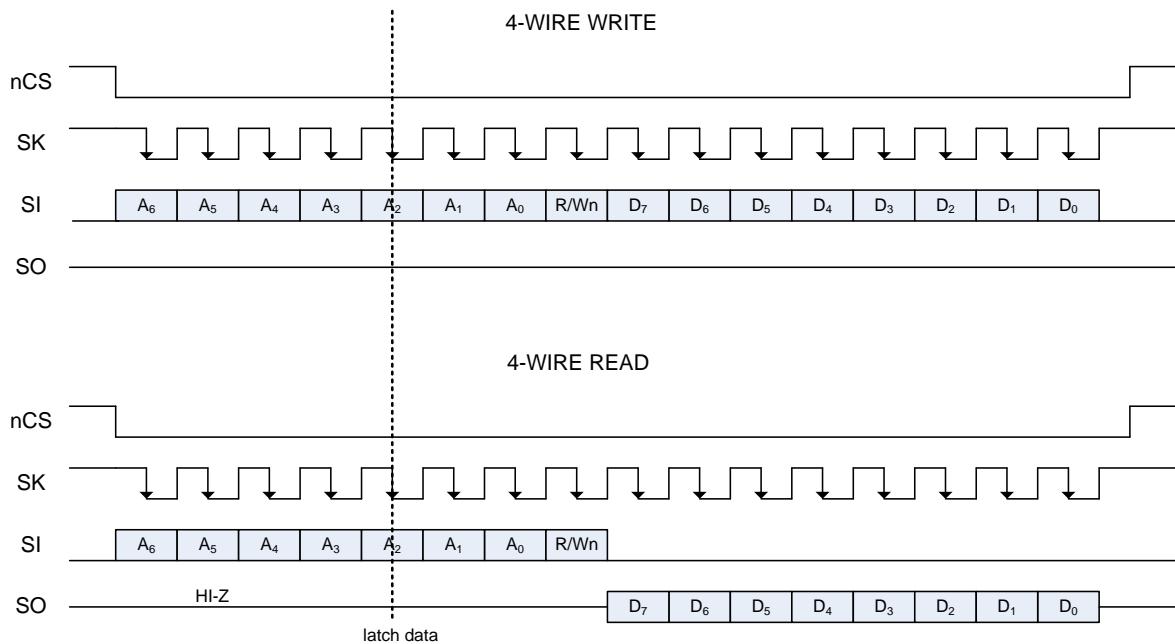


Figure 40: 4-WIRE Host Write and Read Timing (nCS\_POL = '0', CPOL = '1', CPHA = '0')

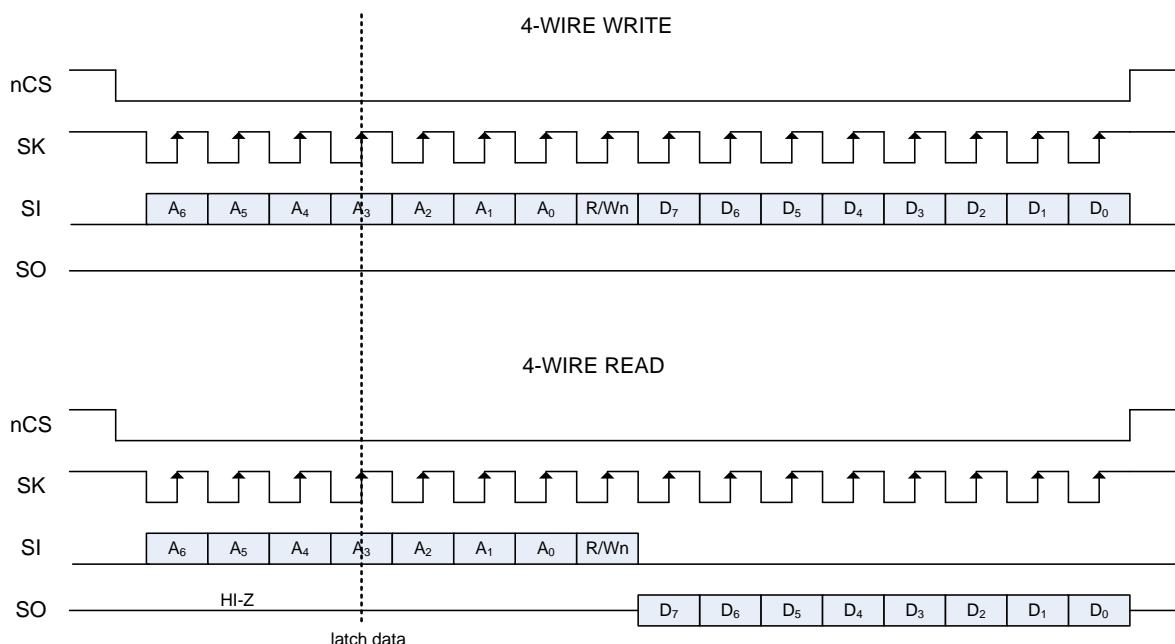


Figure 41: 4-WIRE Host Write and Read Ttiming (nCS\_POL = '0', CPOL = '1', CPHA = '1')

**Datasheet****Table 14: 4-WIRE Interface Summary**

| Parameters     |                           |                                             |
|----------------|---------------------------|---------------------------------------------|
| Signal Lines   | nCS                       | Chip select                                 |
|                | SI Serial input data      | Master out Slave in                         |
|                | SO Serial output data     | Master in Slave out                         |
|                | SK                        | Transmission clock                          |
| Interface      | Push-pull with tristate   |                                             |
| Supply voltage | Selected from VDDIO       | 1.6 V to 3.3 V                              |
| Data rate      | Effective read/write data | Up to 7 Mbps                                |
| Transmission   | Half-duplex               | MSB first                                   |
|                | 16 bit cycles             | 7-bit address, 1 bit read/write, 8-bit data |
| Configuration  | CPOL                      | Clock polarity                              |
|                | CPHA                      | Clock phase                                 |
|                | nCS_POL                   | nCS is active low/high                      |

Note that reading the same register at high clock rates directly after writing it does not guarantee a correct value. It is recommended to keep a delay of one frame until re-accessing a register that has just been written (for example, by writing/reading another register address in between).

### 13.4.2 2-WIRE Communication

The [IF\\_TYPE](#) bit in the INTERFACE2 register can be used to configure the DA9211 and DA9212 control interface as a 2-WIRE serial data interface. In this case the GPIO3 and GPI4 are free for regular input/output functions. DA9211 and DA9212 has a configurable device write address (default: 0xD0) and a configurable device read address (default: 0xD1). See control [IF\\_BASE\\_ADDR1](#) for details of configurable addresses. The [ADDR\\_SEL\\_CONF](#) bit is used to configure the device address as [IF\\_BASE\\_ADDR1](#) or [IF\\_BASE\\_ADDR2](#) depending on the voltage level applied at a configurable GPI port (see [GPIO Extender](#)).

The SK port functions as the 2-WIRE clock and the SI port carries all the power manager bi-directional 2-WIRE data. The 2-WIRE interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (in the 2 kΩ to 20 kΩ range). The attached devices only drive the bus lines LOW by connecting them to ground. As a result two devices cannot conflict if they drive the bus simultaneously. In standard/fast mode the highest frequency of the bus is 400 kHz. The exact frequency can be determined by the application and does not have any relation to the DA9211 and DA9212 internal clock signals. DA9211 and DA9212 will follow the host clock speed within the described limitations, and does not initiate any clock arbitration or slow down. An automatic interface reset can be triggered using control [2WIRE\\_TO](#) if the clock signal stops to toggle for more than 35 ms.

The interface supports operation compatible to Standard, Fast, Fast-Plus and High Speed mode of the I2C-bus specification Rev 4. Operation in high speed mode at 3.4 MHz requires mode changing in order to set spike suppression and slope control characteristics to be compatible with the I2C-bus specification. The high speed mode can be enabled on a transfer by transfer basis by sending the master code (0000 1XXX) at the begin of the transfer. DA9211 and DA9212 do not make use of clock stretching, and deliver read data without additional delay up to 3.4 MHz.

Alternatively, [PM\\_IF\\_HSM](#) configures the interface to use high speed mode continuously. In this case, the master code is not required at the beginning of every transfer. This reduces the communication overhead on the bus but limits the slaves attachable to the bus to compatible devices.

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The communication on the 2-WIRE bus always takes place between two devices, one acting as the master and the other as the slave. The DA9211 and DA9212 will only operate as a SLAVE.

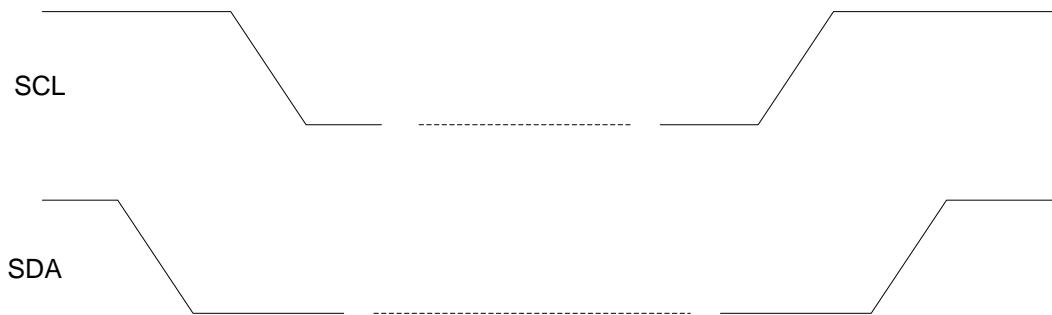
In contrast to the 4-WIRE mode, the 2-WIRE interface has direct access to two pages of the register map (up to 256 addresses). The register at address zero on each page is used as a page control register (with the 2-WIRE bus ignoring the LSB of control [REG\\_PAGE](#)). Writing to the page control register changes the active page for all subsequent read/write operations unless an automatic return to page 0 was selected by asserting control [REVERT](#). Unless [REVERT](#) was asserted after modifying the active page, it is recommended to read back the page control register to ensure that future data exchange is accessing the intended registers.

In 2-WIRE operation DA9211 and DA9212 offer an alternative way to access register page 2 and page 3. It removes the need for preceding page selection writes by incrementing the device write/read address by one (default 0xD2/0xD3) for any direct access of page 2 and page 3 (page 0 and 1 access requires the basic write/read device address with the MSB of [REG\\_PAGE](#) to be '0').

### 13.4.3 Details of the 2-WIRE control bus protocol

All data is transmitted across the 2-WIRE bus in groups of eight bits. To send a bit the SDA line is driven towards the intended state while the SCL is LOW (a low on SDA indicates a zero bit). Once the SDA has settled, the SCL line is brought HIGH and then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register.

A two-byte serial protocol is used containing one byte for address and one byte data. Data and address transfer are transmitted MSB first for both read and write operations. All transmissions begin with the START condition from the master while the bus is in IDLE state (the bus is free). It is initiated by a high to low transition on the SDA line while the SCL is in the high state (a STOP condition is indicated by a low to high transition on the SDA line while the SCL is in the high state).



**Figure 42: Timing of 2-WIRE START and STOP Condition**

The 2-WIRE bus is monitored by DA9211 and DA9212 for a valid SLAVE address whenever the interface is enabled. It responds immediately when it receives its own slave address. The acknowledge is done by pulling the SDA line low during the following clock cycle (white blocks marked with 'A' in [Figure 43](#) to [Figure 47](#)).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by eight bits of data terminated by a STOP condition. DA9211 and DA9212 respond to all bytes with Acknowledge. This is illustrated in [Figure 43](#).

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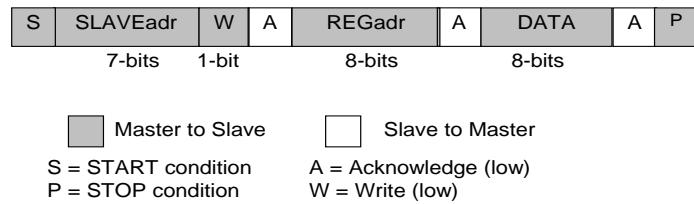


Figure 43: 2-WIRE Byte Write (SDA Line)

When the host reads data from a register it first has to write to DA9211 and DA9212 with the target register address and then read from DA9211 and DA9212 with a Repeated START or alternatively a second START condition. After receiving the data, the host sends No Acknowledge and terminates the transmission with a STOP condition. This is illustrated in Figure 44.

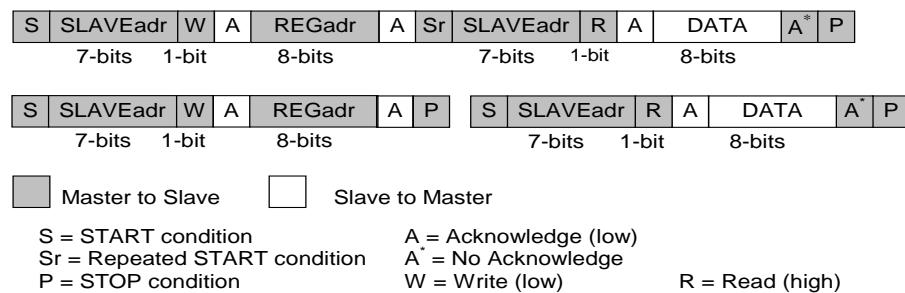


Figure 44: Examples of 2-WIRE Byte Read (SDA Line)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not acknowledge after receipt of the data word. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address and sends the data to the master. This enables an unlimited read of data bytes until the master sends a Not acknowledge directly after the receipt of data, followed by a subsequent STOP condition. If a non-existent 2-WIRE address is read out, the DA9211 and DA9212 will return code zero. This is illustrated in Figure 45.

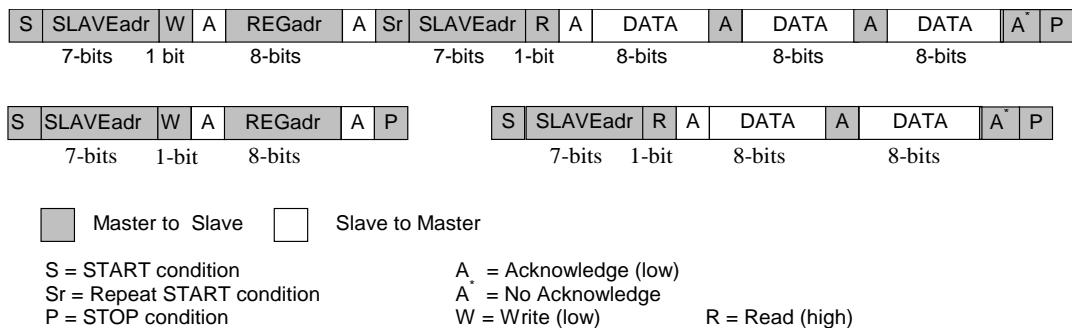


Figure 45: Examples of 2-WIRE Page Read (SDA Line)

Note that the slave address after the Repeated START condition must be the same as the previous slave address.

Consecutive (page) write mode is supported if the Master sends several data bytes following a slave register address. The 2-WIRE control block then increments the address pointer to the next 2-WIRE address, stores the received data and sends an Acknowledge until the master sends the STOP condition. This is illustrated in Figure 46.

**Datasheet**

Master to Slave  Slave to Master

S = START condition  
Sr = Repeat START condition  
P = STOP condition

A<sub>1</sub> = Acknowledge (low)  
A<sub>2</sub> = No Acknowledge  
W = Write (low) R = Read (high)

**Figure 46: 2-WIRE Page Write (SDA Line)**

Via control [WRITE\\_MODE](#) an alternate write mode can be configured. Register addresses and data are sent in alternation like in [Figure 47](#) to support host repeated write operations that access several non consecutive registers. Data will be stored at the previously received register address.

An update of [WRITE\\_MODE](#) can not be done without interruption within a transmission frame. Thus, if not previously selected or not set as OTP default, the activation of Repeated Write must be done with a regular write on [WRITE\\_MODE](#) followed by a stop condition. The next frame after a start condition can be written in Repeated Write.



Master to Slave  Slave to Master

S = START condition  
Sr = Repeat START condition  
P = STOP condition

A<sub>1</sub> = Acknowledge (low)  
A<sub>2</sub> = No Acknowledge  
W = Write (low) R = Read (high)

**Figure 47: 2-WIRE Repeated Write (SDA Line)**

If a new START or STOP condition occurs within a message, the bus will return to IDLE-mode.

## Datasheet

### 13.5 Internal Temperature Supervision

To protect DA9211 and DA9212 from damage due to excessive power dissipation, the internal temperature is continuously monitored. There are three temperature thresholds,

**Table 15: Over-temperature thresholds**

| Temperature threshold | Typical temperature setting | Interrupt event | Status bit | Masking bit |
|-----------------------|-----------------------------|-----------------|------------|-------------|
| TEMP_WARN             | 125 °C                      | E_TEMP_WARN     | TEMP_WARN  | M_TEMP_WARN |
| TEMP_CRIT             | 140 °C                      | E_TEMP_CRIT     | TEMP_CRIT  | M_TEMP_CRIT |
| TEMP_POR              | 150 °C                      |                 |            |             |

When the junction temperature reaches the TEMP\_WARN threshold, DA9211 and DA9212 will assert the bit TEMP\_WARN and will generate the event E\_TEMP\_WARN. If not masked using bit M\_TEMP\_WARN, the output port nIRQ will be asserted. The status bit TEMP\_WARN will remain asserted as long as the junction temperature remains higher than TEMP\_WARN.

When the junction temperature increases further to TEMP\_CRIT, DA9211 and DA9212 will immediately disable the buck converter, assert the bit TEMP\_CRIT, and will generate the event E\_TEMP\_CRIT. If not masked via bit M\_TEMP\_CRIT, the output port nIRQ will be asserted. The status bit TEMP\_CRIT will remain asserted as long as the junction temperature remains higher than TEMP\_CRIT. The buck converter will be kept disabled as long as the junction temperature is above TEMP\_CRIT. It will not be automatically re-enabled even after the temperature drops below the valid threshold (even if the controlling GPIO is asserted). A direct write into [BUCKA\\_EN](#) or [BUCKB\\_EN](#), or a toggling of the controlling GPIO, is needed to enable the buck converter.

Whenever the junction temperature exceeds TEMP\_POR, a power on reset to the digital core is immediately asserted, which will stop all functionalities of DA9211 and DA9212. This is needed to prevent possible permanent damage in the case of a rapid temperature increase.

**Datasheet****14. Register definitions****14.1 Register map****Table 16: Register map**All bits loaded from OTP are marked in **bold**

| Addr            | Function   | 7               | 6             | 5            | 4             | 3           | 2           | 1             | 0           |
|-----------------|------------|-----------------|---------------|--------------|---------------|-------------|-------------|---------------|-------------|
| Register Page 0 |            |                 |               |              |               |             |             |               |             |
| 0x00            | PAGE_CON   | REVERT          | WRITE_MODE    | Reserved     | Reserved      | GP14        | GP8         | GP12          | GP11        |
| REG_PAGE        |            |                 |               |              |               |             |             |               |             |
| 0x50            | STATUS_A   | Reserved        | Reserved      | Reserved     | GP14          | GP8         | GP12        | GP11          | GP10        |
| 0x51            | STATUS_B   | Reserved        | Reserved      | OV_CURR_B    | OV_CURR_A     | TEMP_CRIT   | TEMP_WARN   | PWRGOOD_B     | PWRGOOD_A   |
| 0x52            | EVENT_A    | Reserved        | E_UVLO_IO     | Reserved     | E_GPI4        | E_GPI8      | E_GPI2      | E_GPI1        | E_GPI0      |
| 0x53            | EVENT_B    | Reserved        | Reserved      | E_OV_CURR_B  | E_OV_CURR_A   | E_TEMP_CRIT | E_TEMP_WARN | E_PWRGOOD_B   | E_PWRGOOD_A |
| 0x54            | MASK_A     | Reserved        | M_UVLO_IO     | Reserved     | M_GPI4        | M_GPI3      | M_GPI2      | M_GPI1        | M_GPI0      |
| 0x55            | MASK_B     | Reserved        | Reserved      | M_OV_CURR_B  | M_OV_CURR_A   | M_TEMP_CRIT | M_TEMP_WARN | M_PWRGOOD_B   | M_PWRGOOD_A |
| 0x56            | CONTROL_A  | V_LOCK          | SLEW_RATE_B   | SLEW_RATE_A  | DEBOUNCING    |             |             |               |             |
| 0x57            | Reserved   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x58            | GPIO1-1    | GPIO1_MODE      | GPIO1_TYPE    | GPIO1_PIN    | GPIO1_MODE    | GPIO1_TYPE  | GPIO1_PIN   | GPIO2_MODE    | GPIO2_PIN   |
| 0x59            | GPIO2-3    | GPIO3_MODE      | GPIO3_TYPE    | GPIO3_PIN    | GPIO2_MODE    | GPIO2_TYPE  | GPIO2_PIN   | GPIO4_MODE    | GPIO4_PIN   |
| 0x5A            | GPIO4      | Reserved        | Reserved      | Reserved     | GPIO4_MODE    | GPIO4_TYPE  | GPIO4_PIN   | Reserved      | Reserved    |
| 0x5B            | Reserved   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x5C            | Reserved   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x5D            | BUCKA_CONT | Reserved        | VBUCKA_GPI    | VBUCKA_SEL   | BUCKA_PD_DIS  | BUCKA_GPI   | BUCKA_EN    | BUCKB_GPI     | BUCKB_EN    |
| 0x5E            | BUCKB_CONT | Reserved        | VBUCKB_GPI    | VBUCKB_SEL   | BUCKB_PD_DIS  | BUCKB_GPI   | BUCKB_EN    | BUCKA_GPI     | BUCKA_EN    |
| Register Page 1 |            |                 |               |              |               |             |             |               |             |
| 0x00            | PAGE_CON   | REVERT          | WRITE_MODE    | Reserved     | Reserved      | Reserved    | Reserved    | REG_PAGE      |             |
| 0x00            | BUCK_ILIM  | BUCKA_ILIM      |               |              | BUCKA_ILIM    |             |             | BUCKA_MODE    |             |
| 0x01            | BUCKA_CONF | BUCKA_DOWN_CTRL |               |              | BUCKA_UP_CTRL |             |             | BUCKB_MODE    |             |
| 0x02            | BUCKB_CONF | BUCKB_DOWN_CTRL |               |              | BUCKB_UP_CTRL |             |             | PHASE_SEL_A   |             |
| 0x03            | BUCK_CONF  | Reserved        | Reserved      | Reserved     | PH_SH_EN_B    | PH_SH_EN_A  | PHASE_SEL_B | PHASE_SEL_A   |             |
| 0x04            | Reserved   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x05            | VBUCKA_MAX | Reserved        | VBUCKA_MAX    |              |               | VBUCKA_MAX  |             |               |             |
| 0x06            | VBUCKB_MAX | Reserved        | VBUCKB_MAX    |              |               | VBUCKB_MAX  |             |               |             |
| 0x07            | VBUCKA_A   | Reserved        | VBUCKA_A      |              |               | VBUCKA_A    |             |               |             |
| 0x08            | VBUCKB_B   | Reserved        | VBUCKB_B      |              |               | VBUCKB_B    |             |               |             |
| 0x09            | VBUCKB_A   | Reserved        | VBUCKB_A      |              |               | VBUCKB_B    |             |               |             |
| 0x0A            | VBUCKB_B   | Reserved        | VBUCKB_B      |              |               | VBUCKB_B    |             |               |             |
| Register Page 2 |            |                 |               |              |               |             |             |               |             |
| 0x00            | PAGE_CON   | REVERT          | WRITE_MODE    | Reserved     | Reserved      | PC_DONE     | OTP_APPS_RD | Reserved      | OTP_TM      |
| 0x01            | OTP_CONT   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x02            | Reserved   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x03            | Reserved   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x04            | Reserved   | Reserved        | Reserved      | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x05            | INTERFACE  | IF_BASE_ADDR1   |               |              | R/W_POL       |             |             | CPHA          | CPOL        |
| 0x06            | INTERFACE2 | IF_TYPE         | PM_IF_HSM     | PM_IF_FMP    | PM_IF_V       | Reserved    | Reserved    | Reserved      | nS_POL      |
| 0x00            | OTP_CONT2  | OTP_CONF_LOCK   | OTP_APPS_LOCK | Reserved     | Reserved      | Reserved    | Reserved    | Reserved      | Reserved    |
| 0x11            | OTP_ADDR   | OTP_ADDR        |               |              | OTP_DATA      |             |             |               |             |
| 0x12            | OTP_DATA   | OTP_DATA        |               |              | OTP_DATA      |             |             |               |             |
| 0x13            | CONFIG_A   | Reserved        | Reserved      | Reserved     | 2WIRE_TO      | GPIO_V      | Reserved    | IRQ_TYPE      | IRQ_LEVEL   |
| 0x14            | CONFIG_B   | UVLO_IO_DIS     | PGB_DVC_MASK  | PGA_DVC_MASK | OCB_MASK      | Reserved    | OCA_MASK    | Reserved      | Reserved    |
| 0x15            | CONFIG_C   | Reserved        | Reserved      | Reserved     | GP14_PUPD     | GPIO3_PUPD  | GPIO2_PUPD  | GPIO1_PUPD    | GPIO0_PUPD  |
| 0x16            | CONFIG_D   | BUCKB_PG_SEL    | BUCKA_PG_SEL  |              |               | READYB_CONF | READYA_CONF |               |             |
| 0x17            | CONFIG_E   | STAND_ALONE     | SLAVE_SEL     | Reserved     | Reserved      | Reserved    | OSC_TUNE    |               |             |
| 0x18            | CONFIG_F   | IF_BASE_ADDR2   |               |              | Reserved      |             |             | ADDR_SEL_CONF |             |

**Datasheet****14.2 Register Definitions****14.2.1 Register Page Control**

| Register         | Bit | Type | Label      | Def | Description                                                                                                                                                |
|------------------|-----|------|------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x00<br>PAGE_CON | 7   | R/W  | REVERT     | 0   | Resets REG_PAGE to 000 after read/write access has finished                                                                                                |
|                  | 6   | R/W  | WRITE_MODE | 0   | 2-WIRE multiple write mode ( <a href="#">Note 1</a> )<br>0: Page Write Mode<br>1: Repeated Write Mode                                                      |
|                  | 5:3 | R/W  | (reserved) | 000 |                                                                                                                                                            |
|                  | 3:0 | R/W  | REG_PAGE   | 000 | 000: Selects Register 0x01 to 0x3F<br>001: Selects Register 0x81 to 0xCF<br>010: Selects Register 0x101 to 0x1CF<br>>010: Reserved for production and test |

**Note 1** Not used for 4-WIRE-IF

**14.2.2 Register Page 0****14.2.2.1 System Control and Event**

The STATUS registers report the current value of the various signals at the time that it is read out.

| Register         | Bit | Type | Label      | Def | Description |
|------------------|-----|------|------------|-----|-------------|
| 0x50<br>STATUS_A | 7:5 | R    | (reserved) | 000 |             |
|                  | 4   | R    | GPI4       | 0   | GPI4 level  |
|                  | 3   | R    | GPI3       | 0   | GPI3 level  |
|                  | 2   | R    | GPI2       | 0   | GPI2 level  |
|                  | 1   | R    | GPI1       | 0   | GPI1 level  |
|                  | 0   | R    | GPI0       | 0   | GPI0 level  |

| Register         | Bit | Type | Label      | Def | Description                                                   |
|------------------|-----|------|------------|-----|---------------------------------------------------------------|
| 0x51<br>STATUS_B | 7:6 | R    | (reserved) | 00  |                                                               |
|                  | 5   | R    | OV_CURR_B  | 0   | Asserted as long as the current limit for Buck B is hit       |
|                  | 4   | R    | OV_CURR_A  | 0   | Asserted as long as the current limit for Buck A is hit       |
|                  | 3   | R    | TEMP_CRIT  | 0   | Asserted as long as the thermal shutdown threshold is reached |
|                  | 2   | R    | TEMP_WARN  | 0   | Asserted as long as the thermal warning threshold is reached  |

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| Register | Bit | Type | Label     | Def | Description                                               |
|----------|-----|------|-----------|-----|-----------------------------------------------------------|
|          | 1   | R    | PWRGOOD_B | 0   | Asserted as long as the Buck B output voltage is in range |
|          | 0   | R    | PWRGOOD_A | 0   | Asserted as long as the Buck A output voltage is in range |

The EVENT registers hold information about events that have occurred in DA9211 and DA9212. Events are triggered by a change in the status register which contains the status of monitored signals. When an EVENT bit is set in the event register, the IRQ signal is asserted unless the event is masked by a bit in the mask register. **The IRQ triggering event register will be cleared from the host by writing back its read value.** New events occurring during clearing will be delayed before they are passed to the event register, ensuring that the host controller does not miss them.

| Register        | Bit | Type | Label      | Def | Description                                   |
|-----------------|-----|------|------------|-----|-----------------------------------------------|
| 0x52<br>EVENT_A | 7   | R    | (reserved) | 0   |                                               |
|                 | 6   | R    | E_UVLO_IO  | 0   | UVLO_IO caused the event                      |
|                 | 5   | R    | (reserved) | 0   |                                               |
|                 | 4   | R    | E_GPI4     | 0   | GPI4 event according to active state setting  |
|                 | 3   | R    | E_GPI3     | 0   | GPI3 event according to active state setting  |
|                 | 2   | R    | E_GPI2     | 0   | GPI2 event according to active state setting  |
|                 | 1   | R    | E_GPI1     | 0   | GPI1 event according to active state setting  |
|                 | 0   | R    | E_GPIO0    | 0   | GPIO0 event according to active state setting |

| Register        | Bit | Type | Label       | Def | Description                         |
|-----------------|-----|------|-------------|-----|-------------------------------------|
| 0x53<br>EVENT_B | 7:6 | R    | (reserved)  | 00  |                                     |
|                 | 5   | R    | E_OV_CURR_B | 0   | OV_CURR Buck B caused event         |
|                 | 4   | R    | E_OV_CURR_A | 0   | OV_CURR Buck A caused event         |
|                 | 3   | R    | E_TEMP_CRIT | 0   | TEMP_CRIT caused event              |
|                 | 2   | R    | E_TEMP_WARN | 0   | TEMP_WARN caused event              |
|                 | 1   | R    | E_PWRGOOD_B | 0   | PWRGOOD loss at Buck B caused event |
|                 | 0   | R    | E_PWRGOOD_A | 0   | PWRGOOD loss at Buck A caused event |

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| Register       | Bit | Type | Label            | Def | Description                  |
|----------------|-----|------|------------------|-----|------------------------------|
| 0x54<br>MASK_A | 7   | R/W  | (reserved)       | 0   |                              |
|                | 6   | R/W  | <b>M_UVLO_IO</b> | 0   | Mask UVLO_IO caused nIRQ     |
|                | 5   | R/W  | (reserved)       | 0   |                              |
|                | 4   | R/W  | <b>M_GPI4</b>    | 0   | Masks nIRQ interrupt at GPI4 |
|                | 3   | R/W  | <b>M_GPI3</b>    | 0   | Masks nIRQ interrupt at GPI3 |
|                | 2   | R/W  | <b>M_GPI2</b>    | 0   | Masks nIRQ interrupt at GPI2 |
|                | 1   | R/W  | <b>M_GPI1</b>    | 0   | Masks nIRQ interrupt at GPI1 |
|                | 0   | R/W  | <b>M_GPIO</b>    | 0   | Masks nIRQ interrupt at GPIO |

| Register       | Bit | Type | Label              | Def | Description                 |
|----------------|-----|------|--------------------|-----|-----------------------------|
| 0x55<br>MASK_B | 7:6 | R/W  | (reserved)         | 00  |                             |
|                | 5   | R/W  | <b>M_OV_CURR_B</b> | 0   | OV_CURR Buck B caused event |
|                | 4   | R/W  | <b>M_OV_CURR_A</b> | 0   | OV_CURR Buck A caused event |
|                | 3   | R/W  | <b>M_TEMP_CRIT</b> | 0   | TEMP_CRIT caused event      |
|                | 2   | R/W  | <b>M_TEMP_WARN</b> | 0   | TEMP_WARN caused event      |
|                | 1   | R/W  | <b>M_PWRGOOD_B</b> | 0   | PWRGOOD Buck B caused event |
|                | 0   | R/W  | <b>M_PWRGOOD_A</b> | 0   | PWRGOOD Buck A caused event |

**Datasheet**

| Register          | Bit | Type | Label              | Def | Description                                                                                                                                                                |
|-------------------|-----|------|--------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x56<br>CONTROL_A | 7   | R/W  | <b>V_LOCK</b>      | 0   | 0: Allows host writes into registers 0xD0 to 0x14F<br>1: Disables register 0xD0 to 0x14F re-programming from control interfaces                                            |
|                   | 6:5 | R/W  | <b>SLEW_RATE_B</b> | 10  | Buck B DVC slewing is executed at<br>00: 10mV every 4.0 $\mu$ s<br>01: 10mV every 2.0 $\mu$ s<br><b>10: 10mV every 1.0 <math>\mu</math>s</b><br>11: 10mV every 0.5 $\mu$ s |
|                   | 4:3 | R/W  | <b>SLEW_RATE_A</b> | 10  | Buck A DVC slewing is executed at<br>00: 10mV every 4.0 $\mu$ s<br>01: 10mV every 2.0 $\mu$ s<br><b>10: 10mV every 1.0 <math>\mu</math>s</b><br>11: 10mV every 0.5 $\mu$ s |
|                   | 0:2 | R/W  | <b>DEBOUNCE</b>    | 011 | Input signals debounce time:<br>000: no debounce time<br>001: 0.1 ms<br>010: 1.0 ms<br><b>011: 10 ms</b><br>100: 50 ms<br>101: 250 ms<br>110: 500 ms<br>111: 1000 ms       |

**14.2.2.2 GPIO Control**

| Register       | Bit | Type | Label            | Def | Description                                                             |
|----------------|-----|------|------------------|-----|-------------------------------------------------------------------------|
| 0x58<br>GPIO-1 | 7   | R/W  | <b>GPI1_MODE</b> | 0   | <b>0: GPI: debouncing off</b><br>1: GPI: debouncing on                  |
|                | 6   | R/W  | <b>GPI1_TYPE</b> | 1   | 0: GPI: active low<br><b>1: GPI: active high</b>                        |
|                | 5:4 | R/W  | <b>GPI1_PIN</b>  | 00  | PIN assigned to:<br><b>00: GPI</b><br>>00: Reserved                     |
|                | 3   | R/W  | <b>GPIO_MODE</b> | 0   | <b>0: GPIO: debouncing off</b><br>1: GPIO: debouncing on                |
|                | 2   | R/W  | <b>GPIO_TYPE</b> | 1   | 0: GPIO: active low<br><b>1: GPIO: active high</b>                      |
|                | 1:0 | R/W  | <b>GPIO_PIN</b>  | 00  | PIN assigned to:<br><b>00: GPIO</b><br>01: Track enable<br>1x: Reserved |

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| Register        | Bit | Type | Label             | Def | Description                                                                                                                            |
|-----------------|-----|------|-------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------|
| 0x59<br>GPIO2-3 | 7   | R/W  | <b>GPIO3_MODE</b> | 0   | <b>0: GPI: debouncing off</b><br><b>GPO: Sets output to passive level</b><br>1: GPI: debouncing on<br>GPO: Sets output to active level |
|                 | 6   | R/W  | <b>GPIO3_TYPE</b> | 1   | 0: GPI/GPO: active low<br><b>1: GPI/GPO: active high</b>                                                                               |
|                 | 5:4 | R/W  | <b>GPIO3_PIN</b>  | 00  | PIN assigned to:<br><b>00: GPI</b><br>01: Reserved<br>10: GPO (Open drain)<br>11: GPO (Push-pull)                                      |
|                 | 3   | R/W  | <b>GPIO2_MODE</b> | 0   | <b>0: GPI: debouncing off</b><br><b>GPO: Sets output to passive level</b><br>1: GPI: debouncing on<br>GPO: Sets output to active level |
|                 | 2   | R/W  | <b>GPIO2_TYPE</b> | 1   | 0: GPI/GPO: active low<br><b>1: GPI/GPO: active high</b>                                                                               |
|                 | 1:0 | R/W  | <b>GPIO2_PIN</b>  | 00  | PIN assigned to:<br><b>00: GPI</b><br>01: Reserved<br>10: GPO (Open drain)<br>11: GPO (Push-pull)                                      |

| Register     | Bit | Type | Label            | Def  | Description                                                        |
|--------------|-----|------|------------------|------|--------------------------------------------------------------------|
| 0x5A<br>GPI4 | 7:4 | R/W  | (reserved)       | 0000 |                                                                    |
|              | 3   | R/W  | <b>GPI4_MODE</b> | 0    | <b>0: GPI: debouncing off</b><br>1: GPI: debouncing on             |
|              | 2   | R/W  | <b>GPI4_TYPE</b> | 1    | 0: GPI: active low<br><b>1: GPI: active high</b>                   |
|              | 1:0 | R/W  | <b>GPI4_PIN</b>  | 00   | PIN assigned to:<br><b>00: GPI</b><br>01: Reserved<br>1x: Reserved |

**Datasheet****14.2.2.3 Regulators Control**

| Register               | Bit | Type | Label               | Def | Description                                                                                                                                                                                                                                                                                                          |
|------------------------|-----|------|---------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x5D<br>BUCKA_CON<br>T | 7   | R/W  | (reserved)          | 0   |                                                                                                                                                                                                                                                                                                                      |
|                        | 6:5 | R/W  | <b>VBUCKA_GPI</b>   | 00  | Selects the GPI that specifies the target voltage of VBUCKA. This is VBUCKA_A on active to passive transition, VBUCKA_B on passive to active transition.<br>Active high/low is controlled by GPIx_TYPE.<br><b>00: Not controlled by GPIO</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO4 controlled |
|                        | 4   | R/W  | <b>VBUCKA_SEL</b>   | 0   | Buck A voltage is selected from (ramping):<br><b>0: VBUCKA_A</b><br>1: VBUCKA_B                                                                                                                                                                                                                                      |
|                        | 3   | R/W  | <b>BUCKA_PD_DIS</b> | 0   | <b>0: Enable pull-down resistor of Buck A when the buck is disabled</b><br>1: Disable pull-down resistor of Buck A when the buck is disabled                                                                                                                                                                         |
|                        | 2:1 | R/W  | <b>BUCKA_GPI</b>    | 00  | GPIO enables the Buck A on passive to active state transition, disables the Buck A on active to passive state transition<br><b>00: Not controlled by GPIO</b><br>01: GPIO0 controlled<br>10: GPIO1 controlled<br>11: GPIO3 controlled                                                                                |
|                        | 0   | R/W  | <b>BUCKA_EN</b>     | 0   | <b>0: Buck A disabled</b><br>1: Buck A enabled                                                                                                                                                                                                                                                                       |

| Register               | Bit | Type | Label             | Def | Description                                                                                                                                                                                                                                                                                                          |
|------------------------|-----|------|-------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x5E<br>BUCKB_CON<br>T | 7   | R/W  | (reserved)        | 0   |                                                                                                                                                                                                                                                                                                                      |
|                        | 6:5 | R/W  | <b>VBUCKB_GPI</b> | 00  | Selects the GPI that specifies the target voltage of VBUCKB. This is VBUCKB_A on active to passive transition, VBUCKB_B on passive to active transition.<br>Active high/low is controlled by GPIx_TYPE.<br><b>00: Not controlled by GPIO</b><br>01: GPIO1 controlled<br>10: GPIO2 controlled<br>11: GPIO4 controlled |
|                        | 4   | R/W  | <b>VBUCKB_SEL</b> | 0   | Buck A voltage is selected from (ramping):<br><b>0: VBUCKB_A</b><br>1: VBUCKB_B                                                                                                                                                                                                                                      |

## Datasheet

| Register | Bit | Type | Label               | Def | Description                                                                                                                                                                                                                                                  |
|----------|-----|------|---------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|          | 3   | R/W  | <b>BUCKB_PD_DIS</b> | 0   | <p><b>0: Enable pull-down resistor of Buck B when the buck is disabled</b></p> <p>1: Disable pull-down resistor of Buck B when the buck is disabled</p>                                                                                                      |
|          | 2:1 | R/W  | <b>BUCKB_GPI</b>    | 00  | <p>GPIO enables the Buck B on passive to active state transition, disables the Buck B on active to passive state transition</p> <p><b>00: Not controlled by GPIO</b></p> <p>01: GPIO0 controlled</p> <p>10: GPIO1 controlled</p> <p>11: GPIO3 controlled</p> |
|          | 0   | R/W  | <b>BUCKB_EN</b>     | 0   | <p><b>0: Buck B disabled</b></p> <p>1: Buck B enabled</p>                                                                                                                                                                                                    |

## Datasheet

### 14.2.3 Register Page 1

| Register         | Bit | Type | Label      | Def | Description                                                                                                                                                |
|------------------|-----|------|------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x80<br>PAGE_CON | 7   | R/W  | REVERT     | 0   | Resets REG_PAGE to 000 after read/write access has finished                                                                                                |
|                  | 6   | R/W  | WRITE_MODE | 0   | 2-WIRE multiple write mode<br>0: Page Write Mode<br>1: Repeated Write Mode                                                                                 |
|                  | 5:3 | R/W  | (reserved) | 000 |                                                                                                                                                            |
|                  | 3:0 | R/W  | REG_PAGE   | 000 | 000: Selects Register 0x01 to 0x3F<br>001: Selects Register 0x81 to 0xCF<br>010: Selects Register 0x101 to 0x1CF<br>>010: Reserved for production and test |

#### 14.2.3.1 Regulators Settings

| Register          | Bit | Type | Label             | Def  | Description                                                                                                                                                                     |
|-------------------|-----|------|-------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD0<br>BUCK_ILIM | 7:4 | R/W  | <b>BUCKB_ILIM</b> | 1001 | Current limit per phase:<br>0000: 2000 mA<br>0001: 2200 mA<br>0010: 2400 mA<br><br>continuing through...<br><b>1001: 3800 mA</b><br>to...<br><br>1110: 4800 mA<br>1111: 5000 mA |
|                   |     |      |                   |      |                                                                                                                                                                                 |
|                   | 3:0 | R/W  | <b>BUCKA_ILIM</b> | 1001 | Current limit per phase:<br>0000: 2000 mA<br>0001: 2200 mA<br>0010: 2400 mA<br><br>continuing through...<br><b>1001: 3800 mA</b><br>to...<br><br>1110: 4800 mA<br>1111: 5000 mA |
|                   |     |      |                   |      |                                                                                                                                                                                 |

**Datasheet**

| Register               | Bit | Type | Label                  | Def | Description                                                                                                                                                                                                                                |
|------------------------|-----|------|------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD1<br>BUCKA_CON<br>F | 7:5 | R/W  | <b>BUCKA_DOWN_CTRL</b> | 111 | Buck A voltage ramping during power down<br>000: 1.25 mV/μs<br>001: 2.5 mV/μs<br>010: 5 mV/μs<br>011: 10 mV/μs<br>100: 20 mV/μs<br>101: 30 mV/μs<br>110: 40 mV/μs<br><b>111: no ramped power down</b>                                      |
|                        | 4:2 | R/W  | <b>BUCKA_UP_CTRL</b>   | 100 | Buck A voltage ramping during start up<br>000: 1.25 mV/μs<br>001: 2.5 mV/μs<br>010: 5 mV/μs<br>011: 10 mV/μs<br><b>100: 20 mV/μs (Note 1)</b><br>101: 30 mV/μs<br>110: 40 mV/μs<br>111: target voltage applied immediately (no soft start) |
|                        | 1:0 | R/W  | <b>BUCKA_MODE</b>      | 10  | 00: Reserved<br>01: Reserved<br><b>10: Buck A always operates in PWM mode</b><br>11: Automatic mode                                                                                                                                        |

**Note 1** Settings higher than 20 mV/μs may cause significant overshoot

## Datasheet

| Register               | Bit | Type | Label                  | Def | Description                                                                                                                                                                                                                                |
|------------------------|-----|------|------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD2<br>BUCKB_CON<br>F | 7:5 | R/W  | <b>BUCKB_DOWN_CTRL</b> | 111 | Buck B voltage ramping during power down<br>000: 1.25 mV/μs<br>001: 2.5 mV/μs<br>010: 5 mV/μs<br>011: 10 mV/μs<br>100: 20 mV/μs<br>101: 30 mV/μs<br>110: 40 mV/μs<br><b>111: no ramped power down</b>                                      |
|                        | 4:2 | R/W  | <b>BUCKB_UP_CTRL</b>   | 100 | Buck B voltage ramping during start up<br>000: 1.25 mV/μs<br>001: 2.5 mV/μs<br>010: 5 mV/μs<br>011: 10 mV/μs<br><b>100: 20 mV/μs (Note 1)</b><br>101: 30 mV/μs<br>110: 40 mV/μs<br>111: target voltage applied immediately (no soft start) |
|                        | 1:0 | R/W  | <b>BUCKB_MODE</b>      | 10  | 00: Reserved<br>01: Reserved<br><b>10: Buck B always operates in PWM mode</b><br>11: Automatic mode                                                                                                                                        |

**Note 1** Settings higher than 20mV/μs may cause significant overshoot

## Datasheet

| Register          | Bit | Type | Label              | Def | Description                                                                                                                                                                                                                                                                             |
|-------------------|-----|------|--------------------|-----|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD3<br>BUCK_CONF | 7:5 | R/W  | (reserved)         | 000 |                                                                                                                                                                                                                                                                                         |
|                   | 4   | R/W  | <b>PH_SH_EN_B</b>  | 1   | Enable current dependant phase shedding in PWM for Buck B                                                                                                                                                                                                                               |
|                   | 3   | R/W  | <b>PH_SH_EN_A</b>  | 1   | Enable current dependant phase shedding in PWM for Buck A                                                                                                                                                                                                                               |
|                   | 2   | R/W  | <b>PHASE_SEL_B</b> | 1   | Phase selection for Buck B in PWM<br>0: 1 phase is selected<br><b>1: 2 phases are selected</b>                                                                                                                                                                                          |
|                   | 1:0 | R/W  | <b>PHASE_SEL_A</b> | 11  | Phase selection for Buck A in PWM mode.<br>Settings >01 apply only for DA9211 otherwise the number of phases is limited to max 2<br>00: 1 phase is selected<br>01: 2 phases are selected<br>10: 3 phases are selected (uneven 0/90/180 phase shift)<br><b>11: 4 phases are selected</b> |

| Register           | Bit | Type | Label             | Def  | Description                                                                                                                                                                                                                                                                     |
|--------------------|-----|------|-------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD5<br>VBUCKA_MAX | 7   | R/W  | (reserved)        | 0    |                                                                                                                                                                                                                                                                                 |
|                    | 6:0 | R    | <b>VBUCKA_MAX</b> | 0x7F | Sets the maximum voltage allowed for Buck A (OTP programmed, access only in test mode)<br><br>0000000: 0.30 V<br>0000001: 0.31 V<br>0000010: 0.32 V<br><br>Continuing through...<br>1000110: 1.0 V<br>to...<br><br>1111101: 1.55 V<br>1111110: 1.56 V<br><b>1111111: 1.57 V</b> |

## Datasheet

| Register   | Bit | Type | Label             | Def  | Description                                                                                                                                                                                                                                                                                                   |
|------------|-----|------|-------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD6       | 7   | R/W  | (reserved)        | 0    |                                                                                                                                                                                                                                                                                                               |
| VBUCKB_MAX | 6:0 | R    | <b>VBUCKB_MAX</b> | 0x7F | <p>Sets the maximum voltage allowed for Buck B (OTP programmed, access only in test mode)</p> <p>0000000: 0.30 V<br/> 0000001: 0.31 V<br/> 0000010: 0.32 V</p> <p>Continuing through...</p> <p><b>1000110: 1.0 V</b></p> <p>to...</p> <p>1111101: 1.55 V<br/> 1111110: 1.56 V<br/> <b>1111111: 1.57 V</b></p> |

| Register | Bit | Type | Label           | Def  | Description                                                                                                                                                                                                     |
|----------|-----|------|-----------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD7     | 7   | R/W  | (reserved)      | 0    |                                                                                                                                                                                                                 |
| VBUCKA_A | 6:0 | R/W  | <b>VBUCKA_A</b> | 0x46 | <p>0000000: 0.30 V<br/> 0000001: 0.31 V<br/> 0000010: 0.32 V</p> <p>Continuing through...</p> <p><b>1000110: 1.0 V</b></p> <p>to...</p> <p>1111101: 1.55 V<br/> 1111110: 1.56 V<br/> <b>1111111: 1.57 V</b></p> |

## Datasheet

| Register | Bit | Type | Label           | Def  | Description                                                                                                                                                                                          |
|----------|-----|------|-----------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD8     | 7   | R/W  | (reserved)      | 0    |                                                                                                                                                                                                      |
| VBUCKA_B | 6:0 | R/W  | <b>VBUCKA_B</b> | 0x46 | <p>0000000: 0.30 V<br/> 0000001: 0.31 V<br/> 0000010: 0.32 V</p> <p>Continuing through...<br/> <b>1000110: 1.0 V</b><br/> to...</p> <p>1111101: 1.55 V<br/> 1111110: 1.56 V<br/> 1111111: 1.57 V</p> |

| Register | Bit | Type | Label           | Def  | Description                                                                                                                                                                                          |
|----------|-----|------|-----------------|------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xD9     | 7   | R/W  | (reserved)      | 0    |                                                                                                                                                                                                      |
| VBUCKB_A | 6:0 | R/W  | <b>VBUCKB_A</b> | 0x46 | <p>0000000: 0.30 V<br/> 0000001: 0.31 V<br/> 0000010: 0.32 V</p> <p>Continuing through...<br/> <b>1000110: 1.0 V</b><br/> to...</p> <p>1111101: 1.55 V<br/> 1111110: 1.56 V<br/> 1111111: 1.57 V</p> |

## Datasheet

| Register | Bit | Type | Label           | Def  | Description                                                                                                                                                                   |
|----------|-----|------|-----------------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0xDA     | 7   | R/W  | (reserved)      | 0    |                                                                                                                                                                               |
| VBUCKB_B | 6:0 | R/W  | <b>VBUCKB_B</b> | 0x46 | 0000000: 0.30 V<br>0000001: 0.31 V<br>0000010: 0.32 V<br>Continuing through...<br><b>1000110: 1.0 V</b><br>to...<br><br>1111101: 1.55 V<br>1111110: 1.56 V<br>1111111: 1.57 V |

**Datasheet****14.2.4 Register Page 2**

| Register          | Bit | Type | Label      | Def | Description                                                                                                                                                |
|-------------------|-----|------|------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x100<br>PAGE_CON | 7   | R/W  | REVERT     | 0   | Resets REG_PAGE to 000 after read/write access has finished                                                                                                |
|                   | 6   | R/W  | WRITE_MODE | 0   | 2-WIRE multiple write mode<br>0: Page Write Mode<br>1: Repeated Write Mode                                                                                 |
|                   | 5:3 | R/W  | (reserved) | 000 |                                                                                                                                                            |
|                   | 3:0 | R/W  | REG_PAGE   | 000 | 000: Selects Register 0x01 to 0x3F<br>001: Selects Register 0x81 to 0xCF<br>010: Selects Register 0x101 to 0x1CF<br>>010: Reserved for production and test |

**14.2.4.1 Interface and OTP Settings (shared with DA9063)**

| Register          | Bit | Type | Label       | Def  | Description                                                                                                                           |
|-------------------|-----|------|-------------|------|---------------------------------------------------------------------------------------------------------------------------------------|
| 0x101<br>OTP_CONT | 7:4 | R/W  | (reserved)  | 0000 |                                                                                                                                       |
|                   | 3   | R/W  | PC_DONE     | 0    | Asserted from Power Commander software after the emulated OTP read has finished, automatically cleared when leaving emulated OTP read |
|                   | 2   | R/W  | OTP_APPS_RD | 0    | Reads on assertion application specific registers 0x105, 0x106, 0x143 to 0x149 and OTP_APPS_LOCK) from OTP                            |
|                   | 1   | R/W  | (reserved)  | 0    |                                                                                                                                       |
|                   | 0   | R/W  | OTP_TIM     | 0    | OTP read timing:<br>0: normal read<br>1: marginal read (for OTP fuse verification)                                                    |

## Datasheet

| Register           | Bit | Type | Label                | Def  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|--------------------|-----|------|----------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x105<br>INTERFACE | 7:4 | R/W  | <b>IF_BASE_ADDR1</b> | 1101 | <p>4 MSB of 2-WIRE control interfaces base address XXXX0000</p> <p><b>11010000</b> = 0xD0 write address of PM 2-WIRE interface (page 0 and 1)</p> <p><b>11010001</b> = 0xD1 read address of PM 2-WIRE interface (page 0 and 1)</p> <p><b>11010010</b> = 0xD2 write address of PM-2-WIRE interface (page 2 and 3)</p> <p><b>11010011</b> = 0xD3 read address of PM-2-WIRE interface (page 2 and 3)</p> <p>Code '0000' is reserved for unprogrammed OTP (triggers start-up with hardware default interface address)</p> |
|                    | 3   | R/W  | <b>R/W_POL</b>       | 1    | <p>4-WIRE: Read/Write bit polarity</p> <p>0: Host indicates reading access via R/W bit = '0'</p> <p><b>1: Host indicates reading access via R/W bit = '1'</b></p>                                                                                                                                                                                                                                                                                                                                                     |
|                    | 2   | R/W  | <b>CPHA</b>          | 0    | 4-WIRE interface clock phase (see Table 13)                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
|                    | 1   | R/W  | <b>CPOL</b>          | 0    | <p>4-WIRE interface clock polarity</p> <p>0: <b>SK is low during idle</b></p> <p>1: SK is high during idle</p>                                                                                                                                                                                                                                                                                                                                                                                                        |
|                    | 0   | R/W  | <b>nCS_POL</b>       | 1    | <p>4-WIRE chip select polarity</p> <p>0: nCS is low active</p> <p><b>1: nCS is high active</b></p>                                                                                                                                                                                                                                                                                                                                                                                                                    |

**Datasheet**

| Register            | Bit | Type                                                          | Label            | Def  | Description                                                                                                                                                                                         |
|---------------------|-----|---------------------------------------------------------------|------------------|------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x106<br>INTERFACE2 | 7   | R/W <sup>Er<br/>ror!<br/>Bookma<br/>rk not<br/>defined.</sup> | <b>IF_TYPE</b>   | 1    | 0: Power manager interface is 4-WIRE.<br>Automatically configures GPIO3 and GPI4 as interface signals. The GPIO configuration is overruled.<br><b>1: Power manager interface is 2-WIRE</b>          |
|                     | 6   | R/W                                                           | <b>PM_IF_HSM</b> | 0    | Enables continuous high speed mode on 2-WIRE interface if asserted (no master code required)                                                                                                        |
|                     | 5   | R/W                                                           | <b>PM_IF_FMP</b> | 0    | Enables 2-WIRE interface operating with fast mode+ timings if asserted                                                                                                                              |
|                     | 4   | R/W                                                           | <b>PM_IF_V</b>   | 0    | <b>0: Power manager interface in 2-WIRE mode is supplied from VDDCORE (4-WIRE always from VDDIO)</b><br>1: Power manager interface in 2-WIRE mode is supplied from VDDIO (4-WIRE always from VDDIO) |
|                     | 0:3 | R/W                                                           | (reserved)       | 0000 |                                                                                                                                                                                                     |

**14.2.4.2 OTP Fusing Registers**

| Register           | Bit | Type | Label                 | Def        | Description                                                                                                                                                                                                                            |
|--------------------|-----|------|-----------------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x140<br>OTP_CONT2 | 7   | R/W  | <b>OTP_CONF_LOC_K</b> | 0          | <b>0: Registers 0x54 to 0x5E and 0xD0 to 0xDA are not locked for OTP programming (should be selected for unmarked evaluation samples)</b><br>1: Registers 0x54 to 0x5E and 0xD0 to 0xDA are locked in OTP (no further fusing possible) |
|                    | 6   | R/W  | <b>OTP_APPS_LOC_K</b> | 0          | <b>0: Registers 0x105, 0x106, 0x143 to 0x149 are not locked for OTP programming (should be selected for unmarked evaluation samples)</b><br>1: Registers 0x105, 0x106, 0x143 to 0x149 are locked in OTP (no further fusing possible)   |
|                    | 5:0 | R/W  | (reserved)            | 0000<br>00 |                                                                                                                                                                                                                                        |

| Register          | Bit | Type | Label    | Def  | Description       |
|-------------------|-----|------|----------|------|-------------------|
| 0x141<br>OTP_ADDR | 7:0 | R/W  | OTP_ADDR | 0x00 | OTP Array address |

| Register          | Bit | Type | Label    | Def  | Description                                                                                                  |
|-------------------|-----|------|----------|------|--------------------------------------------------------------------------------------------------------------|
| 0x142<br>OTP_DATA | 7:0 | R/W  | OTP_DATA | 0x00 | OTP read/write data<br>OTP_DATA written to OTP_ADDR selects the IC and accepts unlock sequence (1 + 3 bytes) |

## Datasheet

### 14.2.4.3 Application Configuration Settings

| Register          | Bit | Type | Label            | Def | Description                                                                                                       |
|-------------------|-----|------|------------------|-----|-------------------------------------------------------------------------------------------------------------------|
| 0x143<br>CONFIG_A | 7:5 | R/W  | (reserved)       | 000 |                                                                                                                   |
|                   | 4   | R/W  | <b>2WIRE_TO</b>  | 1   | Enables automatic reset of 2-WIRE interface if the clock stays low for >35 ms<br>0: Disabled<br><b>1: Enabled</b> |
|                   | 3   | R/W  | <b>GPI_V</b>     | 0   | GPIs are supplied from:<br><b>0: VDDCORE</b><br>1: VDDIO                                                          |
|                   | 2   | R/W  | (reserved)       | 0   |                                                                                                                   |
|                   | 1   | R/W  | <b>IRQ_TYPE</b>  | 1   | nIRQ output port is:<br>0: Push-pull<br><b>1: Open drain (requires external pull-up resistor)</b>                 |
|                   | 0   | R/W  | <b>IRQ_LEVEL</b> | 0   | nIRQ output port is:<br><b>0: Active low</b><br>1: Active high                                                    |

**Datasheet**

| Register          | Bit | Type | Label               | Def | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|-------------------|-----|------|---------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x144<br>CONFIG_B | 7   | R/W  | <b>UVLO_IO_DIS</b>  | 0   | Disable the UVLO for the VDDIO rail and its comparator (suggested for rail voltages different to 1.8 V and to save quiescent current)                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|                   | 6   | R/W  | <b>PGB_DVC_MASK</b> | 0   | Power-good configuration for Buck B<br><b>0: Power-good signal not masked during DVC transitions</b><br>1: Power-good signal masked during DVC transitions (keep previous status)                                                                                                                                                                                                                                                                                                                                                                                                                |
|                   | 5   | R/W  | <b>PGA_DVC_MASK</b> | 0   | Power-good configuration for Buck A<br><b>0: Power-good signal not masked during DVC transitions</b><br>1: Power-good signal masked during DVC transitions (keep previous status)                                                                                                                                                                                                                                                                                                                                                                                                                |
|                   | 4:3 | R/W  | <b>OCB_MASK</b>     | 00  | Over Current configuration for Buck B<br><b>00: Event generation due to over current hit is always active during DVC transitions of the Buck converter</b><br>01: Event generation due to over current hit is masked during DVC transitions of the buck converter + 2 $\mu$ s extra masking at the end<br>10: Event generation due to over current hit is masked during DVC transitions of the buck converter + 10 $\mu$ s extra masking at the end<br>11: Event generation due to over current hit is masked during DVC transitions of the buck converter + 50 $\mu$ s extra masking at the end |
|                   | 2:1 | R/W  | <b>OCA_MASK</b>     | 00  | Over Current configuration for Buck A<br><b>00: Event generation due to over current hit is always active during DVC transitions of the buck converter</b><br>01: Event generation due to over current hit is masked during DVC transitions of the buck converter + 2 $\mu$ s extra masking at the end<br>10: Event generation due to over current hit is masked during DVC transitions of the buck converter + 10 $\mu$ s extra masking at the end<br>11: Event generation due to over current hit is masked during DVC transitions of the buck converter + 50 $\mu$ s extra masking at the end |
|                   | 0   | R/W  | (reserved)          | 0   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

## Datasheet

| Register          | Bit | Type | Label             | Def | Description                                                                                                                                                                                                      |
|-------------------|-----|------|-------------------|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x145<br>CONFIG_C | 7:5 | R/W  | (reserved)        | 000 |                                                                                                                                                                                                                  |
|                   | 4   | R/W  | <b>GPI4_PUPD</b>  | 0   | <b>0: GPI: pull-down resistor disabled</b><br>1: GPI: pull-down resistor enabled                                                                                                                                 |
|                   | 3   | R/W  | <b>GPIO3_PUPD</b> | 0   | <b>0: GPI: pull-down resistor disabled</b><br><b>GPO (open drain): pull up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull up resistor         |
|                   | 2   | R/W  | <b>GPIO2_PUPD</b> | 0   | <b>0: GPI: pull-down resistor disabled</b><br><b>GPO (open drain): pull up resistor disabled (external pull-up resistor)</b><br>1: GPI: pull-down resistor enabled<br>GPO (open drain): pull up resistor enabled |
|                   | 1   | R/W  | <b>GPI1_PUPD</b>  | 0   | <b>0: GPI: pull-down resistor disabled</b><br>1: GPI: pull-down resistor enabled                                                                                                                                 |
|                   | 0   | R/W  | <b>GPI0_PUPD</b>  | 0   | <b>0: GPI: pull-down resistor disabled</b><br>1: GPI: pull-down resistor enabled                                                                                                                                 |

| Register          | Bit | Type | Label               | Def | Description                                                                                  |
|-------------------|-----|------|---------------------|-----|----------------------------------------------------------------------------------------------|
| 0x146<br>CONFIG_D | 7:6 | R/W  | <b>BUCKB_PG_SEL</b> | 00  | Selection of the PG signal for Buck B<br>00: none<br>01: GPO2<br>10: GPO3<br>11: reserved    |
|                   | 5:4 | R/W  | <b>BUCKA_PG_SEL</b> | 00  | Selection of the PG signal for Buck A<br>00: none<br>01: GPO2<br>10: GPO3<br>11: reserved    |
|                   | 3:2 | R/W  | <b>READYB_CONF</b>  | 00  | Selection of the READY signal for Buck B<br>00: none<br>01: GPO2<br>10: GPO3<br>11: reserved |
|                   | 1:0 | R/W  | <b>READYA_CONF</b>  | 00  | Selection of the READY signal for Buck A<br>00: none<br>01: GPO2<br>10: GPO3<br>11: reserved |

## Datasheet

| Register          | Bit | Type | Label              | Def | Description                                                                                                                                                                            |
|-------------------|-----|------|--------------------|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x147<br>CONFIG_E | 7   | R/W  | <b>STAND_ALONE</b> | 0   | <b>0: DA9211 and DA9212 is used as companion IC to DA9063 or DA9063-compliant</b><br>1: DA9211 and DA9212 is stand alone or as companion IC with another PMU not DA9063-compliant      |
|                   | 6   | R/W  | (reserved)         | 0   |                                                                                                                                                                                        |
|                   | 5:3 | R/W  | (reserved)         | 000 |                                                                                                                                                                                        |
|                   | 2:0 | R/W  | <b>OSC_TUNE</b>    | 000 | Tune the main 6 MHz oscillator frequency:<br><b>000: no tune</b><br>001: +180 kHz<br>010: +360 kHz<br>011: +540 kHz<br>100: +720 kHz<br>101: 900 kHz<br>110: 1080 kHz<br>111: 1260 kHz |

| Register          | Bit | Type | Label                | Def  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
|-------------------|-----|------|----------------------|------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 0x148<br>CONFIG_F | 7:4 | R/W  | <b>IF_BASE_ADDR2</b> | 1101 | If a second I2C address is to be selected on ADR_SEL_CONF, this field configures the second address.<br>4 MSB of 2-WIRE control interfaces base address XXXX0000<br><b>11010000</b> = 0xD0 write address of PM 2-WIRE interface (page 0 and 1)<br><b>11010001</b> = 0xD1 read address of PM 2-WIRE interface (page 0 and 1)<br><b>11010010</b> = 0xD2 write address of PM-2-WIRE interface (page 2 and 3)<br><b>11010011</b> = 0xD3 read address of PM-2-WIRE interface (page 2 and 3)<br>Code '0000' is reserved for unprogrammed OTP (triggers start-up with hardware default interface address) |
|                   |     |      |                      |      |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                   | 3:2 | R    | (reserved)           | 00   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|                   | 1   | R/W  | <b>ADDR_SEL_CONF</b> | 00   | Selects the GPIO for the alternative I2C address selection:<br><b>00: none</b><br>01: GPIO0<br>10: GPIO1<br>11: GPIO4                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |

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## 15. Application Information

The following recommended components are examples selected from requirements of a typical application.

### 15.1 Capacitor Selection

Ceramic capacitors are used as bypass capacitors at all VDD and output rails. When selecting a capacitor, especially for types with high capacitance at smallest physical dimension, the DC bias characteristic has to be taken into account.

**Table 17: Recommended capacitor types**

| Application        | Value         | Size  | Temp Char  | Tol       | V-Rate | Type                      |
|--------------------|---------------|-------|------------|-----------|--------|---------------------------|
| VOUT output bypass | 4x 22 $\mu$ F | 0402  | X5R +/-15% | +/-20%    | 4 V    | Semco CL05A226MR5NZNC     |
|                    | 4x 10 $\mu$ F | 0402  | X5R +/-15% | +/-20%    | 10 V   | Semco CL05A106MP5NUNC     |
| VDDx bypass        | 4x 10 $\mu$ F | 0603  | X5R +/-15% | +/-20%    | 6.3 V  | Murata GRM188R60J106ME84  |
| VSYS bypass        | 1x 1 $\mu$ F  | 0402  | X5R +/-15% | +/-10%    | 10 V   | Murata GRM155R61A105KE15# |
| VDDIO bypass       | 1x 100 nF     | 01005 | X5R +/-15% | $\pm$ 10% | 6.3 V  | Semco CL02A104KQ2NNN      |

### 15.2 Inductor Selection

Inductors should be selected based upon the following parameters:

- Rated max. current: usually a coil provides two current limits: The  $I_{sat}$  specifies the maximum current at which the inductance drops by 30% of the nominal value. The  $I_{max}$  is defined by the maximum power dissipation and is applied to the effective current.
- DC resistance: critical for the converter efficiency and should therefore be minimised.
- Inductance: given by converter electrical characteristics; 0.47uH for each DA9211 and DA9212 phase.

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**Table 18: Recommended inductor types**

| Application | Value           | Size            | I <sub>max(dc)</sub> | I <sub>sat</sub> | Tol    | DC res        | Type                          |
|-------------|-----------------|-----------------|----------------------|------------------|--------|---------------|-------------------------------|
| BUCK        | 4x 0.47 $\mu$ H | 2.0x1.6x 1.0 mm | 3.6 A                | 4.1 A            | +/-20% | 32 m $\Omega$ | TOKO DFE201610P-H-R47M        |
|             | 4x 0.47 $\mu$ H | 2.0x1.6x 1.2 mm | 3.8 A                | 4.2 A            | +/-30% | 40 m $\Omega$ | TOKO DFE201612C 1286AS-H-R47M |
|             | 4x 0.47 $\mu$ H | 2.5x2.0x 1.0 mm | 3.6 A                | 3.9 A            | +/-20% | 35 m $\Omega$ | TOKO DFE252010C 1269AS-H-R47M |
|             | 4x 0.47 $\mu$ H | 2.5x2.0x 1.2 mm | 4.4 A                | 4.7 A            | +/-20% | 29 m $\Omega$ | TOKO DFE252012C 1239AS-H-R47M |
|             | 4x 0.47 $\mu$ H | 2.0x1.6x 1.0 mm | 2.7 A                | 3.5 A            | +/-20% | 38 m $\Omega$ | TDK TFM201610A R47M           |
|             | 4x 0.47 $\mu$ H | 2.5x2.0x 1.0 mm | 2.8 A                | 4.5 A            | +/-20% | 34 m $\Omega$ | TDK TFM252010A R47M           |
|             | 4x 0.47 $\mu$ H | 2.0x1.6x 1.0mm  | 2.7 A                | 3.56 A           | +/-20% | 38 m $\Omega$ | Cyntec PIFE20161T             |
|             | 4x 0.47 $\mu$ H | 2.5x2.0x 1.0mm  | 3.5 A                | 4.5 A            | +/-20% | 34 m $\Omega$ | Cyntec PIFE25201T             |
|             | 4x 0.47 $\mu$ H | 2.5x2.0x 1.2mm  | 4.5 A                | 5.0 A            | +/-20% | 23 m $\Omega$ | Cyntec PIFE25201B             |
|             | 4x 0.47 $\mu$ H | 2.5x2.0x 1.2mm  | 3.7 A                | 3.9 A            | +/-20% | 25 m $\Omega$ | Cyntec PST25201B              |
|             | 4x 0.47 $\mu$ H | 2.0x2.0x 1.2mm  | 2.8 A                | 4.2 A            | +/-30% | 30 m $\Omega$ | Taiyo Yuden MDMK2020T R47M    |
|             | 4x 0.47 $\mu$ H | 2.5x2.0x 1.2mm  | 3.9 A                | 4.8 A            | +/-20% | 30 m $\Omega$ | Taiyo Yuden MAMK2520T R47M    |
|             | 4x 0.47 $\mu$ H | 2.0x1.6x 1.0mm  | 3.2 A                | 3.6 A            | +/-20% | 32 m $\Omega$ | Murata LQM2MPNR47MGH          |
|             | 4x 0.47 $\mu$ H | 4x4x1.2 mm      | 8.7 A                | 6.7 A            | +/-20% | 14 m $\Omega$ | Coilcraft XFL4012-471ME       |

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## 16. Package information

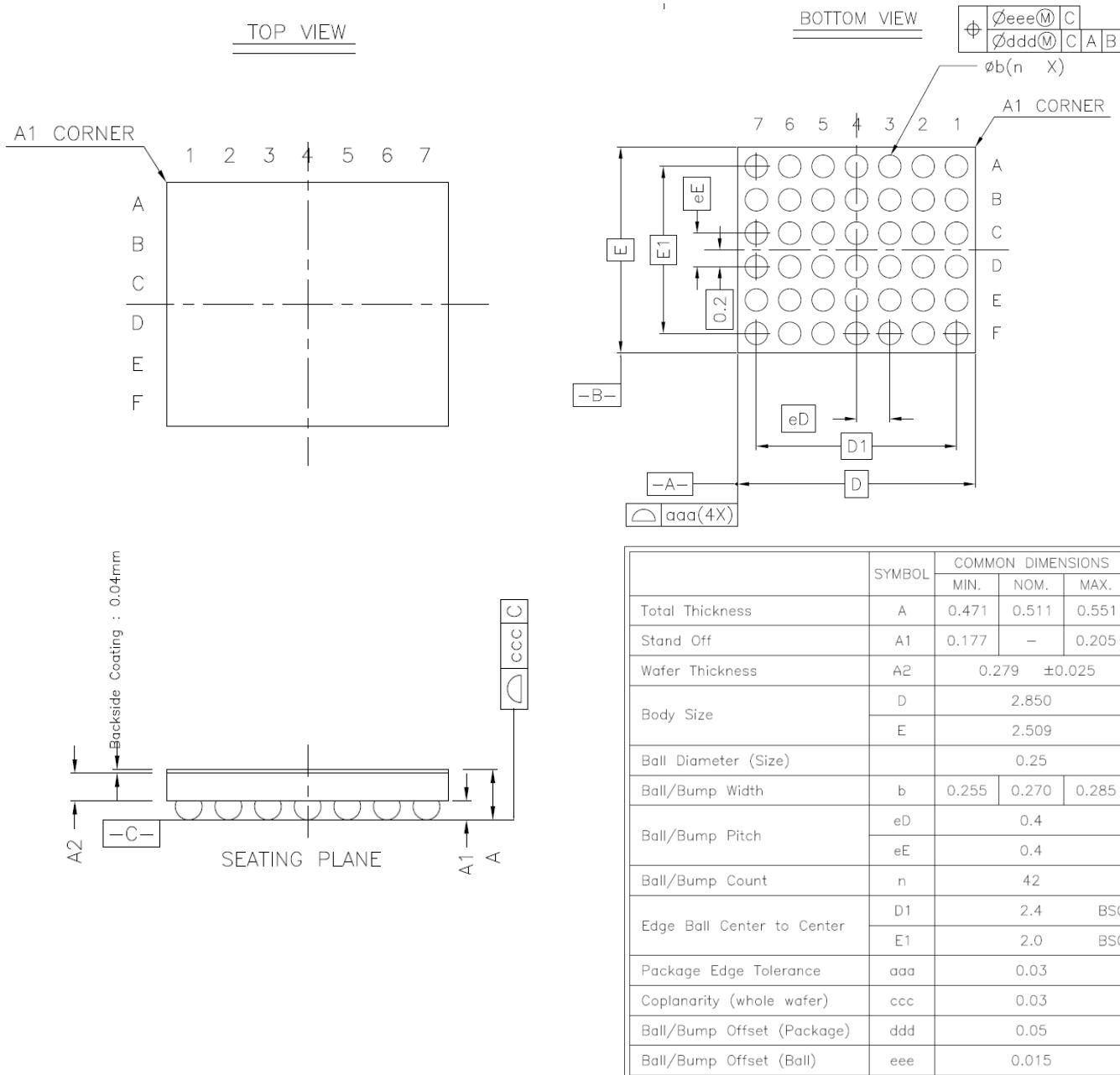


Figure 49: DA9211/12 WL-CSP package outline drawing

## Datasheet

### Status Definitions

| Revision | Datasheet Status | Product Status | Definition                                                                                                                                                                                                                                                                                                                                                                                           |
|----------|------------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.<n>    | Target           | Development    | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice.                                                                                                                                                                                                                                                               |
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(Rev.1.0 Mar 2020)

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