

System PMIC for Dual/Quad-Core Processors

General Description

DA9066 combines an ultra-low-power audio codec with core power management functions targeting standalone application processors and mobile phones. All linear regulators use Dialog's SmartMirror™ dynamic biasing technique, which maintains high performance over a wide range of operating conditions and a power saving mode (Sleep mode) to minimize the quiescent current. The regulators have output voltages independently programmable via the device control interface.

The buck converters do not require external Schottky diodes and offer a Sleep mode (PFM mode) for optimal efficiency at low-load currents. All DC-DC converters use a 2 MHz or 3 MHz switching frequency giving high efficiency and allowing the use of small external inductors (down to 1 μ H).

Beside the power modules there are different core modules like real time clock (RTC), general purpose 12-bit ADC (GPADC) and general purpose IO pins (GPIO) implemented on the IC. These support different functions such as battery voltage supervision and device over-temperature protection. DA9066 can be completely controlled from the host software writes to registers, which brings high flexibility to the design of applications.

DA9066 contains an audio codec, which supports simultaneously stereo line input with up to three microphones with dual switchable bias. Comprehensive analog mixing and bypass paths to the output drivers are available. By optimizing both the power and signal chain paths for performance and efficiency it can provide 98 dB SNR at the headphone while consuming less than 5 mW from the battery. The headphone output is true-ground with integrated charge pump. A dedicated mono line out channel is provided for speaker or beep functionality.

Digital audio transfer to and from the external processor is via bidirectional I²S interface which supports all common sample rates. The device may be operated in slave or master modes using the internal phase-locked loop (PLL), which may be powered down. To fully optimize each customer application, a range of built-in filtering, equalization, or audio DSP enhancements are available. These are accessible by the processor over the 2-wire serial interface and can be used to minimize latency and power consumption.

Key Features

- Operating range 2.5 V to 5.0 V
- Twenty programmable LDO regulators
- One dual-phase 3 A buck converter
- Four single-phase buck converters
- One high-efficiency RF buck converter
- Low-power backup battery charger
- 32 kHz real-time clock (RTC) with alarm capability
- 12-bit general purpose ADC with auto-mode controller
- Accurate bandgap reference
- Temperature/voltage supervision
- High-speed I²C interface
- OTP memory
- Full low-power audio codec
- 98 dB stereo output into 16 Ω to 32 Ω headphones
- Minimum external components; capless, true-ground driver eliminates bulky headphone coupling capacitors
- Supports three microphones with separate low-noise microphone bias outputs
- Low-power PLL provides system clocking and audio sample rate flexibility
- Built-in 5-band EQ, ALC, and noise gate DSP functions
- WLCSP, 5.8 mm x 4.8 mm, 0.4 mm pitch

Applications

- Smartphones and mobile phones
- Ultrabooks, tablet PCs, and eBook readers
- Portable navigation devices,
- TV and media players

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Block Diagram

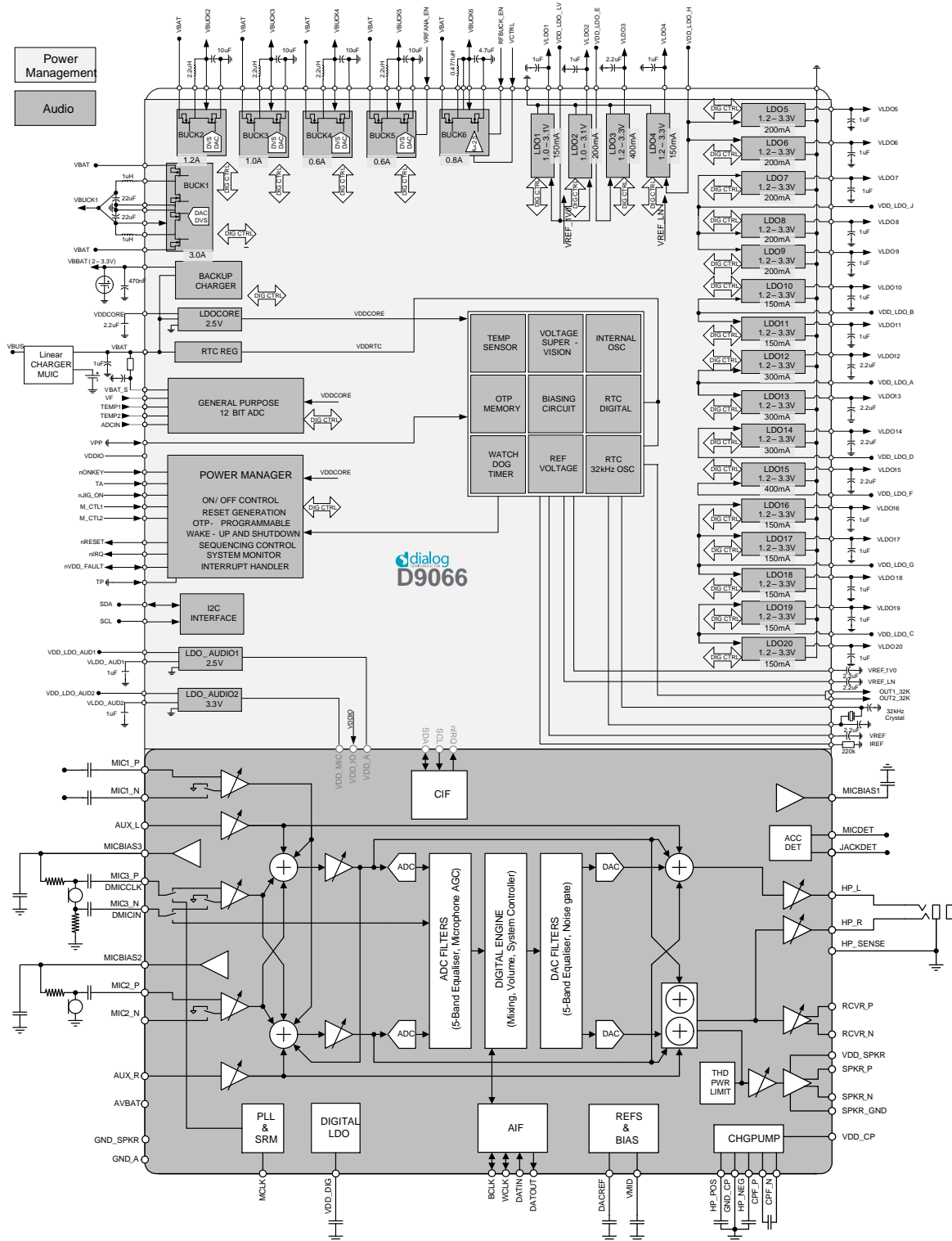


Figure 1: Block Diagram

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1 Pinout

| | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |
|---|----------|----------|----------|----------|--------------|--------------|-----------|-----------|------------|------------|------------|--------------|------------|------------|---|
| A | SPKR_GND | SPKR_P | SPKR_VDD | SPKR_N | SPKR_GND | VDD_LDO_H | VLDO4 | VDD_LDO_J | BUCK_1_VSS | BUCK_1_SW2 | BUCK_1_VDD | BUCK_1_VDD | BUCK_1_SW1 | BUCK_1_VSS | A |
| B | HP_POS | GND_SPKR | AVBAT | N/C | VSS_LDOs | VLDO5 | VLDO6 | VLDO7 | BUCK_1_VSS | BUCK_1_SW2 | BUCK_1_VDD | BUCK_1_VDD | BUCK_1_SW1 | BUCK_1_VSS | B |
| C | CPF_P | GND_CP | GND_A | VDD_DIG | VDD_LDO_AUD2 | VLDO_AUD2 | VLDO8 | VLDO9 | VBAT | VBBAT | VSS | TP | VSS_BUCKs | BUCK_2_VSS | C |
| D | CPF_N | VDD_CP | GND_A | DATOUT | VSS_IOs | VSS_ANA | VCORE | VREF_LN | VREF | VBAT_S | VBUC_K1 | VPP | BUCK_2_VDD | BUCK_2_SW | D |
| E | HP_NEG | DACREF | N/C | DATIN | nIRQ | OUT1_32K | VSS_DIG | VREF_1V0 | ADCIN | TEMP2 | VBUC_K2 | nJIGN | NC | BUCK_3_VDD | E |
| F | HP_R | HP_SENSE | N/C | BCLK | nONKEY | OUT2_32K | VSS | N/C | VF | TEMP1 | VBUC_K3 | MCTL1 | BUCK_3_VSS | BUCK_3_SW | F |
| G | HP_L | VMID | N/C | WCLK | nVDD_FAULT | nRESET | SDA | SCL | N/C | IREF | VBUC_K4 | MCTL2 | NC | BUCK_4_VSS | G |
| H | RCVR_N | MICDET | GND_A | MCLK | VDDIO | VLDO_AUD1 | N/C | N/C | VSS_LDOs | VSS | VBUC_K5 | TA | BUCK_4_VDD | BUCK_4_SW | H |
| J | RCVR_P | JACKDET | GND_A | GND_A | VLDO1 | VDD_LDO_AUD1 | VLDO1_6 | VLDO1_7 | VLDO1_9 | VLDO2_0 | VLDO1_0 | VRFANA_EN | NC | BUCK_5_VDD | J |
| K | AUX_R | MICBIAS1 | MICBIAS2 | MICBIAS3 | VSS_LDOs | VDD_LDO_LV | VDD_LDO_G | VLDO1_8 | VDD_LDO_C | VDD_LDO_B | VLDO1_1 | RFBUCK_EN | BUCK_5_VSS | BUCK_5_SW | K |
| L | AUX_L | MIC1_N | MIC2_N | MIC3_N | VLDO3 | VLDO2 | VDD_LDO_F | VLDO1_4 | VDD_LDO_D | VLDO1_2 | VBUC_K6_FB | VBUC_K_VCTRL | VSS_BUCKs | BUCK_6_VSS | L |
| M | NC | MIC1_P | MIC2_P | MIC3_P | XIN | XOUT | VDD_LDO_E | VLDO1_5 | VLDO1_3 | VDD_LDO_A | VBUC_K6 | BUCK_6_VDD | BUCK_6_SW | VSS_SENSE | M |
| | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | |



Figure 2: Connection Diagram

System PMIC for Dual/Quad-Core Processors

Table 1: Pin Description

| Pin No. | Pin Name | Type (Table 2) | Description |
|----------------------------------|------------|-------------------|---|
| Power Manager | | | |
| F10 | nONKEY | DI | On/off key, hardware (HW) input for watchdog (WD) supervision |
| F3 | MCTL1 | DI | Active high mode-control input 1 |
| G3 | MCTL2 | DI | Active high mode-control input 2 |
| H3 | TA | DI | Travel adaptor wakeup control |
| E3 | nJIG_ON | DI | Test (JTAG) wakeup control |
| G9 | nRESET | DO | Active low RESET towards host |
| E10 | nIRQ | DO | Active low IRQ line towards host |
| G10 | nVDD_FAULT | DIO | Active low indication for low supply voltage |
| K3 | RFBUCK_EN | DI | Active high RF buck enable input |
| J3 | VRFANA_EN | DI | Active high enable input for the ANA_RF supplies (LDO and buck) |
| D3 | VPP | AI | Programming voltage |
| C3 | TP | AI | Test pin |
| I²C Interfaces | | | |
| G7 | SCL | DI | I ² C clock |
| G8 | SDA | DIO | I ² C data |
| Voltage Regulators | | | |
| J10 | VLDO1 | AO | LDO1 output voltage |
| L9 | VLDO2 | AO | LDO2 output voltage |
| L10 | VLDO3 | AO | LDO3 output voltage |
| A8 | VLDO4 | AO | LDO4 output voltage |
| B9 | VLDO5 | AO | LDO5 output voltage |
| B8 | VLDO6 | AO | LDO6 output voltage |
| B7 | VLDO7 | AO | LDO7 output voltage |
| C8 | VLDO8 | AO | LDO8 output voltage |
| C7 | VLDO9 | AO | LDO9 output voltage |
| J4 | VLDO10 | AO | LDO10 output voltage |
| K4 | VLDO11 | AO | LDO11 output voltage |
| L5 | VLDO12 | AO | LDO12 output voltage |
| M6 | VLDO13 | AO | LDO13 output voltage |
| L7 | VLDO14 | AO | LDO14 output voltage |
| M7 | VLDO15 | AO | LDO15 output voltage |
| J8 | VLDO16 | AO | LDO16 output voltage |
| J7 | VLDO17 | AO | LDO17 output voltage |
| K7 | VLDO18 | AO | LDO18 output voltage |
| J6 | VLDO19 | AO | LDO19 output voltage |

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| Pin No. | Pin Name | Type (Table 2) | Description |
|------------------------------|--------------|-------------------|-----------------------------|
| J5 | VLDO20 | AO | LDO20 output voltage |
| M5 | VDD_LDO_A | PWR | LDO12/13 supply voltage |
| K5 | VDD_LDO_B | PWR | LDO10/11 supply voltage |
| K6 | VDD_LDO_C | PWR | LDO19/20 supply voltage |
| L6 | VDD_LDO_D | PWR | LDO14 supply voltage |
| M8 | VDD_LDO_E | PWR | LDO3 supply voltage |
| L8 | VDD_LDO_F | PWR | LDO15 supply voltage |
| K8 | VDD_LDO_G | PWR | LDO16/17/18 supply voltage |
| A9 | VDD_LDO_H | PWR | LDO4/5/6 supply voltage |
| A7 | VDD_LDO_J | PWR | LDO7/8/9 supply voltage |
| K9 | VDD_LDO_LV | PWR | LDO1/2 supply voltage |
| J9 | VDD_LDO_AUD1 | PWR | Audio LDO1 supply voltage |
| C10 | VDD_LDO_AUD2 | PWR | Audio LDO2 supply voltage |
| H9 | VLDO_AUD1 | AO | 1.6 V internal audio supply |
| C9 | VLDO_AUD2 | AO | 3.3 V internal audio supply |
| D8 | VCORE | AO | 2.5 V internal PMIC supply |
| DC-DC Buck Converters | | | |
| D4 | VBUCK1 | AI | Buck1 sense input |
| A2, B2 | SW1BUCK1 | AO | Buck1 switching output P1 |
| A5, B5 | SW2BUCK1 | AO | Buck1 switching output P2 |
| A3, A4, B3, B4 | VDD_BUCK1 | PWR | Buck1 supply |
| A1, A6, B1, B6 | VSS_BUCK1 | VSS | Buck1 ground |
| E4 | VBUCK2 | AI | Buck2 sense input |
| D1 | SWBUCK2 | AO | Buck2 switching output |
| D2 | VDD_BUCK2 | PWR | Buck2 supply |
| C1 | VSS_BUCK2 | VSS | Buck2 ground |
| F4 | VBUCK3 | AI | Buck3 sense input |
| F1 | SWBUCK3 | AO | Buck3 switching output |
| E1 | VDD_BUCK3 | PWR | Buck3 supply |
| F2 | VSS_BUCK3 | VSS | Buck3 ground |
| G4 | VBUCK4 | AI | Buck4 sense input |
| H1 | SWBUCK4 | AO | Buck4 switching output |
| H2 | VDD_BUCK4 | PWR | Buck4 supply |
| G1 | VSS_BUCK4 | VSS | Buck4 ground |
| H4 | VBUCK5 | AI | Buck5 sense input |
| K1 | SWBUCK5 | AO | Buck5 switching output |
| J1 | VDD_BUCK5 | PWR | Buck5 supply |

System PMIC for Dual/Quad-Core Processors

| Pin No. | Pin Name | Type (Table 2) | Description |
|--------------------------------------|-------------|-------------------|---|
| K2 | VSS_BUCK5 | VSS | Buck5 ground |
| RF Buck | | | |
| L3 | BUCK6_VCTRL | AI | Buck6 input voltage control |
| L4 | VBUCK6_FB | AI | Buck6 sense input |
| M2 | SWBUCK6 | AO | Buck6 switching output |
| M4 | VBUCK6 | AO | Buck6 output |
| M3 | VDD_BUCK6 | PWR | Buck6 supply |
| L1 | VSS_BUCK6 | VSS | Buck6 ground |
| M1 | VSS_SENSE | VSS | Buck6 ground sense input |
| GPADC | | | |
| D5 | VBAT_S | AI | Sense connection to battery |
| F5 | TEMP1 | AI | Connection to primary NTC |
| E5 | TEMP2 | AI | Connection to secondary NTC |
| F6 | VF | AI | Connection to battery detect circuit |
| E6 | ADC_IN | AI | General purpose (2.5 V) measurement channel |
| Reference and Bias Generation | | | |
| D6 | VREF | AO | Reference voltage output |
| D7 | VREF_LN | AO | Low-noise reference voltage |
| E7 | VREF_1V0 | AO | Aux. reference voltage |
| G5 | IREF | AO | Connection for R _{REF} resistor |
| XTAL Oscillator | | | |
| M10 | XIN | AIO | 32 kHz crystal connection |
| M9 | XOUT | AIO | 32 kHz crystal connection |
| E9 | OUT1_32K | DO | 32 kHz oscillator buffer output |
| F9 | OUT2_32K | DO | 32 kHz oscillator buffer output |
| Back-Up Battery Charger | | | |
| C5 | VBBAT | AIO | Backup battery connection Coin-cell or super-cap |
| Audio | | | |
| M13 | MIC1_P | AI | Microphone_1 positive input |
| L13 | MIC1_N | AI | Microphone_1 negative input |
| M12 | MIC2_P | AI | Microphone_2 positive input |
| L12 | MIC2_N | AI | Microphone_2 negative input |
| M11 | MIC3_P | AI | Microphone_3 positive input |
| L11 | MIC3_N | AI | Microphone_3 negative input |
| L14 | AUX_L | AI | Aux. audio input left |
| K14 | AUX_R | AI | Aux. audio input right |
| F14 | HP_R | AO | Headphone right output |
| G14 | HP_L | AO | Headphone left output |

System PMIC for Dual/Quad-Core Processors

| Pin No. | Pin Name | Type (Table 2) | Description |
|----------------------------|----------|-------------------|------------------------------|
| F13 | HP_SENSE | AO | Headphone ground |
| A13 | SPKR_P | AI | Class-D output (+) |
| A11 | SPKR_N | AO | Class-D output (-) |
| J14 | RCVR_P | AO | Earpiece/receiver output (+) |
| H14 | RCVR_N | AO | Earpiece/receiver output (-) |
| C12, D12, H12, J12, J11 | GND_A | AO | Quiet audio ground |
| A12 | SPKR_VDD | PWR | Class-D power supply |
| A14, A10 | SPKR_GND | PWR | Class-D power ground |
| B13 | GND_SPKR | PWR | Quiet Class-D ground |
| C13 | GND_CP | PWR | Charge pump ground |
| B14 | HP_POS | PWR | Headphone power supply |
| E14 | HP_NEG | PWR | Headphone power ground |
| D13 | VDD_CP | PWR | Charge pump supply |
| C14 | CPF_P | AIO | Flying cap. P terminal |
| D14 | CPF_N | AIO | Flying cap. N terminal |
| G13 | VMID | AIO | Audio reference voltage |
| E13 | DACREF | AIO | Audio reference voltage |
| C11 | VDD_DIG | AIO | Digital LDO output |
| K13 | MICBIAS1 | AO | Microphone bias 1 |
| K12 | MICBIAS2 | AO | Microphone bias 2 |
| K11 | MICBIAS3 | AO | Microphone bias 3 |
| H11 | MCLK | AO | Master clock input |
| F11 | BCLK | DI | I ² S bit clock |
| G11 | WCLK | DIO | I ² S word clock |
| E11 | DATIN | DI | I ² S data in |
| D11 | DATOUT | DO | I ² S data out |
| H13 | MICDET | DO | Microphone detect input |
| J13 | JACKDET | AI | Jack detect input |
| VDD | | | |
| C6 | VBAT | PWR | PMIC supply rail |
| B12 | AVBAT | PWR | Class D supply rail |
| H10 | VDDIO | PWR | I/O voltage supply |
| VSS | | | |
| B10, H6, K10 | GND | VSS | VSS_LDO |
| C4, F8, H5 | GND | VSS | VSS_SUB |
| C2, L2 | GND | VSS | VSS_BUCK |
| D10 | GND | VSS | VSS_IO |
| E8 | GND | VSS | VSS_DIG |

System PMIC for Dual/Quad-Core Processors

| Pin No. | Pin Name | Type (Table 2) | Description |
|--|----------|-------------------|---------------|
| D9 | GND | VSS | VSS_ANA |
| NC | | | |
| B11, E2, E12, F7, F12, G2, G6, G12, H7, H8, J2, M14 | | NC | No Connection |

Table 2: Pin Type Definition

| Pin Type | Description | Pin Type | Description |
|----------|----------------------|----------|---------------------|
| DI | Digital Input | AI | Analog Input |
| DO | Digital Output | AO | Analog Output |
| DIO | Digital Input/Output | AIO | Analog Input/Output |
| PWR | Power | VSS | Ground |

System PMIC for Dual/Quad-Core Processors

2 Absolute Maximum Ratings

Table 3: Absolute Maximum Ratings

| Parameter | Description | Conditions (Note 1) | Min | Max | Unit |
|----------------------|--|---------------------|------|-----------------------|------|
| T _{STG} | Storage temperature | | -40 | +95 | °C |
| T _A | Operating temperature | | -40 | +85 | °C |
| V _{BAT} | Power supply input | | -0.3 | 5.5 | V |
| | Supply voltage all input pins except power | | -0.3 | V _{DD} + 0.3 | V |
| P _D | Maximum power dissipation | | | 1.2 | W |
| Θ _{JA} | Package thermal resistance | | | TBD | K/W |
| V _{ESD_HBM} | ESD protection | Human Body Model | 2 | | kV |

Note 1 Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

System PMIC for Dual/Quad-Core Processors

3 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

| Parameter | Description | Conditions (Note 1) | Min | Max | Unit |
|-------------------|-----------------------|---------------------|-----|-----|------|
| T _A | Operating temperature | | -30 | +85 | °C |
| V _{BAT} | Supply voltage | | 0 | 4.4 | V |
| V _{DDIO} | Supply voltage IO | | 1.6 | 3.6 | V |
| V _{TA} | Max voltage TA pin | | | 5.5 | V |

Note 1 All voltages are referenced to VSS unless otherwise stated. Currents flowing into DA9066 are deemed positive, currents flowing out are deemed negative. Unless otherwise stated, all parameters are valid over the recommended temperature range and power supply range. Please note that the power dissipation must be limited to avoid overheating of DA9066. The maximum power dissipation should not be reached at maximum ambient temperature.

3.1 Current Consumption

Table 5: Current Consumption

| Operating Mode | Conditions (T _A = 25 °C) (Note 1) | Min | Typ | Max | Unit |
|----------------|---|-----|-----------------|-----|------|
| RTC | No main battery. Supplied by BBAT | | 1.1 | 1.5 | μA |
| NO-POWER | Voltage detection on V _{BAT} < 2.5 V | | 15 | 20 | μA |
| POWERDOWN | RTC unit on, all other blocks off (Note 2). V _{BAT} < 2.9 V | | 45 | 55 | μA |
| SLEEP | 4 x buck converters (PFM mode) 3 x LDOs (Sleep Mode) RTC unit on ACC_DETECT unit on Clock module off (I ² C interface off) | | 170 (Note 3) | 230 | μA |
| ACTIVE | 5 x buck converters (PFM mode) 8 x LDOs (ACTIVE mode) RTC unit on ACC_DETECT unit on Clock module on (I ² C interface on) | | 4503 | 610 | μA |

Note 1 Temperature dependent leakages may result in increased current consumption at higher T_A

Note 2 ACTIVE to POWER DOWN transition with PD_DIS = 0xFF

Note 3 Enabled bucks are set to FORCED Sleep mode

System PMIC for Dual/Quad-Core Processors

4 PMIC Electrical Characteristics

4.1 Standard 150 mA LDO

Unless otherwise noted, $T_A = -30\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 6: LDO10, 11, 16, 17, 18, 19, 20 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------------|--|---|-----|-------------------------|-----|---------------------|
| V _{DD} | Input voltage | | 2.0 | | 5.0 | V |
| | | Supplied from buck | 1.5 | | 5.0 | V |
| V _{LDO} | Output voltage | Programmable in 50 mV steps $I_{OUT} = I_{MAX}$ | 1.2 | | 3.3 | V |
| V _{LDO_ACC} | Output accuracy | $I_{OUT} = I_{MAX}$ | -3 | | +3 | % |
| C _{OUT} | Stabilization capacitor | Including voltage(AC/DC) and temperature coefficients | | 1 | | μF |
| C _{OUT_ACC} | Stabilization capacitor accuracy | Including voltage(AC/DC) and temperature coefficients | -55 | | +35 | % |
| ESR _{COUT} | Effective series resistance (ESR) of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| I _{MAX} | Maximum output current | $V_{DD} \geq 2.1\text{ V}$ | 150 | | | mA |
| | | $V_{DD} < 1.8\text{ V}$ | 100 | | | |
| | | $V_{DD} < 1.5\text{ V}$ | 500 | | | |
| I _{MAX_SLEEP} | Maximum output current | $V_{DD} \geq 1.8\text{ V}$ Sleep mode | 15 | | | mA |
| I _{SHORT} | Short circuit current | | | 300 | | mA |
| V _{DROPOUT} | Dropout voltage | $I_{OUT} = I_{MAX}$ (for $V_{DD} = 1.5\text{ V}$ $I_{OUT} = I_{MAX}/3$) | | 100 | 150 | mV |
| V _{S_LINE} | Static line regulation | $V_{DD} = 3.0\text{ V}$ to 5.0 V $I_{OUT} = I_{MAX}$ | | 5 | 20 | mV |
| V _{S_LOAD} | Static load regulation | $I_{OUT} = 1\text{ mA}$ to I_{MAX} | | 5 | 20 | mV |
| V _{TR_LINE} | Line transient response | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 20 | mV |
| V _{TR_LOAD} | Load transient response | $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_r = t_f = 1\text{ }\mu\text{s}$ | | 25 | 50 | mV |
| PSRR | Power Supply Rejection Ratio | $f = 10\text{ Hz}$ to 10 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = I_{MAX}/2$ | 50 | 60 | | dB |
| N | Output noise | $f = 10\text{ Hz}$ to 100 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{MAX} | | 80 | | μV_{RMS} |
| I _{Q_ON} | Quiescent current when on | $I_{OUT} = I_{MAX}$ | | $5.5 + 0.5\% * I_{OUT}$ | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-----|-------------------------------|-----|------|
| I _{Q_SLEEP} | Quiescent current in Sleep mode | I _{OUT} = 0 mA | | 2 | | μA |
| | | I _{OUT} = 0.1 * I _{MAX} | | 2 + 1 % * I _{OUT} | | μA |
| I _{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| t _{ON} | Turn-on time | 10 % to 90 % | | | 300 | μs |
| t _{OFF} | Turn-off time | 90 % to 10 % | | | 10 | ms |
| R _{OFF} | Pull-down resistance when off | | | 100 | | Ω |

System PMIC for Dual/Quad-Core Processors

4.2 Standard 200 mA LDO

Unless otherwise noted, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 7: LDO5, 6, 7, 8, 9 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--|---|-----|-------------------------|-----|---------------------|
| V_{DD} | Input voltage | | 2.0 | | 5.0 | V |
| | | Supplied from buck | 1.5 | | 5.0 | V |
| V_{LDO} | Output voltage | Programmable in 50 mV steps $I_{OUT} = I_{MAX}$ | 1.2 | | 3.3 | V |
| V_{LDO_ACC} | Output accuracy | $I_{OUT} = I_{MAX}$ | -3 | | +3 | % |
| C_{OUT} | Stabilization capacitor | Including voltage(AC/DC) and temperature coefficients | | 1.0 | | μF |
| C_{OUT_ACC} | Stabilization capacitor accuracy | Including voltage(AC/DC) and temperature coefficients | -55 | | +35 | % |
| ESR_{COUT} | Effective series resistance of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| I_{MAX} | Maximum output current | $V_{DD} \geq 2.1\text{ V}$ | 200 | | | mA |
| | | $V_{DD} < 1.8\text{ V}$ | 120 | | | |
| | | $V_{DD} < 1.5\text{ V}$ | 60 | | | |
| I_{MAX_SLEEP} | Maximum output current | $V_{DD} \geq 1.8\text{ V}$ Sleep mode | 20 | | | mA |
| I_{SHORT} | Short circuit current | | | 400 | | mA |
| $V_{DROPOUT}$ | Dropout voltage | $I_{OUT} = I_{MAX}$ (for $V_{DD} = 1.5\text{ V}$ $I_{OUT} = 0.3 * I_{MAX}$) | | 100 | 150 | mV |
| V_{S_LINE} | Static line regulation | $V_{DD} = 3.0\text{ V}$ to 5.0 V $I_{OUT} = I_{MAX}$ | | 5 | 20 | mV |
| V_{S_LOAD} | Static load regulation | $I_{OUT} = 1\text{ mA}$ to I_{MAX} | | 5 | 20 | mV |
| V_{TR_LINE} | Line transient response | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 20 | mV |
| V_{TR_LOAD} | Load transient response | $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_r = t_f = 1\text{ }\mu\text{s}$ | | 25 | 50 | mV |
| PSRR | Power supply rejection ratio | $f = 10\text{ Hz}$ to 10 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 0.5 * I_{MAX}$ | 50 | 60 | | dB |
| N | Output noise | $f = 10\text{ Hz}$ to 100 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{MAX} | | 80 | | μV_{RMS} |
| I_{Q_ON} | Quiescent current when on | $I_{OUT} = I_{MAX}$ | | $5.5 + 0.5\% * I_{OUT}$ | | μA |
| I_{Q_SLEEP} | Quiescent current in | $I_{OUT} = 0\text{ mA}$ | | 2 | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------|-------------------------------|---------------------------|-----|---------------------------|-----|----------|
| | Sleep mode | $I_{OUT} = 0.1 * I_{MAX}$ | | 2 + 1 % * I_{OUT} | | μA |
| I_{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| t_{ON} | Turn-on time | 10 % to 90 % | | | 300 | μs |
| t_{OFF} | Turn-off time | 90 % to 10 % | | | 10 | ms |
| R_{OFF} | Pull-down resistance when off | | | 100 | | Ω |

System PMIC for Dual/Quad-Core Processors

4.3 Standard 300 mA LDO

Unless otherwise noted, $T_A = -30\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 8: LDO12, 13, 14 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------------|---|-----|-------------------------|-----|---------------------|
| V_{DD} | Input voltage | | 2.0 | | 5.0 | V |
| | | Supplied from buck | 1.5 | | 5.0 | V |
| V_{LDO} | Output voltage | Programmable in 50 mV steps $I_{OUT} = I_{MAX}$ | 1.2 | | 3.3 | V |
| V_{LDO_ACC} | Output accuracy | $I_{OUT} = I_{MAX}$ | -3 | | +3 | % |
| C_{OUT} | Stabilization capacitor | Including voltage(AC/DC) and temperature coefficients | | 2.2 | | μF |
| C_{OUT_ACC} | Stabilization capacitor accuracy | Including voltage(AC/DC) and temperature coefficients | -55 | | +35 | % |
| ESR_{COUT} | ESR of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| I_{MAX} | Maximum output current | $V_{DD} \geq 2.1\text{ V}$ | 300 | | | mA |
| | | $V_{DD} < 1.8\text{ V}$ | 200 | | | |
| | | $V_{DD} < 1.5\text{ V}$ | 100 | | | |
| I_{MAX_SLEEP} | Maximum output current | $V_{DD} \geq 1.8\text{ V}$ Sleep mode | 30 | | | mA |
| I_{SHORT} | Short circuit current | | | 600 | | mA |
| $V_{DROPOUT}$ | Dropout voltage | $I_{OUT} = I_{MAX}$ (for $V_{DD} = 1.5\text{ V}$ $I_{OUT} = I_{MAX}/3$) | | 100 | 150 | mV |
| V_{S_LINE} | Static line regulation | $V_{DD} = 3.0\text{ V}$ to 5.0 V $I_{OUT} = I_{MAX}$ | | 5 | 20 | mV |
| V_{S_LOAD} | Static load regulation | $I_{OUT} = 1\text{ mA}$ to I_{MAX} | | 5 | 20 | mV |
| V_{TR_LINE} | Line transient response | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 20 | mV |
| V_{TR_LOAD} | Load transient response | $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_r = t_f = 1\text{ }\mu\text{s}$ | | 25 | 50 | mV |
| PSRR | Power supply rejection ratio | $f = 10\text{ Hz}$ to 10 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = I_{MAX}/2$ | 50 | 60 | | dB |
| N | Output noise | $f = 10\text{ Hz}$ to 100 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{MAX} | | 80 | | μV_{RMS} |
| I_{Q_ON} | Quiescent current when on | $I_{OUT} = I_{MAX}$ | | $5.5 + 0.5\% * I_{OUT}$ | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-----|--------------------------|-----|------|
| I _{Q_SLEEP} | Quiescent current in Sleep mode | I _{OUT} = 0 mA | | 2 | | μA |
| | | I _{OUT} = 0.1 * I _{MAX} | | 2 + 1 % I _{OUT} | | μA |
| I _{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| t _{ON} | Turn-on time | 10 % to 90 % | | | 300 | μs |
| t _{OFF} | Turn-off time | 90 % to 10 % | | | 10 | ms |
| R _{OFF} | Pull-down resistance when off | | | 100 | | Ω |

System PMIC for Dual/Quad-Core Processors

4.4 Standard 400 mA LDO

Unless otherwise noted, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 9: LDO3, 15 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------------------|---|-------|------------------------|-----|-------------------|
| V _{DD} | Input voltage | | 2.0 | | 5.0 | V |
| | | Supplied from buck | 1.5 | | 5.0 | V |
| V _{LDO} | Output voltage | Programmable in 50 mV steps $I_{OUT} = I_{MAX}$ | 1.2 | | 3.3 | V |
| V _{LDO_ACC} | Output accuracy | $I_{OUT} = I_{MAX}$ | -3 | | +3 | % |
| C _{OUT} | Stabilization capacitor | Including voltage(AC/DC) and temperature coefficients | | 2.2 | | μF |
| C _{OUT_ACC} | Stabilization capacitor accuracy | Including voltage(AC/DC) and temperature coefficients | -55 | | +35 | % |
| ESR _{COUT} | ESR of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| I _{MAX} | Maximum output current | $V_{DD} \geq 2.1\text{ V}$ | 400 | | | mA |
| | | $V_{DD} < 1.8\text{ V}$ | 266.7 | | | |
| | | $V_{DD} < 1.5\text{ V}$ | 133.3 | | | |
| I _{MAX_SLEEP} | Maximum output current | $V_{DD} \geq 1.8\text{ V}$ Sleep mode | 40 | | | mA |
| I _{SHORT} | Short circuit current | | | 800 | | mA |
| V _{DROPOUT} | Dropout voltage | $I_{OUT} = I_{MAX}$ (for $V_{DD} = 1.5\text{ V}$, $I_{OUT} = I_{MAX}/3$) | | 100 | 150 | mV |
| V _{S_LINE} | Static line regulation | $V_{DD} = 3.0\text{ V}$ to 5.0 V $I_{OUT} = I_{MAX}$ | | 5 | 20 | mV |
| V _{S_LOAD} | Static load regulation | $I_{OUT} = 1\text{ mA}$ to I_{MAX} | | 5 | 20 | mV |
| V _{TR_LINE} | Line transient response | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 20 | mV |
| V _{TR_LOAD} | Load transient response | $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_r = t_f = 1\text{ }\mu\text{s}$ | | 25 | 50 | mV |
| PSRR | Power supply rejection ratio | $f = 10\text{ Hz}$ to 10 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = I_{MAX}/2$ | 50 | 60 | | dB |
| N | Output noise | $f = 10\text{ Hz}$ to 100 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{MAX} | | 80 | | μV _{RMS} |
| I _{Q_ON} | Quiescent current when on | $I_{OUT} = I_{MAX}$ | | 7 + 0.5 % I_{OUT} | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-----|-------------------------------|-----|------|
| I _{Q_SLEEP} | Quiescent current in Sleep mode | I _{OUT} = 0 mA | | 2.5 | | μA |
| | | I _{OUT} = 0.1 * I _{MAX} | | 2.5 + 1 % I _{OUT} | | μA |
| I _{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| t _{ON} | Turn-on time | 10 % to 90 % | | | 300 | μs |
| t _{OFF} | Turn-off time | 90 % to 10 % | | | 10 | ms |
| R _{OFF} | Pull-down resistance when off | | | 100 | | Ω |

System PMIC for Dual/Quad-Core Processors

4.5 Low Noise 150 mA LDO

Unless otherwise noted, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 10: LDO4 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------------------|---|-----|----------------------------------|-----|-------------------|
| V _{DD} | Input voltage | | 2.0 | | 5.0 | V |
| | | Supplied from buck | 1.5 | | 5.0 | V |
| V _{LDO} | Output voltage | Programmable in 50 mV steps $I_{OUT} = I_{MAX}$ | 1.2 | | 3.3 | V |
| V _{LDO_ACC} | Output accuracy | $I_{OUT} = I_{MAX}$ | -3 | | +3 | % |
| C _{OUT} | Stabilization capacitor | Including voltage(AC/DC) and temperature coefficients | | 2.2 | | μF |
| C _{OUT_ACC} | Stabilization capacitor accuracy | Including voltage(AC/DC) and temperature coefficients | -55 | | +35 | % |
| ESR _{COUT} | ESR of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| I _{MAX} | Maximum output current | $V_{DD} \geq 2.1\text{ V}$ | 150 | | | mA |
| | | $V_{DD} < 1.8\text{ V}$ | 100 | | | |
| | | $V_{DD} < 1.5\text{ V}$ | 50 | | | |
| I _{MAX_SLEEP} | Maximum output current | $V_{DD} \geq 1.8\text{ V}$ Sleep mode | 15 | | | mA |
| I _{SHORT} | Short circuit current | | | 300 | | mA |
| V _{DROPOUT} | Dropout voltage | $I_{OUT} = I_{MAX}$ (for $V_{DD} = 1.5\text{ V}$ $I_{OUT} = I_{MAX}/3$) | | 100 | 150 | mV |
| V _{S_LINE} | Static line regulation | $V_{DD} = 3.0\text{ V}$ to 5.0 V $I_{OUT} = I_{MAX}$ | | 5 | 20 | mV |
| V _{S_LOAD} | Static load regulation | $I_{OUT} = 1\text{ mA}$ to I_{MAX} | | 5 | 20 | mV |
| V _{TR_LINE} | Line transient response | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 20 | mV |
| V _{TR_LOAD} | Load transient response | $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_r = t_f = 1\text{ }\mu\text{s}$ | | 25 | 50 | mV |
| PSRR | Power supply rejection ratio | $f = 10\text{ Hz}$ to 10 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = I_{MAX}/2$ | 60 | 70 | | dB |
| N | Output noise | $f = 10\text{ Hz}$ to 100 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{MAX} | | 40 | | μV _{RMS} |
| I _{Q_ON} | Quiescent current when on | $I_{OUT} = I_{MAX}$ | | 10 + 0.5 % * I _{OUT} | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-----|-------------------------------|-----|------|
| I _{Q_SLEEP} | Quiescent current in Sleep mode | I _{OUT} = 0 mA | | 2 | | μA |
| | | I _{OUT} = 0.1 * I _{MAX} | | 2 + 1 % * I _{OUT} | | μA |
| I _{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| t _{ON} | Turn-on time | 10 % to 90 % | | | 300 | μs |
| t _{OFF} | Turn-off time | 90 % to 10 % | | | 10 | ms |
| R _{OFF} | Pull-down resistance when off | | | 100 | | Ω |

System PMIC for Dual/Quad-Core Processors

4.6 Low Voltage 150 mA LDO

Unless otherwise stated $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 11: LDO1 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------------------|---|-----|-----------------------------------|-----|-------------------|
| V _{DD} | Input voltage | | 2.0 | | 5.0 | V |
| | | Supplied from buck | 1.5 | | 5.0 | V |
| V _{LDO} | Output voltage | Programmable in 50 mV steps $I_{OUT} = I_{MAX}$ | 1.0 | | 3.1 | V |
| V _{LDO_ACC} | Output accuracy | $I_{OUT} = I_{MAX}$ | -3 | | +3 | % |
| C _{OUT} | Stabilization capacitor | Including voltage(AC/DC) and temperature coefficients | | 1.0 | | μF |
| C _{OUT_ACC} | Stabilization capacitor accuracy | Including voltage(AC/DC) and temperature coefficients | -55 | | +35 | % |
| ESR _{COUT} | ESR of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| I _{MAX} | Maximum output current | V _{DD} ≥ 2.1 V | 150 | | | mA |
| | | V _{DD} < 1.8 V | 100 | | | |
| | | V _{DD} < 1.5 V | 50 | | | |
| I _{MAX_SLEEP} | Maximum output current | V _{DD} ≥ 1.8 V Sleep mode | 15 | | | mA |
| I _{SHORT} | Short circuit current | | | 300 | | mA |
| V _{DROPOUT} | Dropout voltage | $I_{OUT} = I_{MAX}$ (for V _{DD} = 1.5 V, $I_{OUT} = I_{MAX}/3$) | | 100 | 150 | mV |
| V _{S_LINE} | Static line regulation | V _{DD} = 3.0 V to 5.0 V $I_{OUT} = I_{MAX}$ | | 5 | 20 | mV |
| V _{S_LOAD} | Static load regulation | $I_{OUT} = 1\text{ mA}$ to I_{MAX} | | 5 | 20 | mV |
| V _{TR_LINE} | Line transient response | V _{DD} = 3.0 V to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10\text{ }μ\text{s}$ | | 5 | 20 | mV |
| V _{TR_LOAD} | Load transient response | V _{DD} = 3.6 V $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_r = t_f = 1\text{ }μ\text{s}$ | | 25 | 50 | mV |
| PSRR | Power supply rejection ratio | $f = 10\text{ Hz}$ to 10 kHz V _{DD} = 3.6 V $I_{OUT} = I_{MAX}/2$ | 50 | 60 | | dB |
| N | Output noise | $f = 10\text{ Hz}$ to 100 kHz V _{DD} = 3.6 V $I_{OUT} = 5\text{ mA}$ to I_{MAX} | | 80 | | μV _{RMS} |
| I _{Q_ON} | Quiescent current when on | $I_{OUT} = I_{MAX}$ | | 5.5 + 0.5 % * I _{OUT} | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-----|-------------------------------|-----|------|
| I _{Q_SLEEP} | Quiescent current in Sleep mode | I _{OUT} = 0 mA | | 2 | | μA |
| | | I _{OUT} = 0.1 * I _{MAX} | | 2 + 1 % * I _{OUT} | | μA |
| I _{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| t _{ON} | Turn-on time | 10 % to 90 % | | | 300 | μs |
| t _{OFF} | Turn-off time | 90 % to 10 % | | | 10 | ms |
| R _{OFF} | Pull-down resistance when off | | | 100 | | Ω |

System PMIC for Dual/Quad-Core Processors

4.7 Low Voltage 200 mA LDO

Unless otherwise stated $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 12: LDO2 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|----------------------------------|---|-------|-------------------------|-----|---------------------|
| V_{DD} | Input voltage | | 2.0 | | 5.0 | V |
| | | Supplied from buck | 1.5 | | 5.0 | |
| V_{LDO} | Output voltage | Programmable in 50 mV steps $I_{OUT} = I_{MAX}$ | 1.1 | | 3.1 | V |
| V_{LDO_ACC} | Output accuracy | $I_{OUT} = I_{MAX}$ | -3 | | +3 | % |
| C_{OUT} | Stabilization capacitor | Including voltage(AC/DC) and temperature coefficients | | 1.0 | | μF |
| C_{OUT_ACC} | Stabilization capacitor accuracy | Including voltage(AC/DC) and temperature coefficients | -55 | | +35 | % |
| ESR_{COUT} | ESR of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| I_{MAX} | Maximum output current | $V_{DD} \geq 2.1\text{ V}$ | 200 | | | mA |
| | | $V_{DD} < 1.8\text{ V}$ | 133.3 | | | |
| | | $V_{DD} < 1.5\text{ V}$ | 66.7 | | | |
| I_{MAX_SLEEP} | Maximum output current | $V_{DD} \geq 1.8\text{ V}$ Sleep mode | 20 | | | mA |
| I_{SHORT} | Short circuit current | | | 400 | | mA |
| $V_{DROPOUT}$ | Dropout voltage | $I_{OUT} = I_{MAX}$ (for $V_{DD} = 1.5\text{ V}$ $I_{OUT} = I_{MAX}/3$) | | 100 | 150 | mV |
| V_{S_LINE} | Static line regulation | $V_{DD} = 3.0\text{ V}$ to 5.0 V $I_{OUT} = I_{MAX}$ | | 5 | 20 | mV |
| V_{S_LOAD} | Static load regulation | $I_{OUT} = 1\text{ mA}$ to I_{MAX} | | 5 | 20 | mV |
| V_{TR_LINE} | Line transient response | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = I_{MAX}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 20 | mV |
| V_{TR_LOAD} | Load transient response | $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 1\text{ mA}$ to I_{MAX} $t_r = t_f = 1\text{ }\mu\text{s}$ | | 25 | 50 | mV |
| PSRR | Power supply rejection ratio | $f = 10\text{ Hz}$ to 10 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = I_{MAX}/2$ | 50 | 60 | | dB |
| N | Output noise | $f = 10\text{ Hz}$ to 100 kHz $V_{DD} = 3.6\text{ V}$ $I_{OUT} = 5\text{ mA}$ to I_{MAX} | | 80 | | μV_{RMS} |
| I_{Q_ON} | Quiescent current when on | $I_{OUT} = I_{MAX}$ | | $5.5 + 0.5\% * I_{OUT}$ | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|---------------------------------|---|-----|-------------------------------|-----|------|
| I _{Q_SLEEP} | Quiescent current in Sleep mode | I _{OUT} = 0 mA | | 2 | | μA |
| | | I _{OUT} = 0.1 * I _{MAX} | | 2 + 1 % * I _{OUT} | | μA |
| I _{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| t _{ON} | Turn-on time | 10 % to 90 % | | | 300 | μs |
| t _{OFF} | Turn-off time | 90 % to 10 % | | | 10 | ms |
| R _{OFF} | Pull-down resistance when off | | | 100 | | Ω |

System PMIC for Dual/Quad-Core Processors

4.8 Buck1

Unless otherwise stated $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 13: Buck1 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|--------------------|--|---|------|--------|---------|------------------|
| ACTIVE Mode | | | | | | |
| V_{DD} | Input voltage | | 2.8 | | 4.5 | V |
| $C_{1/2OUT}$ | Output capacitance per phase | Including voltage and temperature coefficient | 10 | 22 | | μF |
| $C_{1/2OUT_ACC}$ | Output capacitance per phase accuracy | | | | +30 | % |
| ESR_{COUT} | Output capacitor ESR per phase | $f > 100\text{ kHz}$ All caps + track impedance | | 10 | 25 | $\text{m}\Omega$ |
| ESL_{COUT} | Output capacitor effective series inductance (ESL) per phase | $f > 100\text{ kHz}$ All capacitor and track impedances | | | 1.5 | nH |
| $L_{1/2BUCK}$ | Inductor value per phase | | | 1.0 | | μH |
| $L_{1/2BUCK_ACC}$ | Inductor value per phase accuracy | | -30 | | +30 | % |
| $ESR_{L1/2BUCK}$ | Inductor ESR | | | 75 | 120 | $\text{m}\Omega$ |
| V_{BUCK1} | Output voltage | $I_{OUT} = I_{MAX}$ | 600 | Note 1 | 1393.75 | mV |
| V_{BUCK1_ACC} | Output voltage accuracy | Including static line / load regulation | -3 | Note 2 | +3 | % |
| V_{BUCK1_RPL} | Output voltage ripple | $I_{OUT} = I_{MAX}$ | | 5 | 10 | mV |
| V_{TR_LOAD} | Load regulation transient | $I_{OUT} = 1\text{ mA}$ to 2000 mA , $V_{OUT} > 0.9\text{ V}$ $L = 1\text{ }\mu\text{H}$ $di/dt = 250\text{ mA}/\mu\text{s}$ | | 25 | 35 | mV |
| | | $I_{OUT} = 1\text{ mA}$ to 2000 mA , $V_{OUT} > 0.9\text{ V}$ $L = 1\text{ }\mu\text{H}$ $di/dt = 1000\text{ mA}/\mu\text{s}$ | | 30 | 40 | mV |
| V_{TR_LINE} | Line regulation transient | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = 2000\text{ mA}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 10 | mV |
| I_{MAX} | Output current | | 3000 | | | mA |
| I_{LIM_P} | Peak inductor current limit (programmable) per phase | BUCK1_ILIM_PWM Programmable in steps of 80 mA | 80 | | 2560 | mA |
| I_{Q_OFF} | Quiescent current when off | | | | 1 | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Units |
|----------------------|---|--|-----|-----|-------|-------|
| I _{Q_ON} | Quiescent current in synchronous rectification mode | Open loop (Note 3) | | 15 | | mA |
| f _{SW} | Switching frequency | | | 3 | | MHz |
| D _{SW} | Switching duty cycle | | 10 | | 95 | % |
| t _{ON} | Turn-on time | | | | 1 | ms |
| R _{PD} | Output pull down resistor | At V _{OUT} = 0.5 V, can be switched off | | | 200 | Ω |
| η | Efficiency | I _{OUT} = 300 mA to I _{MAX} V _{DD} < 4.2 V | 75 | 85 | | % |
| R _{PMOS} | On resistance PMOS | Including pin and routing | | | 0.25 | Ω |
| R _{NMOS} | On resistance NMOS | Including pin and routing | | | 0.120 | Ω |
| PFM Mode | | | | | | |
| I _{MODE_SW} | PWM to PFM mode switching current | BUCK1_IMODE_SW Programmable in steps of 128 mA | 128 | | 1024 | mA |
| I _{MAX} | Output current | V _{BUCK1} > 0.725 V | 90 | | | mA |
| I _{PLIM} | Peak inductor current limit per phase | BUCK1_ILIM_PFM Programmable in steps of 80 mA | 80 | | 2560 | mA |
| I _{Q_PFM} | Quiescent current in PFM mode | I _{OUT} = 0 | | 35 | 45 | μA |
| f _{OP} | Frequency of operation | | 0 | | 5 | MHz |
| η | Efficiency | I _{OUT} = 10 mA to 750 mA | | 85 | | % |
| t _{TRANS} | Mode transition time | | | 16 | 18 | μs |

Note 1 Programmable in 6.25 mV steps. DVC ramp rate = 12.5 mV/μs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM mode. In closed loop configuration switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

System PMIC for Dual/Quad-Core Processors

4.9 Buck2

Unless otherwise stated $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 14: Buck 2 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|---|---|-------|--------|-------|------------------|
| ACTIVE Mode | | | | | | |
| V_{DD} | Input voltage | | 2.8 | | 4.5 | V |
| C_{OUT} | Output capacitance | Including voltage and temperature coefficient | 4.7 | 10 | | μF |
| C_{OUT_ACC} | Output capacitance accuracy | Including voltage and temperature coefficient | | | +30 | % |
| ESR_{COUT} | Output capacitor ESR | $f > 100\text{ kHz}$ All capacitor and track impedances | | 15 | 30 | $\text{m}\Omega$ |
| L_{BUCK} | Inductor value | | | 2.2 | | μH |
| L_{BUCK_ACC} | Inductor value accuracy | | -30 | | +30 | % |
| R_{LBUCK} | Inductor resistance | | | 75 | 125 | $\text{m}\Omega$ |
| V_{BUCK2} | Output voltage | $I_{OUT} = I_{MAX}$ | 0.725 | Note 1 | 2.075 | V |
| V_{BUCK2_ACC} | Output voltage accuracy | Including static line / load regulation | -3 | Note 2 | +3 | % |
| V_{BUCK2_RPL} | Output voltage ripple | $I_{OUT} = I_{MAX}$ | | 10 | | mV |
| V_{TRLOAD} | Load regulation transient | $I_{OUT} = 0\text{ mA}$ to 500 mA $dI/dt = 50\text{ mA}/\mu\text{s}$ | | 15 | 30 | mV |
| V_{TRLINE} | Line regulation transient | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = 500\text{ mA}$ $t_r = t_f = 10\mu\text{s}$ | | 5 | 10 | mV |
| I_{MAX} | Output current | $V_{DD} - V_{BUCK2} > 1.1\text{ V}$ | 1200 | | | mA |
| I_{LIM_P} | Current limit (programmable) | $BUCK2_ILIM = 00$ | | 840 | | mA |
| | | $BUCK2_ILIM = 01$ | | 1080 | | mA |
| | | $BUCK2_ILIM = 10$ | | 1440 | | mA |
| | | $BUCK2_ILIM = 11$ | | 1800 | | mA |
| $I_{LIM_P_ACC}$ | Current limit (programmable) accuracy | | -20 | | 20 | % |
| I_{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| I_{Q_ON} | Quiescent current in synchronous rectification mode | Open loop (Note 3) | | 3 | | mA |
| f_{SW} | Switching frequency | | | 2 | | MHz |
| D_{SW} | Switching duty cycle | | 10 | | 95 | % |
| t_{ON} | Turn -on time | | | | 2.2 | ms |
| R_{PD} | Output pull-down resistor | $V_{OUT} = 0.5\text{ V}$, can be switched off | | | 200 | Ω |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------------------|--|-----|-----|-------|---------------|
| η | Efficiency | $I_{OUT}=30\text{ mA to }I_{MAX}$ $V_{DD} < 4.2\text{ V}$ | | 85 | | % |
| R_{PMOS} | On resistance PMOS | Including pin and routing | | | 0.4 | Ω |
| R_{NMOS} | On resistance NMOS | Including pin and routing | | | 0.25 | Ω |
| PFM Mode | | | | | | |
| V_{BUCK2} | Output voltage | $I_{OUT} < 90\text{ mA}$ | 0.5 | | 2.075 | V |
| I_{MODE_SW} | Typical mode switching current | | | 50 | | mA |
| I_{MAX} | Output current | $V_{BUCK2} > 0.725\text{ V}$ | 90 | | | mA |
| I_{LIM} | Current limit | | | 180 | | mA |
| I_{LIM_ACC} | Current limit accuracy | | -30 | | +30 | % |
| I_{Q_PFM} | Quiescent current in PFM mode | $I_{OUT} = 0$ | | 25 | 35 | μA |
| f_{OP} | Frequency of operation | | 0 | | 5 | MHz |
| η | Efficiency | $I_{OUT} = 10\text{ mA to }75\text{ mA}$ | | 80 | | % |
| t_{TRANS} | Mode transition time | | | 16 | 18 | μs |

Note 1 Programmable in 25 mV steps. DVC ramp rate = 12.5 mV/ μs .

Note 2 Limited to $\pm 35\text{ mV}$ at low voltage settings.

Note 3 Open loop PWM mode. In closed loop configuration switching losses at $I_{LOAD}=0$ increase I_{Q_ON} .

System PMIC for Dual/Quad-Core Processors

4.10 Buck3

Unless otherwise stated $T_A = -30\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 15: Buck3 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|---|---|-------|--------|-------|------------------|
| ACTIVE Mode | | | | | | |
| V_{DD} | Input voltage | | 3.0 | | 4.5 | V |
| C_{OUT} | Output capacitance | Including voltage and temperature coefficient | 4.7 | 10 | | μF |
| C_{OUT_ACC} | Output capacitance accuracy | Including voltage and temperature coefficient | | | +30 | % |
| ESR_{COUT} | Output capacitor ESR | $f > 100\text{ kHz}$ All capacitor + track impedances | | 15 | 30 | $\text{m}\Omega$ |
| L_{BUCK} | Inductor value | | | 2.2 | | μH |
| L_{BUCK_ACC} | Inductor value accuracy | | -30 | | +30 | % |
| R_{LBUCK} | Inductor resistance | | | 75 | 125 | $\text{m}\Omega$ |
| V_{BUCK3} | Output voltage | $I_{OUT} = I_{MAX}$ $L = 2.2\text{ }\mu\text{H}$ | 0.725 | Note 1 | 2.075 | V |
| V_{BUCK3_ACC} | Output voltage accuracy | Including static line / load regulation | -3 | Note 2 | +3 | % |
| V_{BUCK3_RPL} | Output voltage ripple | $I_{OUT} = I_{MAX}$ | | 10 | | mV |
| V_{TRLOAD} | Load regulation transient | $I_{OUT} = 0\text{ mA}$ to 500 mA $dl/dt = 50\text{ mA}/\mu\text{s}$ | | 15 | 30 | mV |
| V_{TRLINE} | Line regulation transient | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = 500\text{ mA}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 10 | mV |
| I_{OUT} | Output current | $V_{DD} - V_{BUCK3} > 1.1\text{ V}$ | 1000 | | | mA |
| I_{LIM} | Current limit (programmable) | BUCK3_ILIM=00 | | 840 | | mA |
| | | BUCK3_ILIM=01 | | 1080 | | mA |
| | | BUCK3_ILIM=10 | | 1440 | | mA |
| | | BUCK3_ILIM=11 | | 1800 | | mA |
| I_{LIM_ACC} | Current limit (programmable) accuracy | | -20 | | 20 | % |
| I_{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| I_{Q_ON} | Quiescent current in synchronous rectification mode | Open loop (Note 3) | | 2.5 | | mA |
| f_{SW} | Switching frequency | | | 2 | | MHz |
| D | Switching duty cycle | | 10 | | 95 | % |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|--------------------------------|---|-----|-----|-------|------|
| t _{ON} | Turn on time | | | | 2.2 | ms |
| R _{PD} | Output pull down resistor | V _{OUT} = 0.5 V, can be switched off | | | 200 | Ω |
| η | Efficiency | I _{OUT} = 30 mA to I _{MAX} V _{DD} < 4.2 V | | 85 | | % |
| R _{PMOS} | On resistance PMOS | Including pin and routing | | | 0.4 | Ω |
| R _{NMOS} | On resistance NMOS | Including pin and routing | | | 0.25 | Ω |
| PFM Mode | | | | | | |
| V _{BUCK3} | Output voltage | I _{OUT} < 90 mA | 0.5 | | 2.075 | V |
| I _{MODE_SW} | Typical mode switching current | | | 50 | | mA |
| I _{MAX} | Output current | V _{BUCK3} > 0.725 V | 90 | | | mA |
| I _{LIM} | Current limit | | | 180 | | mA |
| I _{LIM_ACC} | Current limit accuracy | | -30 | | +30 | % |
| I _{Q_PFM} | Quiescent current in PFM mode | I _{OUT} = 0 | | 25 | 35 | μA |
| f _{OP} | Frequency of operation | | 0 | | 5 | MHz |
| η | Efficiency | I _{OUT} = 10 mA to 75 mA | | 80 | | % |
| t _{TRANS} | Mode transition time | | | 16 | 18 | μs |

Note 1 Programmable in 25 mV steps. DVC ramp rate = 12.5 mV/μs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM mode. In closed loop configuration switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

System PMIC for Dual/Quad-Core Processors

4.11 Buck4

Unless otherwise stated $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 16: Buck4 Electrical Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------|---|---|-------|--------|-------|------------------|
| ACTIVE Mode | | | | | | |
| V_{DD} | Input voltage | | 2.8 | | 4.5 | V |
| C_{OUT} | Output capacitance | Including voltage and temperature coefficient | 4.7 | 10 | | μF |
| C_{OUT_ACC} | Output capacitance accuracy | Including voltage and temperature coefficient | | | +30 | % |
| ESR_{COUT} | Output capacitor ESR | $f > 100\text{ kHz}$ All capacitor + track impedances | | 15 | 30 | $\text{m}\Omega$ |
| L_{BUCK} | Inductor value | | | 2.2 | | μH |
| L_{BUCK_ACC} | Inductor value accuracy | | -30 | | +30 | % |
| R_{LBUCK} | Inductor resistance | | | 75 | 125 | $\text{m}\Omega$ |
| V_{BUCK4} | Output voltage | $I_{OUT} = I_{MAX}$ $L = 2.2\text{ }\mu\text{H}$ | 0.725 | Note 1 | 2.075 | V |
| V_{BUCK4_ACC} | Output voltage accuracy | Including static line / load regulation | -3 | Note 2 | +3 | % |
| V_{BUCK4_RPL} | Output voltage ripple | $I_{OUT} = I_{MAX}$ | | 10 | | mV |
| V_{TR_LOAD} | Load regulation transient | $I_{OUT} = 0\text{ mA}$ to 400 mA $di/dt = 40\text{ mA}/\mu\text{s}$ | | 15 | 30 | mV |
| V_{TR_LINE} | Line regulation transient | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = 400\text{ mA}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 10 | mV |
| I_{OUT} | Output current | $V_{DD} - V_{BUCK4} > 1.1\text{ V}$ | 600 | | | mA |
| I_{LIM} | Current limit (programmable) | $BUCK4_ILIM = 00$ | | 700 | | mA |
| | | $BUCK4_ILIM = 01$ | | 900 | | mA |
| | | $BUCK4_ILIM = 10$ | | 1200 | | mA |
| | | $BUCK4_ILIM = 11$ | | 1500 | | mA |
| I_{LIM_ACC} | Current limit (programmable) accuracy | | -20 | | +20 | % |
| I_{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| I_{Q_ON} | Quiescent current in synchronous rectification mode | Open loop (Note 3) | | 2.5 | | mA |
| f | Switching frequency | | | 2 | | MHz |
| D | Switching duty cycle | | 10 | | 95 | % |
| t_{ON} | Turn on time | | | | 2.2 | ms |

System PMIC for Dual/Quad-Core Processors

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|--------------------------------|---|-----|-----|-------|------|
| R _{PD} | Output pull-down resistor | V _{OUT} = 0.5 V, can be switched off | | | 200 | Ω |
| η | Efficiency | I _{OUT} = 30 mA to I _{MAX} V _{DD} < 4.2 V | | 85 | | % |
| R _{PMOS} | On resistance PMOS | Including pin and routing | | | 0.4 | Ω |
| R _{NMOS} | On resistance NMOS | Including pin and routing | | | 0.25 | Ω |
| PFM Mode | | | | | | |
| V _{BUCK4} | Output voltage | I _{OUT} < 75 mA | 0.5 | | 2.075 | V |
| I _{MODE_SW} | Typical mode switching current | | | 40 | | mA |
| I _{MAX} | Output current | V _{BUCK4} > 0.725 V | 75 | | | mA |
| I _{LIM} | Current limit | | | 150 | | mA |
| I _{LIM_ACC} | Current limit accuracy | | -30 | | +30 | % |
| I _{Q_PFM} | Quiescent current in PFM mode | I _{OUT} = 0 | | 25 | 35 | μA |
| f _{OP} | Frequency of operation | | 0 | | 5 | MHz |
| η | Efficiency | I _{OUT} = 10 mA to 75 mA | | 80 | | % |
| t _{TRANS} | Mode transition time | | | 16 | 18 | μs |

Note 1 Programmable in 25 mV steps. DVC ramp rate = 12.5 mV/μs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM mode. In closed loop configuration switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

System PMIC for Dual/Quad-Core Processors

4.12 Buck 5

Unless otherwise stated $T_A = -30\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 17: Buck 5 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|---|---|-------|--------|-------|------------------|
| ACTIVE Mode | | | | | | |
| V_{DD} | Input voltage | | 2.8 | | 4.5 | V |
| C_{OUT} | Output capacitance | Including voltage and temperature coefficient | 4.7 | 10 | | μF |
| C_{OUT_ACC} | Output capacitance accuracy | Including voltage and temperature coefficient | | | +30 | % |
| ESR | Output capacitor ESR | $f > 100\text{ kHz}$ All capacitor + track impedances | | 15 | 30 | $\text{m}\Omega$ |
| L_{BUCK} | Inductor value | | | 2.2 | | μH |
| L_{BUCK_ACC} | Inductor value accuracy | | -30 | | +30 | % |
| R_{LBUCK} | Inductor resistance | | | 75 | 125 | $\text{m}\Omega$ |
| V_{BUCK5} | Output voltage | $I_{OUT} = I_{MAX}$ | 0.725 | Note 1 | 2.075 | V |
| V_{BUCK5_ACC} | Output voltage accuracy | Including static line / load regulation | -3 | Note 2 | +3 | % |
| V_{BUCK5_RPL} | Output voltage ripple | $I_{OUT} = I_{MAX}$ | | | | mV |
| V_{TR_LOAD} | Load regulation transient | $I_{OUT} = 0\text{ mA}$ to 500 mA , $dI/dt = 50\text{ mA}/\mu\text{s}$ | | 15 | 30 | mV |
| V_{TR_LINE} | Line regulation transient | $V_{DD} = 3.0\text{ V}$ to 3.6 V $I_{OUT} = 500\text{ mA}$ $t_r = t_f = 10\text{ }\mu\text{s}$ | | 5 | 10 | mV |
| I_{MAX} | Output current | $V_{DD} - V_{BUCK5} > 1.1\text{ V}$ | 600 | | | mA |
| I_{LIM} | Current limit (programmable) | BUCK5_ILIM=00 | | 700 | | mA |
| | | BUCK5_ILIM=01 | | 900 | | mA |
| | | BUCK5_ILIM=10 | | 1200 | | mA |
| | | BUCK5_ILIM=11 | | 1500 | | mA |
| I_{LIM_ACC} | Current limit (programmable) accuracy | BUCK5_ILIM=00 | -20 | | +20 | % |
| I_{Q_OFF} | Quiescent current when off | | | | 1 | μA |
| I_{Q_ON} | Quiescent current in synchronous rectification mode | Open loop (Note 3) | | 3 | | mA |
| f_{SW} | Switching frequency | | | 2 | | MHz |
| D | Switching duty cycle | | 10 | | 95 | % |
| t_{ON} | Turn on time | | | | 2.2 | ms |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|--------------------------------|---|-----|-----|-------|------|
| R _{PD} | Output pull down resistor | V _{OUT} = 0.5 V, can be switched off | | | 200 | Ω |
| η | Efficiency | I _{OUT} = 30 mA to I _{MAX} V _{DD} < 4.2 V | | 85 | | % |
| R _{PMOS} | On resistance PMOS | Including pin and routing | | | 0.4 | Ω |
| R _{NMOS} | On resistance NMOS | Including pin and routing | | | 0.25 | Ω |
| PFM Mode | | | | | | |
| V _{BUCK5} | Output voltage | I _{OUT} < 75 mA | 0.5 | | 2.075 | V |
| I _{MODE_SW} | Typical mode switching current | | | 40 | | mA |
| I _{MAX} | Output current | V _{BUCK5} > 0.725 V | 75 | | | mA |
| I _{LIM} | Current limit | | | 150 | | mA |
| I _{LIM_ACC} | Current limit accuracy | | -30 | | +30 | % |
| I _{Q_PFM} | Quiescent current in PFM mode | I _{OUT} = 0 | | 25 | 35 | μA |
| f _{OP} | Frequency of operation | | 0 | | 5 | MHz |
| η | Efficiency | I _{OUT} = 10 mA to 75 mA | | 80 | | % |
| t _{TRANS} | Mode transition time | | | 16 | 18 | μs |

Note 1 Programmable in 25 mV steps. DVC ramp rate = 12.5 mV/μs.

Note 2 Limited to ±35 mV at low voltage settings.

Note 3 Open loop PWM mode. In closed loop configuration switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

System PMIC for Dual/Quad-Core Processors

4.13 Buck 6

Unless otherwise stated $T_A = -30\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 18: Buck 6 Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|--------------------------------------|--|-----|-----------|------|------------------|
| ACTIVE Mode | | | | | | |
| V_{DD} | Input voltage | | 2.7 | | 4.5 | V |
| C_{OUT} | Output capacitance | Including voltage and temperature coefficient | | 4.7 | | μF |
| C_{OUT_ACC} | Output capacitance accuracy | Including voltage and temperature coefficient | -55 | | +30 | % |
| ESR_{COUT} | Output capacitor ESR | $f > 100\text{ kHz}$ All capacitor and track impedances | | 5 | 10 | $\text{m}\Omega$ |
| L_{BUCK} | Inductor value | $f = 6\text{ MHz}$ | | 0.5 | | μH |
| | | $f = 3\text{ MHz}$ | | 1.0 | | |
| L_{BUCK_ACC} | Inductor value accuracy | $f = 3\text{ MHz}$ or 6 MHz | -30 | | +30 | % |
| R_{LBUCK} | Inductor resistance | | | 50 | 125 | $\text{m}\Omega$ |
| V_{BUCK6} | Output voltage | $V_{OUT} = 2.5 * V_{CTRL}$ | 0.4 | Note 1 | 3.5 | V |
| V_{BUCK6_ACC} | Output voltage accuracy | Including static line / load regulation | -50 | | +50 | mV |
| I_{MAX} | Output current | | 800 | | | mA |
| I_{LIM_P} | Peak inductor current limit | $BUCK6_ILIM_P = 00$ | | 1.0 | | mA |
| | | $BUCK6_ILIM_P = 01$ | | 1.5 | | |
| | | $BUCK6_ILIM_P = 10$ | | 2.0 | | |
| | | $BUCK5_ILIM_P = 11$ | | 2.5 | | |
| $I_{LIM_P_ACC}$ | Peak inductor current limit accuracy | | -30 | | +30 | % |
| I_{LIM_N} | NMOS negative current limit | $BUCK6_ILIM_N = 00$ | | -0.6 | | mA |
| | | $BUCK6_ILIM_N = 01$ | | -1.1 | | |
| | | $BUCK6_ILIM_N = 10$ | | -1.6 | | |
| | | $BUCK5_ILIM_N = 11$ | | -2.1 | | |
| $I_{LIM_N_ACC}$ | NMOS negative current limit accuracy | | -30 | | +30 | % |
| R_{PMOS} | On resistance PMOS | Including pin and routing | | 0.2 | 0.4 | Ω |
| R_{NMOS} | On resistance NMOS | Including pin and routing | | 0.12 | 0.25 | Ω |
| I_{Q_OFF} | Quiescent current when off | $RFBUCK_EN = 0$ | | | 1 | μA |
| I_{Q_ON} | Quiescent current in Sync (PWM) mode | Open loop (Note 2) | | 800 (TBC) | | μA |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-------------------------|---|---|-----------------|----------|-----|----------|
| f | Switching frequency | L = 0.5 μ H | | 6 | | MHz |
| | | L = 1.0 μ H | | 3 | | |
| t _{ON} | Turn-on time | C _{OUT} = 4.7 μ F V _{IN} = 3.7 V, from RFBUCK_EN = 1 to V _{OUT} = 3.1 V | | 15 | 20 | μ s |
| t _R | Transient response | R _{LOAD} \leq 7 Ω V _{OUT} step = 1.4 V to 3.4 V | | | 10 | μ s |
| t _F | | R _{LOAD} \leq 7 Ω V _{OUT} step = 3.4 V to 1.4 V | | | 10 | |
| η | Efficiency | V _{IN} = 3.8 V V _{OUT} = 3.275 V I _{OUT} = 400 mA | | 95 (TBC) | | % |
| V _{SYNC} | PFM to PWM voltage threshold | Forced PWM mode V _{CTRL} > V _{SYNC} | 160 (Note 3) | | 460 | mV |
| PFM Mode | | | | | | |
| V _{SLEEP} | PWM to PFM voltage threshold | Forced PFM mode V _{CTRL} < V _{SLEEP} | 160 (Note 3) | | 460 | mV |
| I _{SLEEP} | Mode switching current threshold | AUTO mode V _{SLEEP} < V _{CTRL} < V _{SYNC} | 75 | | 125 | mA |
| I _{Q_PFM} | Quiescent current in PFM mode | I _{OUT} = 0 | | TBD | 50 | μ A |
| η | Efficiency | V _{IN} = 3.8 V, V _{OUT} = 0.7 V I _{OUT} = 22.5 mA | | 77 (TBC) | | % |
| BYPASS Mode | | | | | | |
| V _{OUT_BP_I} | Auto BYPASS voltage thresholds | Auto BYPASS mode entry V _{IN} - V _{OUT_BP_I} < 2.5 * V _{CTRL} | | 200 | | mV |
| V _{OUT_BP_O} | | Auto BYPASS mode exit V _{IN} - V _{OUT_BP_O} > 2.5 * V _{CTRL} | | 375 | | |
| V _{CTRL_BP_I} | V _{CTRL} BYPASS voltage thresholds | V _{CTRL} BYPASS mode entry V _{CTRL} > V _{CTRL_BP_I} | 1.5 | | | V |
| V _{CTRL_BP_O} | | V _{CTRL} BYPASS mode exit V _{CTRL} < V _{CTRL_BP_O} | | | 1.4 | |
| I _{LIM_BP} | Bypass PMOS current limit | BUCK6_ILIM_BP = 0 | | 1.1 | | A |
| | | BUCK6_ILIM_BP = 1 | | 1.6 | | |
| I _{LIM_BP_ACC} | Bypass PMOS current limit accuracy | | -30 | | +30 | % |
| R _{PMOS_BP} | On resistance BYPASS PMOS | Including pin and routing | | 0.2 | 0.4 | Ω |
| V _{DROPOUT} | Dropout voltage | I _{OUT} = 500 mV | | 56 | | mV |

Note 1 Fixed gain, A_v = 2.5. Analog control voltage range V_{CTRL} = 0.16 V to 0.4 V.

Note 2 Open loop PWM mode. In closed loop configuration switching losses at I_{LOAD} = 0 increase I_{Q_ON}.

Note 3 Programmable in 20 mV steps. Corresponding V_{OUT} range: 0.4 V to 1.15 V.

System PMIC for Dual/Quad-Core Processors

4.14 GPADC

Unless otherwise noted, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{\text{CORE}} = 2.5\text{ V}$.

Table 19: ADC Electrical Characteristics

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|----------------------------|---|--|------|---------|---------|------------------|
| | ADC resolution | Manual conversion | | 12 | | bit |
| V_{ACC} | Absolute accuracy | | 12 | | 15 | mV |
| INL | Integral non-linearity | | | ± 2 | ± 4 | LSB |
| DNL | Differential non-linearity | | | ± 1 | ± 2 | LSB |
| V_{IN} | ADC supply voltage | | | 2.5 | | V |
| $V_{\text{ADC_REF}}$ | ADC reference voltage | | | 2.5 | | V |
| I_{OUT} | ADC operating current | During conversion | | 135 | | μA |
| $I_{\text{PWR_DWN}}$ | Power-down current | | | | 1 | μA |
| f_{CLK} | ADC clock | | | 0.5 | | MHz |
| $t_{\text{AUTO_ZERO}}$ | Auto-zero time | | | 10 | | μs |
| t_{SAMP} | Total sampling time | Including the Auto-Zero time | | 26 | | μs |
| t_{CONV} | Conversion time | | | 24 | | μs |
| t_{TOT} | Total ADC conversion time | | | 50 | | μs |
| R_{S} | Maximum source impedance | Note 1 | | | 200 | $\text{k}\Omega$ |
| R_{INT} | Internal mux resistance | | | 5 | | $\text{k}\Omega$ |
| C_{S} | Internal sampling capacitor | | | 10 | | pF |
| C_{INT} | Total input capacitance | Including parasitic and pad capacitance | | 11 | | pF |
| t_{ACQ} | Acquisition time | $\sim 9T = 9 * (R_{\text{S}} + R_{\text{INT}}) * C_{\text{INT}}$ | | | 20 | μs |
| V_{VBAT} | V_{BAT} voltage range | ADC = $[(V_{\text{BAT}} - 2.5) * 0.5] * 4095$ Gain = 1.25 | 2.5 | | 4.5 | V |
| V_{TEMP} | TEMP1 / TEMP2 voltage range | ADC = $[V_{\text{IN}} / 2.5] * 4095$ gain = 1.0 | 0 | | 2.5 | V |
| V_{VF} | VF voltage range | ADC = $[V_{\text{IN}} / 2.5] * 4095$ Gain = 1.0 | 0 | | 2.5 | V |
| V_{ADCIN} | ADCIN voltage range | ADC = $[V_{\text{IN}} / 2.5] * 4095$ Gain = 1.0 | 0 | | 2.5 | V |
| | Inter-channel isolation | | | 60 | | dB |
| $I_{\text{SRC_ADC}}$ | TEMP / VF / ADCIN current source | | | 50 | | μA |
| $I_{\text{SRC_ADC_ACC}}$ | TEMP / VF / ADCIN current source accuracy | | -2.5 | | +2.5 | % |

Note 1 R_{S} = impedance of the external source sampled by the ADC

System PMIC for Dual/Quad-Core Processors

4.15 Voltage Monitoring

Unless otherwise noted, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 20: Voltage Monitoring

| Parameter | Description | Min | Typ | Max | Unit |
|-----------------|-----------------------------------|----------------------------|----------------------------|----------------------------|------|
| VDD_FAULT_LOWER | VDD_FAULT lower level (Note 1) | 2.4 (Note 2) | 2.9 | 3.15 | V |
| VDD_FAULT_UPPER | VDD_FAULT upper level (Note 1) | VDD_FAULT_LOWER +150 mV | | VDD_FAULT_LOWER +300 mV | V |
| VDD_FAULT_CRIT | VDD_FAULT critical level | 2.2 | VDD_FAULT_LOWER -200 mV | 2.95 | V |
| VDD_MON | VDD_MON level | | VDD_FAULT_UPPER -3 % | | V |

Note 1 The VDD_FAULT threshold levels are configured via the VDD_FAULT_ADJ and VDD_HYST_ADJ control registers.

Note 2 Settings lower than 2.85 V are intended for test purposes only.

4.16 RTC

Unless otherwise noted $T_A = +25\text{ }^{\circ}\text{C}$, $V_{DDRTC} = 1.5\text{ V}$ to 2.75 V .

Table 21: RTC Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--------------------------------|---|-----|-----|-----|------|
| IDDRTC | RTC domain current consumption | From V _{BAT} | | 1.1 | | μA |
| | | From V _{BAT} | | 6 | | |
| t _{BAT} | Backup time | Supercap connected (22 μAh capacity, V _{BAT} = 3.3 V to 2.0 V) | 12 | | | h |

4.17 Crystal Oscillator

Unless otherwise noted $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, $V_{DDRTC} = 1.5\text{ V}$ to 2.75 V .

Table 22: Crystal Oscillator Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|----------------------|------------------------------------|-----|--------|------|------|
| V _{DDRTC} | Supply voltage | | 1.5 | | 2.75 | V |
| f _{OSC} | Oscillator frequency | | | 32.768 | | kHz |
| J _{PER} | Clock jitter | RMS period jitter 10000 samples | | 25 | | ns |
| C _{TAL} | Crystal capacitance | | | 7 | 9 | pF |
| R _{TAL} | Crystal ESR | | | | 100 | kΩ |
| t _{START} | Start-up time | | | 1 | 2 | s |
| I _{DD} | Current consumption | | | 0.5 | | μA |

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4.18 RTC Domain POR

Unless otherwise stated, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 23: RTC Domain POR Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|---------------------|-----------------|-----|-----|-----|---------------|
| V_{POR} | POR threshold | | | 1.2 | | V |
| I_{DD} | Current consumption | From V_{DDHI} | | 0.1 | | μA |

4.19 Backup Battery Charger

Unless otherwise stated $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V .

Table 24: Backup Battery Charger Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|---------------------|---|---|-----|-------------------------|------|---------------|
| I_{SET_BCHG} | Backup battery charging current | $V_{BAT} = 3.6\text{ V}$ $V_{BBAT} = 2.5\text{ V}$ | 100 | | 6000 | μA |
| V_{SET_BCHG} | Charger termination voltage | $V_{BAT} = 3.6\text{ V}$ | 1.8 | | 3.3 | V |
| I_{SHORT} | Backup battery short circuit current | $V_{BBAT} = 0\text{ V}$ | | 9 | | mA |
| C_{OUT} | Stabilization capacitor | | | 470 | | nF |
| C_{OUT_ACC} | Stabilization capacitor accuracy | | -55 | | +35 | % |
| ESR_{COUT} | ESR of capacitor | $f > 1\text{ MHz}$ | | | 0.1 | Ω |
| $I_{THR_LPM_ON}$ | Low-power mode activation current threshold | | | 65 | | μA |
| $V_{THR_LPM_OFF}$ | Low-power mode de-activation voltage | $V_{SET} - V_{BBAT}$ | | 200 | | mV |
| I_Q | Quiescent current from V_{BAT} | $I_{OUT} > 50\text{ }\mu\text{A}$ | | $5.25 + 1.75\% I_{OUT}$ | | μA |
| | | $I_{OUT} < 50\text{ }\mu\text{A}$ | | $5.25 + 1.50\% I_{OUT}$ | | μA |
| V_{BS_HYS} | Bulk-switch hysteresis | $V_{BAT} - V_{BBAT}$ | | 65 | | mV |
| I_{Q_BS} | Bulk-switch quiescent current | $V_{BAT} = 0\text{ V}$ | | 0.35 | | μA |
| | | $V_{BBAT} = 0\text{ V}$ | | 1.5 | | μA |

4.20 Internal Oscillator

Unless otherwise specified, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and $V_{DDCORE} = 2.5\text{ V}$.

Table 25: Internal Oscillator Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|-------------------------------|------------|-----|-----|-----|------|
| f_{OUT} | Internal oscillator frequency | | 5.7 | 6.0 | 6.3 | MHz |
| D | Duty cycle | | 40 | | 60 | % |

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4.21 GPIO

Table 26 GPIO Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|--|---|-------------------------|----------------|-----------------------|------|
| V _{IH} | M_CTL1, M_CTL2, VRFANA_EN, RFBUCK_EN, nVDDFAULT Input high voltage | VDDINT mode | 1.0 | | V _{DDIO} | V |
| | | VDDIO mode | 0.7 * V _{DDIO} | | V _{DDIO} | V |
| V _{IH} | nONKEY, nJIG_ON Input high voltage | VDDINT mode | 1.0 | | V _{BAT} | V |
| | | VDDIO mode | 0.7 * V _{DDIO} | | V _{BAT} | V |
| V _{IH} | TA Input high voltage | VDDINT mode | 1.0 | | 5.5 | V |
| | | VDDIO mode | 0.7 * V _{DDIO} | | 5.5 | V |
| | | RTC mode | 3.0 | | 5.5 | V |
| V _{IL} | M_CTL1, M_CTL2, nONKEY, nJIG_ON, TA, VRFANA_EN, RFBUCK_EN, nVDDFAULT Input low voltage | VDDINT mode | -0.3 | | 0.4 | V |
| | | VDDIO mode | -0.3 | | 0.3*V _{DDIO} | V |
| V _{OH} | nIRQ, nRESET, nVDD_FAULT, OUT1_32K, OUT2_32K Output high voltage | I _{LOAD} = 1 mA | 0.8*V _{DDIO} | | V _{DDIO} | V |
| V _{OL} | nIRQ, nRESET, nVDD_FAULT, OUT1_32K, OUT2_32K Output low voltage | I _{LOAD} = 1 mA | 0 | | 0.3 | V |
| I _{OUT} | Source current capability GPOs, PM IOs | V _{OUT} = V _{DDIO} - 0.5 V | | -1 (Note 1) | | mA |
| I _{IN} | Sink current capability GPOs, PM IOs | V _{OUT} = 0.5V | | 1 | | mA |
| R _{PU_IO} | IO pull-up resistor | V _{DDIO} = 1.5V | 100 | 180 | 300 | kΩ |
| | | V _{DDIO} = 1.8V | 70 | 120 | 170 | |
| | | V _{DDIO} = 3.3V | 25 | 40 | 60 | |
| R _{PU} | Pull-up resistor nONKEY, nJIG_ON | | 140 | 200 | 260 | kΩ |
| f _{MAX} | Maximum IO frequency | Input and output signals | 10 | | | MHz |

Note 1 For V_{DDIO} < 1.5 V the source current is limited to 0.5 mA

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4.22 2-Wire (I²C) Interface

Unless otherwise noted, $T_A = -30\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, and $V_{BAT} = 2.5\text{ V}$ to 5.0 V , $V_{DDIO} = 1.6\text{ V}$ to 3.6 V , $V_{DDINT} = 1.5\text{ V}$.

Table 27: 2-Wire (I²C) Interface Electrical Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------------|---------------------------------------|--|------------------|-----|---------------------|---------------|
| V_{IH} | SCL, SDA Input high voltage | VDDINT mode | 1.0 | | V_{DDIO} | V |
| | | VDDIO mode | $0.7 * V_{DDIO}$ | | V_{DDIO} | V |
| V_{IL} | SCL, SDA Input low voltage | VDDINT mode | -0.3 | | 0.4 | V |
| | | VDDIO mode | | | $0.3 * V_{DDIO}$ | V |
| V_{OL} | SDA Output low voltage | Standard 1 k Ω pull-up to V_{DD_EXT} | 0 | | $0.2 * V_{DD_EXT}$ | V |
| t_{STOP_START} | Bus free time STOP to START | | 1.3 | | | μs |
| C_{LOAD} | Bus line capacitive load | | | | 100 | pF |
| Standard Mode | | | | | | |
| f_{CLK} | CLK clock frequency | | 1 | | 400 | kHz |
| t_{STOP_START} | Bus free time STOP to START | | 1.3 | | | μs |
| t_{START_SETUP} | Start condition set-up time | | 0.6 | | | μs |
| t_{START_HOLD} | Start condition hold time | | 0.6 | | | μs |
| t_{CLK_LO} | CLK low time | | 1.3 | | | μs |
| t_{CLK_HI} | CLK high time | | 0.6 | | | μs |
| t_{RISE_FALL} | 2-wire CLK and DATA rise/fall time | | | | 300 | ns |
| t_{DATA_SETUP} | Data set-up time | | 100 | | | ns |
| t_{DATA_HOLD} | Data hold-time | | 0 | | | ns |
| t_{STOP_SETUP} | Stop condition set-up time | | 0.6 | | | μs |
| High Speed Mode | | | | | | |
| f_{CLK} | CLK clock frequency | | 1 | | 1700 | kHz |
| t_{START_SETUP} | Start condition set-up time | | 160 | | | ns |
| t_{START_HOLD} | Start condition hold time | | 160 | | | ns |
| t_{CLK_LO} | CLK low time | | 160 | | | ns |
| t_{CLK_HI} | CLK high time | | 60 | | | ns |
| $t_{RISE_FALL_CLK}$ | HS-2-WIRE CLK rise/fall time | | | | 40 | ns |
| $t_{RISE_FALL_DATA}$ | HS-2-WIRE DATA rise/fall time | | | | 80 | ns |
| t_{DATA_SETUP} | Data set-up time | | 10 | | | ns |

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| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-------------------------|----------------------------|------------|-----|-----|-----|------|
| t _{DATA_HOLD} | Data hold-time | | 0 | | | ns |
| t _{STOP_SETUP} | Stop condition set-up time | | 16 | | | ns |

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5 PMIC Functional Description

5.1 Switching Regulators (DC/DC Buck Converters)

Table 28: Switching Regulators

| Block | V _{OUT} (V) | I _{OUT} (mA) | External Components | Control (Note 1) |
|---------------------|----------------------|----------------------------|--|-------------------------------|
| Buck1 Dual-phase | 0.6 to 1.4 | PWM: 3000 PFM: 90 | L ₁ /L ₂ = 1.0 μH C _{1OUT} /C _{2OUT} = 22μF | SC/I ² C |
| Buck2 | 0.725 to 2.075 | PWM: 1200 PFM: 90 | L = 2.2 μH C _{OUT} = 10 μF | SC/I ² C |
| Buck3 | 0.725 to 2.075 | PWM: 1000 PFM: 90 | L = 2.2 μH C _{OUT} = 10 μF | SC/I ² C |
| Buck4 | 0.725 to 2.075 | PWM: 600 PFM: 75 | L = 2.2 μH C _{OUT} = 10 μF | SC/I ² C |
| Buck5 | 0.725 to 2.075 | PWM: 600 PFM: 75 | L = 2.2 μH C _{OUT} = 10 μF | I ² C VRFANA_EN |
| Buck6 RF Buck | 0.4 to 3.5 | PWM: 800 PFM: 75 to 125 | L = 0.5 μH or 1 μH C _{OUT} = 4.7μF | I ² C RFBUCK_EN |

Note 1 In this column, SC = PMIC Sequencer Control

5.1.1 Single-Phase Switching Regulators

DC-DC converters Buck2 to Buck5 (see Figure 3) are high-efficiency, synchronous step-down regulators operating at 2 MHz frequency and providing individual output voltages with $\pm 3\%$ accuracy. The default output voltages of these regulators are loaded from OTP and can be programmed in 25 mV steps. The supply current during PWM (synchronous rectification) mode is in the order of 2.2 mA (quiescent current and charge/discharge current) and drops to $< 1\ \mu\text{A}$ when off. Switching frequency is chosen to be high enough to allow the use of a small 2.2 μH inductor.

The operating mode of the buck converter is selected via the buck control register bits. The buck converter can be forced to operate in either Synchronous rectification mode (PWM) or Sleep mode (PFM). Additionally the buck converter has an AUTO mode where it will switch between PWM and PFM depending on the load current. If the application requires a fast transition from PWM to AUTO mode, using 'Automatic forcing to Synchronous mode' (BUCK<x>_MODE = '11') is recommended because it prepares the internal control signal that is subsequently required in AUTO mode.

In Sleep mode, the buck converter works in PFM. An internal zero-crossing comparator is used to time the turn-off of the NFET, thereby removing the need for an external Schottky diode. The total quiescent current for these DC-DC converters in PFM mode is 25 μA.

All DA9066 DC-DC single-phase converters feature programmable (via BUCK<x>_PD_DIS registers) pull-down resistors, which can be either enabled or disabled when the buck converted is powered down.

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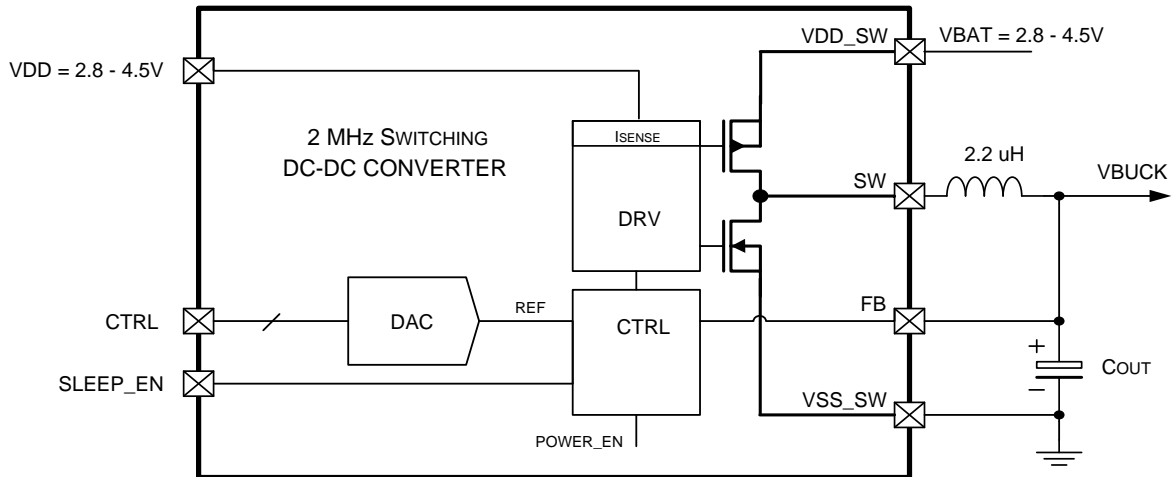


Figure 3: Single-Phase Buck Block Diagram

5.1.2 Multi-Phase Switching Regulators

DC-DC converter Buck1 (see Figure 4) is a dual-phase, high-efficiency, synchronous step-down regulator operating at 3 MHz frequency and providing output voltages with $\pm 3\%$ accuracy. The default output voltage is loaded from OTP and can be programmed in 6.25 mV steps. The dual-phase architecture and the chosen operating frequency allow the use of small 1 μ H inductors, and provide reduced output-voltage ripple even at high current loads up to 3 A.

This DC-DC converter features programmable mode of operation which can be set to either Synchronous rectification mode (PWM) or Sleep mode (PFM). Additionally, this buck can be configured in AUTO mode where it switches between PWM and PFM depending on the load current. The mode transition current threshold is also programmable.

The typical quiescent current of the converter in PFM is 35 μ A.

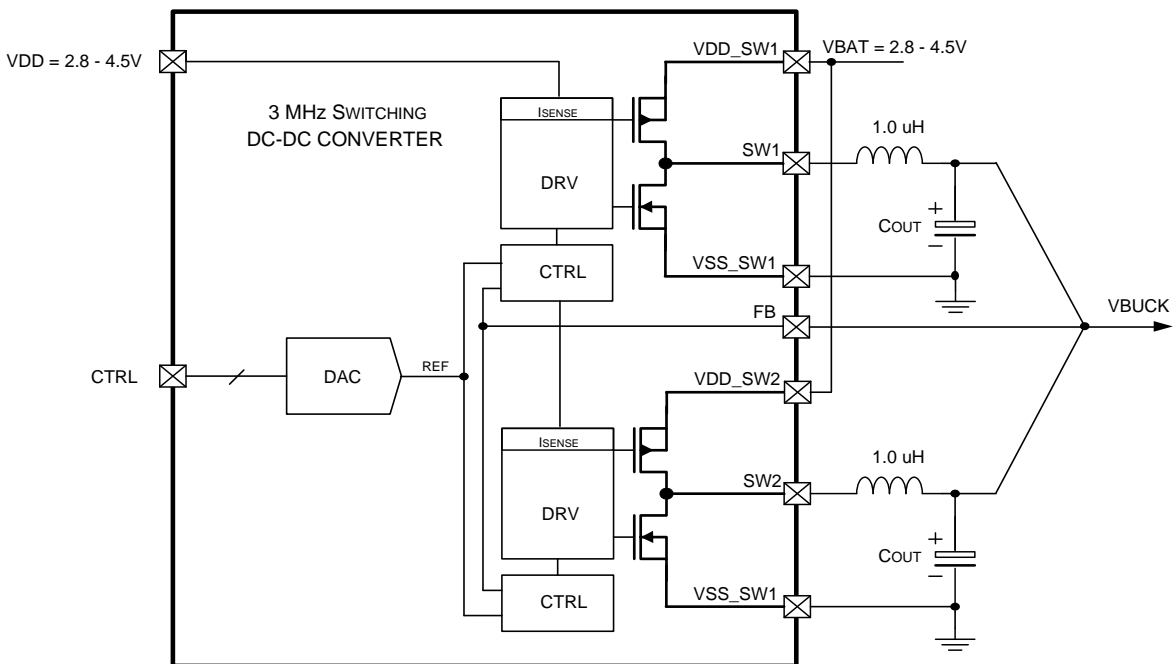


Figure 4: Dual-Phase Buck Block Diagram

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5.1.3 RF Switching Regulators

DC-DC converter Buck6 (see Figure 5) is a high efficiency synchronous step-down regulator operating at 6 MHz or 3 MHz. Its target application is as a power supply for the 3G/3.5G(LTE) RF power amplifiers (PAs) in mobile phone platforms. The regulator has normal mode output voltage range from 0.4 V to 3.5 V (proportional to the input control voltage V_{CTRL}) thus providing dynamically varying power supply to allow maximum efficiency operation of the RF PAs. Additionally, the RF buck features an integrated bypass switch which is automatically turned on when the difference between the input voltage and the target output voltage is less than 200 mV ($V_{IN} < 2.5 * V_{CTRL} + 200$ mV) or when V_{CTRL} is greater than 1.5 V.

The buck architecture and the chosen operating frequency allow the use of small 0.5 μ H or 1 μ H inductors, and provides fast output voltage transient response (typically 5 μ s for a full scale output transition). The operating mode of the buck converter is controlled by the programmable V_{SYNC} and V_{SLEEP} voltage threshold registers. Depending on their setting, the DC-DC converter can be forced to operate in either Synchronous mode or Sleep mode. Additionally, the buck can be configured in AUTO mode where it switches between Synchronous and Sleep mode depending on the load current. This high configurability allows further optimization of the RF system efficiency.

The turning on or off of the regulator is normally controlled via the dedicated $RFBUCK_EN$ input. Optionally, it can also be done via an I²C register write.

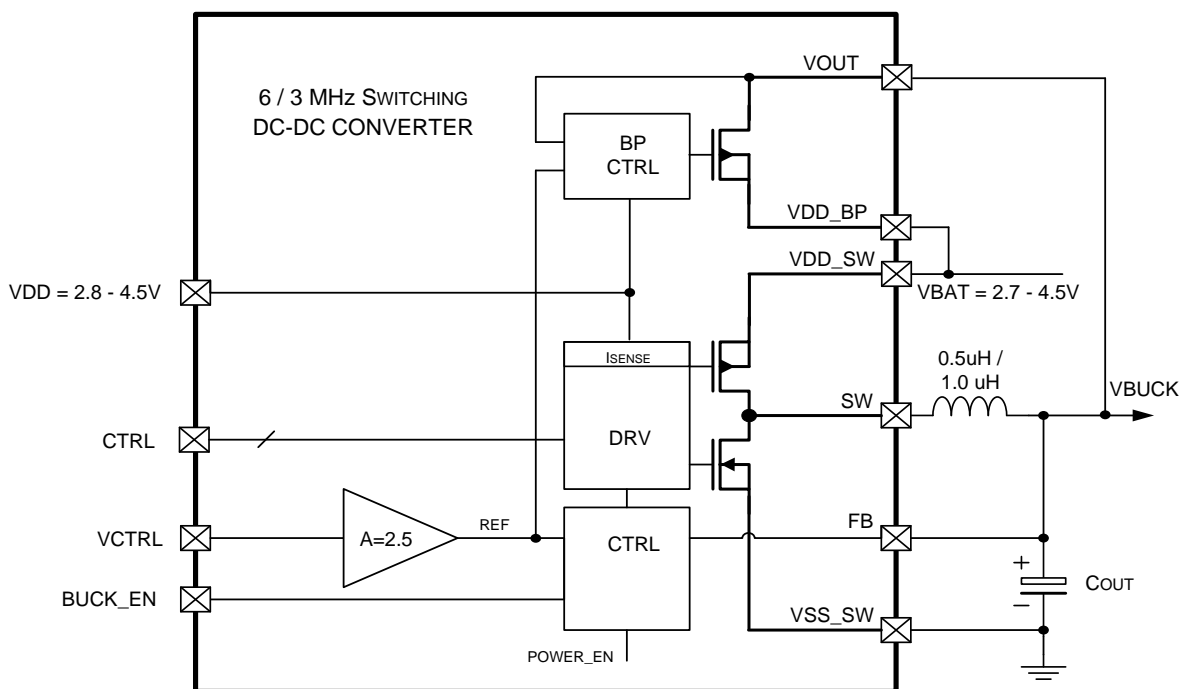


Figure 5: RF Buck Block Diagram

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5.2 Linear Regulators

Seven types ($I_{LOAD} = 150\text{ mA}$, $150\text{ mA [Low Noise]}$, $150\text{ mA [Low Voltage]}$, 200 mA , $200\text{ mA [Low Voltage]}$, 300 mA , and 400 mA) of low dropout regulators are integrated in DA9066, each optimized for performance depending on the most critical parameter of the circuitry supplied. For high performance analog supplies (such as in audio applications) the regulators have been designed to offer high PSRR and low noise. For the digital supplies, PSRR is relaxed saving quiescent current and for the PMIC core/RTC supplies, quiescent current has been optimized as the most important performance parameter.

Table 29: Linear Regulators

| Block | V_{OUT} (V) | I_{OUT} (mA) | Comment | Control (Note 1) |
|----------|---------------|--------------------------|--|---------------------------------|
| LDO1 | 1.0 to 3.1 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV; Low voltage | SC/I ² C |
| LDO2 | 1.0 to 3.1 | 200 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV; Low voltage | SC/I ² C |
| LDO3 | 1.2 to 3.3 | 400 | $C_{OUT} = 2.2\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO4 | 1.2 to 3.3 | 150 | $C_{OUT} = 2.2\ \mu\text{F}$, Step size 50 mV; Low noise | SC/I ² C |
| LDO5 | 1.2 to 3.3 | 200 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO6 | 1.2 to 3.3 | 200 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO7 | 1.2 to 3.3 | 200 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO8 | 1.2 to 3.3 | 200 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO9 | 1.2 to 3.3 | 200 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO10 | 1.2 to 3.3 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO11 | 1.2 to 3.3 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO12 | 1.2 to 3.3 | 300 | $C_{OUT} = 2.2\ \mu\text{F}$, Step size 50 mV | SC/I ² C |
| LDO13 | 1.2 to 3.3 | 300 | $C_{OUT} = 2.2\ \mu\text{F}$, Step size 50 mV | I ² C |
| LDO14 | 1.2 to 3.3 | 300 | $C_{OUT} = 2.2\ \mu\text{F}$, Step size 50 mV | I ² C |
| LDO15 | 1.2 to 3.3 | 400 | $C_{OUT} = 2.2\ \mu\text{F}$, Step size 50 mV | I ² C |
| LDO16 | 1.2 to 3.3 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | I ² C |
| LDO17 | 1.2 to 3.3 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | I ² C |
| LDO18 | 1.2 to 3.3 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | I ² C / VRFANA_EN |
| LDO19 | 1.2 to 3.3 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | I ² C |
| LDO20 | 1.2 to 3.3 | 150 | $C_{OUT} = 1.0\ \mu\text{F}$, Step size 50 mV | I ² C |
| BBAT_CHG | 1.8 to 3.3 | 0.1 to 6 programmable | Programmable output voltage CC/CV regulation loop | I ² C |

Note 1 SC is PMIC sequence control

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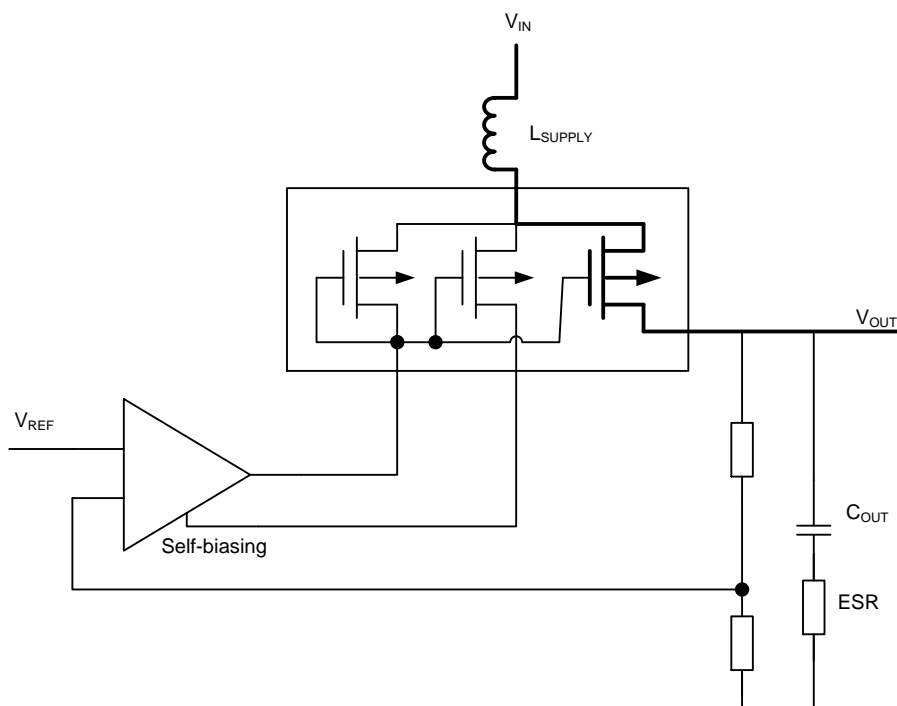


Figure 6: SmartMirror LDO

All regulators employ Dialog Semiconductor's [SmartMirror](#) dynamic biasing technology which guarantees a high phase margin within the regulator control loop and has been designed to offer stable performance with small output capacitances over a wide range of output currents. The circuit technique offers significantly higher gain bandwidth performance than conventional designs, enabling higher power supply rejection performance at higher frequencies. PSRR is also maintained across the full operating current range. However, quiescent current consumption is scaled to demand, giving improved efficiency when current demand is low.

All regulator output voltages are fully programmable via the control interface allowing optimization of the complete system for maximum performance and power efficiency.

The default voltage of all the LDOs under sequencer control (LDO1 to LDO12) is one time programmable (OTP). The voltages can be changed via the I²C interface.

All DA9066 LDO regulators feature programmable (via LDO<x>_PD_DIS registers) pull-down resistors, which can be enabled or disabled when the regulator is powered down.

The input supplies for the DA9066 LDOs are organized in the following groups:

- VDD_LDO_A = LDO12 and LDO13
- VDD_LDO_B = LDO10 and LDO11
- VDD_LDO_C = LDO19 and LDO20
- VDD_LDO_D = LDO14
- VDD_LDO_E = LDO3
- VDD_LDO_F = LDO15
- VDD_LDO_G = LDO16, LDO17, and LDO18
- VDD_LDO_H = LDO4, LDO5, and LDO6
- VDD_LDO_J = LDO7, LDO8, and LDO9
- VDD_LDO_LV = LDO1 and LDO2

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5.3 General Purpose ADC

Table 30: General Purpose ADC

| Channel No. | Channel Name | Nominal Gain (V/V) | Measurement Range (V) | Description |
|-------------|--------------|--------------------|-------------------------|---|
| 0 | VBAT | 1.25 | 2.5 to V _{BAT} | Battery voltage |
| 1 | TEMP1 | 1.0 | 0 to 2.5 | Battery NTC voltage (optional current source) |
| 2 | TEMP2 | 1.0 | 0 to 2.5 | Battery NTC voltage (optional current source) |
| 3 | VF | 1.0 | 0 to 2.5 | Battery detection voltage (optional current source) |
| 4 | ADC_IN | 1.0 | 0 to 2.5 | HW version ID detection voltage (optional current source) |
| 5 | TJUNC | 3.0 | 0 to 0.833 | Internal temperature sensor voltage |

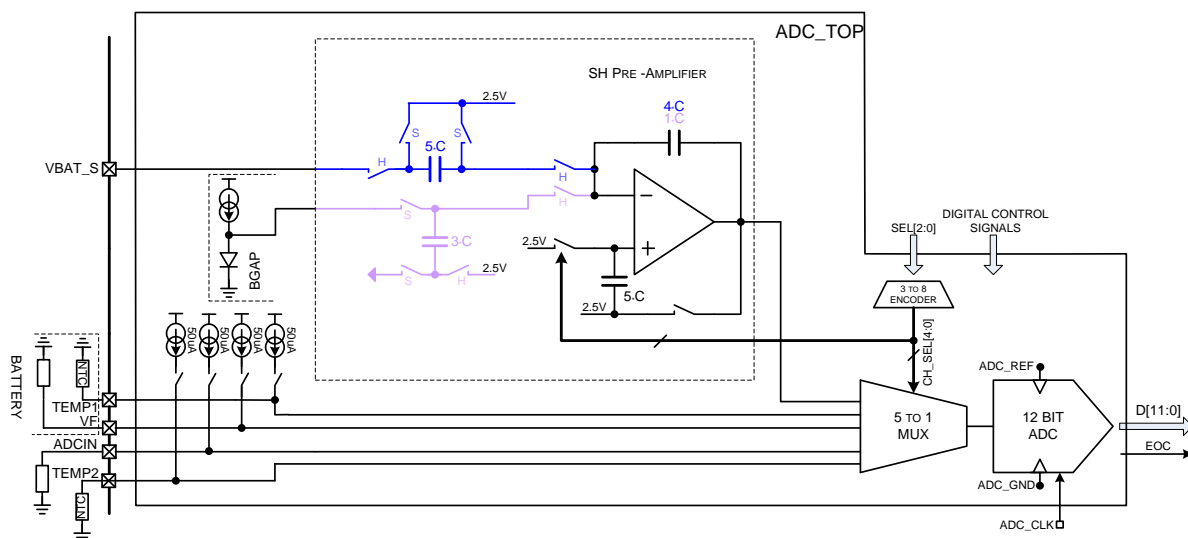


Figure 7: GPADC Block Diagram

On DA9066, the A to D conversion is performed by a switched capacitor (SC) successive approximation register (SAR) ADC. The actual ADC is preceded by a 5:1 input multiplexer that controls the channel selection, routes the appropriate input signal to the SC circuit and ensures the inter-channel isolation. The input voltage range of the SC ADC core is from 0 V to 2.5 V, hence any input signal outside this range has to be pre-scaled before being routed to the input of the converter. The ADC core is supplied from the internal 2.5 V V_{DDCORE} rail, which is also used to provide the positive reference voltage for the ADC. A dedicated, quiet, VSS signal is used for the negative reference voltage of the SC circuit.

The implemented track and hold circuit ensures a stable voltage on the input of the SC ADC during the conversion. Figure 8 shows the polarity and the timing of the external and the internal signals controlling the track and hold sequence of the converter. The clock ($f_{CLK} = 0.5$ MHz) and the enable signal (EN) are provided by the main PM control logic while all the other signals are internally generated. The timing diagram illustrates a tracking period of 13 clock cycles, (26 μ s inclusive of 10 μ s auto-zero time) and a conversion period of 24 μ s, hence a total ADC conversion cycle of 50 μ s.

The end of the conversion is flagged by the EOC signal which indicates the availability of the data bits D[11:0]. Once the PM controller has read the result, it de-asserts the EN signal which terminates the current conversion cycle. A new cycle can be started on the following rising edge of the clock.

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The channel selection control signals SEL[2:0] must be present prior to or at least coincident with the assertion of the ADC enable signal. This is to ensure that the tracking period is not affected by late assertion of the external digital controls. For the same reason, in case of dynamic control of the TEMP and VF current sources they have to be enabled (turned on) at least 100 μs before the next NTC, or respectively VF, measurement.

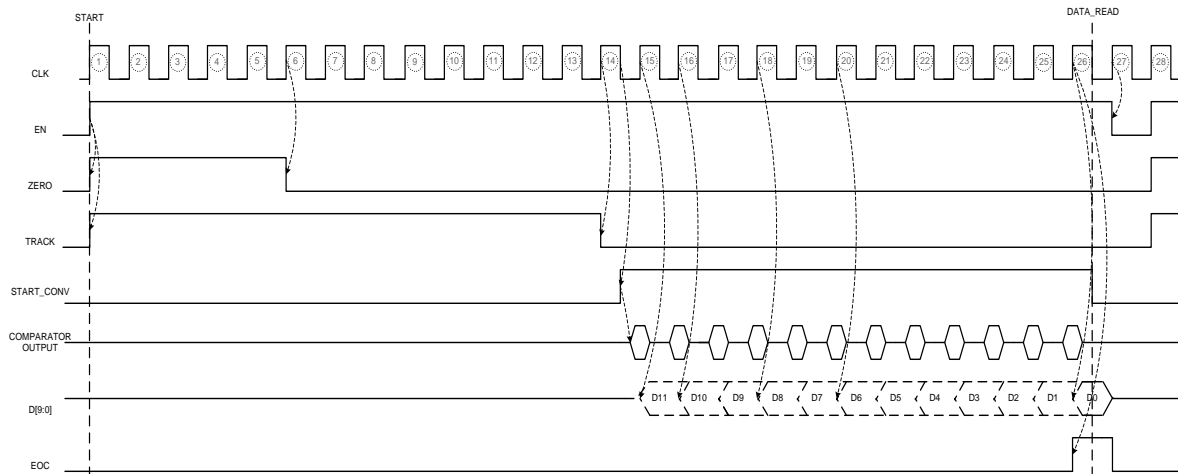


Figure 8: Track and Hold Sequence Timing Diagram

5.3.1 ADC Measurement Modes

5.3.1.1 Manual Conversion Mode

The manual ADC measurements are initiated by host writes to the MAN_CONV register bit. The ADC powers up and performs a single conversion of the selected (via MUX_SEL) input signal. After storing the 12-bit result, the main PM controller powers down the ADC and clears the MAN_CONV register.

5.3.1.2 Automatic Conversion Mode

The automatic conversion mode is controlled by a dedicated automatic measurement scheduler that is part of the main PM controller. The automatic mode allows monitoring of the system voltage V_{BAT} (A0), the battery temperature TEMP1 (A1), an additional temperature TEMP2 (A2), and VF detection (A3) input.

The automatic sequence consists of 10 slots, each with fixed 200 μs duration, see Figure 9.

| | | | | | | | | | | |
|----------|----|---|---|----|----|---|----|----|---|----|
| Slot No. | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
| | A0 | R | M | A3 | A1 | M | A4 | A2 | M | A5 |

- A0 Automatic Measurement of VBAT_S Input
- A1 Automatic Measurement of TEMP1 Input
- A2 Automatic Measurement of TEMP2 Input
- A3 Automatic Measurements of VF Input
- A4 Automatic Measurements of ADCIN Channel
- A5 Automatic Measurement of TJUNC (Internal Junction Temperature)
- M Slot Available for Manual Measurement
- R Reserved Slot

Figure 9: Sequence of Automatic ADC Measurements

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5.3.2 ADC Measurement Channels

5.3.2.1 A0 V_{BAT} Voltage Measurement

This ADC channel is used to monitor the voltage of the main battery. As the voltage level on this input can be higher than 2.5 V, the signal is processed by the pre-amplifier prior to the actual A-to-D conversion. The input VBAT_S is star (Kelvin) connected to the battery. An external RC filter with a cutoff frequency of 45 Hz to 100 Hz (such as R = 100 kΩ and C = 220 nF) is recommended.

V_{BAT} is measured and compared with the VBAT_MON threshold. If the reading is below this level for three consecutive readings an E_VDD_LOW event is generated. After nIRQ assertion, the automatic measurement of channel A0 is paused for reading. The host has to clear the associated event flag (the event causing value is kept inside the result register) to re-enable the supervision of V_{BAT}.

5.3.2.2 A1 TEMP1, A2 TEMP2, A3 VF, A4 ADCIN Voltage Measurements

These channels are included in the automatic measurement sequence and when enabled can provide general purpose voltage monitoring of the corresponding inputs.

Battery temperature is measured on channel A1 and compared with two temperature thresholds, TEMP1_HIGHP and TEMP1_LOW. If three consecutive TEMP1 readings are greater than TEMP1_HIGHP or less than TEMP1_LOW, the event flag is set and E_TEMP1 interrupt is generated. The generation of this interrupt can be masked by M_TEMP1.

The TEMP2 input can be used for monitoring of a different temperature point in the system. The measured value on channel A2 is compared with two temperature thresholds, TEMP2_HIGHP and TEMP2_LOW. If three consecutive TEMP2 readings are greater than TEMP2_HIGHP or less than TEMP2_LOW, the event flag is set and E_TEMP2 interrupt is generated. The generation of this interrupt can be masked by M_TEMP2.

The VF channel is used for battery detection and needs to detect whether a 1.5 kΩ, 4.7 kΩ, 10 kΩ, or 27 kΩ resistor is connected to GND. The VF measured value is compared against two threshold levels, VF_HIGH and VF_LOW. If three consecutive VF readings are greater than VF_HIGH or less than VF_LOW, the corresponding event flag is set and E_VF interrupt is generated. The generation of this interrupt can be masked by M_VF. The VF_HIGH threshold comparison can be used for battery removal detection.

The ADCIN channel is a general purpose measurement channel which is typically used for hardware ID detection.

In addition, the TEMP1/2, VF, and ADCIN channels can also be used for resistance measurements. The external resistor to be measured should be connected to the input pin and the internal 50 μA current source in the ADC should be enabled. The operation of the 50 μA current source is controlled by the TEMP1_ISRC_EN, TEMP2_ISRC_EN, VF_ISR_EN, and ADCIN_ISRC_EN register bits.

When the temperature channels measurements are enabled in the Auto mode sequence and TEMP1/2_ISRC_EN = 0, the current source is dynamically switched off at the end of the conversion and switched back on one slot prior to the next TEMP1/2 measurement. This operation reduces the current consumption but requires extra time to charge the external capacitance on the input node. When TEMP1/2_ISRC_EN = 1 in Auto mode the current source is turned permanently on.

When the VF and ADCIN measurements are enabled in the Auto mode sequence, and the corresponding ISRC_EN = 0, the current source is turned off. When the ISRC_EN = 1 the respective internal current source is dynamically switched on and off with the same timing as for the TEMP1/2 channels.

During manual measurements (the automatic measurement of the respective channel has been disabled) all channels have the same current source control. This means that when <xxx>_ISRC_EN = 0 the internal 50 μA source is off and when <xxx>_ISRC_EN = 1 it is permanently on.

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5.4 Voltage and Temperature Monitoring

5.4.1 System Voltage Monitoring

The supervision of the system supply, V_{BAT} , is done by four comparators. One comparator monitors the $V_{DD_FAULT_UPPER}$ threshold (indicating a valid battery/external supply) and the other three monitor the under-voltage levels: V_{DD_MON} , $V_{DD_FAULT_LOWER}$ (fault condition indicator), and $V_{DD_FAULT_CRIT}$. During normal operation (not in RTC mode), the V_{BAT} monitoring circuit is always on and as such is designed to have low current consumption.

When the V_{BAT} voltage drops below the V_{DD_MON} level (typically 3.1 V) an event and associated interrupt is generated. This is an indication that the battery is discharging and approaching a fault condition level. When the V_{BAT} voltage drops below the $V_{DD_FAULT_LOWER}$ level (typically 2.9 V), the $nRESET$ output signal is asserted after a 150 ms debounce time. This is normally the case when the main battery is being slowly discharged (typical operation).

When the battery is removed and the V_{BAT} discharge is significantly faster, $nRESET$ is asserted 64 μs after the system supply falls below the $V_{DD_FAULT_CRIT}$ level (typically 2.7 V).

After the $nRESET$ assertion the PMIC starts a controlled shutdown sequence that turns off all system supplies. At the end of the sequence the internal PM controller is reset and the PMIC will not automatically boot next time the system supply is above the $V_{DD_FAULT_UPPER}$ threshold, unless the $AUTO_BOOT$ bit is set.

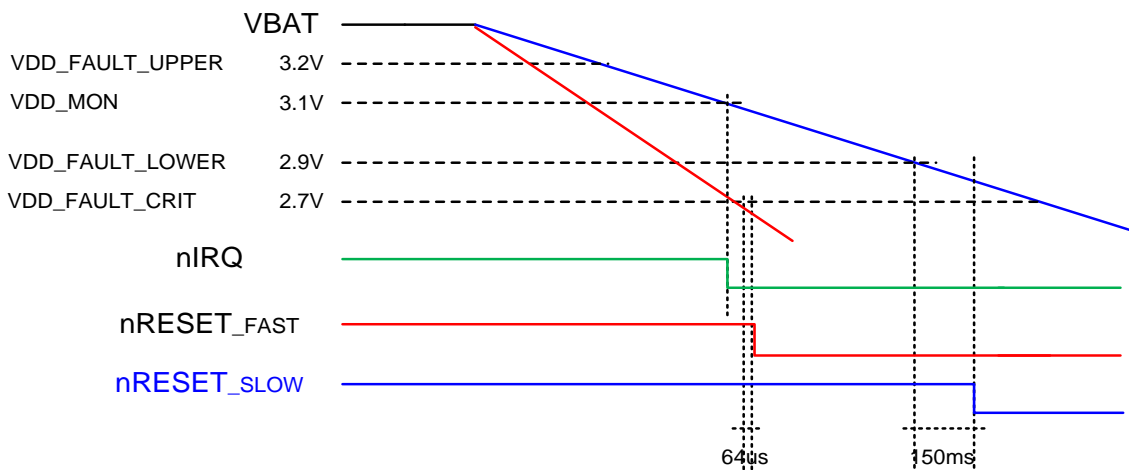


Figure 10: System Voltage Monitoring

5.4.2 Temperature Monitoring

In order to protect DA9066 from damage caused by excessive power dissipation, the internal temperature monitor circuit performs continuous (except for the RTC mode of operation) monitoring of the internal junction temperature.

DA9066 has a critical over-temperature threshold (T_{CRIT}) of about 140 °C.

The output of the internal temperature comparator is monitored by the digital control logic. The control logic shuts down DA9066 (transition to RESET state) and asserts $TEMP_OVER$ in the $FAULT_LOG$ register when three consecutive measurements indicate that the internal junction temperature exceeds the over temperature threshold ($T_{JUNC} > 140$ °C). The fault condition remains asserted until the temperature drops below the safe temperature threshold ($T_{JUNC} < T_{CRIT} - 10$ °C).

By using the junction temperature channel (A5) of the general purpose ADC the host can measure the exact die temperature.

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6 RTC Domain

The RTC mode of operation is an ultra-low power mode in which all blocks, except for the RTC block, are powered down. The active RTC block maintains the RTC clock counter and alarm functions. The RTC block is powered from a dedicated supply rail VDDRTC. The RTC circuit includes the following functional blocks:

- 32 kHz oscillator providing the clock for the RTC counter and the RTC control logic
- RTC counter keeping track of the real time
- Control logic managing the alarm, wake up and enable/disable functions and the proper transfer of control and data from/to the main PMIC logic
- POR circuit
- Auxiliary logic and level shifters

DA9066 can go to RTC mode of operation as described below:

- When the VBBAT (the backup battery supply) is the only available voltage source in the system (no main battery), DA9066 enters RTC mode as all the other supply domains are down. The transfer of control from the main PM control logic to the RTC control logic and the isolation of the interface signals are triggered by the assertion of the main POR signal ($V_{DDCORE} < 2\text{ V}$).
- If the RTC_AUTO_EN register bit is set, PM controller transition to POWERDOWN mode (sequencer slot ID0) automatically forces DA9066 in RTC mode even in the presence of a valid VBAT supply.

The following conditions can wake up DA9066 from RTC mode:

- Re-insertion of the system supply V_{BAT} followed by the assertion of nONKEY, TA or nJIG_ON
- Alarm or tick event in the presence of a valid V_{BAT} supply ($V_{BAT} > V_{BBAT} + 65\text{ mV}$). If V_{BAT} does not fulfill this condition, DA9066 does not wakeup but the alarm event is memorized.

6.1 Crystal Oscillator

The 32 kHz clock on DA9066 is generated by an ultra-low power oscillator that works with an external piezoelectric crystal at 32.768 kHz. The start-up time of the oscillator is typically 0.5 s to 1 s over the VDDRTC supply voltage range. When XTAL_EN = 0, the 32 kHz oscillator is disabled and the clock multiplexer CLK MUX is configured to route in the external clock signal provided at the XOUT port (On DA9066 this feature is only used during the production test of the PMIC).

To achieve the desired crystal frequency, DA9066 requires external capacitors to ground on each of the crystal pins. Depending on the parasitic capacitance of the board, the value of these capacitors varies between 5 pF and 10 pF. When a crystal is not mounted, the XTAL pins that are not driven (external clock signal in bypass mode) should be grounded. The oscillator inputs are designed to withstand a leakage current equivalent at least to the leakage of a 10 M Ω resistor connected between the XTAL pin and any signal level between V_{DDCORE} and GND.

The 32 kHz clock signal is made available at the OUT1_32K and OUT2_32K pins. The output clock buffers can be initially enabled/disabled in the OTP configuration. Additionally, the OUT2_32K can be completely disabled via the control bit settings.

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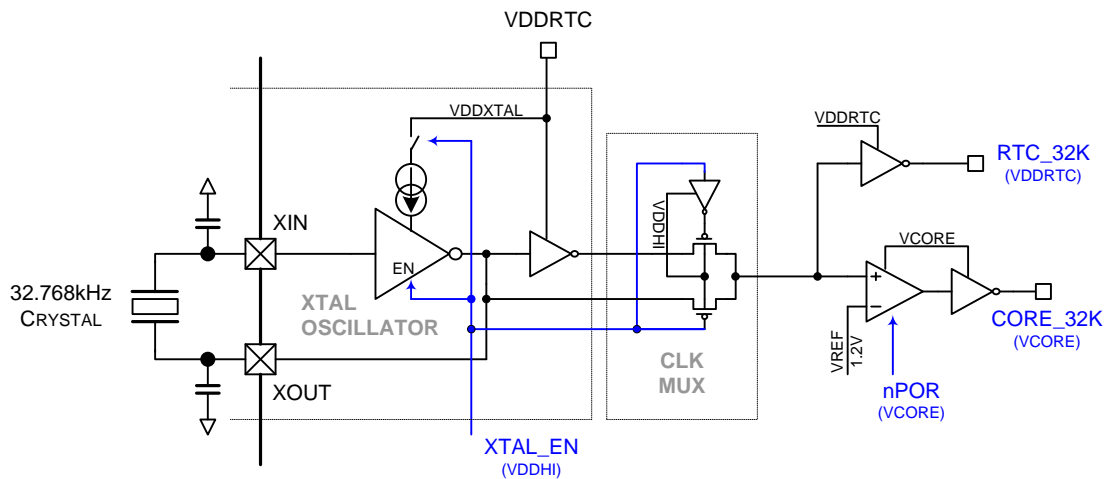


Figure 11: 32 kHz Crystal Oscillator

6.2 RTC Domain POR

The POR circuit ensures the proper initialization of the RTC domain counters and control logic. The circuit is supplied from V_{DDRTC} and is designed to have very low current consumption.

6.3 RTC Counters and Alarms

DA9066 features a calendar counter with an associated alarm register. When set, the calendar alarm generates an IRQ and a wake-up event on the expiry of the calendar counter.

The RTC calendar counter counts the number of 32 kHz clock periods and provides a sec, min, hrs, day, month and year outputs. Year 0 corresponds to 2000. The counter can count up to 63 years. The value of the RTC calendar can be read or written to via the power manager interface. A read of the seconds register (address 0x08A) latches the current RTC calendar count into the 0x08B to 0x08F registers (coherent for approximately 0.5 sec). Receiving an updated calendar value requires a read of register 0x08A.

NOTE

The reading of the calendar registers in page mode must commence at address 0x08A.

DA9066 has an alarm register containing sec, min, hrs, day, month, and year. When the RTC calendar counter register value equals the value set in the calendar alarm register, an IRQ event is generated and DA9066 wakes up from POWERDOWN mode and, given that $V_{BAT} > V_{BBAT}$, also from RTC mode. The trigger also sets a bit in the event register to notify that an alarm has occurred. The alarm can alternatively be asserted from a periodic tick signal that, depending on control TICK_TYPE, is either asserted every second or minute. The power manager registers ALARM_ON and TICK_ON enable/disable the alarm/tick.

NOTE

Values written into the RTC calendar and alarm registers have to be within the allowed value range (see register description).

The RTC calendar counter is reset to zero when the V_{DDRTC} nPOR is asserted. The power manager register bit MONITOR is set to 0 each time the VRTC domain goes through a power-down cycle. When setting the time and date the software has to set the MONITOR bit to 1, in order to enable/re-enable the RTC supply generator and the RTC domain digital block (counters and control logic). Setting MONITOR = 1 also allows the detection of a subsequent loss of the clock.

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6.4 Backup Battery Charger

DA9066 provides a backup battery (BBAT) charger for charging of Lithium-Manganese coin cell batteries and super capacitors. This charger features both constant current (CC) and constant voltage (CV) charging modes. The transition between the modes is automatic as the battery voltage approaches the target voltage level. The termination voltage is programmable in 100 mV steps from 1.8 V to 3.3 V via the BBCHG_VSET control register.

The charging current can be set by the BBCHG_ISET register from 0.1 mA to 6 mA in 100 μ A steps up to 1 mA, and in 1 mA steps in the higher range. The PMIC logic controls the enable/disable of the charger via the BBCHG_EN register bit. The BBAT charger will automatically switch itself off when it reaches the programmed termination voltage. To conserve the charge in the super-capacitor/backup battery the whole RTC domain is then supplied from VBAT. The BBAT charger is periodically restarted by software control.

The automatic termination can be permanently disabled by setting the BBAT_ILIM_IGNORE register bit to 1.

The programming of the BBAT_MCTL[3:0] control registers determines whether the BBAT charger stays on or is turned off in the four different power states defined by the MCTL[2:1] inputs.

The charger also switches off automatically during NO-POWER and RTC mode.

The BBAT charger is powered from the main supply VBAT. To prevent this rail being back-powered from the backup battery (when no main supply is present), the bulk connection of the output P-FET power device is dynamically controlled by a dedicated bulk-switch comparator. When the comparator detects that the backup battery voltage V_{BBAT} is greater than the main supply, it turns off the output pass transistor and connects its bulk to V_{BBAT} . The output PMOS transistor is re-enabled and its bulk switched to V_{BAT} when the comparator detects $V_{BAT} > V_{BBAT} + 65$ mV. Since the bulk-switch comparator is always on, it has been designed to have an extremely low quiescent current (especially when switched to the backup battery side).

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7 Clock Generation

DA9066 features two internal oscillators providing the master clocks used for the generation of all the frequencies and clock phases required for the proper operation of the device. DA9066 integrates one low frequency oscillator (the 32 kHz crystal oscillator described in Section 6.1) and one high frequency (6 MHz) oscillator.

The ultra-low power 32 kHz oscillator provides the clock for the RTC domain and the output clock buffer OUT_32K. The main 6 MHz oscillator generates the clock for all the other DA9066 blocks.

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8 PM Digital Control

8.1 DA9066 Operating Modes

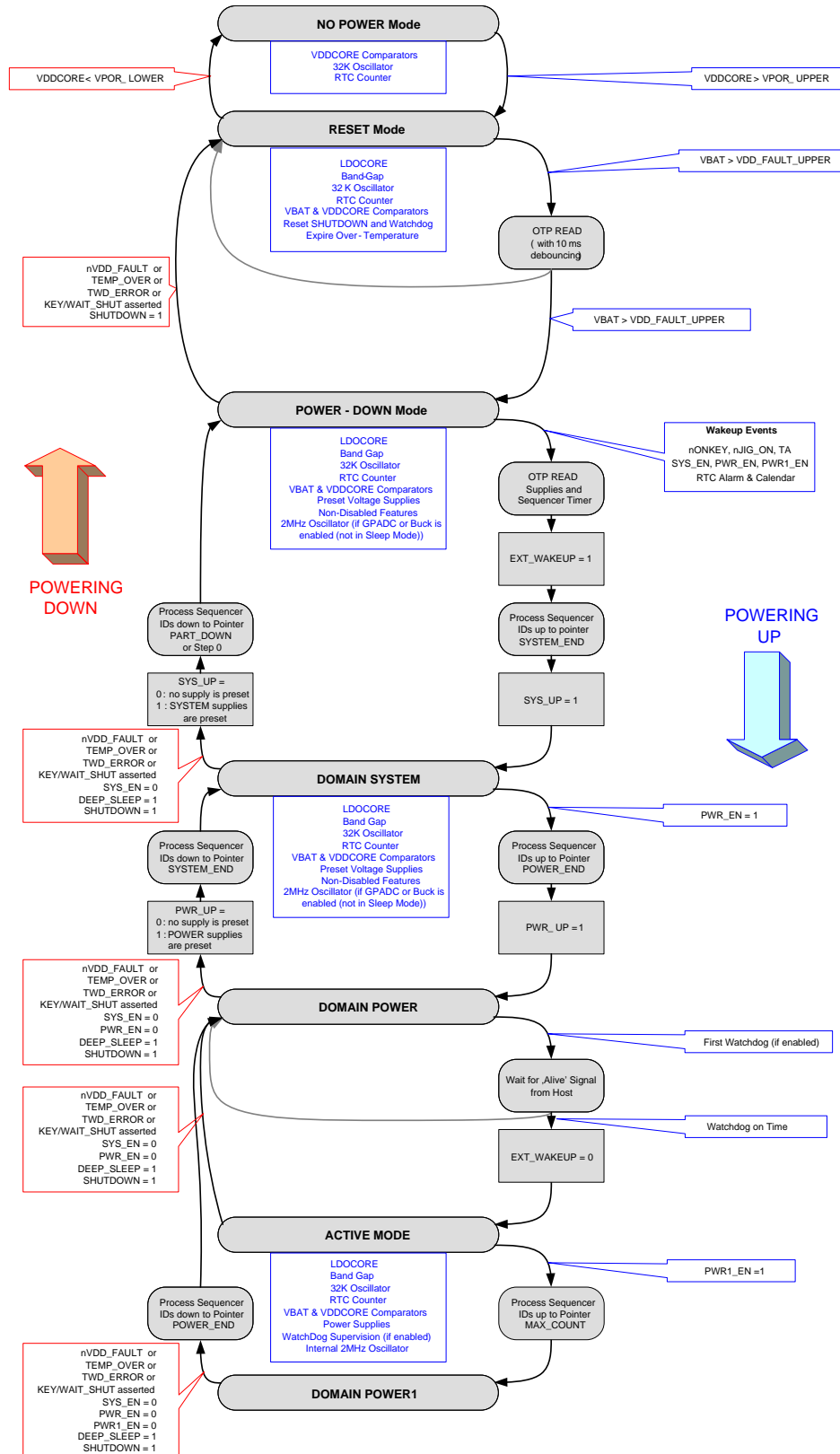


Figure 12: Operating Modes

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8.1.1 NO-POWER Mode

NO-POWER mode is the initial state DA9066 enters when being powered up for the first time (cold start). When active, DA9066 enters NO-POWER mode when a low V_{BAT} supply voltage causes the internally regulated PMIC supply (V_{DDCORE}) to drop below the V_{POR_LOWER} threshold (for example during continued discharge of main battery). Under these conditions, an internal power-on-reset (nPOR) is asserted and the main DA9066 digital controller is reset.

When DA9066 detects a good main battery supply ($V_{BAT} > 2.5\text{ V}$) which allows V_{DDCORE} to rise above V_{POR_UPPER} , the PMIC progresses to RESET mode.

8.1.2 RESET Mode

DA9066 is in RESET mode whenever a complete application reset is required. RESET mode is entered after a cold start when progressing from NO-POWER mode, or it can be forced by the user via a long press of nONKEY (control bit AUTO_BOOT = 0), or from the host processor by assertion of the SHUTDOWN register bit. DA9066 also enters RESET mode after error detection. The following error conditions force RESET mode:

- a WATCHDOG write from the host outside of the watchdog time window (if WD was enabled)
- an under-voltage detection at V_{BAT} ($V_{BAT} < V_{DD_FAULT_LOWER}$ (debounced) or $V_{BAT} < V_{DD_FAULT_CRIT}$)
- an internal die over-temperature detection

In order to allow the host to determine the reason for the RESET a FAULT_LOG register records the cause. The processor resets this register by writing 11111111 via the power manager bus. RESET conditions like the SHUTDOWN via register bit, WATCHDOG and over-temperature errors expire automatically and DA9066 progresses from RESET to POWERDOWN mode in case of a valid V_{BAT} supply. If the RESET was initiated by a hardware reset (nONKEY long press), a 500 ms time out is inserted before the PMIC attempts to power up again.

When returning from POWERDOWN mode, the RESET mode is entered after the complete power down of the SYSTEM domain (sequencer position 0). RESET is a low-power state with LDOCORE, RTC counter, over-temperature monitoring, and V_{BAT} monitoring being the only active blocks. All other DA9066 supplies are automatically disabled to avoid battery discharge. The nRESET port is always asserted low when DA9066 is in RESET mode.

Apart from E_ALARM and E_TICK, all asserted events are automatically cleared on entry to RESET mode. The DA9066 register configuration will be re-loaded from OTP when leaving RESET mode.

8.1.3 POWERDOWN Mode

DA9066 is in POWERDOWN mode whenever the power domain SYSTEM is disabled (even partially). This mode is entered when progressing from RESET mode or by returning from ACTIVE mode. A return from ACTIVE mode is initiated by low-power mode instructions from the host (releasing SYS_EN register bit or asserting register bit DEEP_SLEEP) or it occurs as an interim state during application shutdown to RESET mode.

During POWERDOWN mode, LDOCORE, the nONKEY, nJIG_ON, TA inputs, and the RTC counter are all active. Dedicated power supplies can also be kept enabled during POWERDOWN mode if they have been pre-configured during ACTIVE mode with power down voltages. In addition, GPIO ports, GPADC, backup battery charger, and the control interface keep on running if not disabled via register PD_DIS. Disabling blocks during POWERDOWN mode saves quiescent current, especially if all the blocks that require the main clock are disabled. If the host no longer communicates during POWERDOWN mode, the control interface can be temporarily disabled (controls PM-IF_PD). The internal oscillator (6 MHz) will only run on demand (to support the GPADC or enabled bucks that are not forced to PFM mode). The application supervision by WATCHDOG timer is discontinued in POWERDOWN mode.

After the next wake-up event, if the OTP_READ_EN bit is set, all supplies are re-configured with their default voltage values from OTP and the sequencer timers are set to their default OTP values.

When the return to POWERDOWN mode was initiated by a DEEP_SLEEP command, the sequencer pointer is stopped at position PART_DOWN inside the domain SYSTEM, which will result in a partial

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POWERDOWN mode. If the POWERDOWN mode was caused by releasing SYS_EN, the sequencer pointer is located at position 0, which allows default enabling or disabling of supplies (beside LDOCORE).

8.1.4 ACTIVE Mode

DA9066 is in ACTIVE mode after the host processor has performed at least one initial alive watchdog write (or alternatively an initial assertion of the KEEP_ACT pin) inside the target time window. This watchdog condition can be disabled via setting TWDSSCALE to zero.

In ACTIVE mode, in addition to the core PMIC blocks (LDOCORE, RTC counter, internal oscillator), a set of supplies and peripheral features like the general purpose ADC (GPADC) and back-up battery charger are usually enabled. Status information can be read from the host processor via the power manager interface and DA9066 can flag interrupt requests to the host via a dedicated interrupt port (nIRQ). Temperature and voltages (internal to DA9066) can be monitored and any fault conditions flagged to the host processor.

8.2 System Monitor (Watchdog)

After powering up the POWER domain, DA9066 can initiate an initial watchdog monitor function (if this feature is enabled via control TWDSSCALE). If the watchdog is enabled, the host processor has to write a logic 1 within a configured t_{WDMAX} time to bit WATCHDOG in DA9066 register 0x00E, to indicate that it is alive after SYS_UP was asserted. If the host does not write 1 to the WATCHDOG bit within the t_{WDMAX} time, DA9066 asserts TWD_ERROR in the FAULT_LOG register and powers down to RESET mode.

After this first write to the watchdog, the host must write to the WATCHDOG bit within a configured time window or DA9066 will assert TWD_ERROR in the FAULT_LOG register and power down to RESET mode. The watchdog TWD_ERROR error condition is cleared when entering the RESET mode. The time window has a minimum t_{WDMIN} fixed at 256 ms and a maximum t_{WDMAX} of nominally 2.048 s. The t_{WDMAX} value can be extended by multiplying the nominal t_{WDMAX} by the register bits TWDSSCALE. TWDSSCALE is used to extend the t_{WDMAX} time by x1, x2, x4, x8, x16, x32, or x64.

Changing the maximum value of the time window or the state of KEEPACT_EN bit requires TWDSSCALE to be zero (WATCHDOG disabled) for a minimum of 100 μ s. This requires the host to first switch off the watchdog for at least 150 μ s before configuring it with a new timing window scale value (TWDSSCALE).

The WATCHDOG bit can also be asserted from the host via hardware by asserting KEEP_ACT. This is a mode selected via control KEEPACT_EN, which disables the control of the WATCHDOG bit via the host control interface. The in-time assertion of nONKEY then also enables DA9066 to transfer into ACTIVE mode. Once in the ACTIVE mode, DA9066 continues to monitor the system unless it is disabled via setting TWDSSCALE to zero. If the WATCHDOG register bit is set to a 1 within the time window, the watchdog monitor resets the timer, sets the WATCHDOG bit back to zero (bit is always read as zero), and waits for the next watchdog signal.

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8.3 Power Manager/System I/Os

DA9066 features several unidirectional, dedicated power management I/Os, which are configured in hardware as either inputs or outputs.

8.3.1 Input Ports – nONKEY, TA, nJIG_ON, M_CTL1, M_CTL2, TP

| PAD Name | Type | PAD Description | Configuration |
|-----------|------|--|--|
| nONKEY | DI | ON/OFF key / hardware watchdog input Active low input | Internal 200 kΩ pull up to VBAT V _{DDIO} /V _{DDINT} supply rail |
| TA | DI | TA wakeup input Active high input | 5.5 V tolerant input V _{DDIO} /V _{DDINT} supply rail |
| nJIG_ON | DI | JTAG wakeup input Active low input | Internal 200 kΩ pullup to VBAT V _{DDIO} /V _{DDINT} supply rail |
| M_CTL1 | DI | Mode control input 1 Active high input | V _{DDIO} /V _{DDINT} supply rail |
| M_CTL2 | DI | Mode control input 2 Active high input | V _{DDIO} /V _{DDINT} supply rail |
| VRFANA_EN | DI | ON/OFF control input for the RFANA supplies (Buck5 and LDO18) | V _{DDIO} /V _{DDINT} supply rail |
| RFBUCK_EN | DI | ON/OFF control input for the RF BUCK | V _{DDIO} /V _{DDINT} supply rail |
| TP | AI | Test input Power Commander enable | Internal pull down to GND |

8.3.1.1 ON/OFF and Hardware Watchdog (nONKEY/KEEP_ACT)

The nONKEY signal is a level, active-low wakeup interrupt/event intended to switch on the DA9066 supplied application. nONKEY is always enabled during POWERDOWN mode, so that the application can also be switched on with a disabled GPIO extender. The nONKEY related events can be disabled via the respective interrupt mask M_nONKEY bits. The DA9066 nONKEY port has an internal 200 kΩ resistor to VBAT.

Each nONKEY press generates an event after a programmable (10 ms to 480 ms) debounce time (register nONKEY_DEB). It can generate nONKEY_LO interrupt if enabled via the interrupt mask bit M_nONKEY_LO. The release of the nONKEY also generates an event after the debounce time programmed in the nONKEY_DEB register. The corresponding nONKEY_HI interrupt can be disabled via the M_nONKEY_HI mask bit.

nONKEY_HOLD is an additional event/interrupt generated by a longer press of the nONKEY (hold time 0.5 s to 4 s, programmable via the nONKEY_HOLD_<x>_DEB registers). When the PMIC is in the POWERDOWN state the nONKEY_HOLD event is generated after a debounce time nONKEY_HOLD_ON_DEB. Such an event acts as a wakeup signal causing a transition towards the SYSTEM domain state. When the PMIC is in the ACTIVE state the nONKEY_HOLD event is generated after a debounce time nONKEY_HOLD_OFF_DEB. The nONKEY_HOLD interrupt generation can be masked via the M_nONKEY_HOLD control bit.

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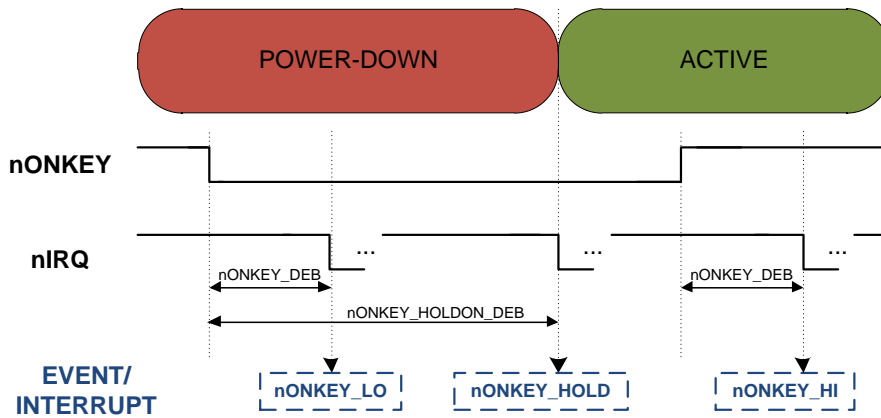


Figure 13: nONKEY ON

With control bit KEEPACT_EN set, the nONKEY can be alternatively assigned to the watchdog unit so that every assertion of the pin (rising edge sensitive) sets the bit WATCHDOG, similar to a write via the power manager bus. The host has to release KEEP_ACT in advance to the next assertion during continuous watchdog supervision (if enabled). The minimum assertion and de-assertion cycle time is 150 μs.

8.3.1.2 Test / Accessory Detect Input (nJIG_ON)

The nJIG_ON signal is an active-low wakeup event intended to switch on DA9066 during the JTAG manufacturing test or when accessory connection is detected. This DA9066 port has an internal 200 kΩ resistor to VBAT. A change of the nJIG_ON input to ACTIVE state (configured by nJIGON_TYPE register) generates an event (stored in the EVENT_C register) and an interrupt if not masked by the M_nJIGON bit. If configured (control register bit nJIGON_MODE = 1), the nJIG_ON event will also generate a wakeup event. nJIG_ON is always enabled during POWERDOWN mode, so that the application can be also switched on with a disabled GPIO extender. nJIG_ON is also a wakeup event in RTC mode (no debouncing).

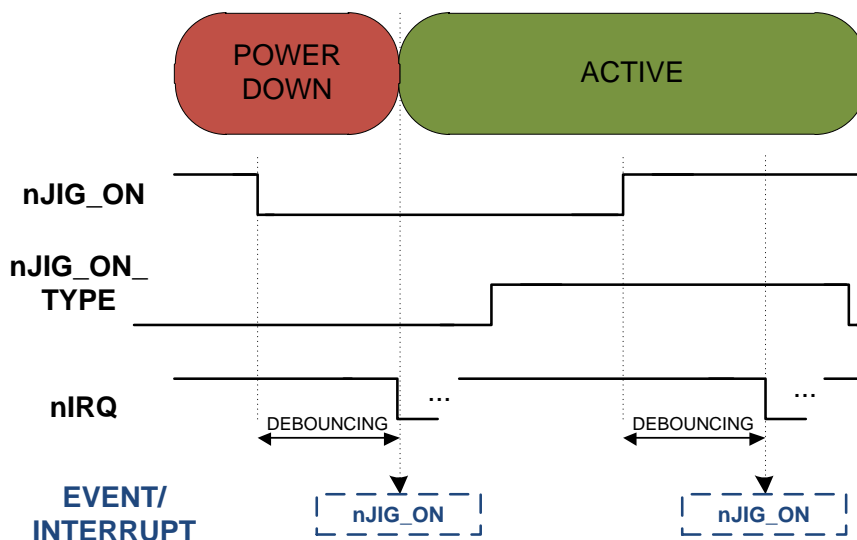


Figure 14: nJIG_ON ON

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8.3.1.3 Travel Adapter Input (TA)

The TA signal is an active-high wakeup interrupt/event intended to switch on the DA9066 supplied application. A change of the TA input to active state (configured by TA_TYPE register) generates an event (stored in the EVENT_C register) and an interrupt if not masked by the M_TA bit. If configured (control register bit TA_MODE=1), the TA event also generates a wake-up event TA is always enabled during POWERDOWN mode, so that the application can be also switched on with a disabled GPIO extender.

TA is also a wakeup event in RTC mode (no debouncing).

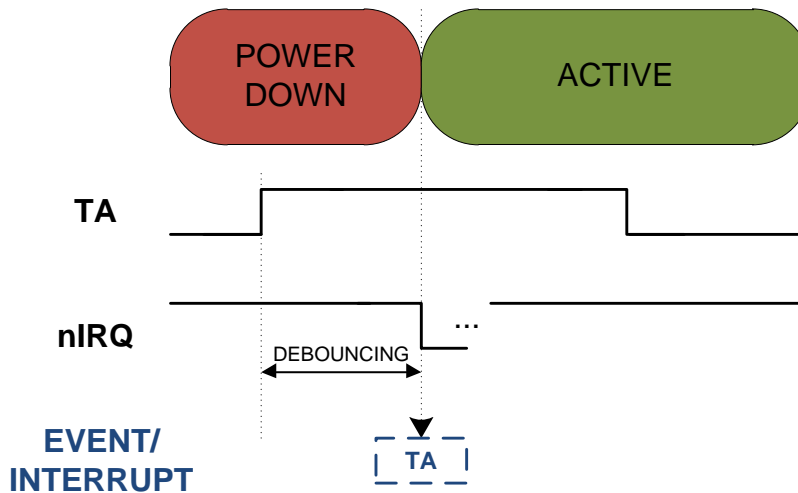


Figure 15: TA ON

The nONKEY, nJIG_ON and TA inputs also act as wakeup events that bring DA9066 out of the low power SLEEP mode and cause a resume of the normal ACTIVE mode operation. Additionally they will cause the PMIC to wake up from RTC mode and transition to POWERDOWN state. These signals are debounced before the PMIC wakes up from POWERDOWN mode (normal ACTIVE mode wakeup). There is no debouncing when waking up from RTC or SLEEP mode.

All DA9066 power manager input buffers can operate from either the VDDIO or the VDDINT supply rail (configuration defined by the PM_I_V register bit).

8.3.1.4 Wakeup from SLEEP

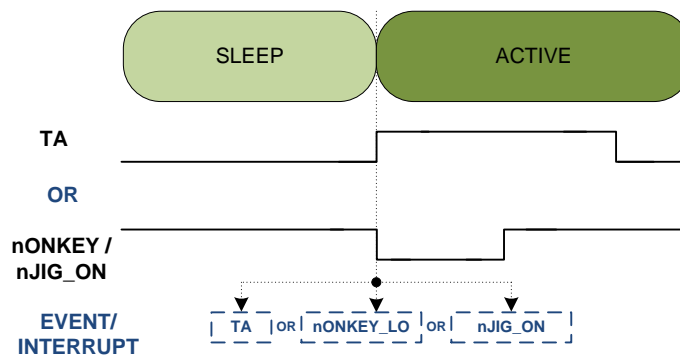


Figure 16: Wakeup from SLEEP

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8.3.1.5 Wakeup from RTC

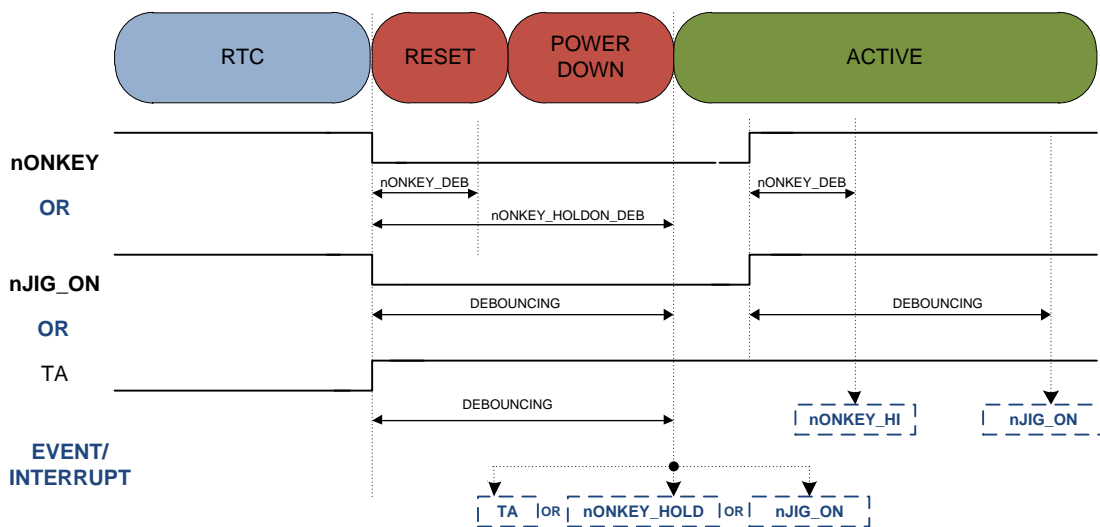


Figure 17: Wakeup from RTC

8.3.1.6 Mode Control Inputs (MCTL1 and MCTL2)

M_CTL1 and M_CTL2 are input signals from the host processor to DA9066 controlling the PMIC and supplies modes of operation. Both inputs are active high and define the functional modes shown in Table 31.

Table 31: Mode Control Inputs

| Input | Mode No. | Operating Mode |
|-------|----------|---------------------------------|
| 00 | Mode_0 | SLEEP/LP (Low Power) mode (TBC) |
| 01 | Mode_1 | NORMAL mode (TBC) |
| 10 | Mode_2 | (TBD) |
| 11 | Mode_3 | TURBO mode (TBC) |

Changes in the state of these control inputs do not generate events/interrupts and do not force PM logic transitions through the main states; they do not trigger power-up, power-down or shutdown sequences.

Mode_0 configures DA9066 in SLEEP/LP mode forcing the DA9066 controlled supplies into a low current consumption mode. This configuration does not change the state of DA9066 but only changes the operational mode of the GPADC, LDO and BUCK supplies as per the settings of the corresponding GPADC_MCTL[3:0], LDO<x>_MCTL[3:0] and BUCK<x>_MCTL[3:0] registers. Normally, in SLEEP/LP mode the LDO output current is reduced to 10 % of the active state I_{MAX} and the buck converters are configured in forced PFM mode. Optionally, every LDO and BUCK supply can be disabled (powered down) or forced to stay on (active state with full current capability) during SLEEP/LP mode via the LDO<x>_MCTL and BUCK<x>_MCTL register settings.

In SLEEP/LP mode the output voltages of Buck1 and Buck4 can be automatically set to a different level as defined in the VBUCK1_RET and VBUCK4_RET retention voltage registers.

When the SLEEP/LP mode is disabled DA9066 returns to its normal operating mode (Mode_1 (TBC)), with supply outputs as defined by the configuration of LDO<x>_MCTL and BUCK<x>_MCTL registers.

The host must ensure the reduced load conditions (10 % of the nominal output current) before forcing DA9066 into SLEEP/LP mode. Similarly, it should first de-assert SLEEP (via MCTL1/2 inputs) before reapplying the full load on the supplies.

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The MCTL pins are only active while the MCTL_EN register is set. While the MCTL pins are active, they have complete control of the supplies, the GPADC and the digital clock, allowing each supply to be independently configured as on, off or in SLEEP/LP mode. The host must set MCTL_EN when it is powered, sequencing has completed and M_CTLx pins are correctly driven. The host can clear MCTL_EN at any time, but it is automatically cleared when the state machine leaves ACTIVE mode. When transitioning between MCTL control and LDO<x>_EN control and when changing MCTL settings, any supplies that are changing will do so simultaneously.

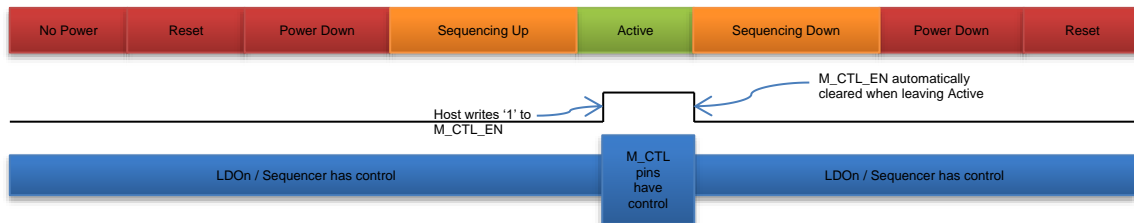


Figure 18: Control from MCTL pins

The LDOs can be set into any of three states: ON, OFF or SLEEP in each of the four MCTL modes. This is controlled by the LDO<x>_MCTLn register. This applies to all user LDOs (except the VRFANA supply LDO18) and the two audio LDOs.

Bucks 1, 2, 3 and 4 can also be set to one of three modes: ON, OFF or SLEEP in each of the M_CTL modes. Bucks 1 and 4 will DVC ramp to a different voltage (VBUCK1/4_RET) when configured to be in SLEEP. The bucks are controlled with BUCK<x>_MCTL[3:0] registers.

The GPADC can be configured as either ON, OFF or SLEEP/LP in each of the MCTL modes via the GPADC_MCTLn registers. When configured is SLEEP/LP mode the ADC operates in the economy mode, i.e. performing measurements every 20ms. If the TEMP1/2, VF and ADCIN current sources are enabled they are dynamically switched off at the end of the conversion when the ADC is configured in SLEEP/LP mode.

The digital clock is also configurable ON or OFF in each of the four MCTL modes. When the clock is off only certain events can re-awaken the clock and hence the PMIC. These are shown in the following table. When not under MCTL control, the digital clock is normally ON. There is a relationship between being able to turn the clock off and the bucks needing the clock to operate as shown in [Table 32](#). The clock is controlled with DIG_CLK_MCTLn.

Table 32: Digital Clock Configurations

| DIG_CLK_MCTLn | BUCK<x>_MCTLn | Digital Clock is: |
|---------------|-------------------|---|
| 1 | | ON |
| 0 | All OFF | OFF |
| 0 | All OFF or SLEEP | OFF (after Buck1/4 has DVCed to VBUCK1/4_RET and all bucks transitioned to PFM) |
| 0 | Any ON (or Turbo) | ON (until all bucks have transitioned into PFM due to low load demand), then OFF. Note that if the load does not reduce, or the bucks are not in AUTO, PFM may never be achieved and the clock will remain ON. Also, if the clock does get stopped, it will NOT start again in response to an increased load. |

8.3.1.7 Analog RF Supplies Enable Input (VRFANA_EN)

The VRFANA_EN pin is an active-high input dedicated to the ON/OFF control of the analog RF supplies – LDO18 and BUCK5.

8.3.1.8 RF BUCK Enable Input (RFBUCK_EN)

The RFBUCK_EN pin is an active-high input dedicated to the ON/OFF control of the RF switching regulator – BUCK6.

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8.3.2 Output Ports - nIRQ, nRESET, nVDD_FAULT, and OUT1/2_32K

| PAD Name | Type | PAD Description | Configuration |
|------------|------|--|------------------|
| nIRQ | DO | Active-low IRQ Line towards host | Push/Pull output |
| nRESET | DO | Active-low RESET towards host | Push/Pull output |
| nVDD_FAULT | DIO | Active-low Indicator for low V_{BAT} | Push/Pull output |
| OUT1_32K | DO | 32 kHz clock buffer | Push/Pull output |
| OUT2_32K | DO | 32 kHz clock buffer | Push/Pull output |

8.3.2.1 Interrupt Request (nIRQ)

The nIRQ is an active-low output signal which indicates that an interrupt causing event has occurred and that the event and status information is available in the related registers. Such information can be temperature and voltage of the PMIC, fault conditions, status changes at input ports, etc. The event registers hold information about the events that have occurred. Events are triggered by a status change of the monitored signals.

When an event bit is set the nIRQ signal is asserted (unless this interrupt is masked by a bit in the IRQ mask register). The nIRQ will not be released until the event registers have been cleared by writing to the related register with an assigned '1' for the event bit to be cleared (bits written containing a zero will leave the related event register bits unchanged). The event registers should be written in page/repeated mode because the nIRQ will not be released until all registers with an asserted event have been reset. New events that occur during writing the event registers will be held until all the event registers have been written. Then they are passed to the event register, ensuring that the host processor does not miss them. The same will happen to all events occurring whilst the sequencer processes time slots (delayed generation of interrupts).

8.3.2.2 Reset Output (nRESET)

The nRESET signal is an active-low output signal from DA9066 to the host processor, which tells the host to enter the hardware-reset state. nRESET is always asserted at the beginning of a DA9066 cold start from NO-POWER Mode and when the DA9066 initiates the power down sequence to RESET Mode via the user assertion of nONKEY long press, reset from host via control bit SHUTDOWN or from a DA9066 detected error condition.

After being asserted nRESET remains low until the reset timer expires. The expiry time can be configured via RESET_TIMER from 1ms to 1s. The reset timer trigger signal can be configured via RESET_EVENT to be EXT_WAKEUP, SYS_UP or PWR_UP.

8.3.2.3 V_{BAT} Supply Fault (nVDD_FAULT)

nVDD_FAULT is an active-low output signal to the host processor to indicate a V_{BAT} low status. The assertion of nVDD_FAULT indicates that the main battery voltage is low ($V_{BAT} < V_{DD_FAULT_LOWER}$) and therefore informs the host processor that if this power condition persists for the next 150ms the PM controller will initiate the power down sequence. When used as a dedicated nVDDFAULT output (GPIO_PIN=00), this port is configured as push-pull (PP) output. During the initial DA9066 start-up sequence this output is in tri-state mode until the device leaves RESET Mode and the port is configured from the OTP.

If nVDDFAULT is not used as a dedicated System/PM output, this port can be configured (via register GPIO_PIN settings) as a GPIO port.

Note that this pin is also used in the PowerCommander boot mode (TP connected to VDDCORE) to indicate that DA9066 waits for a load of control registers with default values from the I²C interface (replacing the standard load from OTP). nVDD_FAULT is released after the last register has been loaded.

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8.3.2.4 Real Time Clock Outputs (OUT1/2_32K)

The OUT1/2_32K outputs provide the system with the buffered DA9066 32 kHz oscillator clock. Once DA9066 is powered from a valid V_{BAT} supply the 32 kHz oscillator will always run after the initial start-up from NO-POWER mode and until the device has reached NO-POWER mode again. However, the OUT1_32K buffer can be disabled during POWERDOWN mode with the OUT_32K_PD control bit. DA9066 also provides a dedicated OUT2_32K_EN OTP control bit that can be used to permanently disable the second clock output.

OUT1/2_32K ports are hardware configured as push-pull output drivers.

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8.4 GPIO

DA9066 features one general purpose I/O pin – nVDDFAULT (if not used as low battery voltage indicator output). It is controlled by a dedicated I²C register and can be configured as either input or output powered from the V_{DDIO} supply voltage.

The nVDDFAULT GPIO can be configured via register 0x014 as:

- Active-high or active-low input
- Push-pull output
- Open-drain output with internal pull-up to V_{DDIO}
- Open-drain output with external pull-up resistor

To guarantee the safe and predictable GPIO operation in all applications, to avoid potential leakage or shorts between the I/O supply rails, and to prevent DA9066 being back-powered by the V_{DDIO} supply, it is imperative that the following condition is met under all circumstances:

$$(V_{SS} - 0.3 \text{ V}) \leq V_{PAD} \leq (V_{DDIO} + 0.3 \text{ V})$$

The input signals can be debounced (configurable debounce time via control DEBOUNCING – 10 ms default) or directly change the state of the assigned status register GPIx to high or low. Whenever the status has changed to its configured active state (edge sensitive), the assigned event register is set and the nIRQ signal is asserted (unless this nIRQ is masked inside the IRQ_MASK register).

In RESET mode (prior to the initial OTP read), the GPIO port is configured as a tri-state OD (open-drain) output with no internal pull-up resistor. When the GPIO module is temporarily disabled by the power sequencer (via GPIO_PD register), level transitions on the input are no longer detected, but the I/O drivers will not change their configuration and programmed levels.

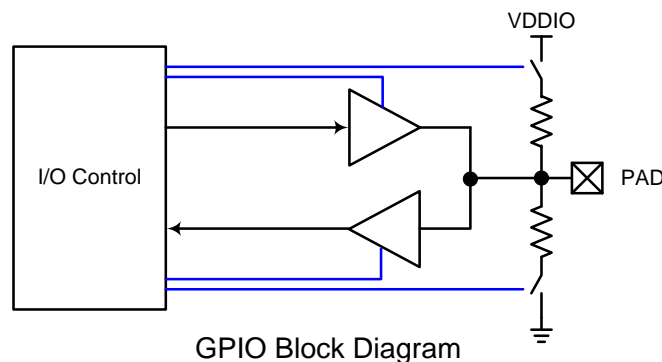


Figure 19: GPIO Block Diagram

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8.5 Power-Up Timing

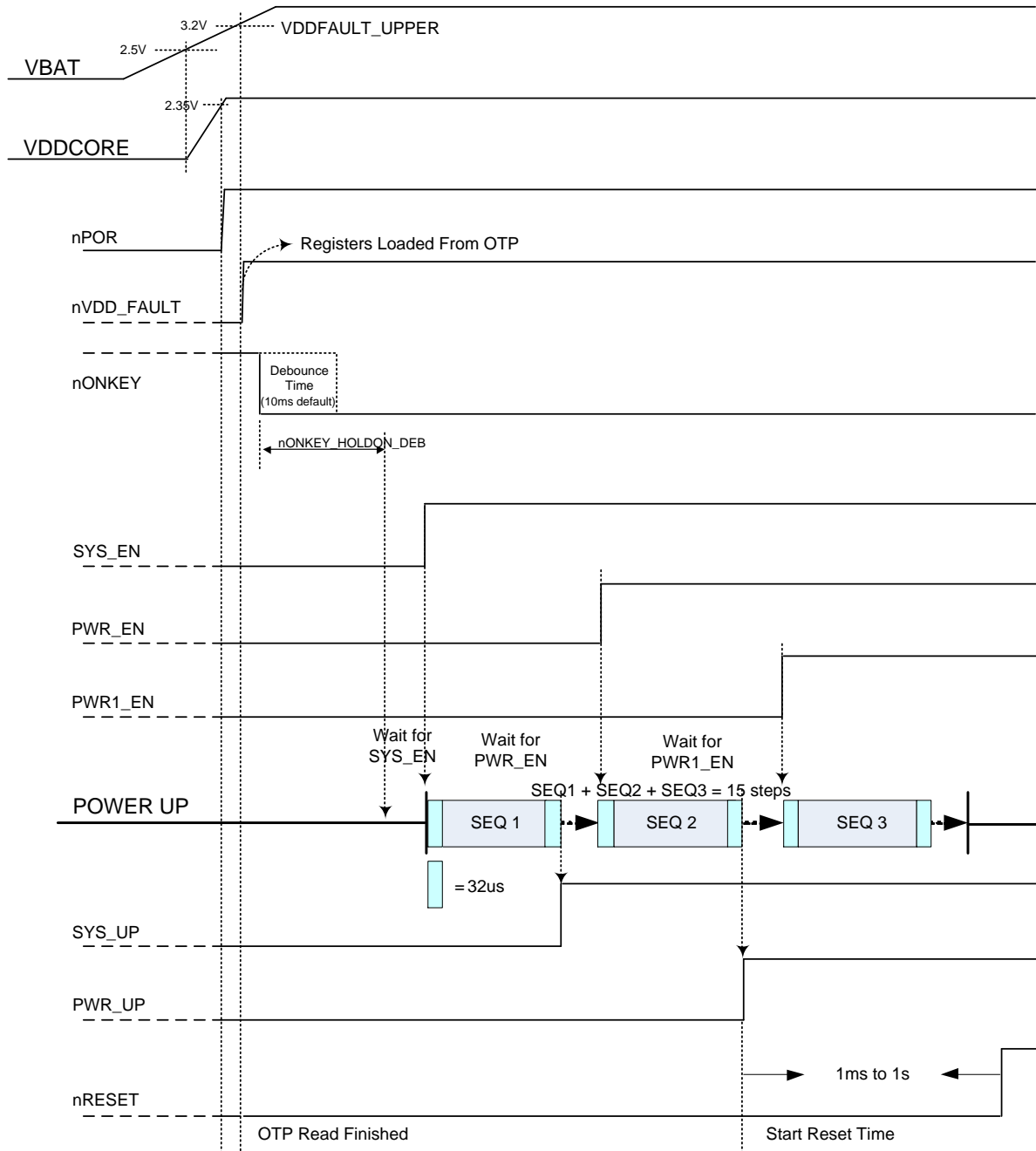


Figure 20: Typical Startup Diagram

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8.5.1 Power-On-Reset (nPOR)

The correct start-up of DA9066 is guaranteed by an internal power-on-reset nPOR (active-low), generated by the initial connection of the V_{BAT} supply. If a backup power source (battery or super capacitor) was connected to the application before the main power, DA9066 remains off and draws no current.

While $V_{DDCORE} < V_{POR_UPPER}$ the internal nPOR is asserted and DA9066 does not turn on (NO-POWER Mode). When V_{DDCORE} rises above V_{POR_UPPER} the nPOR is negated, the RTC counter and FAULT_LOG register are reset and DA9066 progresses to RESET mode.

From POWERDOWN mode, DA9066 continues with powering up supplies if the power domain SYSTEM was asserted via the input port (or set via OTP settings) and AUTO_BOOT was enabled (or a valid wake-event occurred during POWERDOWN mode). The above simplified flow diagram shows the start-up events and an example of a typical initial sequence.

If DA9066 causes a RESET from an under-voltage detected during start-up or within 10 seconds after releasing nRESET (for example due to the initial supply at start-up not being strong enough to supply the application), the PMIC asserts VDD_START in the FAULT_LOG register and temporarily disables the AUTO_BOOT. Only events from the user inputs nONKEY, nJIG_ON or TA trigger a wake-up from this specific state. AUTO_BOOT is set back to its default value (AUTO_BOOT is cleared) the next time DA9066 is in the domain SYSTEM state.

8.5.2 Application Wake-up

A valid wake-up event (nONKEY, nJIG_ON, TA, RTC Alarm or SYS_EN, PWR_EN, PWR1_EN register write) initiates an application power up from POWERDOWN mode. After a wake-up condition is detected, the OTP data for all supplies and the sequencer timer are read (addresses 0x0B and 0x023 to 0x03E) and are used to (re-)configure the supplies and the sequencer timer. If the POWERDOWN mode was reached by progressing from RESET mode, the power sequencer can also be started without waiting for a wake-up event if AUTO_BOOT is asserted.

If the power domains are not pre-enabled by OTP, the host processor has to control the further application start-up (for example via the power domain enable registers). Alternatively, DA9066 continues stand-alone powering up the OTP-enabled domains via the power domain sequencer. Start-up from RESET mode automatically powers up the application only if SYS_EN is asserted from the host processor or is set in OTP.

Continuation into ACTIVE mode requires an assertion of PWR_EN (from host register write or enabled from OTP). After starting the WATCHDOG timer, the host processor has the configured time window to assert the WATCHDOG timer via the power manager bus (if the watchdog is enabled). If this does not happen, the state machine will terminate the ACTIVE mode at the end of the WD time window and return to RESET mode.

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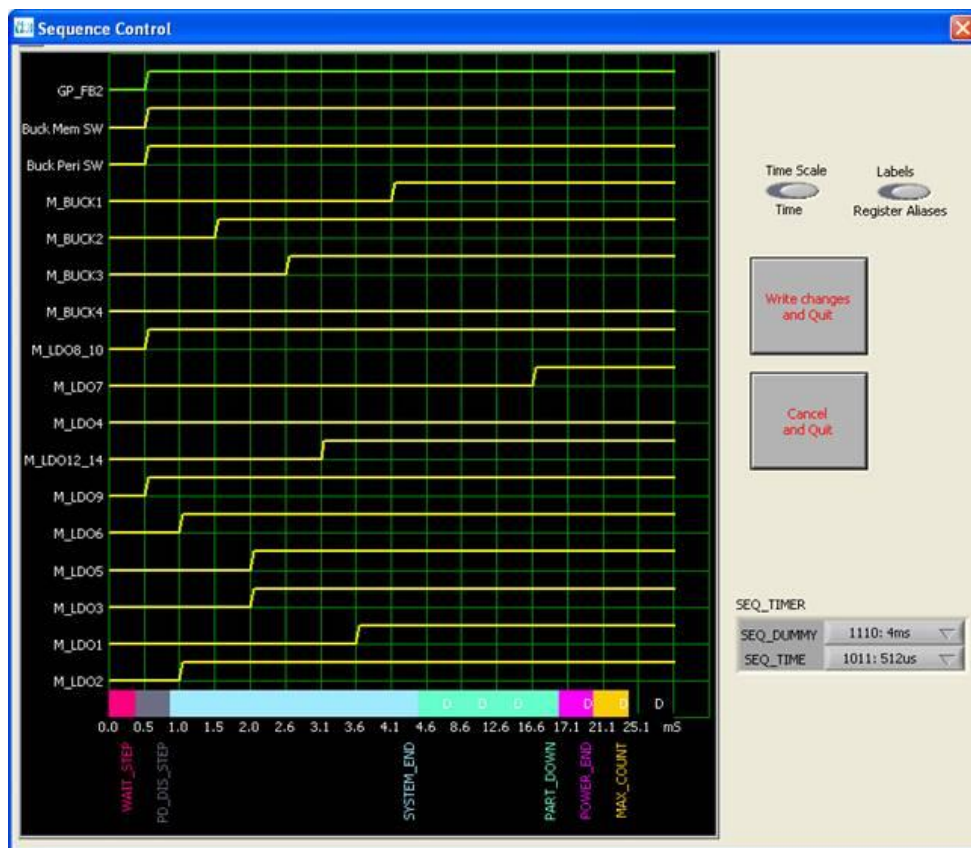


Figure 21: Example Startup of DA9066 Powering Up System Supplies

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8.6 Control Interface

DA9066 is completely software-controlled from the host by registers. DA9066 offers one serial control interface (I²C) to access these registers. Data is shifted into or out from DA9066 under the control of the host processor, which also provides the serial clock.

The DA9066 interface is a general purpose I²C interface that can operate in Fast Mode (up to 400 kHz) and High Speed Mode (up to 1.7 MHz) with external (system) pull-up resistors.

8.6.1 DA9066 2-Wire (I²C) Interface

More information on the I²C interface is provided in Section 11.7.2.

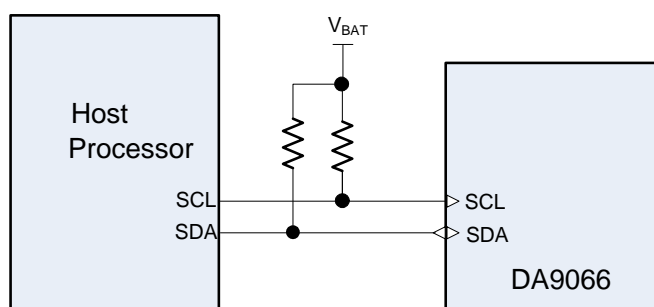


Figure 22: I²C Interface

Table 33: I²C Interface Pads

| PAD Name | Interface | Type | PAD Description |
|----------|------------------|------|---|
| SCL | I ² C | DI | General Purpose I ² C CLOCK (external pull-up) |
| SDA | | DIO | General Purpose I ² C DATA (external pull-up) |

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9 PMIC Register Map

Table 34: PMIC Register Summary

| Register | Addr | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
|------------------------|--------|--------------|------------|-------------|------------|-------------------|------------------|-------------|-------------|--|
| Status / Config | | | | | | | | | | |
| STATUS_A | 0x0001 | Reserved | M_CTL | | VDD_MON_S | Reserved | Reserved | Reserved | Reserved | |
| STATUS_B | 0x0002 | Reserved | SEQUENCING | Reserved 0 | Reserved | Reserved | Reserved 0 | Reserved 0 | nONKEY | |
| STATUS_C | 0x0003 | Reserved 0 | Reserved 0 | Reserved 0 | nJIG_ON | TA | Reserved 0 | Reserved 0 | Reserved 0 | |
| EVENT_A | 0x0004 | E_TICK | E_SEQ_RDY | E_ALARM | E_VDD_MON | E_VDD_LOW | E_TBAT2 | Reserved 0 | E_VF | |
| EVENT_B | 0x0005 | Reserved 0 | Reserved 0 | E_ADC_EOM | E_TBAT1 | E_nONKEY_HOLD_OFF | E_nONKEY_HOLD_ON | E_nONKEY_HI | E_nONKEY_LO | |
| EVENT_C | 0x0006 | E_JACK_DET | E_ACC_DET | GPIO_1 | E_nJIG_ON | E_TA | Reserved 0 | Reserved 0 | Reserved 0 | |
| FAULT_LOG | 0x0007 | WAIT_SHUT | Reserved 0 | KEY_SHUT | Reserved | TEMP_OVR | VDD_START | VDD_FAULT | TWD_ERROR | |
| IRQ_MASK_A | 0x0008 | M_TICK | M_SEQ_RDY | M_ALARM | M_VDD_MON | M_VDD_LOW | M_TBAT2 | Reserved 1 | M_VF | |
| IRQ_MASK_B | 0x0009 | Reserved | Reserved | M_ADC_EOM | M_TBAT1 | M_nONKEY_HOLD_OFF | M_nONKEY_HOLD_ON | M_nONKEY_HI | M_nONKEY_LO | |
| IRQ_MASK_C | 0x000A | M_JACK_DET | M_ACC_DET | Reserved 1 | M_nJIG_ON | M_TA | Reserved 1 | Reserved 1 | Reserved 1 | |
| CONTROL_A | 0x000B | GPI_V | Reserved 1 | Reserved 1 | PM_I_V | PM_IF_V | PWR1_EN | PWR_EN | SYS_EN | |
| CONTROL_B | 0x000C | SHUTDOWN | DEEP_SLEEP | WRITE_MODE | I2C_SPEED | OTPREAD_EN | AUTO_BOOT | Reserved | Reserved | |
| CONTROL_C | 0x000D | Reserved | Reserved | Reserved | DEBOUNCING | | | Reserved | Reserved 0 | |
| CONTROL_D | 0x000E | WATCHDOG | Reserved | Reserved | Reserved | KEEPACT_EN | TWDSCALE | | | |
| PD_DIS | 0x000F | PM_CONT_PD | OUT_32K_PD | CHG_BBAT_PD | Reserved 0 | HS_2_WIRE_PD | PM_IF_PD | GP_ADC_PD | GPIO_PD | |
| INTERFACE | 0x0010 | IF_BASE_ADDR | | | Reserved | Reserved | Reserved | Reserved | Reserved | |
| RESET | 0x0011 | RESET_EVENT | | RESET_TIMER | | | | | | |
| GPIO | | | | | | | | | | |
| Reserved | 0x0012 | Reserved 1 | Reserved 1 | Reserved 1 | Reserved 0 | Reserved 1 | Reserved 1 | Reserved 1 | Reserved 0 | |
| GPIO_TA | 0x0013 | TA_MODE | TA_TYPE | TA_PIN | | Reserved 1 | Reserved 1 | Reserved 1 | Reserved 0 | |
| GPIO_nJIG_ON | 0x0014 | GPIO_MODE | GPIO_TYPE | GPIO_PIN | | nJIG_ON_MODE | nJIG_ON_TYPE | nJIG_ON_PIN | | |
| Sequencer | | | | | | | | | | |
| ID_0_1 | 0x0015 | LDO1_STEP | | | | WAIT_ID_ALWAYS | SYS_PRE | DEF_SUPPLY | nRES_MODE | |
| ID_2_3 | 0x0016 | LDO3_STEP | | | | LDO2_STEP | | | | |
| ID_4_5 | 0x0017 | LDO5_STEP | | | | LDO4_STEP | | | | |
| ID_6_7 | 0x0018 | LDO7_STEP | | | | LDO6_STEP | | | | |
| ID_8_9 | 0x0019 | LDO9_STEP | | | | LDO8_STEP | | | | |
| ID_10_11 | 0x001A | LDO11_STEP | | | | LDO10_STEP | | | | |
| ID_12_13 | 0x001B | PD_DIS_STEP | | | | LDO12_STEP | | | | |
| ID_14_15 | 0x001C | BUCK3_STEP | | | | BUCK2_STEP | | | | |

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| Register | Addr | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|--------|----------------|-----------------|---------------|------------------|--------------------|--------------|--------------------|--------------|
| ID_16_17 | 0x001D | BUCK5_STEP | | | | BUCK4_STEP | | | |
| ID_18_19 | 0x001E | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | BUCK1_STEP | | | |
| Reserved | 0x001F | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |
| SEQ_STATUS | 0x0020 | SEQ_POINTER | | | | WAIT_STEP | | | |
| SEQ_A | 0x0021 | POWER_END | | | | SYSTEM_END | | | |
| SEQ_B | 0x0022 | PART_DOWN | | | | MAX_COUNT | | | |
| SEQ_TIMER | 0x0023 | SEQ_DUMMY | | | | SEQ_TIME | | | |
| Supplies | | | | | | | | | |
| BUCK_A | 0x0024 | BUCK3_ILIM | | BUCK3_MODE | | BUCK2_ILIM | | BUCK2_MODE | |
| BUCK_B | 0x0025 | BUCK5_ILIM | | BUCK5_MODE | | BUCK4_ILIM | | BUCK4_MODE | |
| BUCK_C | 0x0026 | Reserved | BUCK1_SYNC_ILIM | | | | | BUCK1_MODE | |
| BUCK_D | 0x0027 | BUCK1_IAUTSLP | | | BUCK1_SLEEP_ILIM | | | | |
| BUCK1 | 0x0028 | BUCK1_EN | VBUCK_DP | | | | | | |
| BUCK2 | 0x0029 | BUCK2_CONF | BUCK2_EN | VBUCK2 | | | | | |
| BUCK3 | 0x002A | BUCK3_CONF | BUCK3_EN | VBUCK3 | | | | | |
| BUCK4 | 0x002B | BUCK4_CONF | BUCK4_EN | VBUCK4 | | | | | |
| BUCK5 | 0x002C | BUCK5_CONF | BUCK5_EN | VBUCK5 | | | | | |
| BUCKRF_THR | 0x002D | RFBUCK_SNC_THR | | | | RFBUCK_SLP_THR | | | |
| BUCKRF_CONF | 0x002E | RFBUCK_EN | Reserved | RFBUCK_6M_SEL | RFBUCK_I_BYP_LMT | RFBUCK_I_N_LMT_SEL | | RFBUCK_I_P_LMT_SEL | |
| LDO1 | 0x002F | LDO1_CONF | LDO1_EN | VLDO1 | | | | | |
| LDO2 | 0x0030 | LDO2_CONF | LDO2_EN | VLDO2 | | | | | |
| LDO3 | 0x0031 | LDO3_CONF | LDO3_EN | VLDO3 | | | | | |
| LDO4 | 0x0032 | LDO4_CONF | LDO4_EN | VLDO4 | | | | | |
| LDO5 | 0x0033 | LDO5_CONF | LDO5_EN | VLDO5 | | | | | |
| LDO6 | 0x0034 | LDO6_CONF | LDO6_EN | VLDO6 | | | | | |
| LDO7 | 0x0035 | LDO7_CONF | LDO7_EN | VLDO7 | | | | | |
| LDO8 | 0x0036 | LDO8_CONF | LDO8_EN | VLDO8 | | | | | |
| LDO9 | 0x0037 | LDO9_CONF | LDO9_EN | VLDO9 | | | | | |
| LDO10 | 0x0038 | LDO10_CONF | LDO10_EN | VLDO10 | | | | | |
| LDO11 | 0x0039 | LDO11_CONF | LDO11_EN | VLDO11 | | | | | |
| LDO12 | 0x003A | LDO12_CONF | LDO12_EN | VLDO12 | | | | | |
| PULLDOWN_A | 0x003B | LDO4_PD_DIS | LDO3_PD_DIS | LDO2_PD_DIS | LDO1_PD_DIS | BUCK5_PD_DIS | BUCK4_PD_DIS | BUCK3_PD_DIS | BUCK2_PD_DIS |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|--------|------------------|---------------|-------------------|--------------|------------------|--------------|------------------|--------------|
| PULLDOWN_B | 0x003C | LDO12_PD_DIS | LDO11_PD_DIS | LDO10_PD_DIS | LDO9_PD_DIS | LDO8_PD_DIS | LDO7_PD_DIS | LDO6_PD_DIS | LDO5_PD_DIS |
| PULLDOWN_C | 0x003D | Reserved | B2PH_PD_DIS | LDO_VRFANA_PD_DIS | LDO17_PD_DIS | LDO16_PD_DIS | LDO15_PD_DIS | LDO14_PD_DIS | LDO13_PD_DIS |
| PULLDOWN_D | 0x003E | Reserved | Reserved | Reserved | Reserved | LDO22_PD_DIS | LDO21_PD_DIS | LDO20_PD_DIS | LDO19_PD_DIS |
| LDO13 | 0x003F | Reserved | LDO13_EN | VLDO13 | | | | | |
| LDO14 | 0x0040 | Reserved | LDO14_EN | VLDO14 | | | | | |
| LDO15 | 0x0041 | Reserved | LDO15_EN | VLDO15 | | | | | |
| LDO16 | 0x0042 | Reserved | LDO16_EN | VLDO16 | | | | | |
| LDO17 | 0x0043 | Reserved | LDO17_EN | VLDO17 | | | | | |
| LDO_VRFANA | 0x0044 | Reserved | LDO_VRFANA_EN | VLDO_VRFANA | | | | | |
| LDO_19 | 0x0045 | Reserved | LDO19_EN | VLDO19 | | | | | |
| LDO_20 | 0x0046 | Reserved | LDO20_EN | VLDO20 | | | | | |
| LDO_AUD1 | 0x0047 | Reserved | LDO_AUD1_EN | VLDO_AUD1 | | | | | |
| LDO_AUD2 | 0x0048 | Reserved | LDO_AUD2_EN | VLDO_AUD2 | | | | | |
| SUPPLY | 0x0049 | V_LOCK | Reserved | Reserved | BBCHG_EN | VBUCK5_GO | VBUCK4_GO | VBUCK3_GO | VBUCK2_GO |
| Mode Control | | | | | | | | | |
| LDO1_MCTL | 0x004A | LDO1_MCTL3 | | LDO1_MCTL2 | | LDO1_MCTL1 | | LDO1_MCTL0 | |
| LDO2_MCTL | 0x004B | LDO2_MCTL3 | | LDO2_MCTL2 | | LDO2_MCTL1 | | LDO2_MCTL0 | |
| LDO3_MCTL | 0x004C | LDO3_MCTL3 | | LDO3_MCTL2 | | LDO3_MCTL1 | | LDO3_MCTL0 | |
| LDO4_MCTL | 0x004D | LDO4_MCTL3 | | LDO4_MCTL2 | | LDO4_MCTL1 | | LDO4_MCTL0 | |
| LDO5_MCTL | 0x004E | LDO5_MCTL3 | | LDO5_MCTL2 | | LDO5_MCTL1 | | LDO5_MCTL0 | |
| LDO6_MCTL | 0x004F | LDO6_MCTL3 | | LDO6_MCTL2 | | LDO6_MCTL1 | | LDO6_MCTL0 | |
| LDO7_MCTL | 0x0050 | LDO7_MCTL3 | | LDO7_MCTL2 | | LDO7_MCTL1 | | LDO7_MCTL0 | |
| LDO8_MCTL | 0x0051 | LDO8_MCTL3 | | LDO8_MCTL2 | | LDO8_MCTL1 | | LDO8_MCTL0 | |
| LDO9_MCTL | 0x0052 | LDO9_MCTL3 | | LDO9_MCTL2 | | LDO9_MCTL1 | | LDO9_MCTL0 | |
| LDO10_MCTL | 0x0053 | LDO10_MCTL3 | | LDO10_MCTL2 | | LDO10_MCTL1 | | LDO10_MCTL0 | |
| LDO11_MCTL | 0x0054 | LDO11_MCTL3 | | LDO11_MCTL2 | | LDO11_MCTL1 | | LDO11_MCTL0 | |
| LDO12_MCTL | 0x0055 | LDO12_MCTL3 | | LDO12_MCTL2 | | LDO12_MCTL1 | | LDO12_MCTL0 | |
| LDO13_MCTL | 0x0056 | LDO13_MCTL3 | | LDO13_MCTL2 | | LDO13_MCTL1 | | LDO13_MCTL0 | |
| LDO14_MCTL | 0x0057 | LDO14_MCTL3 | | LDO14_MCTL2 | | LDO14_MCTL1 | | LDO14_MCTL0 | |
| LDO15_MCTL | 0x0058 | LDO15_MCTL3 | | LDO15_MCTL2 | | LDO15_MCTL1 | | LDO15_MCTL0 | |
| LDO16_MCTL | 0x0059 | LDO16_MCTL3 | | LDO16_MCTL2 | | LDO16_MCTL1 | | LDO16_MCTL0 | |
| LDO17_MCTL | 0x005A | LDO17_MCTL3 | | LDO17_MCTL2 | | LDO17_MCTL1 | | LDO17_MCTL0 | |
| LDO_VRFANA_MCTL | 0x005B | LDO_VRFANA_MCTL3 | | LDO_VRFANA_MCTL2 | | LDO_VRFANA_MCTL1 | | LDO_VRFANA_MCTL0 | |
| LDO19_MCTL | 0x005C | LDO19_MCTL3 | | LDO19_MCTL2 | | LDO19_MCTL1 | | LDO19_MCTL0 | |
| LDO20_MCTL | 0x005D | LDO20_MCTL3 | | LDO20_MCTL2 | | LDO20_MCTL1 | | LDO20_MCTL0 | |
| BUCK1_MCTL | 0x0060 | BUCK1_MCTL3 | | BUCK1_MCTL2 | | BUCK1_MCTL1 | | BUCK1_MCTL0 | |
| BUCK2_MCTL | 0x0061 | BUCK2_MCTL3 | | BUCK2_MCTL2 | | BUCK2_MCTL1 | | BUCK2_MCTL0 | |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|--------|--------------------|---------------------|---------------|---------------|------------------|--------------------|---------------|--------------|
| BUCK3_MCTL | 0x0062 | BUCK3_MCTL3 | | BUCK3_MCTL2 | | BUCK3_MCTL1 | | BUCK3_MCTL0 | |
| BUCK4_MCTL | 0x0063 | BUCK4_MCTL3 | | BUCK4_MCTL2 | | BUCK4_MCTL1 | | BUCK4_MCTL0 | |
| BUCK5_MCTL | 0x0064 | BUCK5_MCTL3 | | BUCK5_MCTL2 | | BUCK5_MCTL1 | | BUCK5_MCTL0 | |
| BUCK_RF_MCTL | 0x0065 | BUCK_RF_MCTL3 | | BUCK_RF_MCTL2 | | BUCK_RF_MCTL1 | | BUCK_RF_MCTL0 | |
| GPADC_MCTL | 0x0066 | GPADC_MCTL3 | | GPADC_MCTL2 | | GPADC_MCTL1 | | GPADC_MCTL0 | |
| MISC_MCTL | 0x0067 | DIG_CLK_MCTL3 | DIG_CLK_MCTL2 | DIG_CLK_MCTL1 | DIG_CLK_MCTL0 | BBAT_MCTL3 | BBAT_MCTL2 | BBAT_MCTL1 | BBAT_MCTL0 |
| VBUCK1_MCTL_RET | 0x0068 | Reserved | VBUCK1_RET | | | | | | |
| VBUCK4_MCTL_RET | 0x0069 | Reserved | Reserved | VBUCK4_RET | | | | | |
| Control | | | | | | | | | |
| WAIT_CONT | 0x006A | WAIT_DIR | RTC_CLOCK | WAIT_MODE | EN_32K | DELAY_TIME | | | |
| ONKEY_CONT1 | 0x006B | NONKEY_DEB | | | | PRESS_TIME | | | |
| OUT2_32K_ONKEY_CONT | 0x006C | OUT2_32KEN | NONKEY_HOLD_OFF_DEB | | | Reserved | NONKEY_HOLD_ON_DEB | | |
| POWER_CONT | 0x006D | NJIG_MCTRL_WAKE_DS | RTC_AUTO_EN | Reserved 0 | Reserved 0 | BBAT_ILIM_IGNORE | Reserved 0 | Reserved 0 | MCTRL_EN |
| VDDFAULT | 0x006E | Reserved | Reserved | vdd_fault_adj | | | | vdd_hyst_adj | |
| BBAT_CONT | 0x006F | BCHARGER_ISET | | | | BCHARGER_VSET | | | |
| ADC | | | | | | | | | |
| ADC_MAN | 0x0070 | ISRC_50U | Reserved | Reserved | MAN_CONV | MUX_SEL | | | |
| ADC_CONT | 0x0071 | ADC_AUTO_EN | ADC_MODE | TEMP1_ISRC_EN | VF_ISRC_EN | TEMP2_ISRC_EN | AUTO_AIN_EN | AUTO_VF_EN | AUTO_VBAT_EN |
| ADC_CONT2 | 0x0072 | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | AD5_ISRC_EN |
| ADC_RES_L | 0x0073 | Reserved | Reserved | Reserved | Reserved | ADC_RES_LSB | | | |
| ADC_RES_H | 0x0074 | ADC_RES_MSB | | | | | | | |
| VBAT_RES | 0x0075 | VBAT_RES_MSB | | | | | | | |
| VDDOUT_MON | 0x0076 | VDDOUT_MON | | | | | | | |
| TEMP1_RES | 0x0077 | TBAT1_RES | | | | | | | |
| TEMP1_HIGHP | 0x0078 | TEMP1_HIGHP | | | | | | | |
| TEMP1_HIGHN | 0x0079 | TEMP1_HIGHN | | | | | | | |
| TEMP1_LOW | 0x007A | TEMP1_LOW | | | | | | | |
| T_OFFSET | 0x007B | T_OFFSET | | | | | | | |
| VF_RES | 0x007C | VF_RES_MSB | | | | | | | |
| VF_HIGH | 0x007D | VF_HIGH | | | | | | | |
| VF_LOW | 0x007E | VF_LOW | | | | | | | |
| AIN_RES | 0x007F | AIN_RES_MSB | | | | | | | |
| TEMP2_RES | 0x0082 | TBAT2_RES | | | | | | | |
| TEMP2_HIGHP | 0x0083 | TEMP2_HIGHP | | | | | | | |
| TEMP2_HIGHN | 0x0084 | TEMP2_HIGHN | | | | | | | |
| TEMP2_LOW | 0x0085 | TEMP2_LOW | | | | | | | |
| TJUNC_RES | 0x0086 | TJUNC_RES | | | | | | | |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|--------|--------------------|--------------------|-------------------|------------|---------------|------------|------------|--------------|
| ADC_RES_AUTO1 | 0x0087 | TEMP1_RES_LSB | | | | VBAT_RES_LSB | | | |
| ADC_RES_AUTO2 | 0x0088 | AIN_RES_LSB | | | | VF_RES_LSB | | | |
| ADC_RES_AUTO3 | 0x0089 | TJUNC_RES_LSB | | | | TEMP2_RES_LSB | | | |
| RTC | | | | | | | | | |
| COUNT_S | 0x008A | Reserved | Reserved | COUNT_SEC | | | | | |
| COUNT_MI | 0x008B | Reserved | Reserved | COUNT_MIN | | | | | |
| COUNT_H | 0x008C | Reserved | Reserved | Reserved | COUNT_HOUR | | | | |
| COUNT_D | 0x008D | Reserved | Reserved | Reserved | COUNT_DAY | | | | |
| COUNT_MO | 0x008E | Reserved | Reserved | Reserved | Reserved | COUNT_MONTH | | | |
| COUNT_Y | 0x008F | Reserved | MONITOR | COUNT_YEAR | | | | | |
| ALARM_S | 0x0090 | Reserved | Reserved | ALARM_SEC | | | | | |
| ALARM_MI | 0x0091 | TICK_TYPE | Reserved | ALARM_MIN | | | | | |
| ALARM_H | 0x0092 | Reserved | Reserved | Reserved | ALARM_HOUR | | | | |
| ALARM_D | 0x0093 | Reserved | Reserved | Reserved | ALARM_DAY | | | | |
| ALARM_MO | 0x0094 | Reserved | Reserved | Reserved | Reserved | ALARM_MONTH | | | |
| ALARM_Y | 0x0095 | TICK_ON | ALARM_ON | ALARM_YEAR | | | | | |
| OTP Config | | | | | | | | | |
| CHIP_ID | 0x0096 | MRC | | | | TRC | | | |
| CONFIG_ID | 0x0097 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | CONF_ID | | |
| OTP_CONT | 0x0098 | GP_WRITE_DIS | OTP_CONF_LOCK | OTP_GP_LOCK | Reserved | OTP_CONF | OTP_GP | OTP_RP | OTP_TRANSFER |
| OSC_TRIM | 0x0099 | TRIM_32K | | | | | | | |
| GP_ID_0 | 0x009A | GP_0 | | | | | | | |
| GP_ID_1 | 0x009B | GP_1 | | | | | | | |
| GP_ID_2 | 0x009C | GP_2 | | | | | | | |
| GP_ID_3 | 0x009D | GP_3 | | | | | | | |
| GP_ID_4 | 0x009E | GP_4 | | | | | | | |
| GP_ID_5 | 0x009F | GP_5 | | | | | | | |
| Audio | | | | | | | | | |
| AUDIO_REG_DFLT_0 | 0x00A0 | AUD_REG_0 | | | | | | | |
| AUDIO_REG_DFLT_1 | 0x00A1 | AUD_REG_1 | | | | | | | |
| AUDIO_REG_DFLT_2 | 0x00A2 | AUD_REG_2 | | | | | | | |
| AUDIO_REG_DFLT_3 | 0x00A3 | AUD_REG_3 | | | | | | | |
| AUDIO_REG_DFLT_4 | 0x00A4 | AUD_REG_4 | | | | | | | |
| AUDIO_REG_DFLT_5 | 0x00A5 | AUD_REG_5 | | | | | | | |
| AUDIO_REG_DFLT_6 | 0x00A6 | AUD_REG_6 | | | | | | | |
| BUCK2_5_CONF1 | 0x00DF | buck_6_ext_ctrl_en | buck_5_ext_ctrl_en | ldo18_ext_ctrl_en | Reserved | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |

System PMIC for Dual/Quad-Core Processors

10 Audio System Specification

10.1 Block Diagram

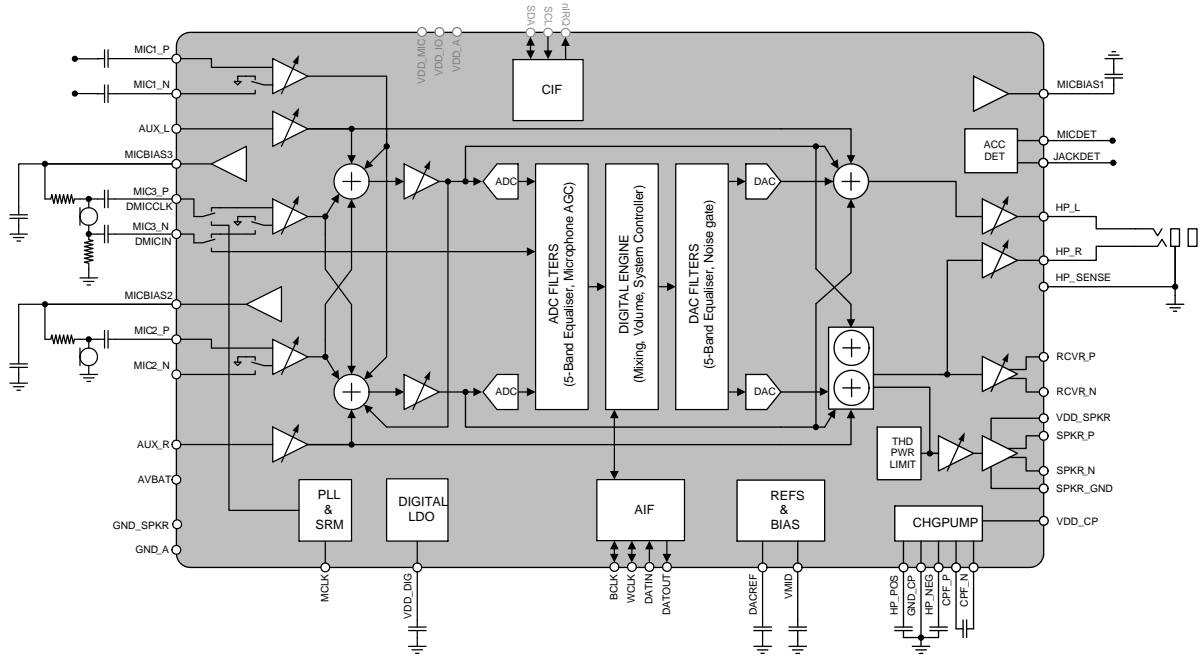


Figure 23: DA9066 Audio with Shared PMIC Connections

System PMIC for Dual/Quad-Core Processors

10.2 Recommended Operating Conditions

Unless otherwise noted the parameters in Table 35 are valid for $V_{DD_DIG} = 1.2\text{ V}$, $V_{DD_A} = V_{DD_CP} = 1.6\text{ V}$, $V_{DD_IO} = 1.8\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_s = 48\text{ kHz}$.

Table 35: Codec Power Dissipation

| Operating Mode | Conditions | Min | Typ | Max | Unit |
|---|--|-----|------|-----|---------------|
| POWERDOWN mode | | | | 5 | μA |
| Digital playback to headphone, no load | DAACL/R to HP_L/R, quiescent | | 2.0 | | mW |
| Digital playback to headphone, with load | DAACL/R to HP_L/R, 16 Ω load, reference track calibrated to 0.1 mA at 0 dBFS | | 2.65 | | mW |
| | DAACL/R to HP_L/R, 16 Ω load, reference track calibrated to 0.1 mA at 0 dBFS, $V_{DD_A} = V_{DD_CP} = 1.8\text{ V}$ | | 2.95 | | mW |
| Analog bypass to headphone, no load | AUX_L/R to HP_L/R, quiescent | | 1.9 | | mW |
| Analog bypass to headphone, with load | AUX_L/R to HP_L/R, 16 Ω load, reference track calibrated to 0.1 mA at 0 dBFS | | 2.55 | | mW |
| Microphone stereo record | Stereo MICs to ADCL/R | | 2.2 | | mW |
| Microphone stereo record and digital playback to headphone, no load | Stereo MICs to ADCL/R and DAACL/R to HP_L/R, quiescent | | 3.7 | | mW |
| Microphone stereo record and digital playback to headphone, with load | Stereo MICs to ADCL/R and DAACL/R to HP_L/R, 16 Ω load, reference track calibrated to 0.1 mA at 0 dBFS | | 4.4 | | mW |

System PMIC for Dual/Quad-Core Processors

11 Audio Electrical Characteristics

Unless otherwise noted the parameters in Table 36 to Table 51 are valid for $V_{DD_DIG} = 1.2\text{ V}$, $V_{DD_A} = V_{DD_CP} = 1.6\text{ V}$, $V_{DD_IO} = 1.8\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$, $f_s = 48\text{ kHz}$.

11.1 Reference Voltage Generation and Temperature Supervision

Table 36: References and Temperature Supervision

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------|---------------------------------|------------|-----|-------------------------|-----|---------------|
| V_{MID} | Audio mid-rail voltage | | | $0.45 \times V_{DD_A}$ | | V |
| C_{VMID} | V_{MID} decoupling capacitor | | | 1.0 | | μF |
| V_{DACREF} | Audio DAC/ADC reference voltage | | | $0.9 \times V_{DD_A}$ | | V |
| C_{DACREF} | DACREF decoupling capacitor | | | | 1.0 | μF |

11.2 Audio Inputs

11.2.1 Microphone Bias

Table 37: Microphone Bias Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------------------|---------------------------------------|--|-----|-----|-----|---------------------|
| $V_{MICBIAS}$ | Bias voltage (Note 1) | No load, $V_{DD_MIC} > V_{MICBIAS} + 200\text{ mV}$ | 1.6 | | 3.0 | V |
| I_{BIAS} | Maximum current | Voltage drop $< 50\text{ mV}$ | | 2 | | mA |
| PSRR with respect to V_{DD_A} | Power supply rejection ratio (Note 2) | 20 Hz to 200 Hz | 70 | | | dB |
| | | $> 2\text{ kHz}$ | 50 | | | |
| V_{NOISE} | Output noise voltage | $V_{MICBIAS} \leq 2.2\text{ V}$ | | 5 | | μV_{RMS} |
| C_{LOAD} | Capacitive load | $I_{BIAS} < 100\text{ }\mu\text{A}$ | | 100 | | pF |
| | | $100\text{ }\mu\text{A} < I_{BIAS} < 2\text{ mA}$ | | 200 | | |

Note 1 Microphone bias voltage is programmable to (1.6, 2.2, 2.5, or 3.0) V

Note 2 PSRR is a measure of the attenuation of a signal on the supply to the signal at the output

System PMIC for Dual/Quad-Core Processors

11.2.2 Input Amplifiers

Table 38: Input Paths Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|--|--|------|-------------------------|------|-------------------|
| V _{MAX} | Full-scale input signal | Single-ended MIC_PGA = AUX_PGA = MIXIN_PGA = 0 dB | | 0.8 * V _{DD_A} | | V _{PP} |
| | | Differential MIC_PGA = AUX_PGA = MIXIN_PGA = 0 dB | | 1.6 * V _{DD_A} | | |
| R _{IN} | Input resistance | MIC, single-ended | 12 | 15 | 18 | kΩ |
| | | AUX | 6 | | 40 | |
| C _{IN} | Input capacitance | | | 1 | | pF |
| | Amplitude ripple | 20 Hz to 20 kHz | -0.5 | | +0.5 | dB |
| | Programmable gain | MIC_PGA | -6 | | 36 | dB |
| AUX_PGA | | -54 | | 15 | | |
| MIXIN_PGA | | -4.5 | | 18 | | |
| | Programmable gain step size | MIC_PGA | | 6 | | dB |
| | | AUX_PGA, MIXIN_PGA | | 1.5 | | |
| | Absolute gain accuracy | 0 dB @ 1 kHz | -1.0 | | +1.0 | dB |
| | Left/right gain mismatch | 20 Hz to 20 kHz | -0.1 | | +0.1 | dB |
| | Gain step error | 20 Hz to 20 kHz | -0.1 | | +0.1 | dB |
| | Input noise level | MIC_PGA = 36 dB Inputs connected to GND, A- weighted, input-referred, measured @ ADC output | | 5 | | μV _{RMS} |
| | | AUX_PGA = 15 dB Inputs connected to GND, A- weighted, input-referred, measured @ ADC output | | 6.5 | | |
| PSRR | Power supply rejection ratio with respect to V _{DD_A} | Single-ended input 20 Hz to 2 kHz | 70 | | | dB |
| | | Single-ended input 20 kHz | 50 | | | |
| | | Differential input 20 Hz to 2 kHz | 90 | | | |
| | | Differential input 20 kHz | 70 | | | |

System PMIC for Dual/Quad-Core Processors

11.2.3 Stereo Audio ADC

Table 39: Audio ADC Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|--|-------------------------------------|-----------------------|-------------------------|-----------------------|-----------------|
| V _{MAX} | Full-scale input signal | Digital output level = 0 dBFS | | 1.6 * V _{DD_A} | | V _{PP} |
| SNR (Note 1) | Signal to noise ratio | A-weighted no input selected | | 90 | | dB |
| THD+N (Note 2) | Total harmonic distortion plus noise | -1 dBFS 44.1 kHz slave mode | | -85 | | dB |
| | | -1 dBFS 32 kHz PLL mode | | -80 | | dB |
| | In band spurious | Analog input level = 0 dBFS | | -85 | | dB |
| | Channel separation | | | 90 | | dB |
| f _{BPASS} | Passband | | | | 0.45 * f _s | Hz |
| f _{BSTOP} | Stopband | | 0.56 * f _s | | | Hz |
| | Passband ripple | Voice mode | | | ±0.3 | dB |
| | | Music mode | | | ±0.1 | |
| | Stopband attenuation | Voice mode | 70 | | | dB |
| | | Music mode | 55 | | | |
| | Group delay | Voice mode | | 4.3 / f _s | 600 | μs |
| | | Music Mode | | 18 / f _s | | |
| | | f _s = 88.2 kHz or 96 kHz | | 9 / f _s | | |
| | Group delay mismatch | Between left and right channels | | | 2 | μs |
| PSRR | Power supply rejection ratio with respect to V _{DD_A} | 20 Hz to 2 kHz | 70 | | | dB |
| | | 20 kHz | 50 | | | |

Note 1 SNR (signal-to-noise ratio) is a ratio of the full-scale output signal level to the noise level with no signal applied.

Note 2 THD+N (total harmonic distortion plus noise) is a ratio of the level of the harmonics and noise to the output signal.

System PMIC for Dual/Quad-Core Processors

11.3 Audio Outputs

11.3.1 Stereo Audio DAC

Table 40: Overall DAC Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-------------|--|---|--------------|-------------------|--------------|---------|
| V_{MAX} | Full-scale output signal | Digital input level = 0 dBFS | | $1.6 * V_{DD_A}$ | | VPP |
| SNR | Signal to noise ratio | A-weighted | | 100 | | dB |
| THD+N | Total harmonic distortion plus noise | -1 dB _{FS} 44.1 kHz slave mode | | -90 | | dB |
| | | -1 dB _{FS} | | -80 | | dB |
| | Channel separation | | | 90 | | dB |
| f_{BPASS} | Passband | | | | $0.45 * f_s$ | kHz |
| f_{BSTOP} | Stopband | | $0.56 * f_s$ | | | kHz |
| | Passband ripple | Voice mode | | | ± 0.15 | dB |
| | | Music mode | | | ± 0.1 | |
| | Stopband attenuation | Voice mode | 70 | | | dB |
| | | Music mode | 55 | | | |
| | Group delay | Voice mode | | $4.8 / f_s$ | 650 | μs |
| | | Music mode | | $18.5 / f_s$ | | |
| | | $f_s = 88.2 \text{ kHz or } 96 \text{ kHz}$ | | $9 / f_s$ | | |
| | Group delay variation | 20 Hz to 20 kHz | | | 1 | μs |
| | Group delay mismatch | Between left and right channels | | | 2 | μs |
| PSRR | Power supply rejection ratio with respect to V_{DD_A} | 20 Hz to 2 kHz | 70 | | | dB |
| | | 20 kHz | 50 | | | |

System PMIC for Dual/Quad-Core Processors

11.3.2 True-Ground Headphone Amplifier

Table 41: True-Ground Headphone Amplifier Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|--------------------|-------------------------------|---|-------|--------------------------|-------|-------------------|
| V _{MAX} | Full-scale output signal | No load | | 1.6 * V _{DD_CP} | | V _{PP} |
| | DC output offset | | | | 100 | μV |
| P _{MAX} | Maximum power per channel | V _{DD_CP} = 1.6 V T _{HD} < 0.1 % R _{LOAD} =16 Ω, 1 kHz | | 22 | | mW _{RMS} |
| | | V _{DD_CP} = 1.8 V T _{HD} < 0.1 % R _{LOAD} =16 Ω, 1 kHz | | 27 | | mW _{RMS} |
| | | V _{DD_CP} = 2.5 V T _{HD} < 0.1 % R _{LOAD} =16 Ω, 1 kHz | | 45 | | mW _{RMS} |
| I _Q | Quiescent current per channel | from V _{DD_CP} | | | 150 | μA |
| R _{LOAD} | Load impedance | | 13 | 16 | | Ω |
| L _{LOAD} | Load impedance | | | | 400 | μH |
| C _{LOAD} | Load impedance | | | | 500 | pF |
| | Frequency response | ±0.5 dB | 20 | | 20k | Hz |
| | Amplitude ripple | 20 Hz to 20 kHz | -0.5 | | +0.5 | dB |
| | Programmable gain | | -56 | | +6 | dB |
| | Mute attenuation | | | 70 | | dB |
| | Programmable gain step size | -6 dB to 6 dB | | 0.5 | | dB |
| | | -24 dB to -6 dB | | 1.0 | | |
| | | -56 dB to -24 dB | | 2.0 | | |
| | Absolute gain accuracy | 0 dB @ 1 kHz | -0.8 | | +0.8 | dB |
| | Input gain L/R mismatch | 20 Hz to 20 kHz | -0.1 | | +0.1 | dB |
| | Input gain step error | 20 Hz to 20 kHz -6 dB to 6 dB | -0.05 | | +0.05 | dB |
| | | 20 Hz to 20 kHz -24 dB to -7 dB | -0.1 | | +0.1 | |
| | | 20 Hz to 20 kHz -56 dB to -26 dB | -0.2 | | +0.2 | |
| SNR | Signal to noise ratio | A-weighted gain = 0 dB V _{DD_CP} = 1.6 V | | 96.5 | | dB |
| | | A-weighted gain = 0 dB V _{DD_CP} = 1.8 V | | 98 | | |
| V _{NOISE} | Output noise level | 20 Hz to 20 kHz, non A-weighted gain < -20dB | | | 2.5 | μV _{RMS} |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|---|---|-----|-----|-----|------|
| THD+N | Total harmonic distortion plus noise | $V_{DD_CP} = 1.6\text{ V}$ -5 dB _{Fs} $R_{LOAD} = 16\ \Omega$ | | -75 | | dB |
| PSRR | Power supply rejection ratio with respect to V_{DD_CP} | 20 Hz to 2 kHz | 70 | | | dB |
| | | 20 kHz | 50 | | | |

11.3.3 Receiver/Earpiece Amplifier

Table 42 Receiver/Earpiece Amplifier Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------|-------------------------------|--|-------|--------------------|--------|---------------|
| V_{MAX} | Full-scale output signal | No load | | $3.2 * V_{DD_CP}$ | | V_{PP} |
| P_{MAX} | Maximum power per channel | $V_{DD_CP} = 1.6\text{ V}$ $T_{HD} < 1\%$ $R_{LOAD} = 32\ \Omega, 1\text{ kHz}$ | | 50 | | mW_{RMS} |
| | | $V_{DD_CP} = 1.8\text{ V}$ $T_{HD} < 1\%$ $R_{LOAD} = 32\ \Omega, 1\text{ kHz}$ | | 65 | | mW_{RMS} |
| | | $V_{DD_CP} = 2.5\text{ V}$ $T_{HD} < 1\%$ $R_{LOAD} = 32\ \Omega, 1\text{ kHz}$ | | 125 | | mW_{RMS} |
| I_Q | Quiescent current per channel | from V_{DD_CP} | | | 150 | μA |
| R_{LOAD} | Load impedance | | 26 | 32 | | Ω |
| L_{LOAD} | Load impedance | | | | 400 | μH |
| C_{LOAD} | Load impedance | | | | 500 | pF |
| | Frequency response | $\pm 0.5\text{ dB}$ | 20 | | 20,000 | Hz |
| | Amplitude ripple | 20 Hz to 20 kHz | -0.5 | | +0.5 | dB |
| | Programmable gain | | -50 | | +12 | dB |
| | Mute attenuation | | | 70 | | dB |
| | Programmable gain step size | 0 dB to 12 dB | | 0.5 | | dB |
| | | -24 dB to -7 dB | | 1.0 | | |
| | | -50 dB to -26 dB | | 2.0 | | |
| | Absolute gain accuracy | 0 dB @ 1 kHz | -0.8 | | +0.8 | dB |
| | Input gain L/R mismatch | 20 Hz to 20 kHz | -0.1 | | +0.1 | dB |
| | Input gain step error | 20 Hz to 20 kHz 0 dB to 12 dB | -0.05 | | +0.05 | dB |
| | | 20 Hz to 20 kHz -24 dB to -1 dB | -0.1 | | +0.1 | |
| | | 20 Hz to 20 kHz -50 dB to -26 dB | -0.2 | | +0.2 | |
| SNR | Signal to noise ratio | A-weighted gain = 0 dB $V_{DD_CP} = 1.6\text{ V}$ | | 96.5 | | dB |

System PMIC for Dual/Quad-Core Processors

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-------------|---|---|-----|-----|-----|---------------------|
| | | A-weighted gain = 0 dB $V_{DD_CP} = 1.8\text{ V}$ | | 98 | | |
| V_{NOISE} | Output noise level | 20 Hz to 20 kHz, non A-weighted gain < -20 dB | | | 2.5 | μV_{RMS} |
| THD+N | Total harmonic distortion plus noise | $V_{DD_CP} = 1.6\text{ V}$ -5 dBFS $R_{LOAD} = 16\ \Omega$ | | -75 | | dB |
| PSRR | Power supply rejection ratio with respect to V_{DD_CP} | 20 Hz to 2 kHz | 70 | | | dB |
| | | 20 kHz | 50 | | | |

11.3.4 Class-D Speaker Driver

Table 43: Class-D Speaker Driver Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------|-------------------------------|---|-----|-----|--------|---------------------|
| V_{DD_SPKR} | Supply voltage | | 2.8 | 3.5 | 5.5 | V |
| R_{LOAD} | Load impedance | | 4 | | | Ω |
| L_{LOAD} | Load impedance | | 10 | | | μH |
| P_{MAX} | Maximum output power | $V_{DD_SPKR} = 4.2\text{ V}$ $R_{LOAD} = 8\ \Omega$ | | | 1.0 | W |
| η | Efficiency | $P_{OUT} = 1.0\text{ W}$ $R_{LOAD} = 8\ \Omega$ $L_{LOAD} = 10\ \mu\text{H}$ 1 kHz | | | 90 | % |
| THD | Total harmonic distortion | $P_{OUT} = 1.0\text{ W}$ $P_{OUT} = 500\text{ mW}$ gain = +6 dB | | -90 | | % dB |
| PSRR | Power supply rejection ratio | AC grounded 217 Hz | -66 | -90 | | dB |
| | | Inputs floating 217 Hz | -75 | -90 | | |
| CMRR | Common mode rejection ratio | 1 kHz | -60 | | | dB |
| BW | Bandwidth | | 20 | | 20,000 | Hz |
| A | Gain | | | +9 | | dB |
| f_{osc} | Internal oscillator frequency | | | 1 | | MHz |
| | Output offset | Referred to 0 dB | -5 | | +5 | mV |
| | Output noise | Integrated over BW gain = 6 dB SNR = 98 dB | | | 27 | μV_{RMS} |

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11.3.5 True-Ground Current Doubler

Table 44: True-Ground Charge Pump Performance Specifications

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------------|----------------------|----------------|-----|--|-----|------|
| V _{DD_CP_POS} | Positive rail output | | | V _{DD_CP} V _{DD_CP} / 2 | | V |
| V _{DD_CP_NEG} | Negative rail output | | | -V _{DD_CP} -(V _{DD_CP} / 2) | | V |
| | Flying capacitor | One capacitor | | 1.0 | | μF |
| | Reservoir capacitors | Two capacitors | | 1.0 | | μF |

11.4 Accessory Detection

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------|-------------------------------|------------|------|-----|------|------|
| | 3-pole jack resistance | | 0 | | 1050 | Ω |
| | 4-pole jack resistance | | 1.35 | | 25 | kΩ |
| | Hook/send button resistance | | 0 | | 108 | Ω |
| | Volume-up button resistance | | 139 | | 270 | Ω |
| | Volume-down button resistance | | 330 | | 680 | Ω |
| | Current consumption | | | | 15 | μA |

11.5 Codec Start-Up Time

After enabling the audio system controller using SYSTEM_MODES_CFGx, the start-up times for the various codec paths are as specified in [Table 45](#).

Table 45: Codec Start-Up Times

| Source | Output | Comment | Min | Typ | Max | Unit |
|----------------------------|------------------|--|-----|-----|-----|------|
| | V _{MID} | V _{MID} > 90% of final value 1μF capacitor | | 25 | | ms |
| Any analog input or DACL/R | HP_L HP_R | PLL bypass or PLL normal mode | 200 | 200 | | ms |
| Any analog input or DACL/R | HP_L HP_R | PLL SRM | | 500 | | ms |
| Any analog input | ADCL ADCR | PLL bypass or PLL normal mode | | 200 | | ms |
| Any analog input | ADCL ADCR | PLL SRM | | 600 | | ms |

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11.6 Clock Generation

11.6.1 Audio Reference Oscillator

Table 46: Audio Reference Oscillator Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|----------------------|----------------------|------------|-----|-----|-----|------|
| f _{OSC} | Oscillator frequency | | 10 | | 25 | MHz |
| t _{STARTUP} | Startup time | | | | 10 | μs |

11.6.2 MCLK Input

Table 47: MCLK Input

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|-----------------|-----------------------|------------|-----|------|------|
| V _{IN} | Input amplitude | MCLK squarer enabled | 0.3 | | AVDD | V |
| | | MCLK squarer disabled | 0.9 * AVDD | | AVDD | |
| R _{IN} | Input impedance | DC impedance > 10 MΩ | 300 | | | Ω |
| C _{IN} | Input impedance | DC impedance > 10 MΩ | 0.5 | 1 | 2 | pF |

11.6.3 Phase Lock Loop (PLL)

Table 48: PLL Mode

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|--------------------|--|-----|-----|-----|-------|
| J _C | MCLK input jitter | Cycle jitter (RMS) | | | 50 | ps |
| J _A | MCLK input jitter | Absolute jitter (RMS) | | | 100 | Ps |
| f _{IN} | Input frequency | Normal mode | 5 | | 50 | MHz |
| | SRM tracking range | AIF slave mode WCLK frequency variation | -4 | | 4 | % |
| | SRM tracking rate | AIF slave mode WCLK drift rate | | | 50 | ppm/s |

Table 49: Bypass Mode

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|-----------------|---|-----|---------|-----|------|
| f _{IN} | Input frequency | Sample frequency: 11.025, 22.05, 44.1, 88.2kHz | | 11.2896 | | MHz |
| | | Sample frequency: 8, 12, 16, 24, 32, 48, 96kHz | | 12.288 | | |

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11.7 Digital Interfaces

11.7.1 I/O Characteristics

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|-----------------|--|--------------|------------------------|-----|------------------------|------|
| V _{IH} | CLK, DATA, Input high voltage | VDDCORE mode | 1.0 | | | V |
| | | VDD_IO mode | 0.7*V _{DD_IO} | | | |
| V _{IL} | CLK, DATA, Input low voltage | VDDCORE mode | | | 0.4 | V |
| | | VDD_IO mode | | | 0.3*V _{DD_IO} | |
| V _{IH} | MCLK, BCLK, WCLK, DATIN, DATOUT Input high voltage | | 0.7*V _{DD_IO} | | | V |
| V _{IL} | MCLK, BCLK, WCLK, DATIN, DATOUT Input low voltage | | | | 0.3*V _{DD_IO} | V |
| V _{OL} | DATA output low voltage | | | | 0.24 | V |

11.7.2 I²C Control Bus

DA9066 has an I²C control bus with timing parameters illustrated in [Figure 24](#) and specified in [Table 50](#).

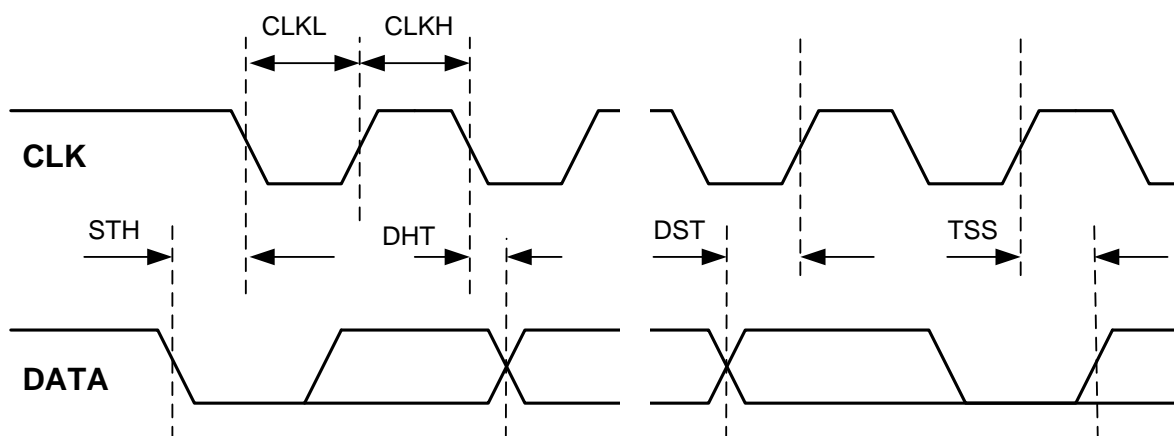


Figure 24: I²C Control Bus Timing Diagram

Table 50: I²C Control Bus Timing Specifications

| Parameter | Description | Conditions (Note 1) | Min | Typ | Max | Unit |
|---------------------------|-----------------------------|---------------------|-----|-----|-----|------|
| | Bus free time STOP to START | | 1.3 | | | μs |
| | Bus line capacitive load | | | | 100 | pF |
| Standard/Fast Mode | | | | | | |
| | CLK clock frequency | | 1 | | 400 | kHz |
| | Start condition setup time | | 0.6 | | | μs |
| STH | Start condition hold time | | 0.6 | | | μs |
| CLKL | CLK low time | | 1.3 | | | μs |
| CLKH | CLK high time | | 0.6 | | | μs |

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| Parameter | Description | Conditions (Note 1) | Min | Typ | Max | Unit |
|------------------------|----------------------------|---------------------|-----|-----|------|------|
| | CLK rise/fall time | | | | 300 | ns |
| | DATA rise/fall time | | | | 300 | ns |
| DST | DATA setup time | | 100 | | | ns |
| DHT | DATA hold time | | 0 | | | ns |
| TSS | Stop condition setup time | | 0.6 | | | μs |
| High Speed Mode | | | | | | |
| | CLK clock frequency | | 1 | | 1700 | kHz |
| | Start condition setup time | | 160 | | | ns |
| STH | Start condition hold time | | 160 | | | ns |
| CLKL | CLK low time | | 160 | | | ns |
| CLKH | CLK high time | | 60 | | | ns |
| | CLK rise/fall time | | | | 40 | ns |
| | DATA rise/fall time | | | | 80 | ns |
| DST | DATA setup time | | 10 | | | ns |
| DHT | DATA hold time | | 0 | | | ns |
| TSS | Stop condition setup time | | 16 | | | ns |

Note 1 $V_{DD_IO} = 1.2\text{ V}$, $V_{DD_DIG} = 1.1\text{ V}$, $V_{DDCORE} = 2.5\text{ V}$

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11.8 Digital Audio Interface

DA9066 has a digital audio interface bus (AIF) with timing parameters illustrated in Figure 25 and specified in Table 51.

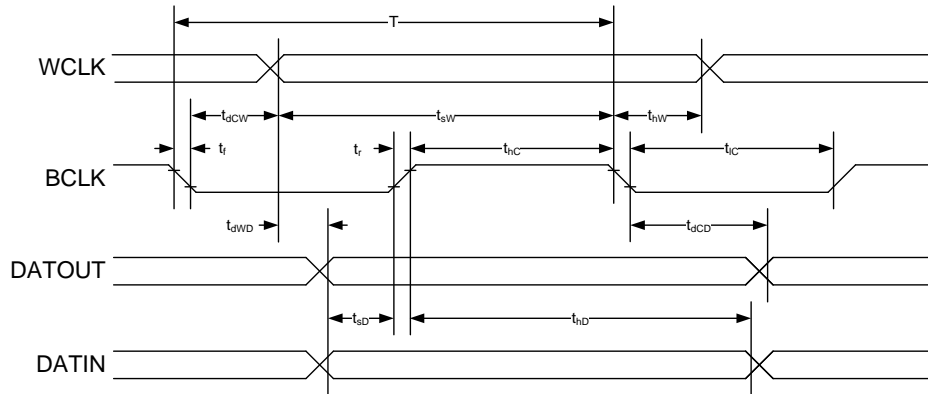


Figure 25: Digital Audio Interface Timing Diagram

Table 51: Digital Audio Interface Timing

| Parameter | Description | Conditions | Min | Typ | Max | Unit |
|------------------|---------------------------------|----------------------|-------------|-----|-----|--------------------------------|
| | Input impedance | DC impedance > 10 MΩ | 300 | | | Ω |
| | Input impedance | DC impedance > 10 MΩ | 1.0 | | 2.5 | pF |
| T | BCLK period | | 55 | | | ns |
| t _R | BCLK rise time | | | | 8 | ns |
| t _F | BCLK fall time | | | | 4 | ns |
| t _{HC} | BCLK high period As a % of T | Slave mode | 40 | | 60 | % |
| t _{LC} | BCLK low period As a % of T | Slave mode | 40 | | 60 | % |
| t _{DCW} | BCLK to WCLK delay | | -45 | | 45 | ns |
| t _{DCD} | BCLK to DATOUT delay | | 20 | | 36 | ns |
| t _{HW} | WCLK high time | DSP slave mode | 55 (Note 1) | | | ns |
| t _{LW} | WCLK low time | DSP slave mode | 55 | | | ns |
| t _{SW} | WCLK setup time | Slave mode | | | 7 | ns |
| t _{HW} | WCLK hold time | Slave mode | 2 | | | ns |
| t _{SD} | DATIN setup time | | | | 7 | ns |
| t _{HD} | DATIN hold time | | 2 | | | ns |
| t _{DWD} | DATOUT to WCLK delay | | | | | DATOUT is synchronized to BCLK |

Note 1 Minimum one complete clock period

12 Audio Functional Description

12.1 Input Signal Chain

DA9066 has a stereo pair of single-ended line inputs as well as three microphone inputs, each of which can be configured as single-ended or differential. Both line and microphone signals can be routed to the ADC or directly to the output mixers via a bypass path. In addition, DA9066 supports both single- and dual-channel digital microphone inputs by routing the digital signals directly to the ADC digital filters. The input routing paths and input amplifier gain ranges are shown in Figure 26, the gain ranges are shown in MIN:STEP:MAX format.

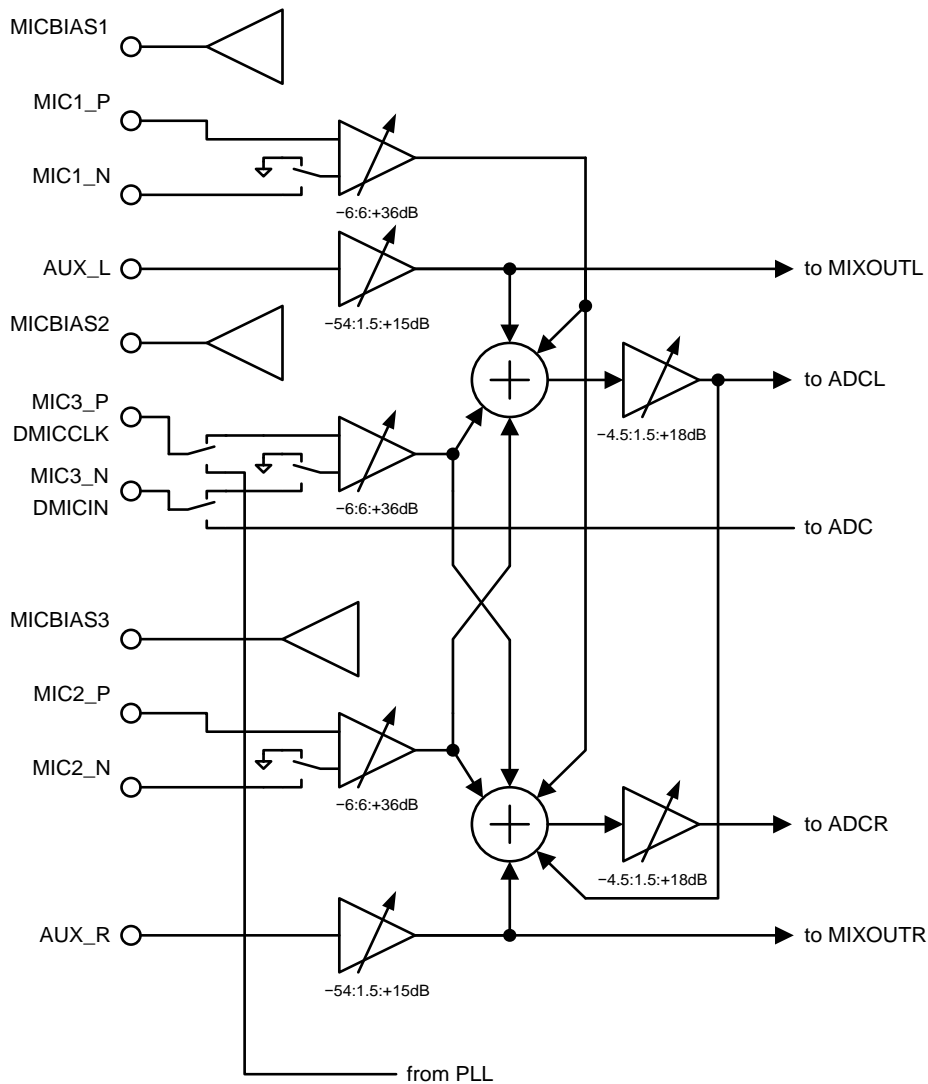


Figure 26: Audio Input Routing Signal Paths and Gain Ranges

System PMIC for Dual/Quad-Core Processors

12.1.1 Analog Microphones

DA9066 includes three pairs of analog microphone inputs, configurable in three different ways, as shown in Figure 27. The microphone amplifiers can be set to single-ended or differential mode using MIC_L_AMP_DIFF_EN and MIC_R_AMP_DIFF_EN.

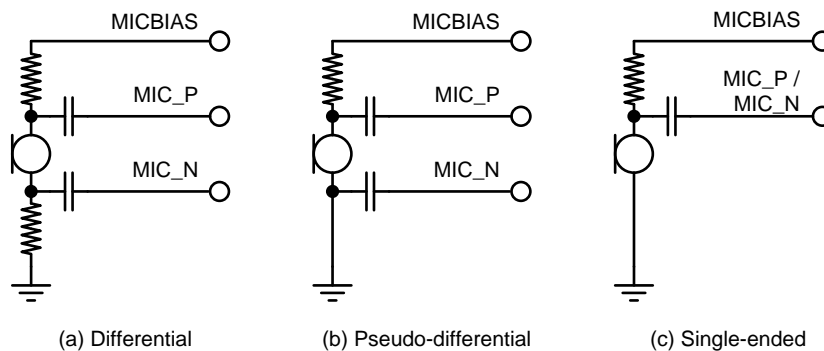


Figure 27: Analog Microphone Configurations

The microphone PGAs are enabled using MIC_L_EN, MIC_R_EN, and MIC_EXT_EN and can be muted using MIC_L_AMP_MUTE_EN, MIC_R_AMP_MUTE_EN, and MIC_EXT_AMP_MUTE_EN.

For maximum flexibility the gain of each microphone channel amplifier can be set in the range of -6 dB to +36 dB in 6 dB steps using MIC_L_GAIN (for MIC1P/N), MIC_R_GAIN (for MIC2P/N), and MIC_EXT_GAIN (for MIC3P/N). The currently active gain setting for each microphone amplifier is stored in MIC_L_GAIN_STATUS, MIC_R_GAIN_STATUS, and MIC_EXT_GAIN_STATUS.

Gain updates can be synchronized with signal zero-crossings by setting MIC_L_AMP_ZC_EN, MIC_R_AMP_ZC_EN, and MIC_EXT_AMP_ZC_EN. If no zero-crossing is detected within the timeout period, the gain change is applied unconditionally.

Standard electret microphones can be supplied from an embedded microphone bias regulator, enabled using the MICBIAS1_EN, MICBIAS2_EN and MICBIAS3_EN register bits. Three separate outputs are available on the MICBIAS1, MICBIAS2, and MICBIAS3 pins.

The voltage on the MICBIAS2 and MICBIAS3 pins is set to 1.6 V, 2.2 V, 2.5 V, or 3.0 V by the MICBIAS2_LEVEL and MICBIAS3_LEVEL bits. The microphone bias generates an ultra-low noise voltage to feed several electret microphones with up to 2 mA.

12.1.2 Digital Microphones

DA9066 implements a digital microphone interface consisting of a clock output, DMICCLK (shared pin with MIC3_P) and serial digital data input, DMICIN (shared pin with MIC3_N). The sharing of the clock and data pins with the two analog microphone inputs allows DA9066 to record from single or dual channel digital microphones, or from conventional mono/stereo analog microphones.

The digital microphone module is supplied from the MICBIAS2 pin. A digital microphone requires a decimation filter to reconstruct the signal at the required sampling rate. The ADC decimation filters are re-used for this purpose, so either digital microphones or analog sources may be used for recording at any one time.

The digital microphone interface is enabled by setting either DMIC_L_EN or DMIC_R_EN. The DMICCLK output may be set to either 1.5 MHz or 3 MHz using DMIC_CLK_RATE. The clock edges associated with left and right data may be changed using DMIC_DATA_SEL. The data sampling phase can be adjusted by 90° using DMIC_SAMPLEPHASE.

Single channel and dual channel digital microphone modules are supported. The dual channel modules change the output data on both the rising and the falling edges of the clock, see Figure 28. In this case DMIC_SAMPLEPHASE must be set to zero in order to enable the sample detection at the edges of the clock. Each DMIC input is enabled via DMIC_L_EN and DMIC_R_EN, and is associated with a clock edge via DMIC_DATA_SEL control.

System PMIC for Dual/Quad-Core Processors

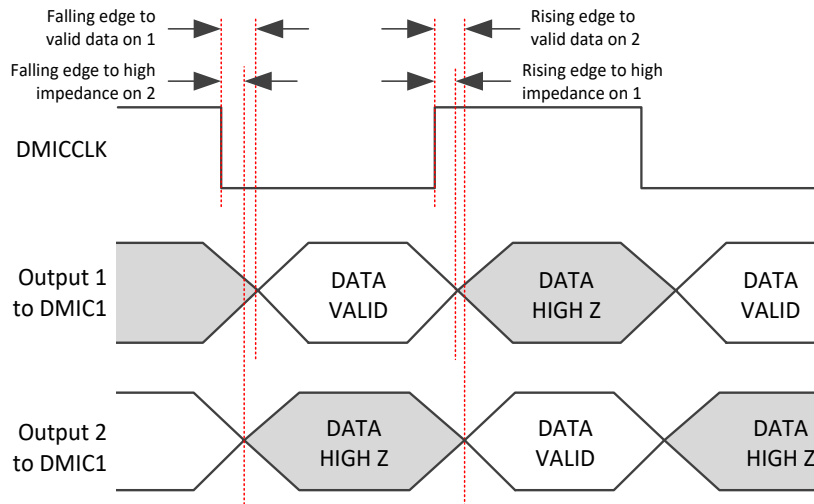


Figure 28: Digital Microphone Timing

12.1.3 Microphone Biases

DA9066 has three separate independently-controlled microphone bias circuits which are nominally associated with each of the three microphone input channels. Each microphone bias is a low-noise programmable voltage source that can be used to supply analog or digital microphones.

The MICBIAS circuits are enabled using MICBIAS1_EN, MICBIAS2_EN, and MICBIAS3_EN.

Each MICBIAS voltage can be set to 1.6 V, 2.2 V, 2.5 V, or 3.0 V using MICBIAS_1_LEVEL, MICBIAS_2_LEVEL, and MICBIAS_3_LEVEL.

12.1.4 Auxiliary Inputs

Standard analog sources (for example FM radio) are supported via the stereo line inputs AUX_L and AUX_R. The auxiliary amplifiers are enabled using AUX_L_AMP_EN and AUX_R_AMP_EN. They can be summed with each other, and with the microphone paths, which enables flexible audio mixing. Mono sound sources are intended to be connected to AUX_R.

Each channel includes individual gain settings in 1.5 dB steps from -54 dB to +15 dB using AUX_L_AMP_GAIN and AUX_R_AMP_GAIN. The auxiliary amplifiers can be muted by asserting AUX_L_AMP_MUTE_EN and AUX_R_AMP_MUTE_EN.

Gain updates can be synchronized with signal zero-crossings by asserting the AUX_L_AMP_ZC_EN and AUX_R_AMP_ZC_EN bits. If no zero-crossing is detected within the timeout period (approximately 85 ms), the gain change is applied unconditionally.

The sensitivity of the zero-cross detector is maximized by automatic selection of whether the zero-cross detection is performed at the input to the AUX amplifier, or the output from it. This is configured using the AUX_L_AMP_ZC_SEL and AUX_R_AMP_ZC_SEL controls.

Smooth changes in gain are enabled by asserting the AUX_L_AMP_RAMP_EN and AUX_R_AMP_RAMP_EN controls. If the ramp controls are asserted, the rate of ramping is specified by the GAIN_RAMP_RATE bits. Any zero-cross activation is over-ridden if gain ramping is set.

The currently active gain setting for each auxiliary amplifier is stored in AUX_L_GAIN_STATUS and AUX_R_GAIN_STATUS.

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12.1.5 Input Mixers

The DA9066 has two second-level input amplifiers (MIXIN_L and MIXIN_R) that mix the analog inputs and provide up to 18 dB of additional gain. The input mixer amplifiers are enabled using MIXIN_L_AMP_EN and MIXIN_R_AMP_EN.

The gain of each mixer amplifier can be set in the range of -4.5 dB to +18 dB in 1.5 dB steps using MIXIN_L_GAIN and MIXIN_R_GAIN. The currently active gain setting for each mixer amplifier is stored in MIXIN_L_GAIN_STATUS and MIXIN_R_GAIN_STATUS.

Zero-crossing can be enabled by setting MIXIN_L_AMP_ZC_EN and MIXIN_R_AMP_ZC_EN. If no zero-crossing is detected within the timeout period (approximately 85 ms), the gain change is applied unconditionally. Smooth changes in gain are enabled by asserting the MIXIN_L_AMP_RAMP_EN and MIXIN_R_AMP_RAMP_EN bits. In this case, the rate of ramping is specified by the GAIN_RAMP_RATE control. Any zero-cross activation is over-ridden if gain ramping is set.

The left mixer will accept inputs from AUXL_PGA and from all of the microphone PGAs (MIC1_PGA, MIC2_PGA, and MIC3_PGA). Similarly, the right channel mixer will accept input signals from AUXR_PGA and from all of the microphone PGAs (MIC1_PGA, MIC2_PGA, and MIC3_PGA). Additionally, the right mixer accepts input from MIXIN_L for stereo-to-mono conversion. The channel input selection is determined using MIXIN_L_MIX_SELECT and MIXIN_R_MIX_SELECT.

The mixer amplifiers can be muted using MIXIN_L_AMP_MUTE_EN and MIXIN_R_AMP_MUTE_EN.

12.1.6 Stereo Audio ADC

DA9066 includes a low power 24-bit high quality audio ADC that supports sampling rates from 8 kHz to 96 kHz.

To use the audio ADC, a valid master clock signal must be provided at the MCLK pin with the PLL enabled or disabled as required. The ADC is clocked at a fixed rate of either 3.072 MHz or 2.8224 MHz, depending on the required output sample rate. The sample rate is specified using the SR register.

The ADC can be enabled and disabled on either channel using ADC_L_EN and ADC_R_EN, thereby providing the opportunity to save power during mono operation.

The ADC channels offer a configurable digital gain from -83.25 dB to +12 dB in 0.75 dB steps after the digital conversion. Individual gain settings can be programmed via controls ADC_L_DIGITAL_GAIN and ADC_R_DIGITAL_GAIN. The currently active gain settings are stored in ADC_L_GAIN_STATUS and ADC_R_GAIN_STATUS registers.

Muting, and the ramping of digital gain changes, can be controlled using the dedicated ADC_L_CTRL and ADC_R_CTRL registers. The ADC output is muted using the ADC_L_MUTE_EN and ADC_R_MUTE_EN bits. If the ramping is enabled, using the register bits ADC_L_RAMP_EN and ADC_R_RAMP_EN, the rate of the ramping is controlled using GAIN_RAMP_RATE.

To enable saturation-free signals with maximum signal to noise ratios, the input levels of the ADC are adjusted with second level PGAs that are enabled with controls MIXIN_L_AMP_EN and MIXIN_R_AMP_EN. The signal routing and mix are configured using the MIXIN_L_SELECT and MIXIN_R_SELECT registers.

On the dedicated MIXIN_L_CTRL and MIXIN_R_CTRL registers, settings such as gain changes at zero-cross (for smooth volume changes), ramping of gain changes at signal zero cross ramping of gain changes, and mute can be configured. If the ramping is enabled using the control bits MIXIN_L_AMP_RAMP_EN and MIXIN_R_AMP_RAMP_EN, the speed of the ramp can be configured on GAIN_RAMP_RATE.

NOTE

The ADC digital high-pass filter must be enabled whenever the ADC output is routed to the DAC input.

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12.1.7 Audio Accessory Detection

DA9066 contains an audio accessory detection (AAD) block which is capable of detecting the insertion/removal of an audio jack as well the button presses from headsets, for example volume up/down controls. The AAD system is on a separate power domain from the codec and so can remain active even when the codec is powered down.

The AAD system can support both 3-pole (TRS) and 4-pole (TRRS) jack connectors. The 3-pole jack is configured (from tip to sleeve) as headphone left, headphone right, and ground. The 4-pole jack is configured (from tip to sleeve) as headphone left, headphone right, ground and microphone. The socket for a 4-pole jack has an additional contact which is electrically shorted to the tip whenever a jack is inserted.

The AAD system can detect the insertion and the removal of an audio jack and can detect the press and release of a headset button. Jack insertion/removal and button presses are both maskable events which can trigger the PMIC to raise an nIRQ signal to the host. In addition, the AAD system can measure the impedance associated with a button press so that the host can determine which of the buttons has been pressed. Upon receipt of the interrupt the host can read the status register to determine which event has occurred and the value of any button press.

The AAD system is enabled using ACCDET_EN and has three different operating modes: no jack inserted, 3-pole jack inserted, and 4-pole jack inserted. The time interval between each button/jack measurement can be set independently for each of the three operating modes in the range of 0.256 ms to 262 ms using ACCDET_[NO|THREE_POLE|FOUR_POLE]_JACK_RATE.

The debounce time for the jack and button detection measurement can be set in the range of 1 kHz to 4 32 kHz clock cycles using ACCDET_JACK_DEBOUNCE and ACCDET_BTN_DEBOUNCE respectively.

The MICDET pin of the AAD system should be decoupled to GND with a 47 nF ceramic capacitor, placed close to the pin. MICBIAS1 should be used for the AAD system.

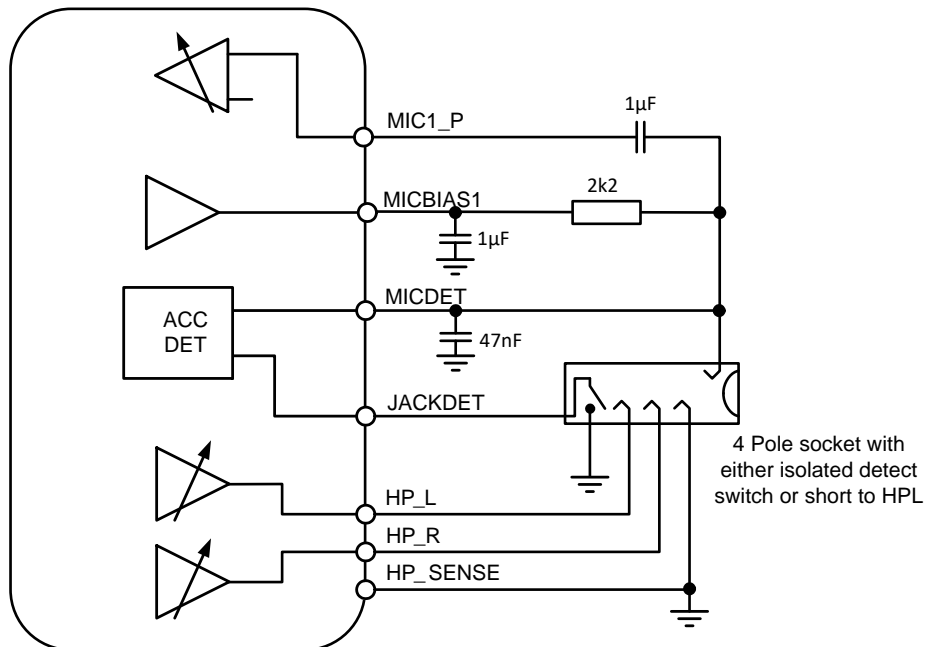


Figure 29: AAD Application Diagram

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12.2 Outputs Signal Chain

DA9066 has four audio outputs: a stereo Class-G headphone driver, a mono Class-G earpiece/receiver driver, and a mono Class-D speaker driver. Three output mixers allow the combination of signals from the DACs and analog bypass paths to the four output amplifiers.

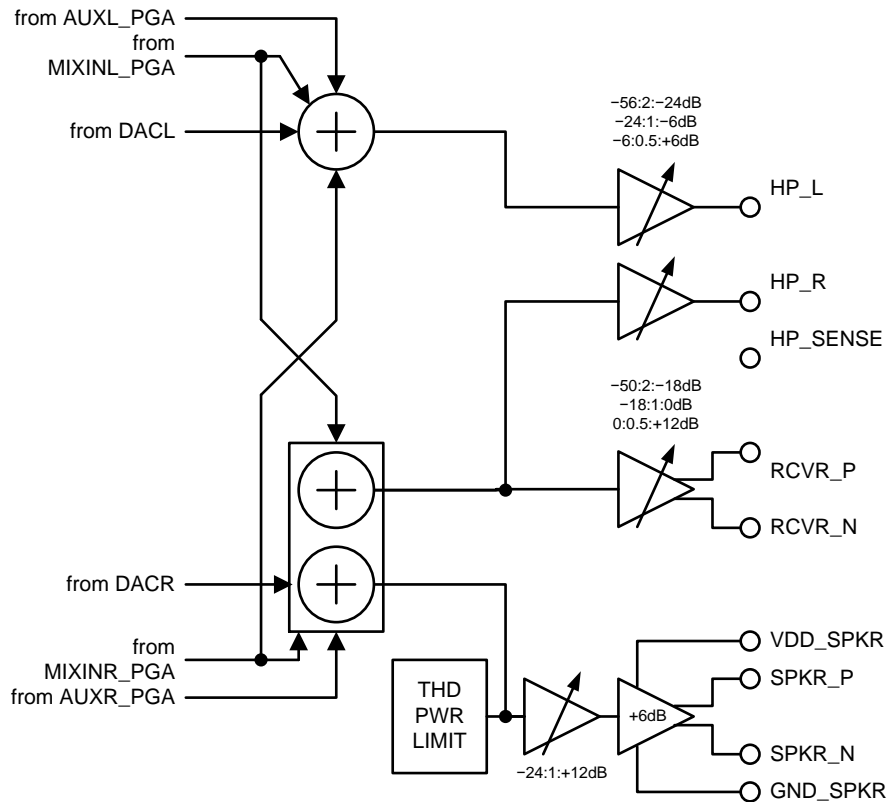


Figure 30: Analog Output Routing Signal Paths

12.2.1 Stereo Audio DAC

The integrated stereo DAC is suitable for high quality audio playback by MP3 players and by portable multimedia players of all kinds.

The DAC is clocked at a fixed rate of either 3.072 MHz or 2.8224 MHz, depending on the required output sample rate. To use the DAC, a valid master clock signal must be provided at the MCLK pin with the PLL enabled or disabled as required.

The left and right channels of the DAC can be individually enabled using controls DAC_L_EN and DAC_R_EN. Either channel of the DAC can be disabled to provide optimum power dissipation in mono operation.

Each channel includes individual gain settings that are controllable in 0.75 dB steps from -78 dB to 12 dB using DAC_L_DIGITAL_GAIN and DAC_R_DIGITAL_GAIN. The currently active gain settings are stored in the DAC_L_GAIN_STATUS and DAC_R_GAIN_STATUS registers.

On the dedicated DAC_L_CTRL and DAC_R_CTRL registers, settings such as mute and ramping of gain changes can be configured. The DAC output can be muted using the DAC_L_MUTE_EN and DAC_R_MUTE_EN bits. If ramping is enabled, using the control bits DAC_L_RAMP_EN or DAC_R_RAMP_EN, the rate of the ramping can be controlled using GAIN_RAMP_RATE.

A digital high-pass filter for each DAC channel is implemented with a 3 dB cut-off frequency controlled by DAC_AUDIO_HPF_CORNER. The high-pass filter is enabled by register bit DAC_HPF_EN. After reset, the high pass filters for both channels are enabled by default.

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12.2.2 Output Mixers

There are three output mixers connected to the four output amplifiers as shown in Figure 30. The output mixers are enabled using register bits MIXOUT_L_AMP_EN, MIXOUT_R_AMP_EN, and MIXOUT_SP_AMP_EN. The audio signal can be mixed from all sources, and can be output simultaneously to both headphones and speakers. The mixing only takes place after asserting the output mixer enable bits.

To allow the selection of mixer input channels to be changed silently, each mixer implements a soft mixer function. The soft mixing function for all inputs is enabled using MIXOUT_L_SOFTMIX_EN, MIXOUT_R_SOFTMIX_EN, and MIXOUT_SP_SOFTMIX_EN.

One mixer is dedicated to the left-channel headphone amplifier, one is dedicated to the Class-D speaker driver, and the other is shared between the earpiece/receiver amplifier and the right-channel headphone amplifier.

The left-channel headphone mixer accepts input signals from DACL, analog bypass signals from MIXINL_PGA and AUXL_PGA, and from MIXINR_PGA for stereo-to-mono conversion. The remaining two output mixers accept input signals from DACR, analog bypass signals from MIXINR_PGA and AUXR_PGA, and from MIXINL_PGA for stereo-to-mono conversion. The headphone mixer input selection is made using the register bits MIXOUT_L_SELECT and MIXOUT_R_SELECT, and the speaker mixer input selection by the MIXOUT_SP_SELECT bits.

The output-mixer control is independent of the input path, so recording of one audio signal while listening to another signal such as FM Radio or an MP3 file is possible. The playback sound can be mixed with background signals or with inverted background microphone signals (side tone) to enable a basic headphone environmental noise reduction, or to compensate for unwanted damping of environmental sound while listening with sealed headphones. Playback signals coming from the AUX or microphone input channels can be individually inverted before being mixed out to the left and right channel by setting the selection register bits accordingly.

12.2.3 Receiver/Earpiece Amplifier

The earpiece driver is a Class-G amplifier with a true-ground differential output designed to drive a 32 Ω load. The true-ground technology removes the requirement for ac-coupling capacitors which reduces the cost and space of external components and improves the bass performance. In comparison to alternative approaches, such as phantom ground, true-ground technology generates real-ground centered output signals which provide common GND, as required for mini-USB connectors and CEA 936 A compliant interfaces.

An embedded offset compensation circuit suppresses click and pop noise during start-up and dynamic supply voltage adjustments; this is enabled by asserting register bit EP_AMP_OE.

The earpiece amplifier, EP_PGA, is enabled using register bit EP_AMP_EN and has a configurable gain range of -50.0 dB to +12.0 dB, set by register bits EP_GAIN.

The actual gain steps implemented by the analog circuit are:

- 2 dB from -50 dB to -18 dB
- 1 dB from -18 dB to 0 dB
- 0.5 dB from 0 dB to +12 dB

The currently active gain setting for the earpiece amplifier is stored in EP_GAIN_STATUS.

Settings such as mute, gain changes at signal zero cross (for smooth volume changes), and the ramping of gain changes are controlled using the dedicated EP_CTRL registers. The earpiece amplifier can be muted using EP_AMP_MUTE_EN. Gain updates can be synchronized with signal zero-crossings by asserting the register bit EP_AMP_ZC_EN. If no zero-crossing is detected within the timeout period (approximately 85 ms), the gain change is applied unconditionally.

As an alternative to zero-cross synchronization, gain updates can be made by ramping through all intermediate gain values by enabling bit EP_AMP_RAMP_EN.

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12.2.4 Stereo Headphone Amplifier

The headphone amplifiers also have a true-ground output. These are capable of driving loads as low as 16 Ω , the paths can also be used as volume controlled line-out signals for external speaker amplifiers and audio devices. Integrated short circuit protection enables a resistor-free connection to a standard audio jack, to achieve a maximum output power of up to 67 mW per channel (referenced to VDD_A). The headphone Class G amplifiers are supplied from the positive VDD_A rail via a capacitive charge pump that generates the negative rail required for true-ground operation. For improved power efficiency, the headphone amplifier supply voltage levels are dynamically adjusted between $\pm V_{DD_A}$ and $\pm V_{DD_A}/2$ to match the levels of the left and right headphone signals.

An embedded offset compensation circuit suppresses click and pop noise during start-up and dynamic supply voltage adjustments; this is enabled by asserting register bits HP_L_OE and HP_R_OE.

The headphone amplifiers, HP_L_PGA and HP_R_PGA, are enabled using HP_L_AMP_EN and HP_R_AMP_EN. Each channel has a configurable gain range of -56.0 dB to +6 dB, set by the register bits HP_L_GAIN and HP_R_GAIN.

The actual gain steps implemented by the analog circuit are:

- 2 dB from -56 dB to -24 dB
- 1 dB from -24 dB to -6 dB
- 0.5 dB from -6 dB to +6 dB

The currently active gain setting for each headphone amplifier is stored in HP_L_GAIN_STATUS and HP_R_GAIN_STATUS.

Settings such as mute, gain changes at signal zero cross (for smooth volume changes), and the ramping of gain changes are controlled using the dedicated HP_L_CTRL and HP_R_CTRL registers. The earpiece amplifier can be muted using HP_L_AMP_MUTE_EN and HP_R_AMP_MUTE_EN. Gain updates can be synchronized with signal zero-crossings by asserting the register bits HP_L_AMP_ZC_EN and HP_R_AMP_ZC_EN. If no zero-crossing is detected within the timeout period (approximately 85 ms), the gain change is applied unconditionally.

As an alternative to zero-cross synchronization, gain updates can be made by ramping through all intermediate gain values by enabling bits HP_L_AMP_RAMP_EN and HP_R_AMP_RAMP_EN.

12.2.5 Speaker Amplifier

The differential speaker amplifier can be used to drive mini-speakers with an impedance of 8 Ω or higher. A direct supply from the battery is provided by the VDD_SPKR pin. This allows maximum speaker power and a wide operating range from 5.0 V down to 1.0 V. This amplifier offers individually programmable volume control in 1.0 dB steps from -24 dB to 12 dB using SP_AMP_GAIN.

In the dedicated SP_CTRL register, settings such as mute, output mode and ramping of gain changes can be configured. If ramping is enabled via control bit SP_AMP_RAMP_EN, the rate of the ramping can be configured by GAIN_RAMP_CTRL.

If the speaker output is not used then VDD_SPKR can be left unconnected.

12.2.5.1 Distortion and Power Limiter

The Class-D speaker driver uses an automatic gain control (AGC) circuit to limit the output power and/or the signal distortion (THD). The power limiter is designed to prevent damage to the speaker, whereas the distortion limiter can be used to preserve the same signal quality regardless of battery voltage.

Both power and distortion limiters use the AGC which can be activated whenever either the power or the distortion limit is exceeded.

The power limiter is enabled by setting SP_PWR_LIMIT_EN. The maximum output power that can be achieved is set by programming SP_PWR_LIMIT.

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The distortion limiter is enabled by setting SP_THD_LIMIT_EN. The maximum distortion level that is tolerated is set by programming SP_THD_LIMIT.

The attack rate of the AGC can be set in the range of 30 μ s/dB to 2 ms/dB using SP_ATK_RATE.

The release rate of the AGC can be set in the range of 20 ms/dB to 1 s/dB using SP_REL_RATE.

The hold time of the AGC can be set using SP_HLD_TIME.

12.2.6 Charge Pump Control

Both the headphone and earpiece amplifiers are supplied by the true-ground charge pump that generates positive and negative rails so that amplifier outputs can remain centered around 0 V. For improved power efficiency the charge pump provides dynamically adjusted supply voltage levels of CPVDD/1 and CPVDD/2.

The charge pump is enabled by asserting the CP_EN bit in the CP_CTRL register. Once enabled, the charge pump can be controlled manually or automatically. When under manual control (CP_MCHANGE = 00), the output voltage level is directly determined by CP_MOD.

The amount of charge stored, and therefore the voltage generated, by the charge pump is controlled by the charge pump controller (CP_CTRL register). As the power consumed by devices such as amplifiers is proportional to Voltage², significant power savings are available by matching the charge pump's output with the system's power requirement.

Under automatic control, there are three modes of operation that are determined by the CP_MCHANGE setting. All four modes (one manual and three automatic) are described in [Table 52](#).

Table 52: Charge Pump Output Voltage Control

| Charge Pump Tracking Mode CP_MCHANGE | Charge Pump Output Voltage | Details |
|---|---|---|
| 00 | Manual | The charge pump's output voltage is determined by the settings of CP_MOD. |
| 01 | Voltage level depends on the programmed gain setting | The charge pump controller monitors the PGA volume settings (HP_L_GAIN or HP_R_GAIN, or EP_GAIN), and generates the minimum voltage that is high enough to drive a full-scale signal at the current gain level. |
| 10 | Voltage level depends on the DAC signal envelope | The charge pump controller monitors the DAC signal, and generates a voltage that is high enough to drive a full-scale output at the current DAC signal volume level |
| 11 | Voltage level depends on the signal magnitude and the programmed gain setting | The charge pump monitors both the programmed volume settings and the actual signal size, and generates the appropriate output voltage. This is the most power-efficient mode of operation. |

When CP_MCHANGE is set to 10 (tracking DAC signal size) or to 11 (tracking the output signal size), the charge pump switches its supply between the CPVDD/1 rail and the CPVDD/2 rail depending on its power requirements. When low output voltages are needed, the charge pump saves power by using the lower-voltage CPVDD/2 rail.

The switching point between using the CPVDD/1 rail and the CPVDD/2 rail is determined by the CP_THRESH_VDD2 register setting. The switching points vary between the two CP_MCHANGE modes, and are summarized in [Table 53](#) and [Table 54](#).

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Table 53: CP_THRESH_VDD2 Settings when Tracking DAC Signal Size

| CP_THRESH_VDD2 Setting | Approximate Switching Point dBFS (Note 1) | Comment |
|------------------------|---|--|
| 0x01 | -30 | Do not use. Very power-inefficient as nearly always CPVDD/1 |
| 0x03 | -24 | Not recommended. Very power-inefficient as nearly always CPVDD/1 |
| 0x07 | -18 | Good to use but not power efficient |
| 0x0E | -12 | Good to use |
| 0x10 | -10 | Recommended setting |
| 0x3F to 0x13 | | Not recommended |

Note 1 Full Scale (FS) = $1.6 * V_{DD_A}$

Table 54: CP_THRESH_VDD2 Settings when Tracking Output Signal Size

| CP_THRESH_VDD2 Setting | Approximate Switching Point dBFS (Note 1) | Comment |
|------------------------|---|--|
| 0x00 | Never | Not recommended. Always CPVDD/1 mode |
| 0x01 | Never | Not recommended. Always CPVDD/1 mode |
| 0x02 | -32 | Not recommended. Very power-inefficient as nearly always CPVDD/1 |
| 0x03 | -24 | Good to use |
| 0x04 | -20 | Good to use |
| 0x05 | -17 | Good to use |
| 0x06 | -15 | Recommended setting |
| 0x07 | -13 | Good to use |
| 0x08 | -12 | Good to use |
| 0x09 | -11 | Good to use |
| 0x0A | -10 | Good to use |
| 0x0B | -9 | Not recommended. CPVDD/2 begins to clip |
| 0x0C | Never | Not recommended. Always CPVDD/2 mode |
| 0x0D | Never | Not recommended. Always CPVDD/2 mode |
| 0x0E | Never | Not recommended. Always CPVDD/2 mode |
| 0x0F | Never | Not recommended. Always CPVDD/2 mode |

Note 1 Full Scale (FS) = $1.6 * V_{DD_A}$

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12.2.6.1 Charge Pump Clock Control

The charge pump on DA9066 requires two clocks (cp_clk and cp_clk2). The cp_clk2 clock runs at a slower frequency than cp_clk. It is cp_clk that actually clocks the charge pump.

To prevent the clocks stopping in an unknown state, there are always two pulses on cp_clk for every one pulse of cp_clk2.

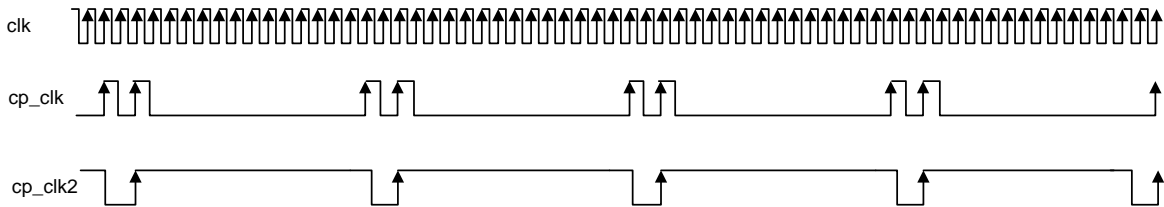


Figure 31: Input (clk) and Output Clocks (cp_clk and cp_clk2) at CP_FCONTROL = 010

When CP_ANALOGUE_LVL = 00 ('No feedback', see Section 12.2.6.2), the charge pump's nominal clock rate cp_clk is controlled by CP_FCONTROL, providing a range from 1 MHz (CP_FCONTROL = 000) down to 63 kHz (CP_FCONTROL = 100). With the slower clock rates, quiescent power consumption is lower but the trade-off is a reduced load current and slower changes to the voltage.

Section 12.2.6.2 and 12.2.6.6 describe how quiescent power and load current can be varied according to demand.

12.2.6.2 Boosting the Charge Pump Using Demand Feedback Control

When CP_ANALOGUE_LVL = 00, the clock frequency for the charge pump is under direct control of the registers as described in Table 67.

When CP_ANALOGUE_LVL = 01 or 10 (11 is reserved and is not used), the demands on the charge pump output are tracked, and the clock frequency is boosted when necessary to give the required output current.

This gives the benefit of a very low (or even zero) quiescent current when the charge pump is not required combined with a maximum output when that is required.

12.2.6.3 Tracking the Demands on the Charge Pump Output

There are three points at which the demands on the charge pump can be tracked, see Table 55. This provides the feedback to boost the clock frequency when necessary. These tracking points are determined by the setting in register bits CP_MCHANGE.

Table 55: Charge Pump Output Demand Tracking

| MCHANGE Setting | Tracking Mode |
|-----------------|--|
| 00 | Manual, the voltage level is controlled by the CP_MOD setting |
| 01 | Tracking the PGA gain setting |
| 10 | Tracking the DAC signal setting |
| 11 | Tracking the output signal magnitude and the programmed gain setting |

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12.2.6.4 Specifying Clock Frequencies when Tracking the Charge Pump Output Demand

CP_FCONTROL specifies the frequency of the charge pump clock. The frequency is fixed and is set manually if CP_MCHANGE = 00 (see Section 12.2.6). The available frequency settings are 1 MHz (the absolute maximum), and 500 kHz, 250 kHz, 125 kHz, and 63 kHz.

For all other CP_MCHANGE settings, the charge pump load is monitored and the clock frequency adjusted accordingly to allow the charge pump to supply the required current. Clock frequency varies depending on the charge pump requirements, and the CP_FCONTROL settings specify the minimum frequency at which the clock will run. The maximum frequency is always 1 MHz.

In addition to the CP_FCONTROL settings outlined above, and which specify the minimum clock frequency, there is an extra setting of CP_FCONTROL = 101 which has no minimum frequency. The clock frequency is under the complete control of the tracking and feedback mechanism. The frequency can vary from 0 Hz when there is no load on the charge pump and no component leakage, up to the maximum of 1 MHz.

These settings are all summarized in Table 67.

12.2.6.5 Controlling the Boost of the Charge Pump Clock-Frequency

The manner in which the charge pump clock-frequency is boosted is controlled by CP_ANALOGUE_LVL. If CP_ANALOGUE_LVL = 00, there is no feedback to the clock generator, and the frequency remains fixed at the frequency specified by CP_FCONTROL.

CP_ANALOGUE_LVL = 01

If CP_ANALOGUE_LVL = 01, the clock frequency is boosted from the base frequency specified in CP_FCONTROL by the insertion of extra clock pulses in to the clock signal as and when required. When no extra pulses are being inserted, the clock frequency remains fixed at the value specified by CP_FCONTROL. The extra clock pulses are inserted in to the clock signal as needed as long as the clock frequency does not exceed its maximum of 1 MHz.

CP_ANALOGUE_LVL = 10

If CP_ANALOGUE_LVL = 10, instead of boosting the clock frequency by inserting extra clock pulses the clock is restarted. By restarting the clock before the next pulse is due, the frequency is effectively increased. The clock frequency can be increased from the minimum frequency specified in CP_FCONTROL, up to the maximum frequency of 1 MHz.

These settings are summarized in Table 56.

Table 56: Charge Pump Current Load Control

| CP_FCONTROL (0x96[2:0]) | CP_ANALOGUE_LVL (0x47[1:0]) | | | |
|----------------------------|-----------------------------|---|---|----------|
| | 00 No Current Boost | 01 Variable Current Boost (Note 1) | 10 Variable Current Boost (Note 1) | 11 |
| 000 | 1 MHz | 1 MHz | 1 MHz | Reserved |
| 001 | 500 kHz | From 500 kHz to 1 MHz depending on demand | From 500 kHz to 1 MHz depending on demand | Reserved |
| 010 | 250 kHz | From 250 kHz to 1 MHz depending on demand | From 250 kHz to 1 MHz depending on demand | Reserved |
| 011 | 125 kHz | From 125 kHz to 1 MHz depending on demand | From 125 kHz to 1 MHz depending on demand | Reserved |
| 100 | 63 kHz | From 63 kHz to 1 MHz depending on demand | From 63 kHz to 1 MHz depending on demand | Reserved |

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| CP_FCONTROL | CP_ANALOGUE_LVL (0x47[1:0]) | | | |
|-------------|-----------------------------|-----------------------------------|-----------------------------------|----------|
| 101 | Reserved | 0 Hz to 1 MHz depending on demand | 0 Hz to 1 MHz depending on demand | Reserved |
| 110 | Reserved | Reserved | Reserved | Reserved |
| 111 | Reserved | Reserved | Reserved | Reserved |

Note 1 Power demand is determined by the PGA gain level if CP_MCHANGE = 01, by the DAC signal level if CP_MCHANGE = 10, or by the output signal level if CP_MCHANGE = 11

12.2.6.6 Other Charge Pump Controls

When a higher charge pump output voltage is needed, the charge pump increases its output as the fastest rate possible given the controls and settings in that currently in place. Once the higher output voltage is no longer needed, the charge pump controller waits for a period determined by the CP_TAU_DELAY setting before reducing the output voltage. For best performance Dialog recommend setting CP_TAU_DELAY to 16 ms or greater.

The charge pump limiter is controlled by CP_ON_OFF. The limiter restricts the current flow to the charge pump's capacitors at start-up.

CP_SMALL_SWITCH_FREQ_EN enables a low-load, low-power switching mode.

If CP_SMALL_SWITCH_FREQ_EN is enabled and CP_FCONTROL is set to a value between 000 and 100, any feedback from the analog level detector results in a switch from low-power to full-power. Full-power is maintained for one CP_TAU_DELAY period after the pulse. Any subsequent pulses restart the CP_TAU_DELAY period.

If CP_FCONTROL = 101, the first feedback from the analog level detector primes the change to full-power mode. If another pulse occurs within 32 clock cycles of the first feedback from the analog level detector, full power is enabled for one CP_TAU_DELAY period.

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12.3 Digital Signal Processing

The digital signal processing engine includes a configurable audio processor that offers flexible routing and extensive audio enhancement and effects. Linear phase FIR filters perform the DAC interpolation and decimation for the required sample rates. Configurable high-pass filtering (optionally enabled on both ADC and DAC) removes any signal DC offset and can help to filter out wind noise. A 5-band playback equaliser can be configured to suit the users listening preferences.

12.3.1 Variable High-Pass Audio Filter (DC Cut)

Any DC offset from the input path is removed via IIR filters (typically <2 Hz roll-off, configurable). After reset the filters for both channels are enabled by default, but can be disabled by clearing ADC_HPF_EN and DAC_HPF_EN. The cut-off frequency of the filters can be programmed using ADC_AUDIO_HPF_CORNER and DAC_AUDIO_HPF_CORNER. Enabling the high-pass filter is especially important if the ADC output is fed into the DAC.

Table 57: ADC/DAC Digital High-Pass Filter Specifications in Audio Mode

| Sampling Frequency (kHz) | Cut-Off Frequency (Hz) at ADC_AUDIO_HPF_CORNER and DAC_AUDIO_HPF_CORNER Settings | | | |
|--------------------------|--|-----|-----|------|
| | 00 | 01 | 10 | 11 |
| 8 | 0.3 | 0.7 | 1.3 | 2.7 |
| 11.025 | 0.4 | 0.9 | 1.8 | 3.7 |
| 12 | 0.5 | 1 | 2 | 4 |
| 16 | 0.7 | 1.3 | 2.7 | 5.3 |
| 22.05 | 0.9 | 1.8 | 3.7 | 7.3 |
| 24 | 1 | 2 | 4 | 8 |
| 32 | 1.3 | 2.7 | 5.3 | 10.7 |
| 44.1 | 1.8 | 3.7 | 7.3 | 14.7 |
| 48 | 2 | 4 | 8 | 16 |

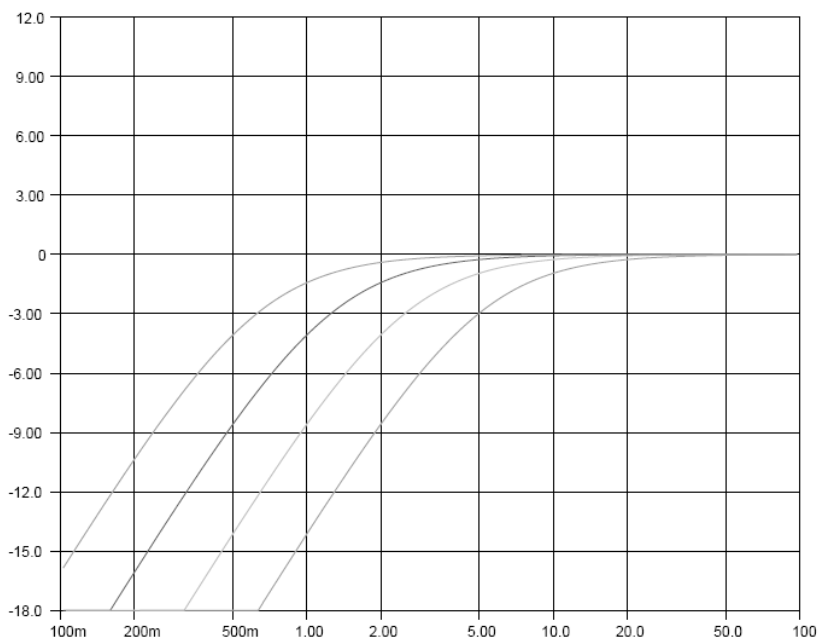


Figure 32: ADC and DAC DC Blocking (Cut-Off Frequency Setting '00' to '11', 16 kHz)

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12.3.2 Variable High-Pass Filter (Wind Noise Filtering)

To improve the quality of microphone recordings, the DA9066 provides a programmable high-pass filter engine, enabled via ADC_VOICE_EN in the ADC_FILTERS1 register.

12.3.3 ADC and DAC 5-Band Equalizers

To enable user controllable listening preferences, the digital playback paths include programmable 5-band equalizers. A low pass filter, a three band-pass filters and a high pass filter offer boosting or damping of each frequency band from 10.5 dB to +12 dB in 1.5 dB steps. The equalizers are enabled by bits ADC_EQ_EN and DAC_EQ_EN.

At a sampling frequency of 48 kHz, the ADC and DAC equalizers have a bandpass response (on a log scale) with center frequencies shown in [Table 58](#) and [Table 59](#).

Table 58: Center Frequency of ADC 5-Band Equalizer at 48 kHz

| Sampling Frequency | Center Frequency of ADC 5-Band Equalizer (Hz) | | | | | Min Gain (dB) | Max Gain (dB) | Step Size (dB) |
|--------------------|---|--------|--------|--------|--------|---------------|---------------|----------------|
| | Band 1 | Band 2 | Band 3 | Band 4 | Band 5 | | | |
| 48 | 29 | 140 | 610 | 2400 | 18500 | -10.5 | 12 | 1.5 |

Table 59: Center Frequency of DAC 5-Band Equalizer at 48 kHz

| Sampling Frequency | Center Frequency of DAC 5-Band Equalizer (Hz) | | | | | Min Gain (dB) | Max Gain (dB) | Step Size (dB) |
|--------------------|---|--------|--------|--------|--------|---------------|---------------|----------------|
| | Band 1 | Band 2 | Band 3 | Band 4 | Band 5 | | | |
| 48 | 15 | 150 | 630 | 2480 | 20000 | -10.5 | 12 | 1.5 |

The gains of each frequency band can be individually configured, from -10.5 dB to +12 dB in 1.5 dB steps, using register bits ADC_EQ_BAND<x> and DAC_EQ_BAND<x>. The overall gain of the ADC equalizer can be set from -12 dB to 0 dB in 6 dB steps using ADC_EQ_GAIN. There is no corresponding overall gain setting for the DAC equalizer because the DAC gain is applied after the equalizer and so can be used to compensate for the equalizer.

The 5-band equalizers cannot be used at the 88.2 kHz and 96 kHz sampling rates. The ADC and DAC 5-band equalizer frequency responses at alternative sampling rates (set via the SR register bits) are shown in [Table 60](#) and [Table 61](#) and from [Figure 33](#) to [Figure 42](#).

Table 60: Center Frequency of ADC 5-Band Equalizer at Alternative Sample Rates

| Sampling Frequency | Center Frequency of DAC 5-Band Equalizer (Hz) | | | | | Min Gain (dB) | Max Gain (dB) |
|--------------------|---|--------|--------|--------|--------|---------------|---------------|
| | Band 1 | Band 2 | Band 3 | Band 4 | Band 5 | | |
| 8 | 24 | 98 | 500 | 1500 | 3600 | -4.8 | 12.5 |
| 11.025 | 29 | 138 | 670 | 2000 | 5000 | -4.8 | 12.5 |
| 12 | 29 | 140 | 740 | 2200 | 5500 | -4.8 | 12.5 |
| 16 | 23 | 98 | 460 | 2000 | 7500 | -12.6 | 12.5 |
| 22.05 | 27 | 130 | 600 | 2700 | 10000 | -12.6 | 12.5 |
| 24 | 30 | 145 | 670 | 3100 | 11000 | -12.6 | 12.5 |
| 32 | 25 | 100 | 400 | 1600 | 12000 | -9.5 | 11.6 |
| 44.1 | 30 | 130 | 550 | 2300 | 17000 | -9.4 | 11.6 |

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Table 61: Center Frequency of DAC 5-Band Equalizer at Alternative Sample Rates

| Sampling Frequency | Center Frequency of DAC 5-Band Equalizer (Hz) | | | | | Min Gain (dB) | Max Gain (dB) |
|--------------------|---|--------|--------|--------|--------|---------------------------|---------------|
| | Band 1 | Band 2 | Band 3 | Band 4 | Band 5 | Worst Case from all Bands | |
| 8 | 13.5 | 100 | 492 | 1530 | 3600 | -4.8 | 12.5 |
| 11.025 | 18 | 136 | 685 | 2100 | 5010 | -4.8 | 12.5 |
| 12 | 20 | 148 | 728 | 2200 | 5500 | -4.8 | 12.5 |
| 16 | 14 | 96 | 440 | 2000 | 7300 | -12.6 | 12.5 |
| 22.05 | 18 | 136 | 620 | 2800 | 10000 | -12.6 | 12.5 |
| 24 | 19 | 145 | 660 | 3000 | 11000 | -12.6 | 12.5 |
| 32 | 13 | 95 | 415 | 1680 | 13800 | -9.5 | 11.6 |
| 44.1 | 18 | 130 | 560 | 2250 | 18900 | -9.4 | 11.6 |

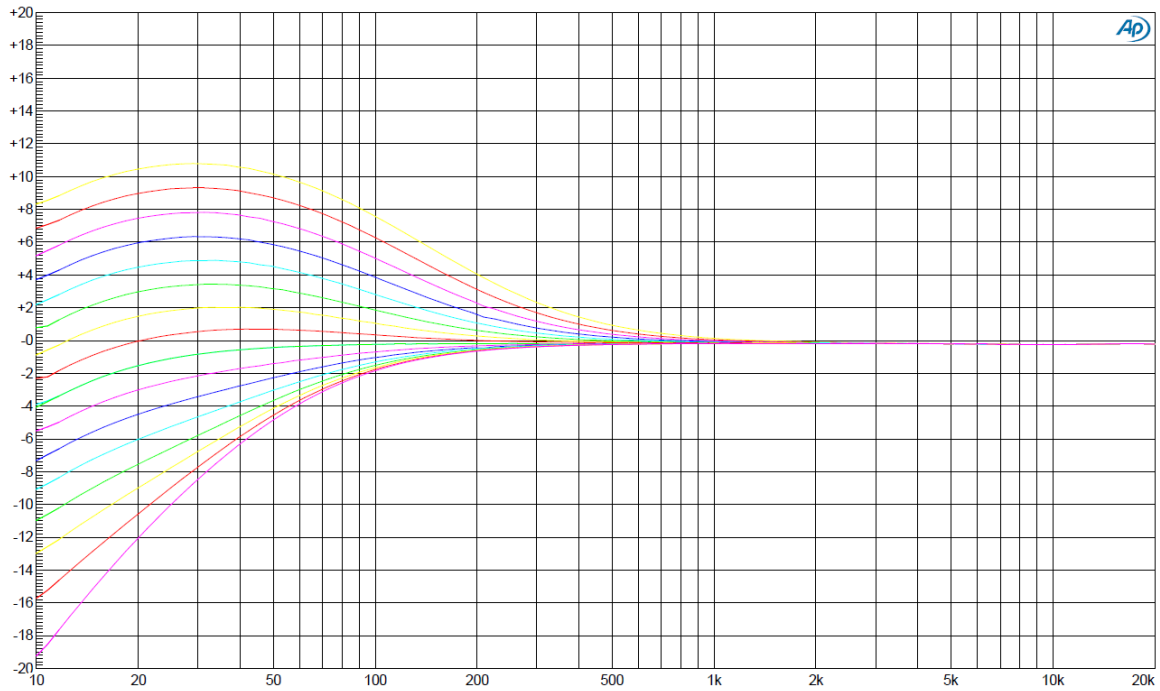


Figure 33: ADC Equalizer Filter Band 1 Frequency Response at FS = 48 kHz

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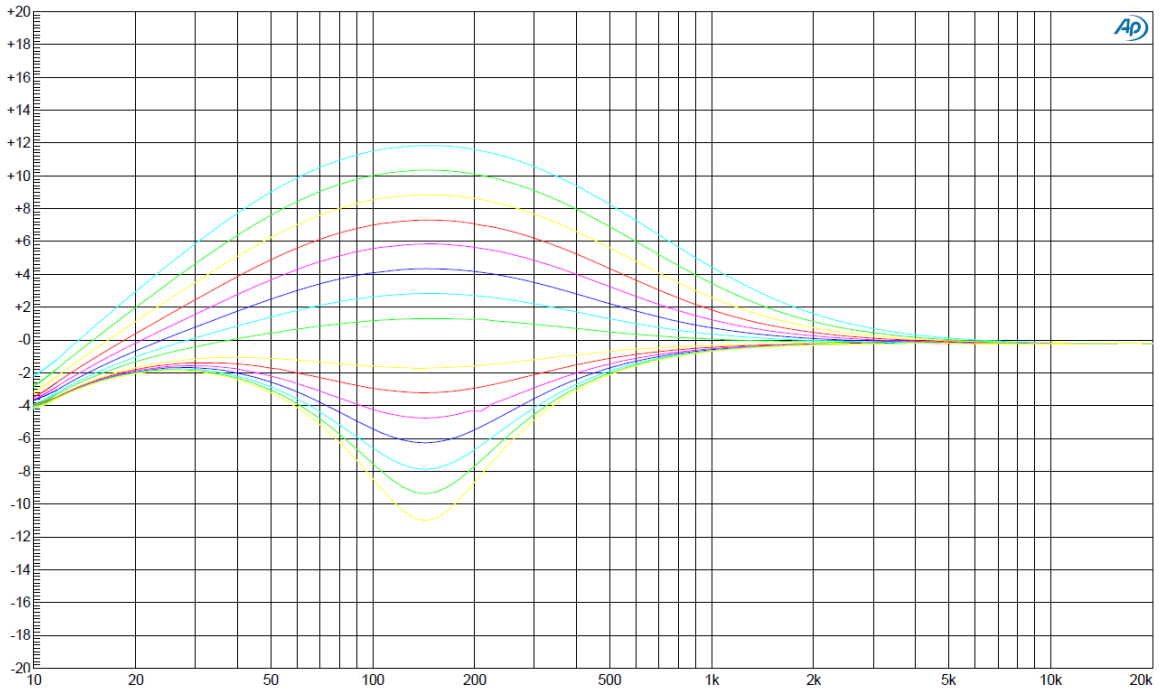


Figure 34: ADC Equalizer Filter Band 2 Frequency Response at FS = 48 kHz

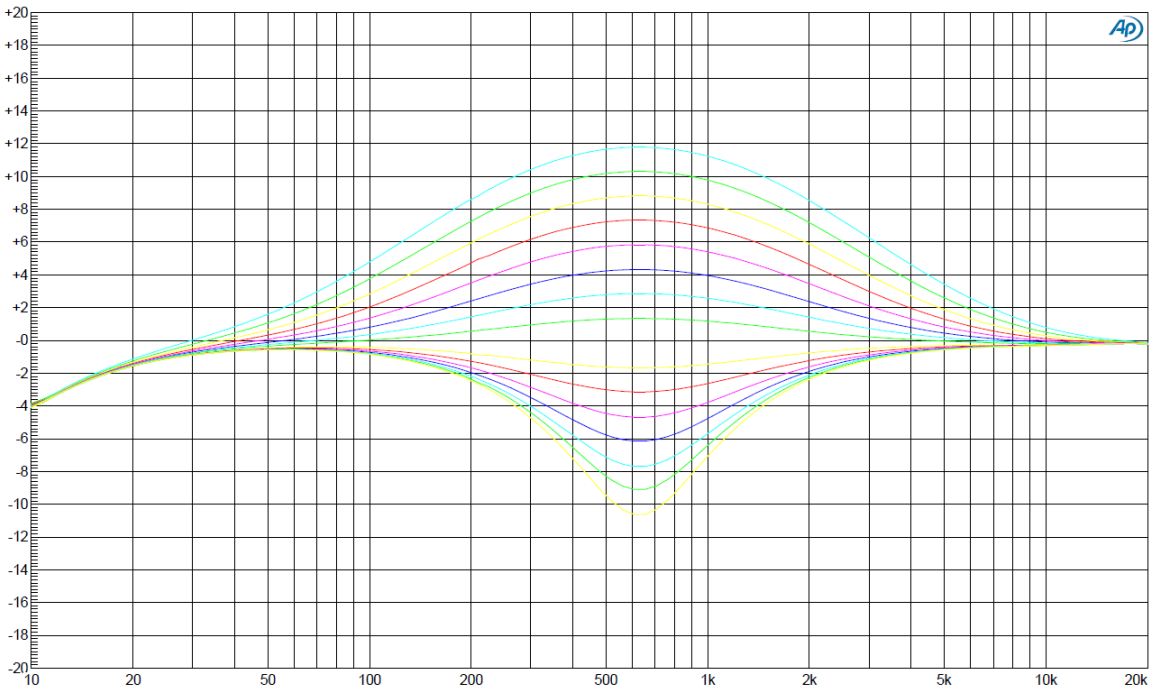


Figure 35: ADC Equalizer Filter Band 3 Frequency Response at FS = 48 kHz

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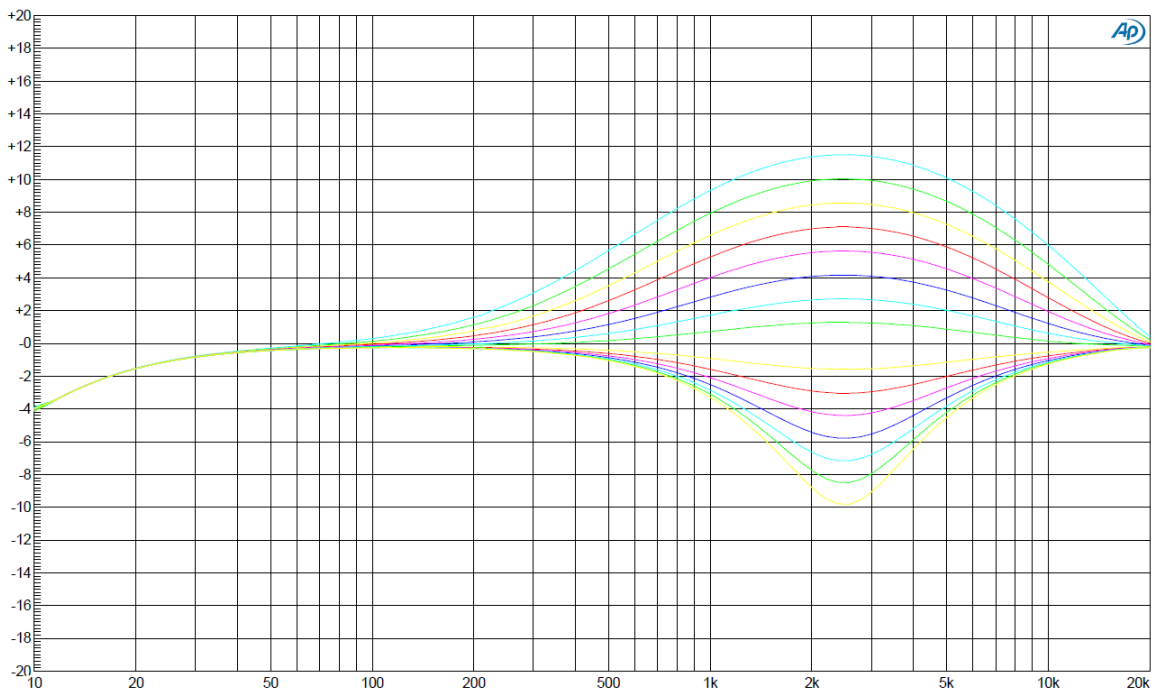


Figure 36: ADC Equalizer Filter Band 4 Frequency Response at FS = 48 kHz

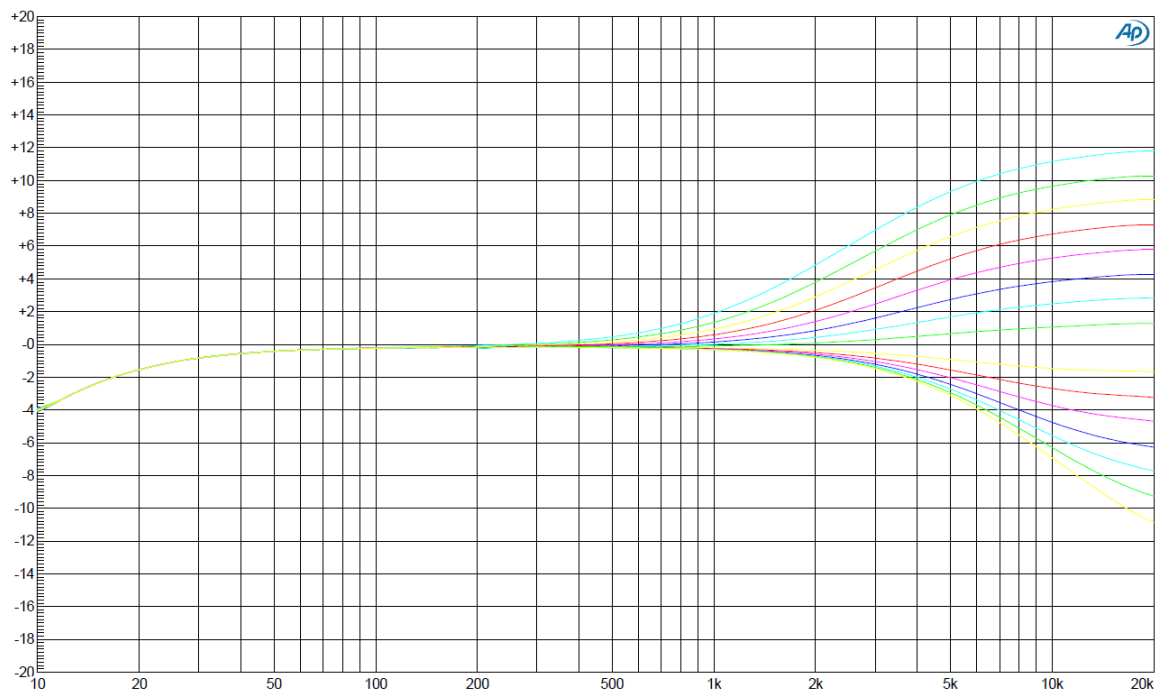


Figure 37: ADC Equalizer Filter Band 5 Frequency Response at FS = 48 kHz

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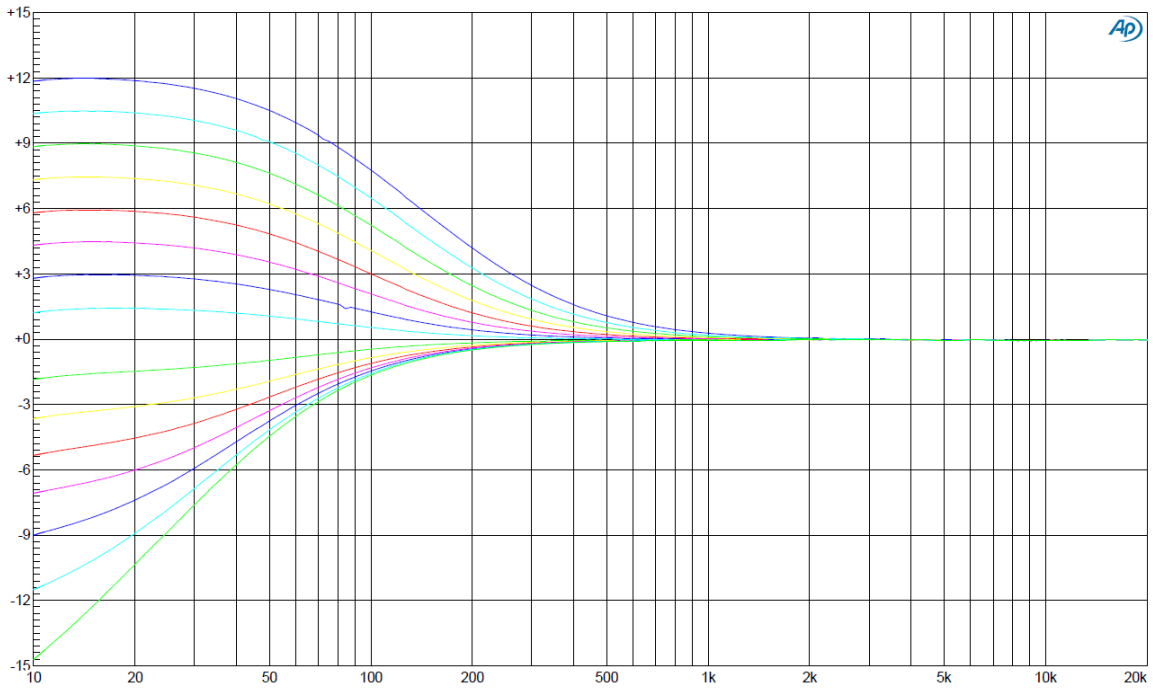


Figure 38: DAC Equalizer Filter Band 1 Frequency Response at FS = 48 kHz

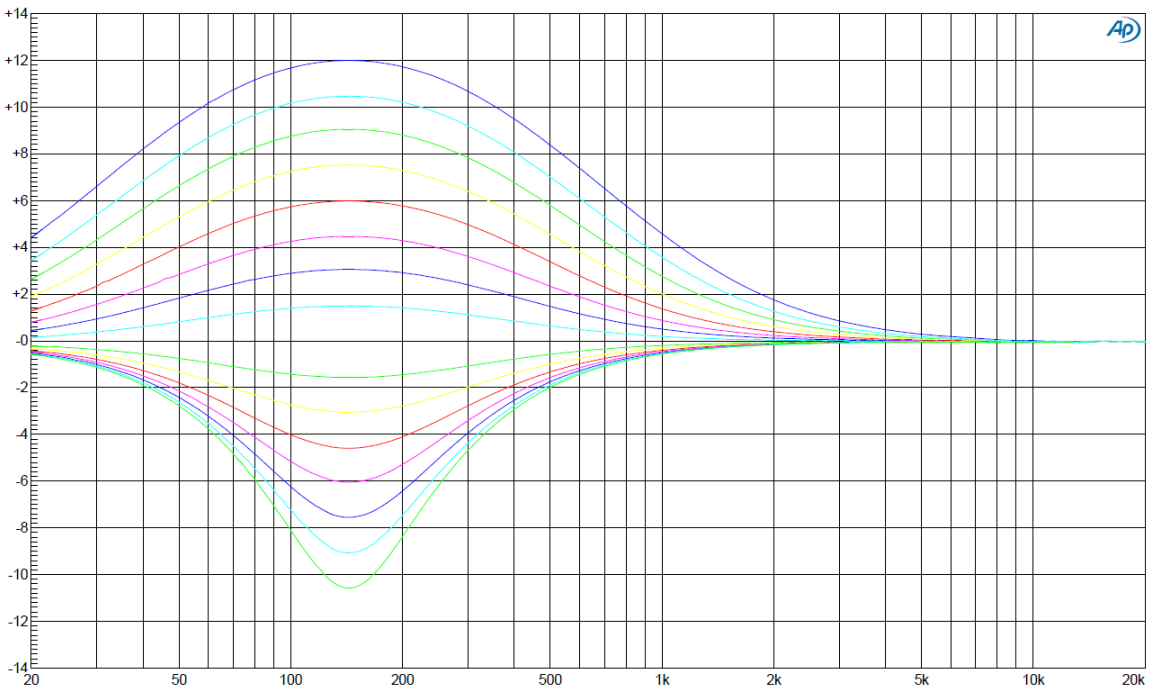


Figure 39: DAC Equalizer Filter Band 2 Frequency Reponse at FS = 48 kHz

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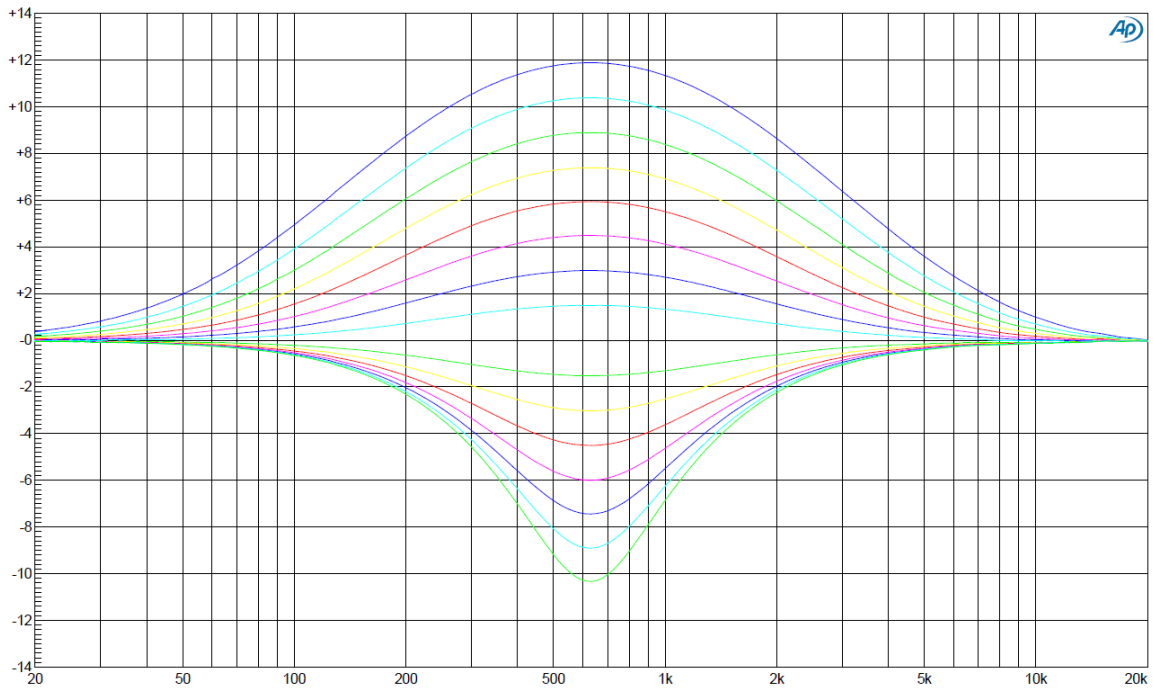


Figure 40: DAC Equalizer Filter Band 3 Frequency Response at FS = 48 kHz

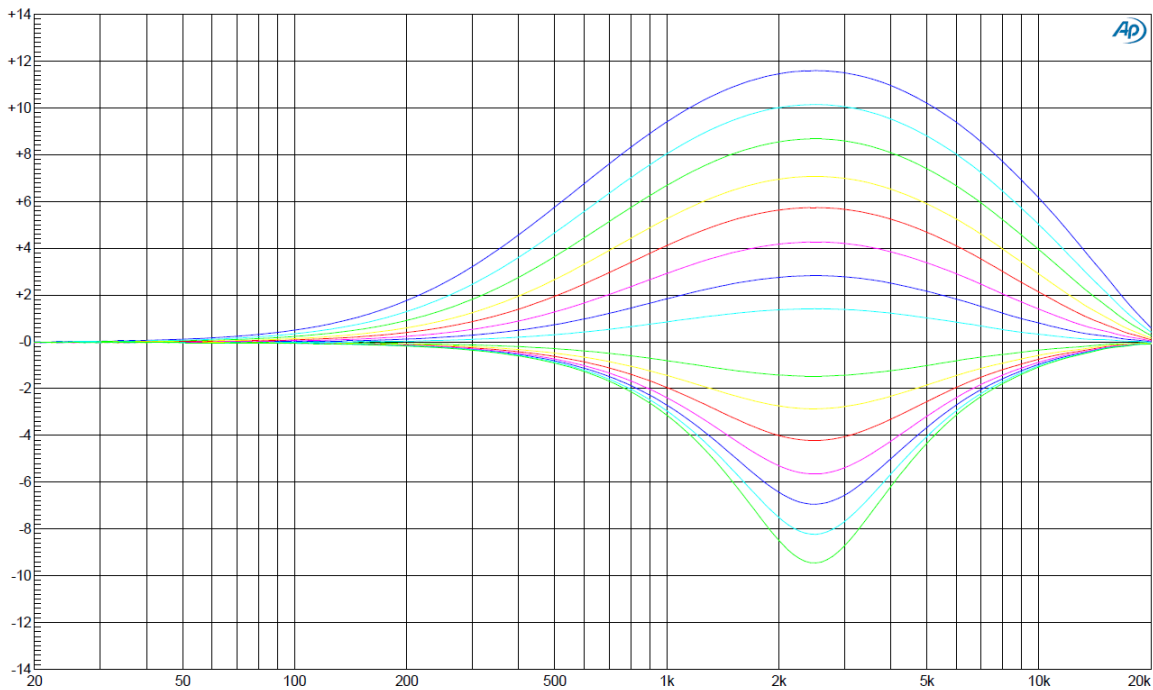


Figure 41: DAC Equalizer Filter Band 4 Frequency Response at FS = 48 kHz

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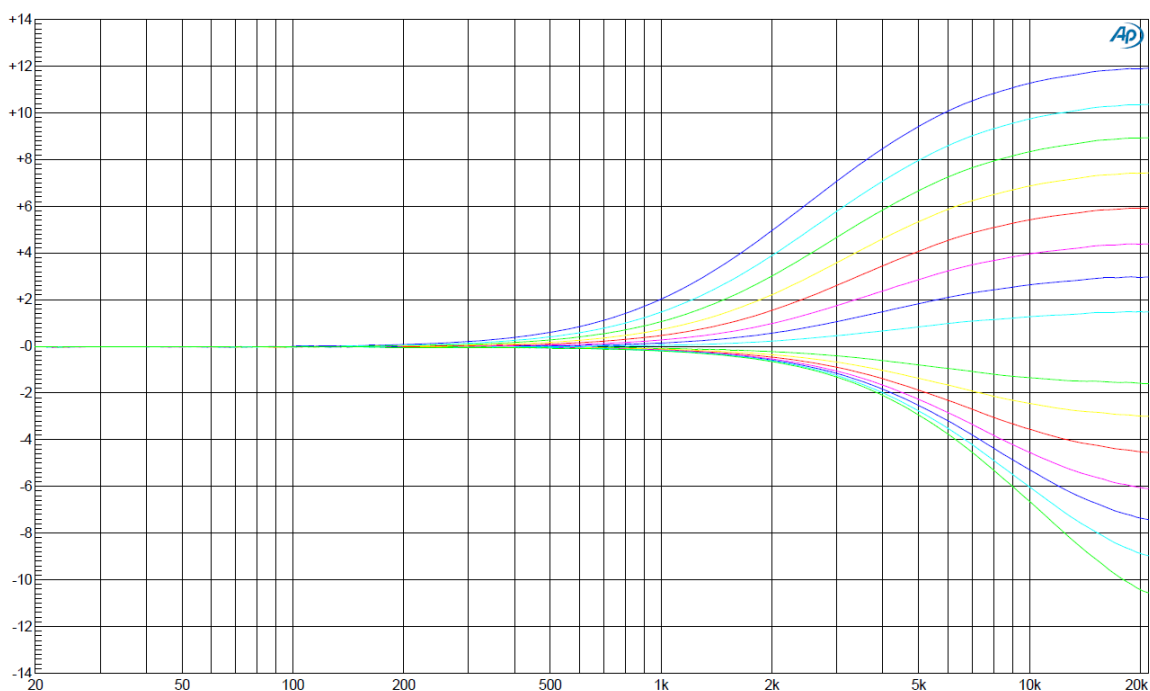


Figure 42: DAC Equalizer Filter Band 5 Frequency Response at FS = 48 kHz

12.3.4 Automatic Level Control (ALC)

For improved sound recordings of signals with a large volume range, the DA9066 offers a fully-configurable automatic recording level control (ALC) for microphone inputs. This is enabled via the ALC_L_EN and ALC_R_EN controls, and can be enabled independently on either left or right channel. It is recommended that the ALC is only enabled in stereo as this applies the same gain to both channels and so protects the pan of stereo signals.

The ALC monitors the digital signal after the ADC and adjusts the microphones' analog and digital gain to maintain a constant recording level, whatever the analog input signal level.

Operation of ALC is illustrated in Figure 43. When the input signal volume is high, the ALC system will reduce the overall gain until the output volume is below the specified maximum value. When the input signal volume is low, the ALC will increase the gain until the output volume increases above the specified minimum value. If the output signal is within the desired signal level (between the specified minimum and maximum levels), the ALC does nothing.

The maximum and the minimum thresholds that trigger a gain change of the ALC are programmed by the ALC_THRESHOLD_MAX and ALC_THRESHOLD_MIN controls.

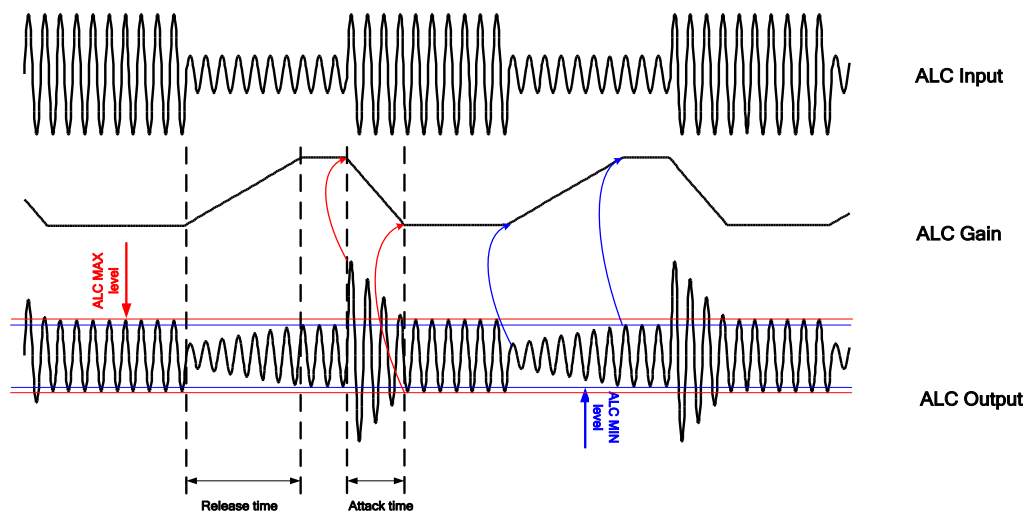


Figure 43: Operation of ALC

The total gain is made up of an analog gain, which is applied to the microphone PGAs, and a digital gain, which is implemented in the filtering stage. The ALC block monitors and controls the gain of the microphone PGAs and the ADC. Note that although the ALC is controlling the gain, it does not modify any of the registers `MIC_L_GAIN`, `MIC_R_GAIN`, `ADC_L_DIGITAL_GAIN`, and `ADC_R_DIGITAL_GAIN`. These registers are ignored while the ALC is in operation.

The minimum and maximum levels of digital gain that can be applied by the ALC are controlled using `ALC_ATTEN_MAX` and `ALC_GAIN_MAX`.

Similarly the minimum and maximum levels of analog gain are controlled by `ALC_ANA_GAIN_MIN` and `ALC_ANA_GAIN_MAX`. The rates at which the gain is changed are defined by the attack and decay rates in register `ALC_CTRL2`. When attacking, the gain decreases with `ALC_ATTACK` rate. When decaying, the gain increases with `ALC_RELEASE` rate.

The hold-time is defined by `ALC_HOLD` in the `ALC_CTRL3` register. This controls the length of time that the system maintains the current gain level before starting to decay. This prevents unwanted changes in the recording level when there is a short-lived spike in input volume, for example when recording speech.

Typically the attack rate should be much faster than the decay rate, as it is necessary to reduce rapidly increasing waveforms as quickly as possible, whereas fast release times will result in the signal appearing to pump. The ALC also has an anti-clipping function that applies a very fast attack rate when the input signal is close to full-range. This prevents clipping of the signal by reducing the signal gain at a faster rate than would normally be applied. The anti-clip function is enabled using `ALC_ANTICLIP_EN`, and the threshold above which it is activated is set in the range 1/128 full scale to full-scale using `ALC_ANTICLIP_LEVEL`.

A recording noise gate feature, see Section 12.3.6, is provided to avoid increasing the gain of the channel when there is no signal, or when only a noise signal is present. Boosting a signal on which only noise is present is known as noise pumping, the noise gate prevents this. Whenever the level of the input signal drops below the noise threshold configured in `ALC_NOISE`, the channel gain remains constant.

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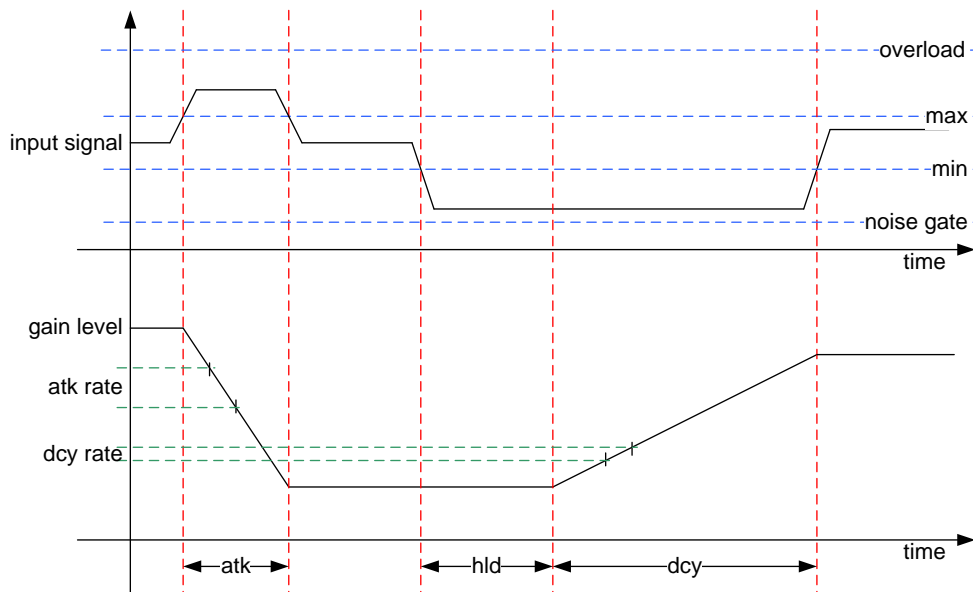


Figure 44: Attack, Delay and Hold Parameters

12.3.5 Soft Mute

To improve the user perception of audio configuration changes the DAC channel signals may be soft muted by enabling register bit `DAC_SOFTMUTE_EN`. The soft mute function attenuates the digital input to the DAC, ramping the gain down in steps of 0.1875 dB from its current level to -77.25 dB, and then completely muting the channel.

When `DAC_SOFTMUTE_EN` is released, the attenuation is set to 77.25 dB, and then ramped up to the previous gain level. Both left and right channels of the soft mute enabled output amplifiers are muted simultaneously. The ramping up and down rate is dependent on the audio sample rate and can be individually configured using register bits `DAC_SOFTMUTE_RATE`.

During active soft muting, the digital gain of the DAC will be different to the value programmed in bits `DAC_L_DIGITAL_GAIN_STATUS` and `DAC_R_DIGITAL_GAIN_STATUS`. DAC Noise Gate

12.3.6 Playback Noise Gate

DA9066 uses a noise gate as an automatic gain control to reduce noise heard during playback if no signal is present. It is enabled using the `DAC_NG_EN` control.

When the output signals on both channels are below a given threshold level, and they stay low for longer than a specified period, then playback noise gate is activated. When the playback noise gate activates, the gain on the active HP and Line amplifiers are ramped down to their lowest levels. This is equivalent to asserting the minimum gain bits `HP_L_AMP_MIN_GAIN_EN`, `HP_R_AMP_MIN_GAIN_EN`, and `LINE_AMP_MIN_GAIN_EN`.

The noise gate threshold level can be specified in 6 dB steps from 90 dB to 48 dB. The noise gate threshold time ranges from 256 samples to 2048 samples and is set using the control `DAC_NG_SETUP_TIME`.

When the averaged level of the two channels exceeds the release threshold configured in `DAC_NG_OFF_THRESHOLD`, the gain of the amplifiers is ramped up back to its original value. When the average level of the two channels is below the attack threshold configured in `DAC_NG_ON_THRESHOLD` for longer than the time specified in `DAC_NG_SETUP_TIME`, the gain is ramped down to its minimum value.

The attack and release rate can be configured via controls `DAC_NG_RAMPDN_RATE` and `DAC_NG_RAMPUP_RATE`. The noise gate release time is usually much faster than the attack time, to allow proper playback as soon as a signal is present at the output amplifiers.

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12.4 Clock Generation

12.4.1 MCLK Input

MCLK is the master clock input for the audio functions. With the default register settings, the clock input should be a square wave with CMOS logic levels (referenced to VDD_IO). A clock squarer circuit can be enabled by asserting the PLL_MCLK_SQR_EN register bit. This clock squarer allows a sine wave or other a low amplitude clock (down to 300 mVPP) to be applied to the codec. The input is AC coupled on chip when using the clock squarer mode. If the MCLK input frequency drops below 1 MHz, the PLL_MCLK_STATUS bit is cleared, and the chip will automatically use its internal audio reference oscillator as a clock source.

12.4.2 Audio Reference Oscillator

The DA9066 codec has an internal oscillator which can be used as an internal system clock for the audio if there is no valid MCLK signal available. The audio reference oscillator is required for analog bypass paths using either the headphone or earpiece outputs. It is automatically enabled when no valid MCLK input (> 1 MHz) is available.

The audio reference oscillator cannot be used for digital playback or record modes.

12.4.3 Phase Locked Loop (PLL)

The DA9066 contains a Phase Locked Loop (PLL) that can be used to generate the required 11.2896 MHz or 12.288 MHz internal system clock when a frequency of between 2 MHz and 54 MHz is applied to MCLK. This allows sharing of clocks between devices in an application, reducing total system cost. For example, the codec may operate from common 13 MHz or 19.2 MHz system clock frequency.

If an MCLK frequency of between 2 MHz and 4.5 MHz is being used, see Section 12.4.4.4.

12.4.4 Clock Modes

There are three ways in which the internal system clock may be generated:

- **Bypass PLL mode:** If digital playback or record is required, the MCLK frequency should be set to one of the following:
 - 11.2896 or 12.288 MHz
 - 22.5792 or 24.576 MHz
 - 45.1584 or 49.152 MHz.

The PLL_INDIV register bit must then be programmed accordingly

- **Normal PLL mode:** Alternative frequency clock applied to MCLK pin (in the range of 2 MHz to 54 MHz), where MCLK is synchronous with WCLK, or Master mode is enabled
- **SRM PLL mode:** Clock applied to MCLK pin (in the range of 2 MHz to 54 MHz) is asynchronous to WCLK

Table 62: PLL Clock Modes

| Mode | Bypass PLL | Normal PLL | SRM PLL |
|--------|--------------|--------------|--------------|
| Master | Yes (Note 1) | Yes (Note 2) | No |
| Slave | Yes (Note 3) | Yes (Note 4) | Yes (Note 5) |

Note 1 11.2896 MHz (or multiples) should be used as MCLK frequency for 11.025 kHz, 22.05 kHz, 44.1 kHz, or 88.2 kHz sample rates and 12.288 MHz (or multiples) should be used for (8, 12, 16, 24, 32, 48, or 96 kHz sample rates

Note 2 MCLK must be between 2 MHz and 54 MHz

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Note 3 MCLK must be exactly 12.288 MHz or 11.2896 MHz or a multiple thereof and synchronous with BCLK and WCLK

Note 4 MCLK must be synchronous with BCLK and WCLK

Note 5 BCLK must be synchronous with WCLK. MCLK must be between 2 MHz and 54 MHz

12.4.4.1 Bypass PLL Mode (AIF Master)

If an MCLK signal (of 11.2896 MHz/12.288 MHz, 22.5792 MHz/24.576 MHz, or 45.1584 MHz/49.152 MHz) that is synchronous with WCLK and BCLK is available, the PLL is not required and should be disabled to save power. PLL bypass mode is activated by setting PLL_EN = 00.

In this mode, the PLL is bypassed and an audio frequency clock is applied to the MCLK pin of the codec. The required clock frequency depends on the sample rate at which the audio DACs and ADCs are operating. These clock frequencies are summarized in [Table 63](#) for the range of DAC and ADC sample rates that can be configured using the SR register.

Table 63: Sample Rate Control and Corresponding System Clock Frequency

| Sample Rate, FS (kHz) | SR Register | System Clock Frequency, (MHz) |
|-----------------------|-------------|-------------------------------|
| 8 | 0001 | 12.288 |
| 11.025 | 0010 | 11.2896 |
| 12 | 0011 | 12.288 |
| 16 | 0101 | 12.288 |
| 22.05 | 0110 | 11.2896 |
| 24 | 0111 | 12.288 |
| 32 | 1001 | 12.288 |
| 44.1 | 1010 | 11.2896 |
| 48 | 1011 | 12.288 |
| 88.2 | 1110 | 11.2896 |
| 96 | 1111 | 12.288 |

If digital playback or record is required in bypass mode then the MCLK frequency should be set to one of 11.2896 MHz/12.288 MHz, 22.5792 MHz/24.576 MHz, or 45.1584 MHz/49.152 MHz, and PLL_INDIV should be programmed accordingly.

If no valid MCLK is detected, the output of the internal reference oscillator is used instead. However in this case only analog bypass paths may be used.

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12.4.4.2 Normal PLL Mode (AIF Master)

The PLL is enabled by asserting PLL_EN. Once the PLL is enabled and has achieved phase lock, PLL bypass mode is disabled, and the output of the PLL is used as the system clock.

The PLL input divider register (PLL_INDIV) is used to reduce the PLL reference frequency to the usable range of 2 MHz to 4.5 MHz as shown in Table 64. The PLL reference frequency is reduced according to the following equation:

$$\text{FREF} = \text{FMCLK} \div (2^{\text{PLL_INDIV}+1})$$

Table 64: PLL Input Divider

| MCLK Input Frequency (MHz) | Input Divider, ($\div N$) | PLL_INDIV Register (0x27 [3:2]) |
|----------------------------|-----------------------------|---------------------------------|
| 2 to 4.5 | $\div 1$ | 000 |
| 4.5 to 9 | $\div 2$ | 001 |
| 9 to 18 | $\div 4$ | 010 |
| 18 to 36 | $\div 8$ | 011 |
| 36 to 54 | $\div 16$ | 100 |

The value of the PLL feedback divider is used to set the voltage controlled oscillator (VCO) frequency to eight times the required system clock frequency (see Table 63).

$$\text{FVCO} = \text{FREF} \times \text{PLL feedback divider}$$

The value of the PLL feedback divider is an unsigned number in the range of 0 to 128. It consists of seven integer bits and 13 fractional bits split across three registers:

- PLL_INTEGER holds the seven integer bits
- PLL_FRAC_TOP holds the top bits (MSB) of the fractional part of the divisor
- PLL_FRAC_BOT holds the bottom bits (LSB) of the fractional part of the divisor

Example Calculation of the Feedback Divider Setting:

A codec operating with F_s (sample rate) = 48 kHz and a reference input clock frequency of 12.288 MHz is used. The required output frequency is 98.304 MHz.

The reference clock input = 12.288 MHz, which falls in the range 9.1 MHz to 18 MHz so PLL_INDIV must be set to 0b010 (dividing the reference input frequency by 4, see Table 64).

The formula for calculating the feedback divider is:

$$\text{Feedback divider (F)} = (\text{VCO output frequency} \times \text{input divider PLL_INDIV}) / \text{reference input clock}$$

Therefore:

$$\text{Feedback divider (F)} = (98.304 \times 4) / 12.288 = 32$$

So:

$$\text{PLL_FBDIV_INTEGER (holding the seven integer bits)} = 0x20$$

$$\text{PLL_FBDIV_FRAC_TOP (holding the top bits (MSB) of the fractional part of the divisor)} = 0x00$$

$$\text{PLL_FBDIV_FRAC_BOT (holding the bottom bits (LSB) of the fractional part of the divisor)} = 0x00$$

Table 65 shows example register settings that will configure the PLL when using a 13 MHz, 15 MHz, or 19.2 MHz clock. Note that any MCLK input frequency between 2 MHz and 54 MHz is supported. PLL_INDIV must be used to reduce the PLL reference frequency to the usable range of 2 MHz to 4.5 MHz, as shown in Table 64.

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Table 65: Example PLL Configurations

| MCLK Input Frequency (MHz) | System Clock Frequency (MHz) | PLL_CTRL Register | PLL_FRAC_TOP Register | PLL_FRAC_BOT Register | PLL_INTEGER Register |
|----------------------------|------------------------------|-------------------|-----------------------|-----------------------|----------------------|
| 13 | 11.2896 | 0x84 | 0x19 | 0x45 | 0x1B |
| 13 | 12.288 | 0x84 | 0x07 | 0xEA | 0x1E |
| 15 | 11.2896 | 0x84 | 0x02 | 0xB4 | 0x18 |
| 15 | 12.288 | 0x84 | 0x06 | 0xDC | 0x1A |
| 19.2 | 11.2896 | 0x84 | 0x1A | 0x1C | 0x12 |
| 19.2 | 12.288 | 0x84 | 0x0F | 0x5C | 0x14 |

12.4.4.3 SRM Mode (AIF Slave)

SRM mode enables the PLL output clock to be synchronized to the incoming WCLK signal on the AIF. The SRM PLL mode is enabled by asserting bit PLL_EN, as for normal PLL mode, and asserting register bit PLL_SRM_EN. Register bit SRM_LOCK indicates whether or not the SRM has achieved synchronization with WCLK.

When using the digital audio interface in slave mode with the SRM enabled, removing and re-applying the AIF interface word clock WCLK may cause the PLL lock to be lost. To re-lock the PLL, it is recommended that you disable the SRM (PLL_SRM_EN = 0), reset the PLL by re-writing to register PLL_INTEGER, and then re-enable the SRM (PLL_SRM_EN = 1) after the AIF WCLK has been reapplied.

When switching sample rates between 44.1 kHz and 48 kHz (or between the multiples of these sample rates), SRM must be disabled and then re enabled using register bit PLL_SRM_EN.

12.4.4.4 Operating with a 2 MHz to 5 MHz MCLK

When using the PLL with a 2 MHz to 5 MHz MCLK, you must follow the procedure below to setup the PLL in the correct mode.

1. Setup PLL and clocking
2. Write F0 = 8b
3. Write F1 = 03
4. Write F0 = 00

When returning from this mode to a mode with an MCLK >5 MHz, you must follow the procedure below.

1. Write F0 = 8b
2. Write F1 = 01
3. Write F0 = 00
4. Setup PLL and clocking

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12.4.5 Music Mode

For the first filter, in music mode ADC_VOICE_EN must be set to 0 and the HPF corner frequency is set using ADC_AUDIO_HPF_CORNER.

12.4.6 ADC Voice Mode

In ADC voice mode, ADC_VOICE_EN must = 1 and ADC_HPF_EN must = 1 in which case the HPF corner frequency is set using ADC_VOICE_HPF_CORNER. The low frequency roll off is configured over a wide range using the ADC_VOICE_HPF_CORNER control. This allows for flexible removal of wind and pop noise.

12.4.7 DAC Voice Mode

During playback, dedicated voiceband filtering can be enabled using DAC_VOICE_EN. In DAC voice mode, DAC_VOICE_EN must = 1 and DAC_HPF_EN must = 1 in which case the HPF corner frequency is set using DAC_VOICE_HPF_CORNER. The low frequency roll off is configured over a wide range using the DAC_VOICE_HPF_CORNER control.

12.4.8 Cut-Off Frequency in Voice Mode

In voice mode, the wind noise high-pass filter cut-off frequency is determined by the settings of the ADC_VOICE_HPF_CORNER and the DAC_VOICE_HPF_CORNER register bits. These cut-off frequencies are not fixed and vary with the sample rate being used. Table 66 shows the cut-off frequencies for all valid settings of ADC_VOICE_HPF_CORNER and DAC_VOICE_HPF_CORNER, at all sample rates of 16 kHz and below.

Table 66: Wind Noise High-Pass Filter Specifications

| Cut-Off Frequency at ADC_VOICE_HPF_CORNER and DAC_VOICE_HPF_CORNER Settings (Voice filtering only, and with sample rate 16 kHz or lower) | | | | | | | | |
|---|------|------|-----|-----|-----|-----|-----|-----|
| fs [kHz] | 000 | 001 | 010 | 011 | 100 | 101 | 110 | 111 |
| 8.0 | 2.5 | 25 | 50 | 100 | 150 | 200 | 300 | 400 |
| 11.025 | 3.4 | 34.5 | 69 | 138 | 207 | 276 | 413 | 551 |
| 12.0 | 3.75 | 37.5 | 75 | 150 | 225 | 300 | 450 | 600 |
| 16.0 | 5 | 50 | 100 | 200 | 300 | 400 | 600 | 800 |

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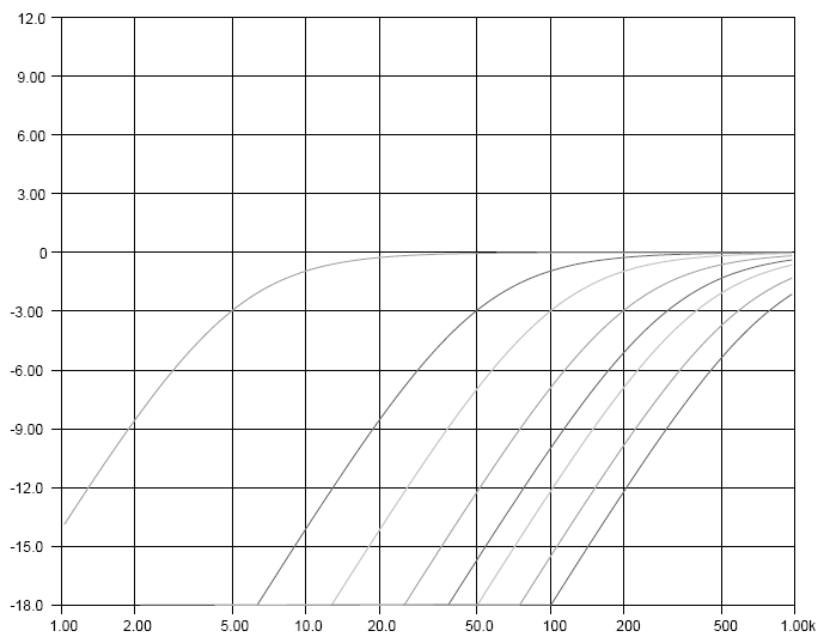


Figure 45: Wind Noise High-Pass Filter (Cut-Off Frequency Setting '000' to '111', 16 kHz)

12.4.9 Digital Routing

Any of the four digital inputs from the AIF (AIF_IL and AIF_IR) and ADCs (ADC_L and ADC_R) can be routed to any of the four digital outputs (DAC_L, DAC_R, AIF_OL, AIF_OR) by setting DAC_L_SRC, DAC_R_SRC, AIF_L_SRC and AIF_R_SRC appropriately.

The AIF input channels can be evenly mixed and then selected as a mono output on either channel by setting the bits DAC_[L|R]_MONO.

The AIF input data can be inverted for either channel by setting DAC_[L|R]_INV.

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12.5 Digital Interfaces

12.5.1 I²C Control Interface (CIF)

DA9066 is completely SW-controlled from the host by registers. DA9066 provides an I²C serial control interface to access these registers. Data is shifted into or out from DA9066 under the control of the host processor that also provides the serial clock.

The Power Management and Audio Codec registers are separate and have different separate 7-bit device addresses.

The Power Management address is configurable using IF_BASE_ADDR.

The Audio address is fixed.

CLK provides the I²C clock and DATA carries the bidirectional I²C data. The I²C interface is open-drain supporting multiple devices on a single line. The bus lines have to be pulled HIGH by external pull-up resistors (2 k Ω to 20 k Ω range). The attached devices only drive the bus lines LOW by connecting them to ground. As a result two devices cannot conflict if they drive the bus simultaneously.

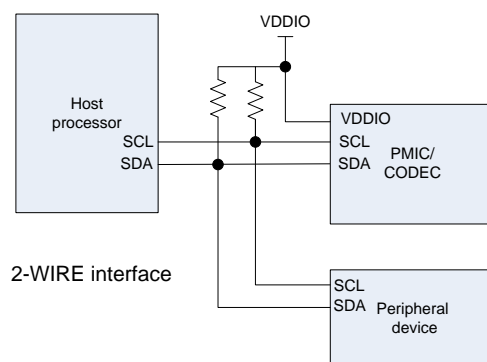


Figure 46: Schematic of I²C Control Interface Bus

In standard/fast mode the highest frequency of the bus is 400 kHz.

The exact frequency can be determined by the application and does not have any relation to the DA9066 internal clock signals. DA9066 will follow the host clock speed within the described limitations and does not initiate any clock arbitration or slow down.

In high speed mode, the maximum frequency of the bus may be increased to 1.7 MHz. This mode is supported if the CLK line is driven with a push-pull stage from the host and if the host enables an external 3 mA pull-up at the DATA pin to decrease the rise time of the data. In this mode, the DATA line on DA9066 is able to sink up to 12 mA. In all other respects the high speed mode behaves as the standard/fast mode.

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12.5.1.1 I²C Control Interface Protocol

All data is transmitted across the I²C bus in groups of 8 bits.

To send a bit, the DATA line is driven towards the intended state while the CLK is LOW (a low on DATA indicates a zero bit).

Once the DATA has settled the CLK line is brought HIGH and then LOW. This pulse on CLK clocks the DATA bit into the receivers shift register.

A two byte serial protocol is used containing one byte for address and one byte data. Data and address transfer is transmitted MSB first for both read and write operations.

All transmission begins with the START condition from the master during the bus is in IDLE state (the bus is free).

The START condition is indicated by a high to low transition on the DATA line while the CLK is in the high state.

The STOP condition is indicated by a low to high transition on the DATA line while the CLK is in the high state.

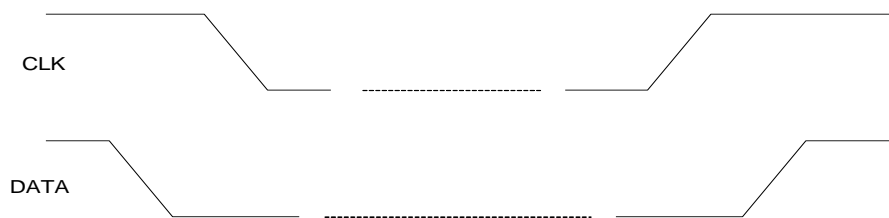


Figure 47: Timing of I²C START and STOP conditions

The I²C bus is monitored by DA9066 for a valid SLAVE address whenever the interface is enabled. It responds immediately with an Acknowledge when it receives its own slave address.

This Acknowledge is done by pulling the DATA line low during the following clock cycle (white blocks marked with 'A' in [Figure 48](#) to [Figure 52](#)).

The protocol for a register write from master to slave consists of a start condition, a slave address with read/write bit and the 8-bit register address followed by 8 bits of data terminated by a STOP condition (all bytes are responded to by DA9066 with an Acknowledge).

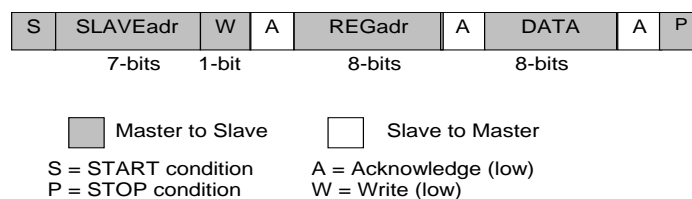


Figure 48: I²C Byte Write (DATA signal)

When the host reads data from a register, it first has to write access DA9066 with the target register address and then read access DA9066 with a Repeated START or alternatively a second START condition.

After receiving the data, the host sends No Acknowledge and terminates the transmission with a STOP condition.

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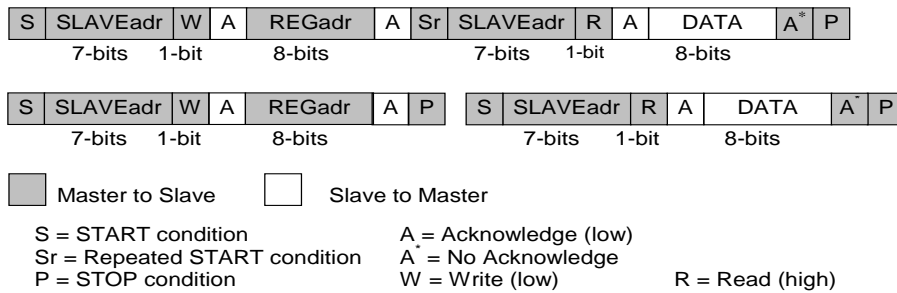


Figure 49: Examples of I²C Byte Read (DATA signal)

Consecutive (page) read out mode is initiated from the master by sending an Acknowledge instead of Not Acknowledge after receipt of the data word.

The I²C control block then increments the address pointer to the next I²C address and sends the data to the master.

This enables an unlimited read of data bytes until the master sends a No Acknowledge directly after the receipt of data, followed by a subsequent STOP condition.

If a non-existent I²C address is read out, then DA9066 returns code zero.

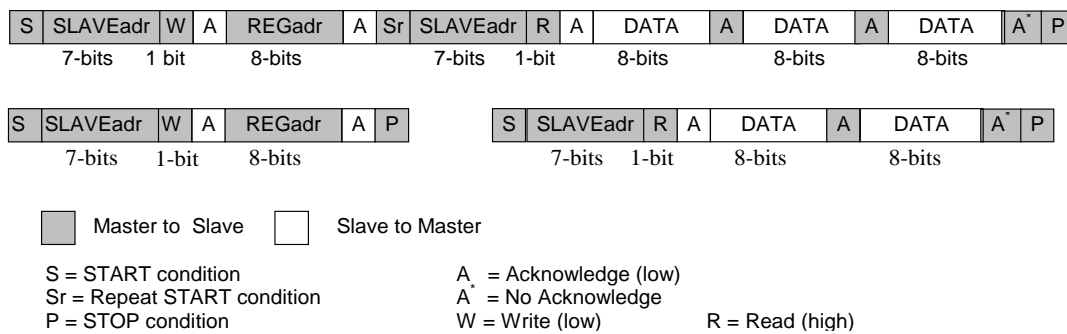


Figure 50: Examples of I²C Page Read (DATA signal)

Consecutive (page) write mode is supported if the Master sends several data bytes following a slave register address.

The I²C control block then increments the address pointer to the next I²C address, stores the received data and sends an Acknowledge until the Master sends the STOP condition.

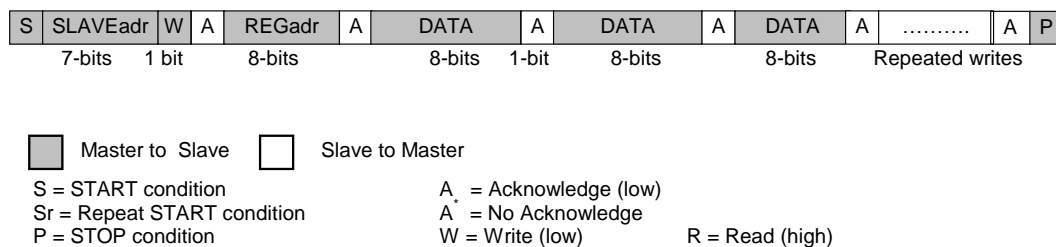


Figure 51: I²C Repeated Write (DATA signal)

Via control WRITE_MODE, an alternate write mode receiving alternated register address and data can be configured to support host repeated write operations that access several non-consecutive registers.

Data will be stored at the previously received register address.

If a new START or STOP condition occurs within a message, the bus will return to IDLE mode.

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12.5.2.2 Left Justified Mode

The AIF supports Left Justified data.

The MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock.

The MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

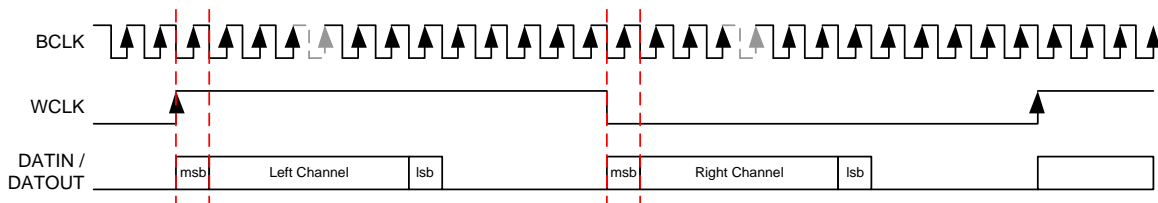


Figure 54: Left Justified Format AIF Data

12.5.2.3 Right Justified Mode

The AIF supports Right Justified data.

The LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of word clock.

The LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

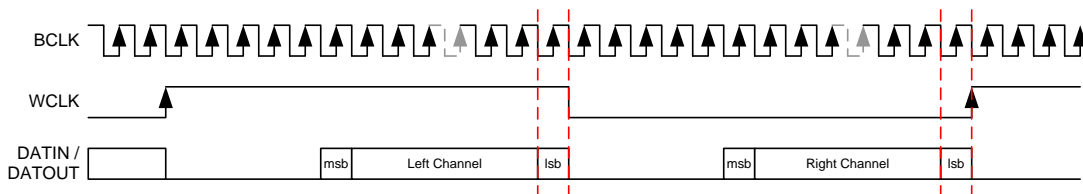


Figure 55: Right Justified Format AIF Data

12.5.2.4 DSP Mode

The AIF supports DSP mode.

The rising edge of the word clock starts the data transfer with the left channel data first and immediately followed by the right channel data.

Each data bit is valid on the falling edge of the bit clock.

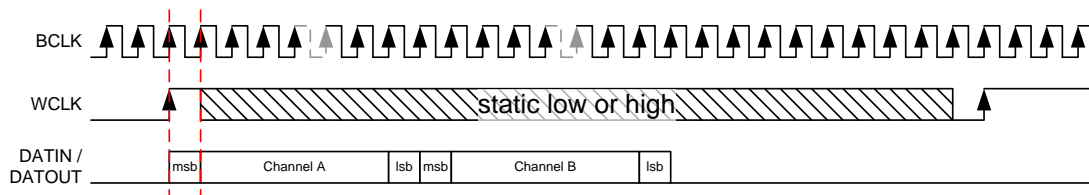


Figure 56: DSP Format AIF Data

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12.5.2.5 TDM Mode

The AIF supports TDM mode which is an extension of the DSP and Left Justified formats.

TDM mode is enabled using the register AIF_TDM_MODE_EN.

The data can be configured to be valid for a certain number of bit clock periods after the start of the frame, as configured by the 8-bit offset value in register AIF_OFFSET.

In the Left Justified TDM mode, the left channel data is valid after a number of offset clock cycles of the rising edge of the word clock, and the right channel data is valid after a number of offset clock cycles of the falling edge of the word clock.

In the DSP TDM mode, the left channel data is valid after a number of offset clock cycles of the rising edge of the word clock pulse, and the right channel data is valid immediately after the left channel data.

The serial data output pin must be tri-stated when the output is not valid.

TDM supports mono mode where only one of the channels is used as controlled by AIF_MONO_MODE_EN.

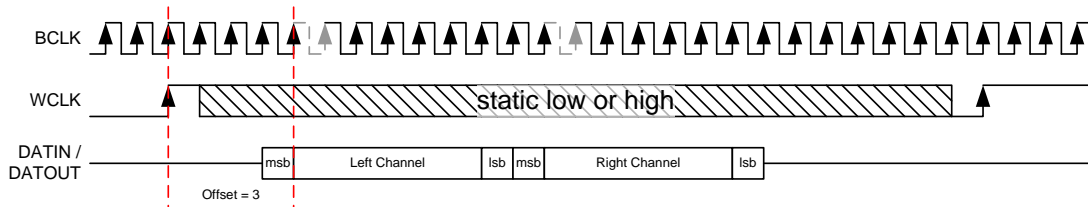


Figure 57: TDM DSP Format

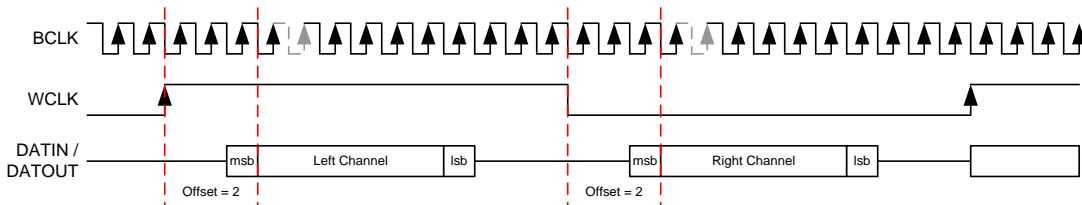


Figure 58: TDM Left Justified Format

12.5.2.6 AIF Clocking

DA9066 can be configured for the AIF to be master or slave using register AIF_CLK_EN. In slave mode, DA9066 receives the required BCLK and WCLK. In master mode, DA9066 generates the required BCLK and WCLK.

The WCLK sample rates that can be generated are defined in the sample rate register FS. The number of BCLKs per WCLK required can be set to 32, 64, 128, or 256 as defined by the frame length register AIF_BCLKS_PER_WCLK.

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12.6 Power Supplies

The DA9066 codec takes its supplies either from the DA9066 PMIC or direct from the battery. The Class-D speaker driver takes its supply directly from the battery via pins VDD_SPKR and GND_SPKR. The charge pump for the Class-G headphone and earpiece drivers takes its supply via the VDD_CP pin.

12.7 Reference Generation

12.7.1 Audio References

The audio circuits on DA9066 use supply-derived references, VMID and DACREF, of $0.45 * V_{DD_A}$ (V_{MID}) and $0.9 * V_{DD_A}$ (V_{DACREF}). The voltage references require off-chip decoupling capacitors.

The V_{MID} reference is decoupled by a capacitor on the VMID pin and is enabled using VMID_EN.

To speed up the start-up and shutdown of the codec, a low-resistance path can be enabled to (dis)charge the decoupling capacitor using bits VMID_FAST_CHARGE and VMID_FAST_DISCHARGE.

There is an additional reference buffer to provide a doubled version of V_{MID} that is decoupled via the DACREF pin. DACREF is enabled automatically by the system controller whenever it is required.

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13 Audio Register Map

Table 67: Audio Register Summary

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default | |
|------|------------------------|------------------------|--------------------------|---------------------------|------------------------|--------------------|---------------------------|---------------------|--------------------|-------------|-------------|
| 0x01 | CIF_CTRL | CIF_REG_SOFT_R ESET | | | | | | | CIF_I2C_WRITE_MODE | 0b0000_0000 | |
| 0x02 | SR | | | | | SR[3:0] | | | | | 0b0000_1010 |
| 0x03 | PC_COUNT | | | | | | | PC_RE_SYNC_AUTO | PC_FREERUN | 0b0000_0000 | |
| 0x04 | GAIN_RAM_P_CTRL | | | | | | | GAIN_RAMP_RATE[1:0] | | 0b0000_0000 | |
| 0x08 | SYSTEM_STATUS | | | | | | | sc2_busy | sc1_busy | 0b0000_0000 | |
| 0x09 | SYSTEM_MODES_CFG1 | MODE_CFG1[6:0] | | | | | | MODE_SUBMIT | | 0b0000_0000 | |
| 0x0a | SYSTEM_MODES_CFG2 | MODE_CFG2[6:0] | | | | | | MODE_SUBMIT | | 0b0000_0000 | |
| 0x0b | SYSTEM_MODES_CFG3 | MODE_CFG3[6:0] | | | | | | MODE_SUBMIT | | 0b0000_0000 | |
| 0x1c | ADC_FILTERS1 | ADC_HPF_EN | | ADC_AUDIO_HPF_CORNER[1:0] | | ADC_VOICE_EN | ADC_VOICE_HPF_CORNER[2:0] | | | 0b1000_0000 | |
| 0x1d | ADC_FILTERS2 | ADC_EQ_BAND2[3:0] | | | | ADC_EQ_BAND1[3:0] | | | | 0b1000_1000 | |
| 0x1e | ADC_FILTERS3 | ADC_EQ_BAND4[3:0] | | | | ADC_EQ_BAND3[3:0] | | | | 0b1000_1000 | |
| 0x1f | ADC_FILTERS4 | ADC_EQ_EN | | ADC_EQ_GAIN[1:0] | | ADC_EQ_BAND5[3:0] | | | | 0b0000_1000 | |
| 0x24 | DAC_FILTERS1 | DAC_HPF_EN | | DAC_AUDIO_HPF_CORNER[1:0] | | DAC_VOICE_EN | DAC_VOICE_HPF_CORNER[2:0] | | | 0b1000_0000 | |
| 0x25 | DAC_FILTERS2 | DAC_EQ_BAND2[3:0] | | | | DAC_EQ_BAND1[3:0] | | | | 0b1000_1000 | |
| 0x26 | DAC_FILTERS3 | DAC_EQ_BAND4[3:0] | | | | DAC_EQ_BAND3[3:0] | | | | 0b1000_1000 | |
| 0x27 | DAC_FILTERS4 | DAC_EQ_EN | | | | DAC_EQ_BAND5[3:0] | | | | 0b0000_1000 | |
| 0x28 | DAC_FILTERS5 | DAC_SOFTMUTE_EN | DAC_SOFTMUTE_RATE[2:0] | | | | | | | 0b0000_0000 | |
| 0x2c | ALC_CTRL1 | ALC_RELEASE | ALC_EXT_MODE | ALC_CALIB_VERIFY | ALC_AUTO_CALIB_EN | ALC_LIMIT | ALC_CALIB_MODE | ALC_SYNC_MODE | ALC_OFFSET_EN | 0b0000_0000 | |
| 0x2d | ALC_CTRL2 | ALC_RELEASE[3:0] | | | | ALC_ATTACK[3:0] | | | | 0b0000_0000 | |
| 0x2e | ALC_CTRL3 | ALC_INTEG_RELEASE[1:0] | | ALC_INTEG_ATTACK[1:0] | | ALC_HOLD[3:0] | | | | 0b0000_0000 | |
| 0x2f | ALC_NOISE | | | | ALC_NOISE[5:0] | | | | | 0b0011_1111 | |
| 0x30 | ALC_TARGET_MIN | | | | ALC_THRESHOLD_MIN[5:0] | | | | | 0b0011_1111 | |
| 0x31 | ALC_TARGET_MAX | | | | ALC_THRESHOLD_MAX[5:0] | | | | | 0b0000_0000 | |
| 0x32 | ALC_GAIN_LIMITS | ALC_GAIN_MAX[3:0] | | | | ALC_ATTEN_MAX[3:0] | | | | 0b1111_1111 | |
| 0x33 | ALC_ANALOG_GAIN_LIMITS | | ALC_ANALOG_GAIN_MAX[2:0] | | | | ALC_ANALOG_GAIN_MIN[2:0] | | | 0b0111_0001 | |

System PMIC for Dual/Quad-Core Processors

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default | |
|------|---------------------|--------------------------|------------|-----------------|------------------|-------------------------|--------------------------|-----------------|-------------------------|----------------|-------------|
| 0x34 | ALC_ANTICLIP_CTRL | ALC_ANTIPCLIP_EN | | | | | | | | | 0b0000_0000 |
| 0x35 | ALC_ANTICLIP_LEVEL | ALC_ANTICLIP_LEVEL[6:0] | | | | | | | | | 0b0000_0000 |
| 0x36 | ALC_OFFSET_AUTO_M_L | ALC_OFFSET_AUTO_M_L[7:0] | | | | | | | | | 0b0000_0000 |
| 0x37 | ALC_OFFSET_AUTO_U_L | | | | | | ALC_OFFSET_AUTO_U_L[3:0] | | | | 0b0000_0000 |
| 0x39 | ALC_OFFSET_MAN_M_L | ALC_OFFSET_MAN_M_L[7:0] | | | | | | | | | 0b0000_0000 |
| 0x3a | ALC_OFFSET_MAN_U_L | | | | | | ALC_OFFSET_MAN_U_L[3:0] | | | | 0b0000_0000 |
| 0x3b | ALC_OFFSET_AUTO_M_R | ALC_OFFSET_AUTO_M_R[7:0] | | | | | | | | | 0b0000_0000 |
| 0x3c | ALC_OFFSET_AUTO_U_R | | | | | | ALC_OFFSET_AUTO_U_R[3:0] | | | | 0b0000_0000 |
| 0x3e | ALC_OFFSET_MAN_M_R | ALC_OFFSET_MAN_M_R[7:0] | | | | | | | | | 0b0000_0000 |
| 0x3f | ALC_OFFSET_MAN_U_R | | | | | | ALC_OFFSET_MAN_U_R[3:0] | | | | 0b0000_0000 |
| 0x40 | ALC_CIC_OP_LVL_CTRL | ALC_CIC_OP_CHANNEL | | | | | | | ALC_CIC_OP_CTRL[1:0] | | 0b0000_0000 |
| 0x41 | ALC_CIC_OP_LVL_DATA | ALC_CIC_OP[7:0] | | | | | | | | | 0b0000_0000 |
| 0x44 | DIG_ROUTING_AIF | | | | AIF_R_SRC[1:0] | | | | | AIF_L_SRC[1:0] | 0b0001_0000 |
| 0x45 | DIG_ROUTING_DAC | DAC_R_MONO | | | DAC_R_SRC[1:0] | | DAC_L_MONO | | | DAC_L_SRC[1:0] | 0b0011_0010 |
| 0x46 | DIG_CTRL | DAC_R_INV | | | | | DAC_L_INV | | | | 0b0000_0000 |
| 0x48 | AIF_CTRL | AIF_EN | AIF_OE | AIF_TDM_MODE_EN | AIF_MONO_MODE_EN | AIF_WORD_LENGTH[1:0] | | AIF_FORMAT[1:0] | | 0b0000_1000 | |
| 0x49 | AIF_OFFSET | AIF_OFFSET[7:0] | | | | | | | | | 0b0000_0000 |
| 0x4a | AIF_CLK_MODE | AIF_CLK_EN | | | | | AIF_WCLK_POL | AIF_CLK_POL | AIF_BCLKS_PER_WCLK[1:0] | | 0b0000_0001 |
| 0x4c | PLL_CTRL | PLL_EN | PLL_SRM_EN | PLL_32K_MODE | PLL_MCLK_SQR_EN | PLL_INDIV[1:0] | | | | | 0b0000_1100 |
| 0x4d | PLL_FRAC_TOP | | | | | PLL_FBDIV_FRAC_TOP[4:0] | | | | 0b0000_0000 | |
| 0x4e | PLL_FRAC_BOT | PLL_FBDIV_FRAC_BOT[7:0] | | | | | | | | | 0b0000_0000 |
| 0x4f | PLL_INTEGER | PLL_FBDIV_INTEGER[6:0] | | | | | | | | | 0b0010_0000 |
| 0x50 | PLL_STATUS | | | | | | PLL_BYPASS_ACTIVE | PLL_MCLK_STATUS | PLL_SRM_LOCK | PLL_LOCK | 0b0000_0000 |
| 0x54 | DAC_NG_CTRL | DAC_NG_EN | | | | | | | | | 0b0000_0000 |
| 0x55 | DAC_NG_S | | | | | | DAC_NG | DAC_NG | DAC_NG_SETUP_TI | | 0b0000_0000 |

System PMIC for Dual/Quad-Core Processors

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|------|----------------------|---------------------------------|-------------------------------|--------------------------|--------------------------|----------------------------------|----------------------------|---------------------------|-------------------------|-------------|
| | ETUP_TIME | | | | | _RAMPD_N_RATE | _RAMPUP_RATE | ME[1:0] | | |
| 0x56 | DAC_NG_OFF_THRESHOLD | | | | | DAC_NG_OFF_THRESHOLD[2:0] | | | | 0b0000_0000 |
| 0x57 | DAC_NG_ON_THRESHOLD | | | | | DAC_NG_ON_THRESHOLD[2:0] | | | | 0b0000_0000 |
| 0x5c | CP_CTRL | CP_EN | CP_SMALL_SWITCH_FREQ_EN | CP_MCHANGE[1:0] | | CP_MOD[1:0] | | CP_ANALOGUE_LVL[1:0] | | 0b0110_0001 |
| 0x5d | CP_DELAY | CP_ONOFF[1:0] | | CP_TAU_DELAY[2:0] | | | CP_FCONTROL[2:0] | | | 0b1001_0101 |
| 0x5e | CP_DETECTOR | | | | | CPDET_DROP[1:0] | | | | 0b0000_0000 |
| 0x5f | CP_VOL_THRESHOLD1 | | | | | CP_THRESH_VDD2[5:0] | | | | 0b0011_0010 |
| 0x68 | MIC_CONFIG | | | | | DMIC_CLK_RATE | DMIC_SAMPLEPHASE | DMIC_DATA_SEL | | 0b0000_0000 |
| 0x6c | ACCDET_CONFIG | ACCDET_BTN_EN | | | | ACCDET_JACK_EN | ACCDET_MODE[1:0] | | | 0b0000_0000 |
| 0x6d | ACCDET_STATUS | ACCDET_BTN_STATUS[7:0] | | | | | | | | 0b0000_0000 |
| 0x6e | ACCDET_CFG1 | ACCDET_NO_JACK_RATE[3:0] | | | | ACCDET_JACK_DEBOUNCE[1:0] | | ACCDET_JACKBOOST[1:0] | | 0b0100_0110 |
| 0x6f | ACCDET_CFG2 | ACCDET_FOUR_POLE_JACK_RATE[3:0] | | | | ACCDET_THREE_POLE_JACK_RATE[3:0] | | | | 0b0100_1000 |
| 0x70 | ACCDET_CFG3 | ACCDET_JACK_MODE[1:0] | ACCDET_TIMEOUT[1:0] | | ACCDET_ADC_DEBOUNCE[1:0] | | ACCDET_BTNBOOST[1:0] | | 0b0000_0000 | |
| 0x72 | ACCDET_CFG5 | | ACCDET_ADC_FRC_EN | ACCDET_JACKDET_HYST_EN | ACCDET_JACKDET_FRC_EN | ACCDET_ISOURCE_MIC_FRC_EN | ACCDET_ISOURCE_JACK_FRC_EN | ACCDET_ADC_PD_MICBIAS_MSK | ACCDET_ADC_FORCE_IN_MSK | 0b0010_0100 |
| 0x76 | ACCDET_THRESHOLD1 | ACCDET_JACK_THR1[7:0] | | | | | | | | 0b0000_0000 |
| 0x77 | ACCDET_THRESHOLD2 | ACCDET_JACK_THR2[7:0] | | | | | | | | 0b0000_0000 |
| 0x78 | ACCDET_THRESHOLD3 | ACCDET_BTN_THR1[7:0] | | | | | | | | 0b0000_0000 |
| 0x79 | ACCDET_THRESHOLD4 | ACCDET_BTN_THR2[7:0] | | | | | | | | 0b0000_0000 |
| 0x81 | CHIP_ID1 | CHIP_ID1[7:0] | | | | | | | | 0b0010_0001 |
| 0x82 | CHIP_ID2 | CHIP_ID2[7:0] | | | | | | | | 0b0101_0011 |
| 0x83 | CHIP_REVISION | CHIP_MAJOR[3:0] | | | | CHIP_MINOR[3:0] | | | | 0b0000_0000 |
| 0x84 | SPARE1 | SPARE1[7:0] | | | | | | | | 0b0000_0000 |
| 0x85 | STATUS1 | STATUS_SPARE1[7:0] | | | | | | | | 0b0000_0000 |
| 0x88 | LIMITER_CTRL1 | SP_PWR_THD_HOLD_TIME[1:0] | | SP_PWR_THD_REL_RATE[2:0] | | | SP_PWR_THD_ATK_RATE[2:0] | | | 0b0000_0000 |
| 0x89 | LIMITER_CTRL2 | SP_LIM_FINE_GAIN_FRC_EN | SP_LIM_FINE_GAIN_FRC_VAL[2:0] | | SP_THD_HYST_DIS | SP_PWR_HYST_DIS | SP_THD_EN | SP_PWR_EN | | 0b0000_0000 |
| 0x8a | LIMITER_PWLIM | | | | SP_PWR_LIM[5:0] | | | | | 0b0000_0000 |
| 0x8b | LIMITER_THDLIM | | | | SP_THD_LIM[5:0] | | | | | 0b0000_0000 |

System PMIC for Dual/Quad-Core Processors

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|------|---------------------|------------------|---------------------|----------------------------|-------------------------|------------------------------|------------------|---------------------|-------------|-------------|
| 0x8c | NG_CTRL1 | SP_NG_EN | | | | | | SP_NG_ATT[1:0] | | 0b0000_0000 |
| 0x8d | NG_CTRL2 | SP_HLD_TIME[1:0] | | SP_REL_RATE[2:0] | | | SP_ATK_RATE[2:0] | | 0b0000_0000 | |
| 0x90 | AUX_L_CTRL | AUX_L_AMP_EN | AUX_L_AMP_MUTE_EN | AUX_L_AMP_RAMP_EN | AUX_L_AMP_ZC_EN | AUX_L_AMP_ZC_SEL[1:0] | | | | 0b0100_0100 |
| 0x91 | AUX_L_GAIN | | | AUX_L_AMP_GAIN[5:0] | | | | | 0b0011_0101 | |
| 0x92 | AUX_L_GAIN_STATUS | | | AUX_L_AMP_GAIN_STATUS[5:0] | | | | | 0b0000_0000 | |
| 0x93 | AUX_R_CTRL | AUX_R_AMP_EN | AUX_R_AMP_MUTE_EN | AUX_R_AMP_RAMP_EN | AUX_R_AMP_ZC_EN | AUX_R_AMP_ZC_SEL[1:0] | | | | 0b0100_0100 |
| 0x94 | AUX_R_GAIN | | | AUX_R_AMP_GAIN[5:0] | | | | | 0b0011_0101 | |
| 0x95 | AUX_R_GAIN_STATUS | | | AUX_R_AMP_GAIN_STATUS[5:0] | | | | | 0b0000_0000 | |
| 0x98 | MIC_L_CTRL | MIC_L_AMP_EN | MIC_L_AMP_MUTE_EN | | | MIC_L_AMP_IN_SEL[1:0] | | | | 0b0100_0000 |
| 0x99 | MIC_L_GAIN | | | | | MIC_L_AMP_GAIN[2:0] | | | 0b0000_0001 | |
| 0x9a | MIC_L_GAIN_STATUS | | | | | MIC_L_AMP_GAIN_STATUS[2:0] | | | 0b0000_0001 | |
| 0x9b | MIC_R_CTRL | MIC_R_AMP_EN | MIC_R_AMP_MUTE_EN | | | MIC_R_AMP_IN_SEL[1:0] | | | | 0b0100_0000 |
| 0x9c | MIC_R_GAIN | | | | | MIC_R_AMP_GAIN[2:0] | | | 0b0000_0001 | |
| 0x9d | MIC_R_GAIN_STATUS | | | | | MIC_R_AMP_GAIN_STATUS[2:0] | | | 0b0000_0001 | |
| 0x9e | MIC_EXT_CTRL | MIC_EXT_AMP_EN | MIC_EXT_AMP_MUTE_EN | | | MIC_EXT_AMP_IN_SEL[1:0] | | | | 0b0100_0000 |
| 0x9f | MIC_EXT_GAIN | | | | | MIC_EXT_AMP_GAIN[2:0] | | | 0b0000_0001 | |
| 0xa0 | MIC_EXT_GAIN_STATUS | | | | | mic_ext_amp_gain_status[2:0] | | | 0b0000_0001 | |
| 0xa1 | MICBIAS1_CTRL | MICBIAS1_EN | | | | | | | | 0b0000_0000 |
| 0xa2 | MICBIAS2_CTRL | MICBIAS2_EN | | | | | | MICBIAS2_LEVEL[1:0] | | 0b0000_0001 |
| 0xa3 | MICBIAS3_CTRL | MICBIAS3_EN | | | | | | MICBIAS3_LEVEL[1:0] | | 0b0000_0001 |
| 0xa8 | MIXIN_L_CTRL | MIXIN_L_AMP_EN | MIXIN_L_AMP_MUTE_EN | MIXIN_L_AMP_RAMP_EN | MIXIN_L_AMP_ZC_EN | MIXIN_L_MIX_EN | | | | 0b0100_0000 |
| 0xa9 | MIXIN_L_GAIN | | | | | MIXIN_L_AMP_GAIN[3:0] | | | 0b0000_0011 | |
| 0xaa | MIXIN_L_GAIN_STATUS | | | | | MIXIN_L_AMP_GAIN_STATUS[3:0] | | | 0b0000_0000 | |
| 0xab | MIXIN_L_SELECT | DMIC_L_EN | | | MIXIN_L_MIX_SELECT[4:0] | | | | | 0b0000_0000 |
| 0xac | MIXIN_R_CTRL | MIXIN_R_AMP_EN | MIXIN_R_AMP | MIXIN_R_AMP | MIXIN_R_AMP_Z | MIXIN_R_MIX_EN | | | | 0b0100_0000 |

System PMIC for Dual/Quad-Core Processors

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default |
|------|---------------------|------------------|--------------------------------|---------------|-----------------------|------------------------------|----------------------|---|---|-------------|
| | | N | _MUTE_EN | _RAMP_EN | C_EN | | | | | |
| 0xad | MIXIN_R_GAIN | | | | | MIXIN_R_AMP_GAIN[3:0] | | | | 0b0000_0011 |
| 0xae | MIXIN_R_GAIN_STATUS | | | | | MIXIN_R_AMP_GAIN_STATUS[3:0] | | | | 0b0000_0000 |
| 0xaf | MIXIN_R_SELECT | DMIC_R_EN | MIC_BIAS_OUTPUT_SELECT | | | MIXIN_R_MIX_SELECT[4:0] | | | | 0b0000_0000 |
| 0xb4 | ADC_L_CTRL | ADC_L_EN | ADC_L_MUTE_EN | ADC_L_RAMP_EN | | | | | | 0b0100_0000 |
| 0xb5 | ADC_L_GAIN | | ADC_L_DIGITAL_GAIN[6:0] | | | | | | | 0b0110_1111 |
| 0xb6 | ADC_L_GAIN_STATUS | | ADC_L_DIGITAL_GAIN_STATUS[6:0] | | | | | | | 0b0000_0000 |
| 0xb8 | ADC_R_CTRL | ADC_R_EN | ADC_R_MUTE_EN | ADC_R_RAMP_EN | | | | | | 0b0100_0000 |
| 0xb9 | ADC_R_GAIN | | ADC_R_DIGITAL_GAIN[6:0] | | | | | | | 0b0110_1111 |
| 0xba | ADC_R_GAIN_STATUS | | ADC_R_DIGITAL_GAIN_STATUS[6:0] | | | | | | | 0b0000_0000 |
| 0xbc | DAC_L_CTRL | DAC_L_EN | DAC_L_MUTE_EN | DAC_L_RAMP_EN | | | | | | 0b0100_0000 |
| 0xbd | DAC_L_GAIN | | DAC_L_DIGITAL_GAIN[6:0] | | | | | | | 0b0110_1111 |
| 0xbe | DAC_L_GAIN_STATUS | | DAC_L_DIGITAL_GAIN_STATUS[6:0] | | | | | | | 0b0000_0000 |
| 0xbf | DAC_R_CTRL | DAC_R_EN | DAC_R_MUTE_EN | DAC_R_RAMP_EN | | | | | | 0b0100_0000 |
| 0xc0 | DAC_R_GAIN | | DAC_R_DIGITAL_GAIN[6:0] | | | | | | | 0b0110_1111 |
| 0xc1 | DAC_R_GAIN_STATUS | | DAC_R_DIGITAL_GAIN_STATUS[6:0] | | | | | | | 0b0000_0000 |
| 0xc4 | MIXOUT_L_CTRL | MIXOUT_L_AMP_EN | | | MIXOUT_L_SOFT_MIX_EN | MIXOUT_L_MIX_EN | | | | 0b0001_0000 |
| 0xc5 | MIXOUT_L_SELECT | | MIXOUT_L_MIX_SELECT[6:0] | | | | | | | 0b0000_0000 |
| 0xc6 | MIXOUT_R_CTRL | MIXOUT_R_AMP_EN | | | MIXOUT_R_SOFT_MIX_EN | MIXOUT_R_MIX_EN | | | | 0b0001_0000 |
| 0xc7 | MIXOUT_R_SELECT | | MIXOUT_R_MIX_SELECT[6:0] | | | | | | | 0b0000_0000 |
| 0xc8 | MIXOUT_S_CTRL | MIXOUT_SP_AMP_EN | | | MIXOUT_SP_SOFT_MIX_EN | MIXOUT_SP_MIX_EN | | | | 0b0001_0000 |
| 0xc9 | MIXOUT_S_SELECT | | MIXOUT_SP_MIX_SELECT[6:0] | | | | | | | 0b0000_0000 |
| 0xcc | HP_L_CTRL | HP_L_AMP_EN | HP_L_AMP_MUTE_EN | HP_L_AMP_EN | HP_L_AMP_ZC_EN | HP_L_AMP_OE | HP_L_AMP_MIN_GAIN_EN | | | 0b0100_0000 |
| 0xcd | HP_L_GAIN | | HP_L_AMP_GAIN[6:0] | | | | | | | 0b0111_0010 |
| 0xce | HP_L_GAIN_STATUS | | HP_L_AMP_GAIN_STATUS[6:0] | | | | | | | 0b0000_0000 |
| 0xcf | HP_R_CTRL | HP_R_AMP_EN | HP_R_AMP_MUTE_EN | HP_R_AMP_EN | HP_R_AMP_ZC_EN | HP_R_AMP_OE | HP_R_AMP_MIN_GAIN_EN | | | 0b0100_0000 |

System PMIC for Dual/Quad-Core Processors

| Addr | Function | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Default | |
|------|------------------|---------------------|---------------------------|-----------------------|------------------|-----------|--------------------|------------------|------------------|-------------|-------------|
| | L | MP_EN | AMP_MUTE_EN | AMP_RAMP_EN | MP_ZC_EN | MP_OE | MP_MIN_GAIN_EN | | | | |
| 0xd0 | HP_R_GAIN | | HP_R_AMP_GAIN[6:0] | | | | | | | 0b0111_0010 | |
| 0xd1 | HP_R_GAIN_STATUS | | HP_R_AMP_GAIN_STATUS[6:0] | | | | | | | 0b0000_0000 | |
| 0xd2 | HP_TEST | | | | | | | | HP_AMP_EMS_EN | 0b0000_0000 | |
| 0xd4 | EP_CTRL | EP_AMP_EN | EP_AMP_MUTE_EN | EP_AMP_RAM_P_EN | EP_AMP_ZC_EN | EP_AMP_OE | EP_AMP_MIN_GAIN_EN | EP_AMP_BIAS[1:0] | | 0b0100_0000 | |
| 0xd5 | EP_GAIN | | EP_AMP_GAIN[6:0] | | | | | | | 0b0111_0010 | |
| 0xd6 | EP_GAIN_STATUS | | EP_AMP_GAIN_STATUS[6:0] | | | | | | | 0b0000_0000 | |
| 0xd8 | SP_CTRL | SP_AMP_EN | SP_AMP_MUTE_EN | SP_AMP_RAM_P_EN | SP_AMP_ZC_EN | | SP_AMP_MIN_GAIN_EN | | | 0b0100_0000 | |
| 0xd9 | SP_GAIN | | SP_AMP_GAIN[5:0] | | | | | | | 0b0011_0011 | |
| 0xda | SP_GAIN_STATUS | | SP_AMP_GAIN_STATUS[5:0] | | | | | | | 0b0000_0000 | |
| 0xdb | SP_CFG1 | SP_AMP_CONFIG1[7:0] | | | | | | | | | 0b0000_0000 |
| 0xdc | SP_CFG2 | SP_AMP_CONFIG2[7:0] | | | | | | | | | 0b0000_0000 |
| 0xde | SP_STATUS | SP_AMP_STATUS[7:0] | | | | | | | | | 0b0000_0000 |
| 0xe4 | REFERENCES | VMID_EN | | VMID_FAST_DISCHARGE | VMID_FAST_CHARGE | BIAS_EN | | | | 0b0000_0000 | |
| 0xe5 | IO_CTRL | | | | | | | | IO_VOLTAGE_LEVEL | 0b0000_0000 | |
| 0xe6 | LDO_CTRL | LDO_EN | | LDO_LEVEL_SELECT[1:0] | | | | | 0b0000_0000 | | |

System PMIC for Dual/Quad-Core Processors

14 Package Information

14.1 Package Outline

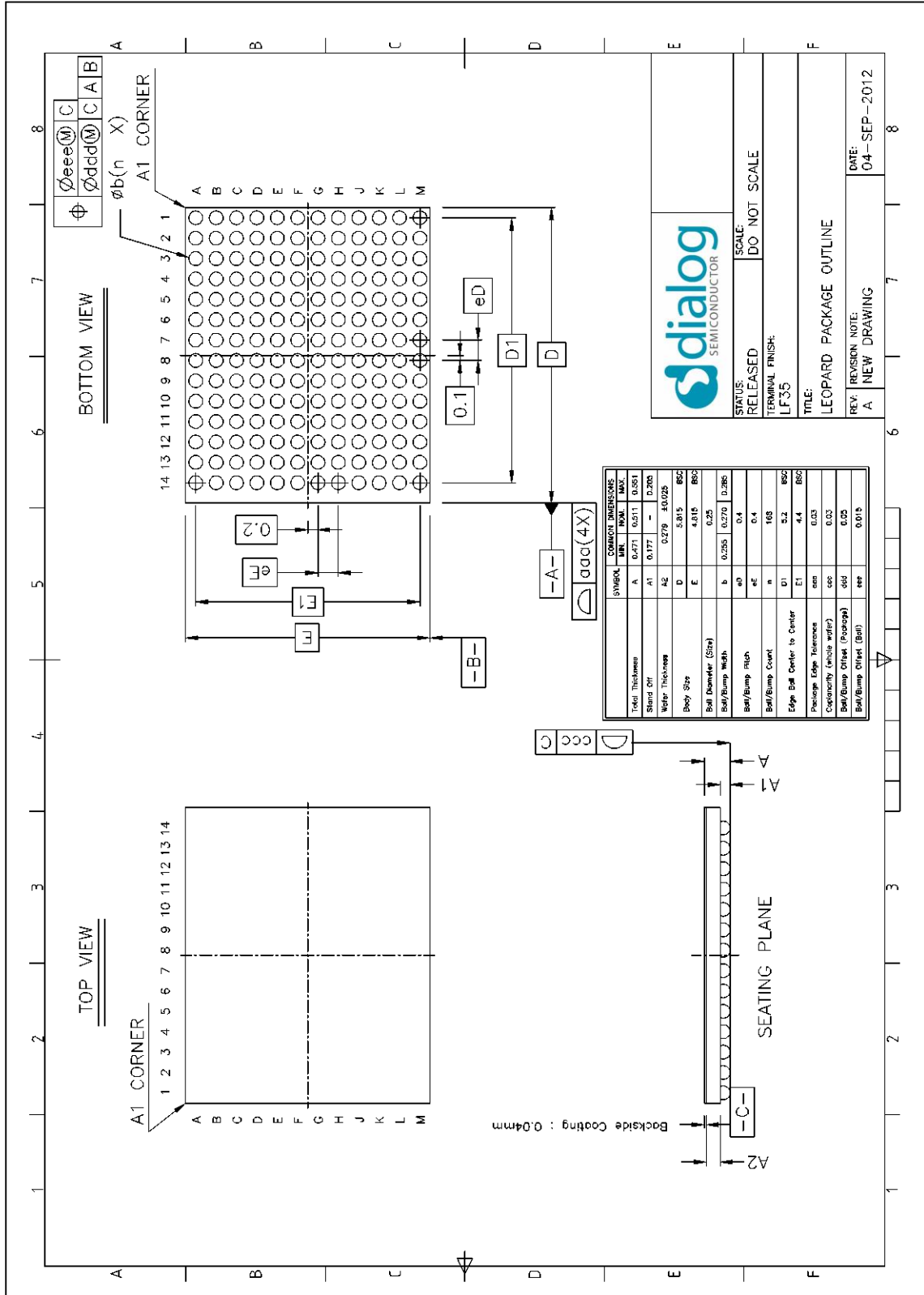


Figure 59: Package Outline Drawing

System PMIC for Dual/Quad-Core Processors**15 Ordering Information**

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Dialog Semiconductor sales representative.

Table 68: Ordering information

| Part number (Note 1) | Package | Size (mm) | Shipment form | Pack quantity |
|-------------------------|---------|-----------------|---------------|---------------|
| DA9066-xxUL2 | WLCSP | 5.8 x 4.8 x 0.4 | T&R | 3000 |

Note 1 xx represents a placeholder for the specific OTP variant.

System PMIC for Dual/Quad-Core Processors

Appendix A PMIC Register Descriptions

A.1 Status / Config

Table 69: Register Status_A

| Address | Name | POR value | Status |
|---------|----------|-----------|--------|
| 0x0001 | STATUS_A | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------|---|-----------|----------|----------|----------|----------|
| Reserved | M_CTL | | VDD_MON_S | Reserved | Reserved | Reserved | Reserved |

| Field name | Bits | Type | POR | Description |
|------------|-------|------|-----|-------------------|
| M_CTL | [6:5] | RO | 0x0 | M_CTL pin level |
| VDD_MON_S | [4] | RO | 0x0 | VDD monitor level |

Table 70: Register STATUS_B

| Address | Name | POR value | Status |
|---------|----------|-----------|--------|
| 0x0002 | STATUS_B | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|------------|------------|----------|----------|------------|------------|--------|
| Reserved | SEQUENCING | Reserved 0 | Reserved | Reserved | Reserved 0 | Reserved 0 | nONKEY |

| Field name | Bits | Type | POR | Description |
|------------|------|------|-----|-----------------------------|
| SEQUENCING | [6] | RO | 0x0 | Sequencer is processing IDs |
| nONKEY | [0] | RO | 0x0 | nONKEY status |

Table 71: Register STATUS_C

| Address | Name | POR value | Status |
|---------|----------|-----------|--------|
| 0x0003 | STATUS_C | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------|------------|---------|----|------------|------------|------------|
| Reserved 0 | Reserved 0 | Reserved 0 | nJIG_ON | TA | Reserved 0 | Reserved 0 | Reserved 0 |

| Field name | Bits | Type | POR | Description |
|------------|------|------|-----|-----------------------|
| nJIG_ON | [4] | RO | 0x0 | nJIG_ON monitor level |
| TA | [3] | RO | 0x0 | TA monitor level |

System PMIC for Dual/Quad-Core Processors

Table 72: Register EVENT_A

| Address | Name | POR value | IRQ event |
|---------|---------|-----------|-----------|
| 0x0004 | EVENT_A | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|---------|-----------|-----------|---------|---------------|------|
| E_TICK | E_SEQ_RDY | E_ALARM | E_VDD_MON | E_VDD_LOW | E_TBAT2 | Reserved 0 | E_VF |

| Field name | Bits | Type | POR | Description |
|------------|------|---------|-----|---|
| E_TICK | [7] | RW W1CL | 0x0 | Event - RTC tick alarm |
| E_SEQ_RDY | [6] | RW W1CL | 0x0 | Event - sequencer reached stop position |
| E_ALARM | [5] | RW W1CL | 0x0 | Event - RTC calendar alarm |
| E_VDD_MON | [4] | RW W1CL | 0x0 | Event - VDD below vdd_mon comparator threshold (3.1V) |
| E_VDD_LOW | [3] | RW W1CL | 0x0 | Event - VDD below vddout_mon ADC threshold |
| E_TBAT2 | [2] | RW W1CL | 0x0 | Event - TBAT2 temperature threshold out of range |
| E_VF | [0] | RW W1CL | 0x0 | Event - VF is out of range |

Table 73: Register EVENT_B

| Address | Name | POR value | IRQ event |
|---------|---------|-----------|-----------|
| 0x0005 | EVENT_B | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------|-----------|---------|-------------------|------------------|-------------|-------------|
| Reserved 0 | Reserved 0 | E_ADC_EOM | E_TBAT1 | E_nONKEY_HOLD_OFF | E_nONKEY_HOLD_ON | E_nONKEY_HI | E_nONKEY_LO |

| Field name | Bits | Type | POR | Description |
|-------------------|------|---------|-----|---|
| E_ADC_EOM | [5] | RW W1CL | 0x0 | Event - ADC manual conversion result ready |
| E_TBAT1 | [4] | RW W1CL | 0x0 | Event TBAT1 temperature threshold out of range |
| E_nONKEY_HOLD_OFF | [3] | RW W1CL | 0x0 | Event - nONKEY low for longer than NONKEY_HOLD_OFF_DEB in active state Assertion |
| E_nONKEY_HOLD_ON | [2] | RW W1CL | 0x0 | Event - nONKEY low for longer than NONKEY_HOLD_ON_DEB in inactive state Assertion |
| E_nONKEY_HI | [1] | RW W1CL | 0x0 | Event - nONKEY high for field: NONKEY_DEB (Reg: ONKEY_CONT1 [0x006B]) assertion |
| E_nONKEY_LO | [0] | RW W1CL | 0x0 | Event - nONKEY low for field: NONKEY_DEB (Reg: ONKEY_CONT1 [0x006B]) assertion |

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Table 74: Register EVENT_C

| Address | Name | POR value | IRQ event |
|---------|---------|-----------|-----------|
| 0x0006 | EVENT_C | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----------|--------|-----------|------|---------------|---------------|---------------|
| E_JACK_DET | E_ACC_DET | GPIO_1 | E_nJIG_ON | E_TA | Reserved 0 | Reserved 0 | Reserved 0 |

| Field name | Bits | Type | POR | Description |
|------------|------|------------|-----|--------------------------------|
| E_JACK_DET | [7] | RW W1CL | 0x0 | Jack detect status |
| E_ACC_DET | [6] | RW W1CL | 0x0 | Accessory detect event flag |
| GPIO_1 | [5] | RW W1CL | 0x0 | unused |
| E_nJIG_ON | [4] | RW W1CL | 0x0 | Event - nJIG_ON monitor active |
| E_TA | [3] | RW W1CL | 0x0 | Event - TA monitor active |

Table 75: Register FAULT_LOG

| Address | Name | POR value | |
|---------|-----------|-----------|--|
| 0x0007 | FAULT_LOG | 0x02 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---------------|----------|----------|-----------|-----------|-----------|-----------|
| WAIT_SHUT | Reserved 0 | KEY_SHUT | Reserved | TEMP_OVER | VDD_START | VDD_FAULT | TWD_ERROR |

| Field name | Bits | Type | POR | Description |
|------------|------|------------|-----|--|
| WAIT_SHUT | [7] | RW W1CL | 0x0 | Power down by time out of ID WAIT_STEP |
| KEY_SHUT | [5] | RW W1CL | 0x0 | Power down by a long press of nONKEY |
| TEMP_OVER | [3] | RW W1CL | 0x0 | Junction over temperature detection |
| VDD_START | [2] | RW W1CL | 0x0 | Power down by VBAT under voltage detection (within 10 seconds from releasing nRESET) |
| VDD_FAULT | [1] | RW W1CL | 0x1 | Power down by VBAT under voltage detection |
| TWD_ERROR | [0] | RW W1CL | 0x0 | Watchdog time violation |

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Table 76: Register IRQ_MASK_A

| Address | Name | POR value | IRQ event mask |
|---------|------------|-----------|----------------|
| 0x0008 | IRQ_MASK_A | 0x02 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|-----------|---------|-----------|-----------|---------|---------------|------|
| M_TICK | M_SEQ_RDY | M_ALARM | M_VDD_MON | M_VDD_LOW | M_TBAT2 | Reserved 1 | M_VF |

| Field name | Bits | Type | POR | Description |
|------------|------|-----------|-----|--|
| M_TICK | [7] | RW OTP | 0x0 | nIRQ Mask - RTC tick alarm event |
| M_SEQ_RDY | [6] | RW OTP | 0x0 | nIRQ Mask - sequencer reached stop position event |
| M_ALARM | [5] | RW OTP | 0x0 | nIRQ Mask - RTC calendar alarm event |
| M_VDD_MON | [4] | RW OTP | 0x0 | nIRQ_Mask - VDD_MON voltage level warning |
| M_VDD_LOW | [3] | RW OTP | 0x0 | nIRQ_Mask - VDD below ADC vdd_mon threshold |
| M_TBAT2 | [2] | RW OTP | 0x0 | nIRQ Mask - TBAT1 temperature threshold out of range |
| M_VF | [0] | RW OTP | 0x0 | nIRQ_Mask - VF out of range |

Table 77: Register IRQ_MASK_B

| Address | Name | POR value | IRQ event mask |
|---------|------------|-----------|----------------|
| 0x0009 | IRQ_MASK_B | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|---------------|-------------|-----------------------|----------------------|-----------------|-----------------|
| Reser ved | Reser ved | M_ADC_ EOM | M_TB AT1 | M_nONKEY_HOL D_OFF | M_nONKEY_HO LD_ON | M_nONKE Y_HI | M_nONKE Y_LO |

| Field name | Bits | Type | POR | Description |
|-------------------|------|-----------|-----|--|
| M_ADC_EOM | [5] | RW OTP | 0x0 | nIRQ Mask - ADC manual conversion result ready event |
| M_TBAT1 | [4] | RW OTP | 0x0 | nIRQ Mask - TBAT1 temperature threshold out of range |
| M_nONKEY_HOLD_OFF | [3] | RW OTP | 0x0 | nIRQ Mask - nONKEY_HOLD_OFF assertion event |
| M_nONKEY_HOLD_ON | [2] | RW OTP | 0x0 | nIRQ Mask - nONKEY_HOLD_ON assertion event |
| M_nONKEY_HI | [1] | RW OTP | 0x0 | nIRQ Mask - nONKEY_HI assertion event |
| M_nONKEY_LO | [0] | RW OTP | 0x0 | nIRQ Mask - nONKEY_LO assertion event |

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Table 78: Register IRQ_MASK_C

| Address | Name | POR value | IRQ event mask |
|---------|------------|-----------|----------------|
| 0x000A | IRQ_MASK_C | 0x27 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|-----------|---------------|-----------|------|---------------|---------------|---------------|
| M_JACK_DET | M_ACC_DET | Reserved 1 | M_nJIG_ON | M_TA | Reserved 1 | Reserved 1 | Reserved 1 |

| Field name | Bits | Type | POR | Description |
|------------|------|-----------|-----|------------------------------|
| M_JACK_DET | [7] | RW OTP | 0x0 | nIRQ Mask - Jack detect |
| M_ACC_DET | [6] | RW OTP | 0x0 | nIRQ Mask - Accessory detect |
| M_nJIG_ON | [4] | RW OTP | 0x0 | nIRQ Mask - nJIG_ON montior |
| M_TA | [3] | RW OTP | 0x0 | nIRQ Mask - TA montior |

Table 79: Register CONTROL_A

| Address | Name | POR value | System control |
|---------|-----------|-----------|----------------|
| 0x000B | CONTROL_A | 0x63 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|------------|------------|--------|---------|---------|--------|--------|
| GPI_V | Reserved 1 | Reserved 1 | PM_I_V | PM_IF_V | PWR1_EN | PWR_EN | SYS_EN |

| Field name | Bits | Type | POR | Description | |
|------------|------|-----------|-----|--|--------------------|
| GPI_V | [7] | RW OTP | 0x0 | GPIO input buffers, VRFANA_EN, RFBUCK_EN and M_CTL powered from: | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | VDDINT |
| | | | | 0x1 | VDDIO |
| PM_I_V | [4] | RW OTP | 0x0 | nONKEY, TA and nJIG_ON inputs powered from: | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | VDDINT |
| | | | | 0x1 | VDDIO |
| PM_IF_V | [3] | RW OTP | 0x0 | SCL and SDA inputs powered from: | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | VDDINT |
| | | | | 0x1 | VDDIO |
| PWR1_EN | [2] | RW OTP | 0x0 | Target status of power domain POWER1: - OTP/SW configured | |
| PWR_EN | [1] | RW OTP | 0x1 | Target status of power domain POWER: - OTP/SW configured | |

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| Field name | Bits | Type | POR | Description |
|------------|------|-----------|-----|--|
| SYS_EN | [0] | RW OTP | 0x1 | Target status of power domain SYSTEM: - State of GPI (OTP default ignored) or - OTP/SW configured (configured by GPIO_2_PIN register setting) |

Table 80: Register CONTROL_B

| Address | Name | POR value | System control |
|---------|-----------|-----------|----------------|
| 0x000C | CONTROL_B | 0x2C | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|------------|------------|-----------|------------|-----------|----------|----------|
| SHUTDOWN | DEEP_SLEEP | WRITE_MODE | I2C_SPEED | OTPREAD_EN | AUTO_BOOT | Reserved | Reserved |

| Field name | Bits | Type | POR | Description | | | | | | |
|------------|--|-----------|-----|---|-------|-------------|-----------|---|-----------|--|
| SHUTDOWN | [7] | RW RT0 | 0x0 | If set to '1' the sequencer powers down to RESET mode. Automatically cleared (back to 0) before leaving RESET mode | | | | | | |
| DEEP_SLEEP | [6] | RW RT0 | 0x0 | If set to '1' PMIC goes to Deep Sleep mode (sequencer stops at pointer PART_DOWN). Automatically cleared (back to 0) before powering up from POWER_DOWN mode | | | | | | |
| WRITE_MODE | [5] | RW OTP | 0x1 | I2C write mode <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0: Page write mode</td> </tr> <tr> <td>0x1 (POR)</td> <td>1: Repeated write mode</td> </tr> </tbody> </table> | Value | Description | 0x0 | 0: Page write mode | 0x1 (POR) | 1: Repeated write mode |
| Value | Description | | | | | | | | | |
| 0x0 | 0: Page write mode | | | | | | | | | |
| 0x1 (POR) | 1: Repeated write mode | | | | | | | | | |
| I2C_SPEED | [4] | RW OTP | 0x0 | I2C DATA READ speed <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: 400 kHz</td> </tr> <tr> <td>0x1</td> <td>1: 1.7 MHz</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: 400 kHz | 0x1 | 1: 1.7 MHz |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: 400 kHz | | | | | | | | | |
| 0x1 | 1: 1.7 MHz | | | | | | | | | |
| OTPREAD_EN | [3] | RW OTP | 0x1 | OTP Read control <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0: OTP Read after POWERDOWN mode disabled</td> </tr> <tr> <td>0x1 (POR)</td> <td>1: Power supplies configured with OTP values (when leaving POWERDOWN mode)</td> </tr> </tbody> </table> | Value | Description | 0x0 | 0: OTP Read after POWERDOWN mode disabled | 0x1 (POR) | 1: Power supplies configured with OTP values (when leaving POWERDOWN mode) |
| Value | Description | | | | | | | | | |
| 0x0 | 0: OTP Read after POWERDOWN mode disabled | | | | | | | | | |
| 0x1 (POR) | 1: Power supplies configured with OTP values (when leaving POWERDOWN mode) | | | | | | | | | |
| AUTO_BOOT | [2] | RW OTP | 0x1 | Sequencer startup requires: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0: Valid wake up event</td> </tr> <tr> <td>0x1 (POR)</td> <td>1: No wake up (PMIC automatically starts)</td> </tr> </tbody> </table> | Value | Description | 0x0 | 0: Valid wake up event | 0x1 (POR) | 1: No wake up (PMIC automatically starts) |
| Value | Description | | | | | | | | | |
| 0x0 | 0: Valid wake up event | | | | | | | | | |
| 0x1 (POR) | 1: No wake up (PMIC automatically starts) | | | | | | | | | |

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Table 81: Register CONTROL_C

| Address | Name | POR value | System control |
|---------|-----------|-----------|----------------|
| 0x000D | CONTROL_C | 0x04 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|------------|---|---|----------|------------|
| Reserved | Reserved | Reserved | DEBOUNCING | | | Reserved | Reserved 0 |

| Field name | Bits | Type | POR | Description | |
|------------|----------------|-----------|-----|-----------------------------------|--------------------|
| DEBOUNCING | [4:2] | RW OTP | 0x1 | GPI, TA and nJIG_ON debounce time | |
| | | | | Value | Description |
| | | | | 0x0 | 000: No debounce |
| | | | | 0x1 (POR) | 001: 10.24 msec |
| | | | | 0x2 | 010: 20.48 msec |
| | | | | 0x3 | 011: 40.96 msec |
| | | | | 0x4 | 100: 102.4 msec |
| | | | | 0x5 | 101: 1024 msec |
| | | | | 0x6 | 110: 2048 msec |
| 0x7 | 111: 5120 msec | | | | |

Table 82: Register CONTROL_D

| Address | Name | POR value | System control |
|---------|-----------|-----------|----------------|
| 0x000E | CONTROL_D | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|------------|-----------|---|---|
| WATCHDOG | reserved | reserved | reserved | KEEPACT_EN | TWDSSCALE | | |

| Field name | Bits | Type | POR | Description |
|------------|---|-----------|-----|---|
| WATCHDOG | [7] | RO | 0x0 | If set to '1', watchdog timer is reset. Automatically cleared back to '0' |
| | | | | reserved |
| | | | | reserved |
| | | | | reserved |
| KEEPACT_EN | [3] | RW OTP | 0x0 | Value |
| | | | | Description |
| | | | | 0x0 (POR) |
| 0x1 | 1: nONKEY disabled, KEEPACT enabled (hardware assertion of bit WATCHDOG) | | | |

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| Field name | Bits | Type | POR | Description | |
|------------|----------|-----------|-----|------------------------|--|
| TWDSCALE | [2:0] | RW OTP | 0x0 | Watchdog timer control | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | 000: Watchdog disabled |
| | | | | 0x1 | 001: 1x scaling applied to t_{WDMAX} |
| | | | | 0x2 | 010: 2x |
| | | | | 0x3 | 011: 4x |
| | | | | 0x4 | 100: 8x |
| | | | | 0x5 | 101: 16x |
| | | | | 0x6 | 110: 32x |
| 0x7 | 111: 64x | | | | |

Table 83: Register PD_DIS

| Address | Name | POR value | Power down disable |
|---------|--------|-----------|--------------------|
| 0x000F | PD_DIS | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------|-------------|----------------|--------------|--------------|---------------|-------------|
| PM_CONT_PD | OUT_32K_PD | CHG_BBAT_PD | Reserv ed 0 | HS_2_WIRE_PD | PM_IF_P D | GP_ADC_ PD | GPIO_P D |

| Field name | Bits | Type | POR | Description | |
|--------------|------|-----------|-----|--------------|---|
| PM_CONT_PD | [7] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: SYS_EN enabled during POWERDOWN |
| | | | | 0x1 | 1: Auto-disable SYS_EN during POWERDOWN (force the detection of a pending active state by re-enabling the pin through a passive state of the related GPI status register) |
| OUT_32K_PD | [6] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: OUT_32K enabled during POWERDOWN |
| | | | | 0x1 | 1: Auto-disable OUT_32K output buffer during POWERDOWN mode (auto re-enable when executing PD_DIS ID during power-up from NO-POWER mode) |
| CHG_BBAT_PD | [5] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Backup battery charger enabled during POWERDOWN mode |
| | | | | 0x1 | 1: Auto-disable backup battery charger during POWERDOWN |
| HS_2_WIRE_PD | [3] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: High speed interface (I2C_1) not disabled during POWERDOWN |
| | | | | 0x1 | 1: Auto-disable high speed interface during POWERDOWN |

System PMIC for Dual/Quad-Core Processors

| Field name | Bits | Type | POR | Description | |
|------------|------|-----------|-----|--------------|---|
| PM_IF_PD | [2] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Power manager interface (I2C_2) not disabled during POWERDOWN |
| | | | | 0x1 | 1: Auto-disable power manager interface during POWERDOWN |
| GP_ADC_PD | [1] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Allow configured ADC measurements during POWERDOWN |
| | | | | 0x1 | 1: Auto-disable auto and manual measurements |
| GPIO_PD | [0] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: GPIO extender enabled during POWERDOWN |
| | | | | 0x1 | 1: Auto-disable of features configured as GPIO pins during POWERDOWN mode (force the detection of a pending active state on GPIs by re-enabling the pin through a passive state of the related GPI status register) |

Table 84: Register INTERFACE

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x0010 | INTERFACE | 0x80 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|----------|----------|----------|----------|----------|
| IF_BASE_ADDR | | | Reserved | Reserved | Reserved | Reserved | Reserved |

| Field name | Bits | Type | POR | Description |
|--------------|-------|-----------|-----|--|
| IF_BASE_ADDR | [7:5] | RW OTP | 0x4 | 3 MSB of the I2C interfaces base address XXX10000 10010010 = 0x92 write address of HS (I2C) IF 10010011 = 0x93 read address of HS (I2C) IF |

Table 85: Register RESET

| Address | Name | POR value |
|---------|-------|-----------|
| 0x0011 | RESET | 0x45 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-------------|---|---|---|---|---|
| RESET_EVENT | | RESET_TIMER | | | | | |

| Field name | Bits | Type | POR | Description | |
|-------------|-------------------------------|-----------|-----|-------------------------|------------------------------|
| RESET_EVENT | [7:6] | RW OTP | 0x1 | RESET timer started by: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: EXT_WAKEUP |
| | | | | 0x1 (POR) | 01: SYS_UP |
| | | | | 0x2 | 10: PWR_UP (internal signal) |
| 0x3 | 11: PWR1_UP (internal signal) | | | | |

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| Field name | Bits | Type | POR | Description | |
|-------------|-----------------------|-----------|-----|----------------------|------------------------|
| RESET_TIMER | [5:0] | RW OTP | 0x5 | RESET timer duration | |
| | | | | Value | Description |
| | | | | 0x0 | 000000: RESET disabled |
| | | | | 0x1 | 000001: 1.024 msec |
| | | | | 0x2 | 000010: 2.048 msec |
| | | | | 0x3 | 000011: 3.072 msec |
| | | | | 0x4 | 000100: 4.096 msec |
| | | | | 0x5 (POR) | 000101: 5.120 msec |
| | | | | ... | |
| | | | | 0x1E | 011110: 30.720 msec |
| | | | | 0x1F | 011111: 31.744 msec |
| | | | | 0x20 | 100000: 32.768 msec |
| | | | | 0x21 | 100001: 65.536 msec |
| | | | | 0x22 | 100010: 98.304 msec |
| | | | | ... | |
| | | | | 0x3D | 111101: 983.040 msec |
| 0x3E | 111110: 1015.808 msec | | | | |
| 0x3F | 111111: 1048.576 msec | | | | |

System PMIC for Dual/Quad-Core Processors

A.2 GPIO

Table 86: Register Reserved

| Address | Name | POR value | | | | | |
|---------|----------|-----------|--|--|--|--|--|
| 0x0012 | Reserved | 0xEE | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| Reserved 1 | Reserved 1 | Reserved 1 | Reserved 0 | Reserved 1 | Reserved 1 | Reserved 1 | Reserved 0 |

Table 87: Register GPIO_TA

| Address | Name | POR value | | | | | |
|---------|---------|-----------|--|--|--|--|--|
| 0x0013 | GPIO_TA | 0xDE | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---------|--------|---|------------|------------|------------|------------|
| TA_MODE | TA_TYPE | TA_PIN | | Reserved 1 | Reserved 1 | Reserved 1 | Reserved 0 |

| Field name | Bits | Type | POR | Description | |
|------------|-------|-----------|-----|---|-----------------------------|
| TA_MODE | [7] | RW OTP | 0x1 | TA monitor: input/output configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 0: TA monitor: debounce off |
| | | | | 0x1 (POR) | 1: TA monitor: debounce on |
| TA_TYPE | [6] | RW OTP | 0x1 | TA monitor: input/output configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 0: TA monitor: active-low |
| | | | | 0x1 (POR) | 1: TA monitor: active-high |
| TA_PIN | [5:4] | RW OTP | 0x1 | TA monitor: PIN configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: N/A |
| | | | | 0x1 (POR) | 01: TA monitor |
| | | | | 0x2 | 10: N/A |
| | | | | 0x3 | 11: N/A |

System PMIC for Dual/Quad-Core Processors

Table 88: Register GPIO_nJIG_ON

| Address | Name | POR value |
|---------|--------------|-----------|
| 0x0014 | GPIO_nJIG_ON | 0xE9 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----------|----------|---|--------------|--------------|-------------|---|
| GPIO_MODE | GPIO_TYPE | GPIO_PIN | | nJIG_ON_MODE | nJIG_ON_TYPE | nJIG_ON_PIN | |

| Field name | Bits | Type | POR | Description | |
|--------------|------------------------|-----------|-----|--|---|
| GPIO_MODE | [7] | RW OTP | 0x1 | GPIO MODE configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 0: GPI: debounce off; GPO: output driven low |
| | | | | 0x1 (POR) | 1: GPI: debounce on; GPO: output driven high |
| GPIO_TYPE | [6] | RW OTP | 0x1 | GPIO TYPE configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 0: GPI:active-low ; GPO_OD: internal PUP to VDDIO |
| | | | | 0x1 (POR) | 1: GPI:active-high ; GPO_OD: external PUP |
| GPIO_PIN | [5:4] | RW OTP | 0x2 | GPIO PIN configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: nVDDFAULT |
| | | | | 0x1 | 01: GPI |
| | | | | 0x2 (POR) | 10: GPO_OD (open drain) |
| 0x3 | 11: GPO_PP (push-pull) | | | | |
| nJIG_ON_MODE | [3] | RW OTP | 0x1 | nJIG_ON monitor: Input/Output Configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 0: nJIG_ON monitor: debounce off |
| | | | | 0x1 (POR) | 1: nJIG_ON monitor: debounce on |
| nJIG_ON_TYPE | [2] | RW OTP | 0x0 | nJIG_ON monitor: input/output configured as: | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | 0: nJIG_ON monitor: active-low |
| | | | | 0x1 | 1: nJIG_ON monitor: active-high |
| nJIG_ON_PIN | [1:0] | RW OTP | 0x1 | nJIG_ON monitor: PIN configured as: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: N/A |
| | | | | 0x1 (POR) | 01: nJIG_ON monitor |
| | | | | 0x2 | 10: N/A |
| 0x3 | 11: N/A | | | | |

System PMIC for Dual/Quad-Core Processors

A.3 Sequencer

Table 89: Register ID_0_1

| Address | Name | POR value |
|---------|--------|-----------|
| 0x0015 | ID_0_1 | 0x11 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|----------------|---------|------------|-----------|
| LDO1_STEP | | | | WAIT_ID_ALWAYS | SYS_PRE | DEF_SUPPLY | nRES_MODE |

| Field name | Bits | Type | POR | Description | | | | | | |
|----------------|--|-----------|-----|--|-------|-------------|-----------|--|-----------|--|
| LDO1_STEP | [7:4] | RW OTP | 0x1 | Power sequencer time for LDO1 | | | | | | |
| WAIT_ID_ALWAYS | [3] | RW OTP | 0x0 | WAIT_ID Configuration: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Only perform the WAIT_ID step on first use of sequencer</td> </tr> <tr> <td>0x1</td> <td>1: Perform the WAIT_ID step on subsequent uses of sequencer.</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Only perform the WAIT_ID step on first use of sequencer | 0x1 | 1: Perform the WAIT_ID step on subsequent uses of sequencer. |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Only perform the WAIT_ID step on first use of sequencer | | | | | | | | | |
| 0x1 | 1: Perform the WAIT_ID step on subsequent uses of sequencer. | | | | | | | | | |
| SYS_PRE | [2] | RW OTP | 0x0 | <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Set SYS_UP as configured from supplies pre-settings</td> </tr> <tr> <td>0x1</td> <td>1: Always de-assert SYS_UP before powering down domain SYSTEM</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Set SYS_UP as configured from supplies pre-settings | 0x1 | 1: Always de-assert SYS_UP before powering down domain SYSTEM |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Set SYS_UP as configured from supplies pre-settings | | | | | | | | | |
| 0x1 | 1: Always de-assert SYS_UP before powering down domain SYSTEM | | | | | | | | | |
| DEF_SUPPLY | [1] | RW OTP | 0x0 | All supplies (except LDOCORE) are enabled/disabled from OTP Default mode <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>Disabled</td> </tr> <tr> <td>0x1</td> <td>Enabled</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | Disabled | 0x1 | Enabled |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | Disabled | | | | | | | | | |
| 0x1 | Enabled | | | | | | | | | |
| nRES_MODE | [0] | RW OTP | 0x1 | <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0</td> <td>0: No assertion of nRESET during POWERDOWN mode</td> </tr> <tr> <td>0x1 (POR)</td> <td>1: Assert nRESET when entering POWER DOWN mode (release after leaving POWERDOWN)</td> </tr> </tbody> </table> | Value | Description | 0x0 | 0: No assertion of nRESET during POWERDOWN mode | 0x1 (POR) | 1: Assert nRESET when entering POWER DOWN mode (release after leaving POWERDOWN) |
| Value | Description | | | | | | | | | |
| 0x0 | 0: No assertion of nRESET during POWERDOWN mode | | | | | | | | | |
| 0x1 (POR) | 1: Assert nRESET when entering POWER DOWN mode (release after leaving POWERDOWN) | | | | | | | | | |

System PMIC for Dual/Quad-Core Processors

Table 90: Register ID_2_3

| Address | Name | POR value | | | | | |
|------------|--------|-----------|-----|-------------------------------|---|---|---|
| 0x0016 | ID_2_3 | 0x03 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO3_STEP | | | | LDO2_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO3_STEP | [7:4] | RW OTP | 0x0 | Power sequencer time for LDO3 | | | |
| LDO2_STEP | [3:0] | RW OTP | 0x3 | Power sequencer time for LDO2 | | | |

Table 91: Register ID_4_5

| Address | Name | POR value | | | | | |
|------------|--------|-----------|-----|-------------------------------|---|---|---|
| 0x0017 | ID_4_5 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO5_STEP | | | | LDO4_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO5_STEP | [7:4] | RW OTP | 0x0 | Power sequencer time for LDO5 | | | |
| LDO4_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for LDO4 | | | |

Table 92: Register ID_6_7

| Address | Name | POR value | | | | | |
|------------|--------|-----------|-----|-------------------------------|---|---|---|
| 0x0018 | ID_6_7 | 0x50 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO7_STEP | | | | LDO6_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO7_STEP | [7:4] | RW OTP | 0x5 | Power sequencer time for LDO7 | | | |
| LDO6_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for LDO6 | | | |

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Table 93: Register ID_8_9

| Address | Name | POR value | | | | | |
|------------|--------|-----------|-----|-------------------------------|---|---|---|
| 0x0019 | ID_8_9 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO9_STEP | | | | LDO8_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO9_STEP | [7:4] | RW OTP | 0x0 | Power sequencer time for LDO9 | | | |
| LDO8_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for LDO8 | | | |

Table 94: Register ID_10_11

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----|--------------------------------|---|---|---|
| 0x001A | ID_10_11 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO11_STEP | | | | LDO10_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO11_STEP | [7:4] | RW OTP | 0x0 | Power sequencer time for LDO11 | | | |
| LDO10_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for LDO10 | | | |

Table 95: Register ID_12_13

| Address | Name | POR value | | | | | |
|-------------|----------|-----------|-----|--|---|---|---|
| 0x001B | ID_12_13 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PD_DIS_STEP | | | | LDO12_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| PD_DIS_STEP | [7:4] | RW OTP | 0x0 | Power sequencer time for power down disable (PD_DIS) | | | |
| LDO12_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for LDO12 | | | |

System PMIC for Dual/Quad-Core Processors

Table 96: Register ID_14_15

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----|--------------------------------|---|---|---|
| 0x001C | ID_14_15 | 0x35 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK3_STEP | | | | BUCK2_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK3_STEP | [7:4] | RW OTP | 0x3 | Power sequencer time for BUCK3 | | | |
| BUCK2_STEP | [3:0] | RW OTP | 0x5 | Power sequencer time for BUCK2 | | | |

Table 97: Register ID_16_17

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----|--------------------------------|---|---|---|
| 0x001D | ID_16_17 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK5_STEP | | | | BUCK4_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK5_STEP | [7:4] | RW OTP | 0x0 | Power sequencer time for BUCK5 | | | |
| BUCK4_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for BUCK4 | | | |

Table 98: Register ID_18_19

| Address | Name | POR value | | | | | |
|------------|------------|------------|------------|--|---|---|---|
| 0x001E | ID_18_19 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | BUCK1_STEP | | | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK1_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for dual phase buck (BUCK1) | | | |

System PMIC for Dual/Quad-Core Processors

Table 99: Register Reserved

| Address | Name | POR value | | | | | |
|---------|----------|-----------|--|--|--|--|--|
| 0x001F | Reserved | 0x00 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|------------|------------|------------|------------|------------|------------|------------|
| Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |

Table 100: Register SEQ_STATUS

| Address | Name | POR value | | | | | |
|---------|------------|-----------|--|--|--|--|--|
| 0x0020 | SEQ_STATUS | 0x00 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|-----------|---|---|---|
| SEQ_POINTER | | | | WAIT_STEP | | | |

| Field name | Bits | Type | POR | Description |
|-------------|-------|-----------|-----|--|
| SEQ_POINTER | [7:4] | RW | 0x0 | Actual pointer position (time slot) of power sequencer |
| WAIT_STEP | [3:0] | RW OTP | 0x0 | Power sequencer time for wait step |

Table 101: Register SEQ_A

| Address | Name | POR value | | | | | |
|---------|-------|-----------|--|--|--|--|--|
| 0x0021 | SEQ_A | 0x96 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|------------|---|---|---|
| POWER_END | | | | SYSTEM_END | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|--|
| POWER_END | [7:4] | RW OTP | 0x9 | OTP pointer - last supply of domain POWER |
| SYSTEM_END | [3:0] | RW OTP | 0x6 | OTP pointer - last supply of domain SYSTEM |

Table 102: Register SEQ_B

| Address | Name | POR value | | | | | |
|---------|-------|-----------|--|--|--|--|--|
| 0x0022 | SEQ_B | 0x49 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|-----------|---|---|---|
| PART_DOWN | | | | MAX_COUNT | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|--|
| PART_DOWN | [7:4] | RW OTP | 0x4 | OTP pointer - partial POWERDOWN mode |
| MAX_COUNT | [3:0] | RW OTP | 0x9 | OTP pointer - last supply of domain POWER1 |

System PMIC for Dual/Quad-Core Processors

Table 103: Register SEQ_TIMER

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x0023 | SEQ_TIMER | 0x3D |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|----------|---|---|---|
| SEQ_DUMMY | | | | SEQ_TIME | | | |

| Field name | Bits | Type | POR | Description | |
|------------|------------------|-----------|-----|-------------------------------|---------------------|
| SEQ_DUMMY | [7:4] | RW OTP | 0x3 | Time for empty sequence slots | |
| | | | | Value | Description |
| | | | | 0x0 | 0000: 32 μ sec |
| | | | | 0x1 | 0001: 64 μ sec |
| | | | | 0x2 | 0010: 96 μ sec |
| | | | | 0x3 (POR) | 0011: 128 μ sec |
| | | | | 0x4 | 0100: 160 μ sec |
| | | | | 0x5 | 0101: 192 μ sec |
| | | | | 0x6 | 0110: 224 μ sec |
| | | | | 0x7 | 0111: 256 μ sec |
| | | | | 0x8 | 1000: 288 μ sec |
| | | | | 0x9 | 1001: 384 μ sec |
| | | | | 0xA | 1010: 448 μ sec |
| | | | | 0xB | 1011: 512 μ sec |
| | | | | 0xC | 1100: 1.024 msec |
| | | | | 0xD | 1101: 2.048 msec |
| 0xE | 1110: 4.096 msec | | | | |
| 0xF | 1111: 8.192 msec | | | | |

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| Field name | Bits | Type | POR | Description | |
|------------|------------------|-----------|-----|---------------------------------------|---------------------|
| SEQ_TIME | [3:0] | RW OTP | 0xd | Time for each non-empty sequence slot | |
| | | | | Value | Description |
| | | | | 0x0 | 0000: 32 μ sec |
| | | | | 0x1 | 0001: 64 μ sec |
| | | | | 0x2 | 0010: 96 μ sec |
| | | | | 0x3 | 0011: 128 μ sec |
| | | | | 0x4 | 0100: 160 μ sec |
| | | | | 0x5 | 0101: 192 μ sec |
| | | | | 0x6 | 0110: 224 μ sec |
| | | | | 0x7 | 0111: 256 μ sec |
| | | | | 0x8 | 1000: 288 μ sec |
| | | | | 0x9 | 1001: 384 μ sec |
| | | | | 0xA | 1010: 448 μ sec |
| | | | | 0xB | 1011: 512 μ sec |
| | | | | 0xC | 1100: 1.024 msec |
| | | | | 0xD | 1101: 2.048 msec |
| 0xE | 1110: 4.096 msec | | | | |
| 0xF | 1111: 8.192 msec | | | | |

System PMIC for Dual/Quad-Core Processors

A.4 Supplies

Table 104: Register BUCK_A

| Address | Name | POR value | | | | | |
|---------|--------|-----------|--|--|--|--|--|
| 0x0024 | BUCK_A | 0x99 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|------------|---|------------|---|------------|---|
| BUCK3_ILIM | | BUCK3_MODE | | BUCK2_ILIM | | BUCK2_MODE | |

| Field name | Bits | Type | POR | Description | |
|------------|---|-----------|-----|-----------------------|----------------------------|
| BUCK3_ILIM | [7:6] | RW OTP | 0x2 | BUCK3 current limit: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: 840 mA |
| | | | | 0x1 | 01: 1080 mA |
| | | | | 0x2 (POR) | 10: 1440 mA |
| 0x3 | 11: 1800 mA | | | | |
| BUCK3_MODE | [5:4] | RW OTP | 0x1 | BUCK3 Operating Mode: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: Sleep mode (PFM) |
| | | | | 0x1 (POR) | 01: Automatic mode |
| | | | | 0x2 | 10: Synchronous mode (PWM) |
| 0x3 | 11: Automatic forcing to synchronous mode | | | | |
| BUCK2_ILIM | [3:2] | RW OTP | 0x2 | BUCK2 Current Limit: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: 840 mA |
| | | | | 0x1 | 01: 1080 mA |
| | | | | 0x2 (POR) | 10: 1440 mA |
| 0x3 | 11: 1800 mA | | | | |
| BUCK2_MODE | [1:0] | RW OTP | 0x1 | BUCK2 operating mode: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: Sleep mode (PFM) |
| | | | | 0x1 (POR) | 01: Automatic mode |
| | | | | 0x2 | 10: Synchronous mode (PWM) |
| 0x3 | 11: Automatic forcing to Synchronous mode | | | | |

System PMIC for Dual/Quad-Core Processors

Table 105: Register BUCK_B

| Address | Name | POR value |
|---------|--------|-----------|
| 0x0025 | BUCK_B | 0x99 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|------------|---|------------|---|------------|---|
| BUCK5_ILIM | | BUCK5_MODE | | BUCK4_ILIM | | BUCK4_MODE | |

| Field name | Bits | Type | POR | Description | |
|------------|---|-----------|-----|-----------------------|----------------------------|
| BUCK5_ILIM | [7:6] | RW OTP | 0x2 | BUCK5 Current Limit: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: 700 mA |
| | | | | 0x1 | 01: 900 mA |
| | | | | 0x2 (POR) | 10: 1200 mA |
| 0x3 | 11: 1500 mA | | | | |
| BUCK5_MODE | [5:4] | RW OTP | 0x1 | BUCK5 Operating Mode: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: Sleep mode (PFM) |
| | | | | 0x1 (POR) | 01: Automatic mode |
| | | | | 0x2 | 10: Synchronous mode (PWM) |
| 0x3 | 11: Automatic forcing to Synchronous mode | | | | |
| BUCK4_ILIM | [3:2] | RW OTP | 0x2 | BUCK4 Current Limit: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: 700 mA |
| | | | | 0x1 | 01: 900 mA |
| | | | | 0x2 (POR) | 10: 1200 mA |
| 0x3 | 11: 1500 mA | | | | |
| BUCK4_MODE | [1:0] | RW OTP | 0x1 | BUCK4 Operating Mode: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: Sleep mode (PFM) |
| | | | | 0x1 (POR) | 01: Automatic mode |
| | | | | 0x2 | 10: Synchronous mode (PWM) |
| 0x3 | 11: Automatic forcing to Synchronous mode | | | | |

System PMIC for Dual/Quad-Core Processors

Table 106: Register BUCK_C

| Address | Name | POR value | | | | | |
|---------|--------|-----------|--|--|--|--|--|
| 0x0026 | BUCK_C | 0x09 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|-----------------|---|---|---|------------|---|
| Reserved | | BUCK1_SYNC_ILIM | | | | BUCK1_MODE | |

| Field name | Bits | Type | POR | Description | |
|-----------------|----------------|-----------|-----|-------------------------------------|----------------------------|
| BUCK1_SYNC_ILIM | [6:2] | RW OTP | 0x2 | BUCK1 sync current limit per phase: | |
| | | | | Value | Description |
| | | | | 0x0 | 00000: 80 mA |
| | | | | 0x1 | 00001: 160 mA |
| | | | | & | ... |
| | | | | 0x30 | 11110: 2240 mA |
| 0x31 | 11111: 2560 mA | | | | |
| BUCK1_MODE | [1:0] | RW OTP | 0x1 | BUCK1 operating mode: | |
| | | | | Value | Description |
| | | | | 0x0 | 00: Sleep mode (PFM) |
| | | | | 0x1 (POR) | 01: Automatic mode |
| | | | | 0x2 | 10: Synchronous mode (PWM) |
| 0x3 | 11: Reserved | | | | |

Table 107: Register BUCK_D

| Address | Name | POR value | | | | | |
|---------|--------|-----------|--|--|--|--|--|
| 0x0027 | BUCK_D | 0x42 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---|---|------------------|---|---|---|---|
| BUCK1_IAUTSLP | | | BUCK1_SLEEP_ILIM | | | | |

| Field name | Bits | Type | POR | Description | |
|---------------|----------------|-----------|-----|-----------------------------|--------------------|
| BUCK1_IAUTSLP | [7:5] | RW OTP | 0x2 | BUCK1 auto sleep threshold: | |
| | | | | Value | Description |
| | | | | 0x0 | 00000: 128 mA |
| | | | | 0x1 | 00001: 360 mA |
| | | | | & | ... |
| | | | | 0x30 | 11110: 896 mA |
| 0x31 | 11111: 1024 mA | | | | |

System PMIC for Dual/Quad-Core Processors

| Field name | Bits | Type | POR | Description | |
|------------------|----------------|-----------|-----|--------------------------------------|--------------------|
| BUCK1_SLEEP_ILIM | [4:0] | RW OTP | 0x2 | BUCK1 sleep current limit per phase: | |
| | | | | Value | Description |
| | | | | 0x0 | 00000: 80 mA |
| | | | | 0x1 | 00001: 160 mA |
| | | | | & | ... |
| | | | | 0x30 | 11110: 2240 mA |
| 0x31 | 11111: 2560 mA | | | | |

Table 108: Register BUCK1

| Address | Name | POR value |
|---------|-------|-----------|
| 0x0028 | BUCK1 | 0x50 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|---|---|---|---|---|---|
| BUCK1_EN | VBUCK_DP | | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|--------------------|-----------|------|--------------------------|--------------------|
| BUCK1_EN | [7] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: BUCK1 disabled |
| | | | | 0x1 | 1: BUCK1 enabled |
| VBUCK_DP | [6:0] | RW OTP | 0x50 | Buck Dual Phase voltage. | |
| | | | | Value | Description |
| | | | | 0x0 | 0000000: 600 mV |
| | | | | 0x1 | 0000001: 606.25 mV |
| | | | | 0x2 | 0000001: 612.5 mV |
| | | | | ... | ... |
| | | | | 0x3D | 1111101: 1.38125 V |
| | | | | 0x3E | 1111110: 1.3875 V |
| 0x3F | 1111111: 1.39375 V | | | | |

System PMIC for Dual/Quad-Core Processors

Table 109: Register BUCK2

| Address | Name | POR value |
|---------|-------|-----------|
| 0x0029 | BUCK2 | 0x34 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|----------|--------|---|---|---|---|---|
| BUCK2_CONF | BUCK2_EN | VBUCK2 | | | | | |

| Field name | Bits | Type | POR | Description |
|-------------------------|-------|-----------|------|---|
| BUCK2_CONF | [7] | RW OTP | 0x0 | Value Description |
| | | | | 0x0 (POR) 0: Normal mode: VBUCK2_GO ramps the buck voltage |
| | | | | 0x1 1: Sequencer supply voltage preset |
| BUCK2_EN | [6] | RW OTP | 0x0 | Value Description |
| | | | | 0x0 (POR) 0: BUCK2 disabled |
| | | | | 0x1 1: BUCK2 enabled |
| VBUCK2 | [5:0] | RW OTP | 0x34 | Buck 2 voltage. Settings below 0.725 automatically force the buck into PFM mode |
| | | | | Value Description |
| | | | | 0x0 000000: 0.500 V |
| | | | | 0x1 000001: 0.525 V |
| | | | | 0x2 000010: 0.550 V |
| | | | | |
| | | | | 0x7 000111: 0.675 V |
| | | | | 0x8 001000: 0.700 V |
| | | | | 0x9 001001: 0.725 V |
| | | | | |
| | | | | 0x1B 011011: 1.175 V |
| | | | | 0x1C 011100: 1.200 V (default) |
| | | | | 0x1D 011101: 1.225 V |
| | | | | |
| | | | | 0x3D 111101: 2.025 V |
| 0x3E 111110: 2.050 V | | | | |
| 0x3F 111111: 2.075 V | | | | |

System PMIC for Dual/Quad-Core Processors

Table 110: Register BUCK3

| Address | Name | POR value | | | | | |
|---------|-------|-----------|--|--|--|--|--|
| 0x002A | BUCK3 | 0x34 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|----------|--------|---|---|---|---|---|
| BUCK3_CONF | BUCK3_EN | VBUCK3 | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|-------|-----------|------|---|--|
| BUCK3_CONF | [7] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Normal mode: VBUCK3_GO ramps the buck voltage |
| | | | | 0x1 | 1: Sequencer supply voltage preset |
| BUCK3_EN | [6] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: BUCK3 disabled |
| | | | | 0x1 | 1: BUCK3 enabled |
| VBUCK3 | [5:0] | RW OTP | 0x34 | Buck 3 voltage. Settings below 0.725 automatically force the buck into PFM mode | |
| | | | | Value | Description |
| | | | | 0x0 | 000000: 0.500 V voltage settings as for buck 3 |
| | | | | ... | ... |
| | | | 0x3F | 111111: 2.075 V | |

Table 111: Register BUCK4

| Address | Name | POR value | | | | | |
|---------|-------|-----------|--|--|--|--|--|
| 0x002B | BUCK4 | 0x34 | | | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|----------|--------|---|---|---|---|---|
| BUCK4_CONF | BUCK4_EN | VBUCK4 | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|------|-----------|-----|--------------|--|
| BUCK4_CONF | [7] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Normal mode: VBUCK4_GO ramps the buck voltage |
| | | | | 0x1 | 1: Sequencer supply voltage preset |
| BUCK4_EN | [6] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: BUCK4 disabled |
| | | | | 0x1 | 1: BUCK4 enabled |

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| Field name | Bits | Type | POR | Description | |
|------------|-----------------|-----------|------|-----------------|---------------------------|
| VBUCK4 | [5:0] | RW OTP | 0x34 | Buck 4 Voltage. | |
| | | | | Value | Description |
| | | | | 0x0 | 000000: 0.500 V |
| | | | | 0x1 | 000001: 0.525 V |
| | | | | 0x2 | 000010: 0.550 V |
| | | | | ... | ... |
| | | | | 0x7 | 000111: 0.675 V |
| | | | | 0x8 | 001000: 0.700 V |
| | | | | 0x9 | 001001: 0.725 V |
| | | | | ... | ... |
| | | | | 0x1B | 011011: 1.175 V |
| | | | | 0x1C | 011100: 1.200 V (default) |
| | | | | 0x1D | 011101: 1.225 V |
| | | | | ... | ... |
| | | | | 0x3D | 111101: 2.025 V |
| | | | | 0x3E | 111110: 2.050 V |
| 0x3F | 111111: 2.075 V | | | | |

Table 112: Register BUCK5

| Address | Name | POR value |
|---------|-------|-----------|
| 0x002C | BUCK5 | 0x34 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|----------|--------|---|---|---|---|---|
| BUCK5_CONF | BUCK5_EN | VBUCK5 | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|------|-----------|-----|--------------|--|
| BUCK5_CONF | [7] | RW OTP | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Normal mode: VBUCK5_GO ramps the buck voltage |
| | | | | 0x1 | 1: Sequencer supply voltage preset |
| BUCK5_EN | [6] | RW OTP | 0x0 | Buck5 Enable | |

System PMIC for Dual/Quad-Core Processors

| Field name | Bits | Type | POR | Description | |
|------------|-----------------|-----------|------|-----------------|---------------------------|
| VBUCK5 | [5:0] | RW OTP | 0x34 | Buck 5 Voltage. | |
| | | | | Value | Description |
| | | | | 0x0 | 000000: 0.500 V |
| | | | | 0x1 | 000001: 0.525 V |
| | | | | 0x2 | 000010: 0.550 V |
| | | | | ... | ... |
| | | | | 0x7 | 000111: 0.675 V |
| | | | | 0x8 | 001000: 0.700 V [3] |
| | | | | 0x9 | 001001: 0.725 V |
| | | | | ... | ... |
| | | | | 0x1B | 011011: 1.175 V |
| | | | | 0x1C | 011100: 1.200 V (default) |
| | | | | 0x1D | 011101: 1.225 V |
| | | | | ... | ... |
| | | | | 0x3D | 111101: 2.025 V |
| | | | | 0x3E | 111110: 2.050 V |
| 0x3F | 111111: 2.075 V | | | | |

Table 113: Register BUCKRF_THR

| Address | Name | POR value |
|---------|------------|-----------|
| 0x002D | BUCKRF_THR | 0xC0 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|----------------|---|---|---|
| RFBUCK_SNC_THR | | | | RFBUCK_SLP_THR | | | |

| Field name | Bits | Type | POR | Description | |
|----------------|--------------|-----------|-----|--|--------------------|
| RFBUCK_SNC_THR | [7:4] | RW OTP | 0xc | Force sync(PWM) mode threhsold. The device is forced in the sync mode if Vcon is higher than this. | |
| | | | | Value | Description |
| | | | | 0x0 | 0000: 160 mV |
| | | | | 0x1 | 0001: 180 mV |
| | | | | & | . |
| | | | | 0x14 | 1110: 440 mV |
| 0x15 | 1111: 460 mV | | | | |

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| Field name | Bits | Type | POR | Description | | | | | | | | | | | | |
|----------------|--------------|-----------|-----|---|-------|-------------|-----------|--------------|-----|--------------|---|---|------|--------------|------|--------------|
| RFBUCK_SLP_THR | [3:0] | RW OTP | 0x0 | Force sleep mode threshold. The device is forced in the sleep mode if Vcon is lower than this. | | | | | | | | | | | | |
| | | | | <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0000: 160 mV</td> </tr> <tr> <td>0x1</td> <td>0001: 180 mV</td> </tr> <tr> <td>&</td> <td>.</td> </tr> <tr> <td>0x14</td> <td>1110: 440 mV</td> </tr> <tr> <td>0x15</td> <td>1111: 460 mV</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0000: 160 mV | 0x1 | 0001: 180 mV | & | . | 0x14 | 1110: 440 mV | 0x15 | 1111: 460 mV |
| Value | Description | | | | | | | | | | | | | | | |
| 0x0 (POR) | 0000: 160 mV | | | | | | | | | | | | | | | |
| 0x1 | 0001: 180 mV | | | | | | | | | | | | | | | |
| & | . | | | | | | | | | | | | | | | |
| 0x14 | 1110: 440 mV | | | | | | | | | | | | | | | |
| 0x15 | 1111: 460 mV | | | | | | | | | | | | | | | |

Table 114 Register BUCKRF_CONF

| Address | Name | POR value |
|---------|-------------|-----------|
| 0x002E | BUCKRF_CONF | 0x25 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----------|---------------|------------------|--------------------|---|--------------------|---|
| RFBUCK_EN | Reserved | RFBUCK_6M_SEL | RFBUCK_I_BYP_LMT | RFBUCK_I_N_LMT_SEL | | RFBUCK_I_P_LMT_SEL | |

| Field name | Bits | Type | POR | Description |
|--------------------|-------|-----------|-----|---|
| RFBUCK_EN | [7] | RW OTP | 0x0 | Host control of RF buck |
| RFBUCK_6M_SEL | [5] | RW OTP | 0x1 | 1:6 MHz, 0:3 MHz |
| RFBUCK_I_BYP_LMT | [4] | RW OTP | 0x0 | 0:1.0 A, 1:1.5 A |
| RFBUCK_I_N_LMT_SEL | [3:2] | RW OTP | 0x1 | Negative current limit selection (00:0.6 A, 01:1.1 A, 10:1.6 A, 11:2.1 A) |
| RFBUCK_I_P_LMT_SEL | [1:0] | RW OTP | 0x1 | Current limit selection (00:1 A, 01:1.5 0A, 10:2 A, 11:2.5 A) |

Table 115: Register LDO1

| Address | Name | POR value |
|---------|------|-----------|
| 0x002F | LDO1 | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---------|-------|---|---|---|---|---|
| LDO1_CONF | LDO1_EN | VLDO1 | | | | | |

| Field name | Bits | Type | POR | Description | | | | | | |
|------------|------------------------------------|-----------|-----|--|-------|-------------|-----------|------------------------------------|-----|--------------------------|
| LDO1_CONF | [7] | RW OTP | 0x0 | LDO configure bit | | | | | | |
| | | | | <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Immediate supply voltage change</td> </tr> <tr> <td>0x1</td> <td>1: Supply voltage preset</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Immediate supply voltage change | 0x1 | 1: Supply voltage preset |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Immediate supply voltage change | | | | | | | | | |
| 0x1 | 1: Supply voltage preset | | | | | | | | | |

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| Field name | Bits | Type | POR | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--------------|------------------|-----------|-----|---|-------|-------------|--------------|------------------|-----|-----------------|-----|----------------|-----|-----|-----|----------------|-----|----------------|-----|----------------|-----|-----|------|----------------|------|----------------|------|----------------|-----|-----|------|----------------|------|----------------|------|----------------|-----|----------------|
| LDO1_EN | [6] | RW OTP | 0x0 | LDO enable <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: LDO1 disabled</td> </tr> <tr> <td>0x1</td> <td>1: LDO1 enabled</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: LDO1 disabled | 0x1 | 1: LDO1 enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0 (POR) | 0: LDO1 disabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1 | 1: LDO1 enabled | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VLDO1 | [5:0] | RW OTP | 0x0 | LDO voltage select <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>000000: 1.00 V</td> </tr> <tr> <td>0x1</td> <td>000001: 1.05 V</td> </tr> <tr> <td>0x2</td> <td>000010: 1.10 V</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0xB</td> <td>001011: 1.55 V</td> </tr> <tr> <td>0xC</td> <td>001100: 1.60 V</td> </tr> <tr> <td>0xD</td> <td>001101: 1.65 V</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0x20</td> <td>100000: 2.60 V</td> </tr> <tr> <td>0x21</td> <td>100001: 2.65 V</td> </tr> <tr> <td>0x22</td> <td>100010: 2.70 V</td> </tr> <tr> <td>...</td> <td>...</td> </tr> <tr> <td>0x28</td> <td>101000: 3.00 V</td> </tr> <tr> <td>0x29</td> <td>101001: 3.05 V</td> </tr> <tr> <td>0x2A</td> <td>101010: 3.10 V</td> </tr> <tr> <td>...</td> <td>101010: 3.10 V</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 000000: 1.00 V | 0x1 | 000001: 1.05 V | 0x2 | 000010: 1.10 V | ... | ... | 0xB | 001011: 1.55 V | 0xC | 001100: 1.60 V | 0xD | 001101: 1.65 V | ... | ... | 0x20 | 100000: 2.60 V | 0x21 | 100001: 2.65 V | 0x22 | 100010: 2.70 V | ... | ... | 0x28 | 101000: 3.00 V | 0x29 | 101001: 3.05 V | 0x2A | 101010: 3.10 V | ... | 101010: 3.10 V |
| Value | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0 (POR) | 000000: 1.00 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x1 | 000001: 1.05 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x2 | 000010: 1.10 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | ... | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0xB | 001011: 1.55 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0xC | 001100: 1.60 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0xD | 001101: 1.65 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | ... | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x20 | 100000: 2.60 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x21 | 100001: 2.65 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x22 | 100010: 2.70 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | ... | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x28 | 101000: 3.00 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x29 | 101001: 3.05 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x2A | 101010: 3.10 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ... | 101010: 3.10 V | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Table 116: Register LDO2

| Address | Name | POR value |
|---------|------|-----------|
| 0x0030 | LDO2 | 0x20 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---------|-------|---|---|---|---|---|
| LDO2_CONF | LDO2_EN | VLDO2 | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|------|---|
| LDO2_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See Register: LDO1 [0x002F] for details |
| LDO2_EN | [6] | RW OTP | 0x0 | LDO Enable. See Register: LDO1 [0x002F] for details |
| VLDO2 | [5:0] | RW OTP | 0x20 | LDO voltage select. See Register: LDO1 [0x002F] for details |

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Table 117: Register LDO3

| Address | Name | POR value | | | | | |
|------------|----------------|-----------|----------|---------------------|------------------------------------|----------|----------|
| 0x0031 | LDO3 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO3_CONF | LDO3_EN | VLDO3 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO3_CONF | [7] | RW OTP | 0x0 | LDO configure bit | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | 0: Immediate supply voltage change | | |
| | | | | 0x1 | 1: Supply voltage preset | | |
| LDO3_EN | [6] | RW OTP | 0x0 | LDO enable | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | 0: LDO1 disabled | | |
| | | | | 0x1 | 1: LDO1 enabled | | |
| VLDO3 | [5:0] | RW OTP | 0x0 | LDO3 voltage select | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | 000000: 1.20 V | | |
| | | | | 0x1 | 000001: 1.25 V | | |
| | | | | 0x2 | 000010: 1.30 V | | |
| | | | | ... | ... | | |
| | | | | 0xB | 001011: 1.75 V | | |
| | | | | 0xC | 001100: 1.80 V | | |
| | | | | 0xD | 001101: 1.85 V | | |
| | | | | ... | ... | | |
| | | | | 0x20 | 100000: 2.80 V | | |
| | | | | 0x21 | 100001: 2.85 V | | |
| | | | | 0x22 | 100010: 2.90 V | | |
| | | | | ... | ... | | |
| | | | | 0x28 | 101000: 3.20 V | | |
| | | | | 0x29 | 101001: 3.25 V | | |
| 0x2A | 101010: 3.30 V | | | | | | |
| ... | 101010: 3.30 V | | | | | | |

System PMIC for Dual/Quad-Core Processors

Table 118: Register LDO4

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0032 | LDO4 | 0x0C | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO4_CONF | LDO4_EN | VLDO4 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO4_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details | | | |
| LDO4_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO4 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

Table 119: Register LDO5

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0033 | LDO5 | 0x0C | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO5_CONF | LDO5_EN | VLDO5 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO5_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details | | | |
| LDO5_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO5 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

Table 120: Register LDO6

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0034 | LDO6 | 0x0C | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO6_CONF | LDO6_EN | VLDO6 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO6_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details | | | |
| LDO6_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO6 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

System PMIC for Dual/Quad-Core Processors

Table 121: Register LDO7

| Address | Name | POR value | |
|---------|------|-----------|--|
| 0x0035 | LDO7 | 0x0C | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---------|-------|---|---|---|---|---|
| LDO7_CONF | LDO7_EN | VLDO7 | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|---|
| LDO7_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details |
| LDO7_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details |
| VLDO7 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details |

Table 122: Register LDO8

| Address | Name | POR value | |
|---------|------|-----------|--|
| 0x0036 | LDO8 | 0x0C | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---------|-------|---|---|---|---|---|
| LDO8_CONF | LDO8_EN | VLDO8 | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|---|
| LDO8_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details |
| LDO8_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details |
| VLDO8 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details |

Table 123: Register LDO9

| Address | Name | POR value | |
|---------|------|-----------|--|
| 0x0037 | LDO9 | 0x0C | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---------|-------|---|---|---|---|---|
| LDO9_CONF | LDO9_EN | VLDO9 | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|---|
| LDO9_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details |
| LDO9_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details |
| VLDO9 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details |

System PMIC for Dual/Quad-Core Processors

Table 124 Register LDO10

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0038 | LDO10 | 0x0C | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO10_CONF | LDO10_EN | VLDO10 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO10_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details | | | |
| LDO10_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO10 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

Table 125: Register LDO11

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0039 | LDO11 | 0x0C | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO11_CONF | LDO11_EN | VLDO11 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO11_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details | | | |
| LDO11_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO11 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

Table 126: Register LDO12

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x003A | LDO12 | 0x0C | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO12_CONF | LDO12_EN | VLDO12 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO12_CONF | [7] | RW OTP | 0x0 | LDO configure bit. See register: LDO3 [0x0031] for details | | | |
| LDO12_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO12 | [5:0] | RW OTP | 0xc | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

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Table 127: Register PULLDOWN_A

| Address | Name | POR value | Pull down disable |
|---------|------------|-----------|-------------------|
| 0x003B | PULLDOWN_A | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|--------------|--------------|--------------|--------------|
| LDO4_PD_DIS | LDO3_PD_DIS | LDO2_PD_DIS | LDO1_PD_DIS | BUCK5_PD_DIS | BUCK4_PD_DIS | BUCK3_PD_DIS | BUCK2_PD_DIS |

| Field name | Bits | Type | POR | Description | | | | | | |
|--------------|--------------------------------------|-----------|-----|---|-------|-------------|--------------|------------------------------|-----|--------------------------------------|
| LDO4_PD_DIS | [7] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO3_PD_DIS | [6] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO2_PD_DIS | [5] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO1_PD_DIS | [4] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| BUCK5_PD_DIS | [3] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| BUCK4_PD_DIS | [2] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| BUCK3_PD_DIS | [1] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| BUCK2_PD_DIS | [0] | RW OTP | 0x0 | Pull down disable <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Enable pull down resistor</td> </tr> <tr> <td>0x1</td> <td>1: No pull down resistor in off mode</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Enable pull down resistor | 0x1 | 1: No pull down resistor in off mode |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Enable pull down resistor | | | | | | | | | |
| 0x1 | 1: No pull down resistor in off mode | | | | | | | | | |

Table 128: Register PULLDOWN_B

| Address | Name | POR value | Pull down disable |
|---------|------------|-----------|-------------------|
| 0x003C | PULLDOWN_B | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|--------------|-------------|-------------|-------------|-------------|-------------|
| LDO12_PD_DIS | LDO11_PD_DIS | LDO10_PD_DIS | LDO9_PD_DIS | LDO8_PD_DIS | LDO7_PD_DIS | LDO6_PD_DIS | LDO5_PD_DIS |

| Field name | Bits | Type | POR | Description |
|--------------|------|-----------|-----|--------------------|
| LDO12_PD_DIS | [7] | RW OTP | 0x0 | Pull down disable. |
| LDO11_PD_DIS | [6] | RW OTP | 0x0 | Pull down disable. |
| LDO10_PD_DIS | [5] | RW OTP | 0x0 | Pull down disable. |
| LDO9_PD_DIS | [4] | RW OTP | 0x0 | Pull down disable. |

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| Field name | Bits | Type | POR | Description | | | | | | |
|--------------|--------------------------------------|-----------|-----|---|-------|-------------|--------------|------------------------------|-----|--------------------------------------|
| LDO8_PD_DIS | [3] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO7_PD_DIS | [2] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO6_PD_DIS | [1] | RW OTP | 0x0 | Pull down disable. See above for details | | | | | | |
| LDO5_PD_DIS | [0] | RW OTP | 0x0 | Pull down disable <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Enable pull down resistor</td> </tr> <tr> <td>0x1</td> <td>1: No pull down resistor in off mode</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Enable pull down resistor | 0x1 | 1: No pull down resistor in off mode |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Enable pull down resistor | | | | | | | | | |
| 0x1 | 1: No pull down resistor in off mode | | | | | | | | | |

Table 129: Register PULLDOWN_C

| Address | Name | POR value | Pull down disable |
|---------|------------|-----------|-------------------|
| 0x003D | PULLDOWN_C | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------|-------------------|--------------|--------------|--------------|--------------|--------------|
| Reserved | B2PH_PD_DIS | LDO_VRFANA_PD_DIS | LDO17_PD_DIS | LDO16_PD_DIS | LDO15_PD_DIS | LDO14_PD_DIS | LDO13_PD_DIS |

| Field name | Bits | Type | POR | Description | | | | | | |
|-------------------|--------------------------------------|-----------|-----|---|-------|-------------|--------------|------------------------------|-----|--------------------------------------|
| B2PH_PD_DIS | [6] | RW OTP | 0x0 | Pull down disable | | | | | | |
| LDO_VRFANA_PD_DIS | [5] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO17_PD_DIS | [4] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO16_PD_DIS | [3] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO15_PD_DIS | [2] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO14_PD_DIS | [1] | RW OTP | 0x0 | Pull down disable. | | | | | | |
| LDO13_PD_DIS | [0] | RW OTP | 0x0 | Pull down disable <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Enable pull down resistor</td> </tr> <tr> <td>0x1</td> <td>1: No pull down resistor in off mode</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Enable pull down resistor | 0x1 | 1: No pull down resistor in off mode |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Enable pull down resistor | | | | | | | | | |
| 0x1 | 1: No pull down resistor in off mode | | | | | | | | | |

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Table 130: Register PULLDOWN_D

| Address | Name | POR value | Pull down disable |
|---------|------------|-----------|-------------------|
| 0x003E | PULLDOWN_D | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|--------------|--------------|------------------|------------------|------------------|------------------|
| Reserve d | Reserve d | Reserve d | Reserve d | LDO22_PD_D IS | LDO21_PD_D IS | LDO20_PD_D IS | LDO19_PD_D IS |

| Field name | Bits | Type | POR | Description | |
|--------------|------|-----------|-----|--------------------|--------------------------------------|
| LDO22_PD_DIS | [3] | RW OTP | 0x0 | Pull down disable. | |
| LDO21_PD_DIS | [2] | RW OTP | 0x0 | Pull down disable. | |
| LDO20_PD_DIS | [1] | RW OTP | 0x0 | Pull down disable. | |
| LDO19_PD_DIS | [0] | RW OTP | 0x0 | Pull down disable | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | 0: Enable pull down resistor |
| | | | | 0x1 | 1: No pull down resistor in off mode |

Table 131: Register LDO13

| Address | Name | POR value | |
|---------|-------|-----------|--|
| 0x003F | LDO13 | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|--------|---|---|---|---|---|
| Reserved | LDO13_EN | VLDO13 | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|---|
| LDO13_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details |
| VLDO13 | [5:0] | RW OTP | 0x0 | LDO voltage select. See register: LDO3 [0x0031] for details |

Table 132: Register LDO14

| Address | Name | POR value | |
|---------|-------|-----------|--|
| 0x0040 | LDO14 | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|--------|---|---|---|---|---|
| Reserved | LDO14_EN | VLDO14 | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|---|
| LDO14_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details |
| VLDO14 | [5:0] | RW OTP | 0x0 | LDO voltage select. See register: LDO3 [0x0031] for details |

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Table 133: Register LDO15

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0041 | LDO15 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | LDO15_EN | VLDO15 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO15_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO15 | [5:0] | RW OTP | 0x0 | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

Table 134: Register LDO16

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0042 | LDO16 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | LDO16_EN | VLDO16 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO16_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO16 | [5:0] | RW OTP | 0x0 | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

Table 135: Register LDO17

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|----------|----------|----------|
| 0x0043 | LDO17 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | LDO17_EN | VLDO17 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO17_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO17 | [5:0] | RW OTP | 0x0 | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

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Table 136: Register LDO_VRFANA

| Address | Name | POR value | | | | | |
|---------------|---------------|-------------|------|---|---|---|---|
| 0x0044 | LDO_VRFANA | 0x14 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | LDO_VRFANA_EN | VLDO_VRFANA | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO_VRFANA_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO_VRFANA | [5:0] | RW OTP | 0x14 | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

Table 137: Register LDO_19

| Address | Name | POR value | | | | | |
|------------|----------|-----------|------|---|---|---|---|
| 0x0045 | LDO_19 | 0x14 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | LDO19_EN | VLDO19 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO19_EN | [6] | RW OTP | 0x0 | LDO Enable. See Register: LDO3 [0x0031] for details | | | |
| VLDO19 | [5:0] | RW OTP | 0x14 | LDO voltage select. See Register: LDO3 [0x0031] for details | | | |

Table 138: Register LDO_20

| Address | Name | POR value | | | | | |
|------------|----------|-----------|------|---|---|---|---|
| 0x0046 | LDO_20 | 0x14 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | LDO20_EN | VLDO20 | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| LDO20_EN | [6] | RW OTP | 0x0 | LDO enable. See register: LDO3 [0x0031] for details | | | |
| VLDO20 | [5:0] | RW OTP | 0x14 | LDO voltage select. See register: LDO3 [0x0031] for details | | | |

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Table 139: Register SUPPLY

| Address | Name | POR value |
|---------|--------|-----------|
| 0x0049 | SUPPLY | 0x10 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------|--------------|--------------|--------------|---------------|---------------|---------------|---------------|
| V_LOCK | Reserve d | Reserve d | BBCHG_E N | VBUCK5_G O | VBUCK4_G O | VBUCK3_G O | VBUCK2_G O |

| Field name | Bits | Type | POR | Description | |
|------------|------|------------------|-----|-------------------------------|---|
| V_LOCK | [7] | RW | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Allows writing new values into BUCK and LDO voltage registers |
| | | | | 0x1 | 1: Disables output voltage reprogramming from the host (enable/disable, DVC, power sequencing including deferred update still possible) |
| BBCHG_EN | [4] | RW VOL OTP | 0x1 | BackUp Battery Charger Enable | |
| | | | | Value | Description |
| | | | | 0x0 | 0: BBAT charger disabled |
| VBUCK5_GO | [3] | RW VOL | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Hold VBUCK5 at current setting. |
| | | | | 0x1 | 1: Ramp BUCK5 to configured voltage (While ramping - no write access to BUCK5 register. Buck forced in PWM. VBUCK5_GO is cleared when the target voltage is reached.) |
| VBUCK4_GO | [2] | RW VOL | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Hold VBUCK3 at current setting. |
| | | | | 0x1 | 1: Ramp BUCK4 to configured voltage (While ramping - no write access to BUCK4 register. Buck forced in PWM. VBUCK4_GO is cleared when the target voltage is reached.) |
| VBUCK3_GO | [1] | RW VOL | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Hold VBUCK3 at current setting. |
| | | | | 0x1 | 1: Ramp BUCK3 to configured voltage (While ramping - no write access to BUCK3 register. Buck forced in PWM. VBUCK3_GO is cleared when the target voltage is reached.) |
| VBUCK2_GO | [0] | RW VOL | 0x0 | Value | Description |
| | | | | 0x0 (POR) | 0: Hold VBUCK2 at current setting. |
| | | | | 0x1 | 1: Ramp BUCK2 to configured voltage (While ramping - no write access to BUCK2 register. Buck forced in PWM. VBUCK2_GO is cleared when the target voltage is reached.) |

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A.5 Mode Control

Table 140: Register LDO1_MCTL

| Address | Name | POR value | | | | | |
|------------|-----------|------------|----------|---|--------------------|------------|----------|
| 0x004A | LDO1_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO1_MCTL3 | | LDO1_MCTL2 | | LDO1_MCTL1 | | LDO1_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO1_MCTL3 | [7:6] | RW OTP | 0x1 | LDO1 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO1_MCTL2 | [5:4] | RW OTP | 0x1 | LDO1 mode when in M_CTL mode == 10. See Field: LDO1_MCTL3 (Reg: LDO1_MCTL [0x004A]) for details | | | |
| LDO1_MCTL1 | [3:2] | RW OTP | 0x1 | LDO1 mode when in M_CTL mode == 01. See Field: LDO1_MCTL3 (Reg: LDO1_MCTL [0x004A]) for details | | | |
| LDO1_MCTL0 | [1:0] | RW OTP | 0x1 | LDO1 mode when in M_CTL mode == 00. See Field: LDO1_MCTL3 (Reg: LDO1_MCTL [0x004A]) for details | | | |

Table 141: Register LDO2_MCTL

| Address | Name | POR value | | | | | |
|------------|-----------|------------|----------|---|--------------------|------------|----------|
| 0x004B | LDO2_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO2_MCTL3 | | LDO2_MCTL2 | | LDO2_MCTL1 | | LDO2_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO2_MCTL3 | [7:6] | RW OTP | 0x1 | LDO2 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO2_MCTL2 | [5:4] | RW OTP | 0x1 | LDO2 mode when in M_CTL mode == 10. See Field: LDO2_MCTL3 (Reg: LDO2_MCTL [0x004B]) for details | | | |
| LDO2_MCTL1 | [3:2] | RW OTP | 0x1 | LDO2 mode when in M_CTL mode == 01. See Field: LDO2_MCTL3 (Reg: LDO2_MCTL [0x004B]) for details | | | |
| LDO2_MCTL0 | [1:0] | RW OTP | 0x1 | LDO2 mode when in M_CTL mode == 00. See Field: LDO2_MCTL3 (Reg: LDO2_MCTL [0x004B]) for details | | | |

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Table 142: Register LDO3_MCTL

| Address | Name | POR value | | | | | |
|------------|-----------|------------|----------|---|--------------------|------------|----------|
| 0x004C | LDO3_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO3_MCTL3 | | LDO3_MCTL2 | | LDO3_MCTL1 | | LDO3_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO3_MCTL3 | [7:6] | RW OTP | 0x1 | LDO3 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO3_MCTL2 | [5:4] | RW OTP | 0x1 | LDO3 mode when in M_CTL mode == 10. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | | | |
| LDO3_MCTL1 | [3:2] | RW OTP | 0x1 | LDO3 mode when in M_CTL mode == 01. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | | | |
| LDO3_MCTL0 | [1:0] | RW OTP | 0x1 | LDO3 mode when in M_CTL mode == 00. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | | | |

Table 143: Register LDO4_MCTL

| Address | Name | POR value | | | | | |
|------------|-----------|------------|----------|---|--------------------|------------|----------|
| 0x004D | LDO4_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO4_MCTL3 | | LDO4_MCTL2 | | LDO4_MCTL1 | | LDO4_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO4_MCTL3 | [7:6] | RW OTP | 0x1 | LDO4 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO4_MCTL2 | [5:4] | RW OTP | 0x1 | LDO4 mode when in M_CTL mode == 10. See Field: LDO4_MCTL3 (Reg: LDO4_MCTL [0x004D]) for details | | | |
| LDO4_MCTL1 | [3:2] | RW OTP | 0x1 | LDO4 mode when in M_CTL mode == 01. See Field: LDO4_MCTL3 (Reg: LDO4_MCTL [0x004D]) for details | | | |
| LDO4_MCTL0 | [1:0] | RW OTP | 0x1 | LDO4 mode when in M_CTL mode == 00. See Field: LDO4_MCTL3 (Reg: LDO4_MCTL [0x004D]) for details | | | |

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Table 144: Register LDO5_MCTL

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x004E | LDO5_MCTL | 0x55 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|------------|---|------------|---|------------|---|
| LDO5_MCTL3 | | LDO5_MCTL2 | | LDO5_MCTL1 | | LDO5_MCTL0 | |

| Field name | Bits | Type | POR | Description | |
|------------|-------|-----------|-----|---|--------------------|
| LDO5_MCTL3 | [7:6] | RW OTP | 0x1 | LDO5 mode when in M_CTL mode == 11. | |
| | | | | Value | Description |
| | | | | 0x0 | Off |
| | | | | 0x1 (POR) | On |
| | | | | 0x2 | Sleep |
| | | | | 0x3 | n/a |
| LDO5_MCTL2 | [5:4] | RW OTP | 0x1 | LDO5 mode when in M_CTL mode == 10. See Field: LDO5_MCTL3 (Reg: LDO5_MCTL [0x004E]) for details | |
| LDO5_MCTL1 | [3:2] | RW OTP | 0x1 | LDO5 mode when in M_CTL mode == 01. See Field: LDO5_MCTL3 (Reg: LDO5_MCTL [0x004E]) for details | |
| LDO5_MCTL0 | [1:0] | RW OTP | 0x1 | LDO5 mode when in M_CTL mode == 00. See Field: LDO5_MCTL3 (Reg: LDO5_MCTL [0x004E]) for details | |

Table 145: Register LDO6_MCTL

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x004F | LDO6_MCTL | 0x55 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|------------|---|------------|---|------------|---|
| LDO6_MCTL3 | | LDO6_MCTL2 | | LDO6_MCTL1 | | LDO6_MCTL0 | |

| Field name | Bits | Type | POR | Description | |
|------------|-------|-----------|-----|---|--------------------|
| LDO6_MCTL3 | [7:6] | RW OTP | 0x1 | LDO6 mode when in M_CTL mode == 11. | |
| | | | | Value | Description |
| | | | | 0x0 | Off |
| | | | | 0x1 (POR) | On |
| | | | | 0x2 | Sleep |
| | | | | 0x3 | n/a |
| LDO6_MCTL2 | [5:4] | RW OTP | 0x1 | LDO6 mode when in M_CTL mode == 10. See Field: LDO6_MCTL3 (Reg: LDO6_MCTL [0x004F]) for details | |
| LDO6_MCTL1 | [3:2] | RW OTP | 0x1 | LDO6 mode when in M_CTL mode == 01. See Field: LDO6_MCTL3 (Reg: LDO6_MCTL [0x004F]) for details | |
| LDO6_MCTL0 | [1:0] | RW OTP | 0x1 | LDO6 mode when in M_CTL mode == 00. See Field: LDO6_MCTL3 (Reg: LDO6_MCTL [0x004F]) for details | |

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Table 146: Register LDO7_MCTL

| Address | Name | POR value | | | | | |
|------------|-----------|------------|----------|---|--------------------|------------|----------|
| 0x0050 | LDO7_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO7_MCTL3 | | LDO7_MCTL2 | | LDO7_MCTL1 | | LDO7_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO7_MCTL3 | [7:6] | RW OTP | 0x1 | LDO7 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO7_MCTL2 | [5:4] | RW OTP | 0x1 | LDO7 mode when in M_CTL mode == 10. See Field: LDO7_MCTL3 (Reg: LDO7_MCTL [0x0050]) for details | | | |
| LDO7_MCTL1 | [3:2] | RW OTP | 0x1 | LDO7 mode when in M_CTL mode == 01. See Field: LDO7_MCTL3 (Reg: LDO7_MCTL [0x0050]) for details | | | |
| LDO7_MCTL0 | [1:0] | RW OTP | 0x1 | LDO7 mode when in M_CTL mode == 00. See Field: LDO7_MCTL3 (Reg: LDO7_MCTL [0x0050]) for details | | | |

Table 147 Register LDO8_MCTL

| Address | Name | POR value | | | | | |
|------------|-----------|------------|----------|---|--------------------|------------|----------|
| 0x0051 | LDO8_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO8_MCTL3 | | LDO8_MCTL2 | | LDO8_MCTL1 | | LDO8_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO8_MCTL3 | [7:6] | RW OTP | 0x1 | LDO8 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO8_MCTL2 | [5:4] | RW OTP | 0x1 | LDO8 mode when in M_CTL mode == 10. See Field: LDO8_MCTL3 (Reg: LDO8_MCTL [0x0051]) for details | | | |
| LDO8_MCTL1 | [3:2] | RW OTP | 0x1 | LDO8 mode when in M_CTL mode == 01. See Field: LDO8_MCTL3 (Reg: LDO8_MCTL [0x0051]) for details | | | |
| LDO8_MCTL0 | [1:0] | RW OTP | 0x1 | LDO8 mode when in M_CTL mode == 00. See Field: LDO8_MCTL3 (Reg: LDO8_MCTL [0x0051]) for details | | | |

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Table 148: Register LDO9_MCTL

| Address | Name | POR value | | | | | |
|------------|-----------|------------|----------|---|--------------------|------------|----------|
| 0x0052 | LDO9_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO9_MCTL3 | | LDO9_MCTL2 | | LDO9_MCTL1 | | LDO9_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO9_MCTL3 | [7:6] | RW OTP | 0x1 | LDO9 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO9_MCTL2 | [5:4] | RW OTP | 0x1 | LDO9 mode when in M_CTL mode == 10. See Field: LDO9_MCTL3 (Reg: LDO9_MCTL [0x0052]) for details | | | |
| LDO9_MCTL1 | [3:2] | RW OTP | 0x1 | LDO9 mode when in M_CTL mode == 01. See Field: LDO9_MCTL3 (Reg: LDO9_MCTL [0x0052]) for details | | | |
| LDO9_MCTL0 | [1:0] | RW OTP | 0x1 | LDO9 mode when in M_CTL mode == 00. See Field: LDO9_MCTL3 (Reg: LDO9_MCTL [0x0052]) for details | | | |

Table 149: Register LDO10_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x0053 | LDO10_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO10_MCTL3 | | LDO10_MCTL2 | | LDO10_MCTL1 | | LDO10_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO10_MCTL3 | [7:6] | RW OTP | 0x1 | LDO10 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO10_MCTL2 | [5:4] | RW OTP | 0x1 | LDO10 mode when in M_CTL mode == 10. See Field: LDO10_MCTL3 (Reg: LDO10_MCTL [0x0053]) for details | | | |
| LDO10_MCTL1 | [3:2] | RW OTP | 0x1 | LDO10 mode when in M_CTL mode == 01. See Field: LDO10_MCTL3 (Reg: LDO10_MCTL [0x0053]) for details | | | |
| LDO10_MCTL0 | [1:0] | RW OTP | 0x1 | LDO10 mode when in M_CTL mode == 00. See Field: LDO10_MCTL3 (Reg: LDO10_MCTL [0x0053]) for details | | | |

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Table 150: Register LDO11_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x0054 | LDO11_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO11_MCTL3 | | LDO11_MCTL2 | | LDO11_MCTL1 | | LDO11_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO11_MCTL3 | [7:6] | RW OTP | 0x1 | LDO11 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO11_MCTL2 | [5:4] | RW OTP | 0x1 | LDO11 mode when in M_CTL mode == 10. See Field: LDO11_MCTL3 (Reg: LDO11_MCTL [0x0054]) for details | | | |
| LDO11_MCTL1 | [3:2] | RW OTP | 0x1 | LDO11 mode when in M_CTL mode == 01. See Field: LDO11_MCTL3 (Reg: LDO11_MCTL [0x0054]) for details | | | |
| LDO11_MCTL0 | [1:0] | RW OTP | 0x1 | LDO11 mode when in M_CTL mode == 00. See Field: LDO11_MCTL3 (Reg: LDO11_MCTL [0x0054]) for details | | | |

Table 151: Register LDO12_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x0055 | LDO12_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO12_MCTL3 | | LDO12_MCTL2 | | LDO12_MCTL1 | | LDO12_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO12_MCTL3 | [7:6] | RW OTP | 0x1 | LDO12 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep | | |
| 0x3 | n/a | | | | | | |
| LDO12_MCTL2 | [5:4] | RW OTP | 0x1 | LDO12 mode when in M_CTL mode == 10. See Field: LDO12_MCTL3 (Reg: LDO12_MCTL [0x0055]) for details | | | |
| LDO12_MCTL1 | [3:2] | RW OTP | 0x1 | LDO12 mode when in M_CTL mode == 01. See Field: LDO12_MCTL3 (Reg: LDO12_MCTL [0x0055]) for details | | | |
| LDO12_MCTL0 | [1:0] | RW OTP | 0x1 | LDO12 mode when in M_CTL mode == 00. See Field: LDO12_MCTL3 (Reg: LDO12_MCTL [0x0055]) for details | | | |

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Table 152: Register LDO13_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x0056 | LDO13_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO13_MCTL3 | | LDO13_MCTL2 | | LDO13_MCTL1 | | LDO13_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO13_MCTL3 | [7:6] | RW OTP | 0x0 | LDO13 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO13_MCTL2 | [5:4] | RW OTP | 0x0 | LDO13 mode when in M_CTL mode == 10. See Field: LDO13_MCTL3 (Reg: LDO13_MCTL [0x0056]) for details | | | |
| LDO13_MCTL1 | [3:2] | RW OTP | 0x0 | LDO13 mode when in M_CTL mode == 01. See Field: LDO13_MCTL3 (Reg: LDO13_MCTL [0x0056]) for details | | | |
| LDO13_MCTL0 | [1:0] | RW OTP | 0x0 | LDO13 mode when in M_CTL mode == 00. See Field: LDO13_MCTL3 (Reg: LDO13_MCTL [0x0056]) for details | | | |

Table 153: Register LDO14_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x0057 | LDO14_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO14_MCTL3 | | LDO14_MCTL2 | | LDO14_MCTL1 | | LDO14_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO14_MCTL3 | [7:6] | RW OTP | 0x0 | LDO14 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO14_MCTL2 | [5:4] | RW OTP | 0x0 | LDO14 mode when in M_CTL mode == 10. See Field: LDO14_MCTL3 (Reg: LDO14_MCTL [0x0057]) for details | | | |
| LDO14_MCTL1 | [3:2] | RW OTP | 0x0 | LDO14 mode when in M_CTL mode == 01. See Field: LDO14_MCTL3 (Reg: LDO14_MCTL [0x0057]) for details | | | |
| LDO14_MCTL0 | [1:0] | RW OTP | 0x0 | LDO14 mode when in M_CTL mode == 00. See Field: LDO14_MCTL3 (Reg: LDO14_MCTL [0x0057]) for details | | | |

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Table 154: Register LDO15_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x0058 | LDO15_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO15_MCTL3 | | LDO15_MCTL2 | | LDO15_MCTL1 | | LDO15_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO15_MCTL3 | [7:6] | RW OTP | 0x0 | LDO15 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO15_MCTL2 | [5:4] | RW OTP | 0x0 | LDO15 mode when in M_CTL mode == 10. See Field: LDO15_MCTL3 (Reg: LDO15_MCTL [0x0058]) for details | | | |
| LDO15_MCTL1 | [3:2] | RW OTP | 0x0 | LDO15 mode when in M_CTL mode == 01. See Field: LDO15_MCTL3 (Reg: LDO15_MCTL [0x0058]) for details | | | |
| LDO15_MCTL0 | [1:0] | RW OTP | 0x0 | LDO15 mode when in M_CTL mode == 00. See Field: LDO15_MCTL3 (Reg: LDO15_MCTL [0x0058]) for details | | | |

Table 155: Register LDO16_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x0059 | LDO16_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO16_MCTL3 | | LDO16_MCTL2 | | LDO16_MCTL1 | | LDO16_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO16_MCTL3 | [7:6] | RW OTP | 0x0 | LDO16 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO16_MCTL2 | [5:4] | RW OTP | 0x0 | LDO16 mode when in M_CTL mode == 10. See Field: LDO16_MCTL3 (Reg: LDO16_MCTL [0x0059]) for details | | | |
| LDO16_MCTL1 | [3:2] | RW OTP | 0x0 | LDO16 mode when in M_CTL mode == 01. See Field: LDO16_MCTL3 (Reg: LDO16_MCTL [0x0059]) for details | | | |
| LDO16_MCTL0 | [1:0] | RW OTP | 0x0 | LDO16 mode when in M_CTL mode == 00. See Field: LDO16_MCTL3 (Reg: LDO16_MCTL [0x0059]) for details | | | |

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Table 156: Register LDO17_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x005A | LDO17_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO17_MCTL3 | | LDO17_MCTL2 | | LDO17_MCTL1 | | LDO17_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO17_MCTL3 | [7:6] | RW OTP | 0x0 | LDO17 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO17_MCTL2 | [5:4] | RW OTP | 0x0 | LDO17 mode when in M_CTL mode == 10. See Field: LDO17_MCTL3 (Reg: LDO17_MCTL [0x005A]) for details | | | |
| LDO17_MCTL1 | [3:2] | RW OTP | 0x0 | LDO17 mode when in M_CTL mode == 01. See Field: LDO17_MCTL3 (Reg: LDO17_MCTL [0x005A]) for details | | | |
| LDO17_MCTL0 | [1:0] | RW OTP | 0x0 | LDO17 mode when in M_CTL mode == 00. See Field: LDO17_MCTL3 (Reg: LDO17_MCTL [0x005A]) for details | | | |

Table 157: Register LDO_VRFANA_MCTL

| Address | Name | POR value | | | | | |
|------------------|-----------------|------------------|----------|---|--------------------|------------------|----------|
| 0x005B | LDO_VRFANA_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO_VRFANA_MCTL3 | | LDO_VRFANA_MCTL2 | | LDO_VRFANA_MCTL1 | | LDO_VRFANA_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO_VRFANA_MCTL3 | [7:6] | RW OTP | 0x0 | LDO_VRFANA mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO_VRFANA_MCTL2 | [5:4] | RW OTP | 0x0 | LDO_VRFANA mode when in M_CTL mode == 10. See Unknown Register: LDOVRFANA_MCTL3 for details | | | |
| LDO_VRFANA_MCTL1 | [3:2] | RW OTP | 0x0 | LDO_VRFANA mode when in M_CTL mode == 01. See Unknown Register: LDOVRFANA_MCTL3 for details | | | |
| LDO_VRFANA_MCTL0 | [1:0] | RW OTP | 0x0 | LDO_VRFANA mode when in M_CTL mode == 00. See Unknown Register: LDOVRFANA_MCTL3 for details | | | |

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Table 158: Register LDO19_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x005C | LDO19_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO19_MCTL3 | | LDO19_MCTL2 | | LDO19_MCTL1 | | LDO19_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO19_MCTL3 | [7:6] | RW OTP | 0x0 | LDO19 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO19_MCTL2 | [5:4] | RW OTP | 0x0 | LDO19 mode when in M_CTL mode == 10. See Field: LDO19_MCTL3 (Reg: LDO19_MCTL [0x005C]) for details | | | |
| LDO19_MCTL1 | [3:2] | RW OTP | 0x0 | LDO19 mode when in M_CTL mode == 01. See Field: LDO19_MCTL3 (Reg: LDO19_MCTL [0x005C]) for details | | | |
| LDO19_MCTL0 | [1:0] | RW OTP | 0x0 | LDO19 mode when in M_CTL mode == 00. See Field: LDO19_MCTL3 (Reg: LDO19_MCTL [0x005C]) for details | | | |

Table 159: Register LDO20_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|--------------------|-------------|----------|
| 0x005D | LDO20_MCTL | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| LDO20_MCTL3 | | LDO20_MCTL2 | | LDO20_MCTL1 | | LDO20_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| LDO20_MCTL3 | [7:6] | RW OTP | 0x0 | LDO20 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | Off | | |
| | | | | 0x1 | On | | |
| | | | | 0x2 | Sleep | | |
| | | | | 0x3 | n/a | | |
| LDO20_MCTL2 | [5:4] | RW OTP | 0x0 | LDO20 mode when in M_CTL mode == 10. See Field: LDO20_MCTL3 (Reg: LDO20_MCTL [0x005D]) for details | | | |
| LDO20_MCTL1 | [3:2] | RW OTP | 0x0 | LDO20 mode when in M_CTL mode == 01. See Field: LDO20_MCTL3 (Reg: LDO20_MCTL [0x005D]) for details | | | |
| LDO20_MCTL0 | [1:0] | RW OTP | 0x0 | LDO20 mode when in M_CTL mode == 00. See Field: LDO20_MCTL3 (Reg: LDO20_MCTL [0x005D]) for details | | | |

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Table 160: Register LDO_AUD1_MCTL

| Address | Name | POR value |
|---------|---------------|-----------|
| 0x005E | LDO_AUD1_MCTL | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|----------------|---|----------------|---|----------------|---|
| LDO_AUD1_MCTL3 | | LDO_AUD1_MCTL2 | | LDO_AUD1_MCTL1 | | LDO_AUD1_MCTL0 | |

| Field name | Bits | Type | POR | Description | |
|----------------|-------|-----------|-----|--|--------------------|
| LDO_AUD1_MCTL3 | [7:6] | RW OTP | 0x0 | LDO_AUDIO 1 mode when in M_CTL mode == 11. | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | Off |
| | | | | 0x1 | On |
| | | | | 0x2 | Sleep |
| | | | | 0x3 | n/a |
| LDO_AUD1_MCTL2 | [5:4] | RW OTP | 0x0 | LDO_AUDIO 1 mode when in M_CTL mode == 10. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | |
| LDO_AUD1_MCTL1 | [3:2] | RW OTP | 0x0 | LDO_AUDIO 1 mode when in M_CTL mode == 01. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | |
| LDO_AUD1_MCTL0 | [1:0] | RW OTP | 0x0 | LDO_AUDIO 1 mode when in M_CTL mode == 00. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | |

Table 161: Register LDO_AUD2_MCTL

| Address | Name | POR value |
|---------|---------------|-----------|
| 0x005F | LDO_AUD2_MCTL | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|----------------|---|----------------|---|----------------|---|
| LDO_AUD2_MCTL3 | | LDO_AUD2_MCTL2 | | LDO_AUD2_MCTL1 | | LDO_AUD2_MCTL0 | |

| Field name | Bits | Type | POR | Description | |
|----------------|-------|-----------|-----|--|--------------------|
| LDO_AUD2_MCTL3 | [7:6] | RW OTP | 0x0 | LDO_AUDIO 2 mode when in M_CTL mode == 11. | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | Off |
| | | | | 0x1 | On |
| | | | | 0x2 | Sleep |
| | | | | 0x3 | n/a |
| LDO_AUD2_MCTL2 | [5:4] | RW OTP | 0x0 | LDO_AUDIO 2 mode when in M_CTL mode == 10. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | |
| LDO_AUD2_MCTL1 | [3:2] | RW OTP | 0x0 | LDO_AUDIO 2 mode when in M_CTL mode == 01. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | |
| LDO_AUD2_MCTL0 | [1:0] | RW OTP | 0x0 | LDO_AUDIO 2 mode when in M_CTL mode == 00. See Field: LDO3_MCTL3 (Reg: LDO3_MCTL [0x004C]) for details | |

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Table 162: Register BUCK1_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|------------------------|-------------|----------|
| 0x0060 | BUCK1_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK1_MCTL3 | | BUCK1_MCTL2 | | BUCK1_MCTL1 | | BUCK1_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK1_MCTL3 | [7:6] | RW OTP | 0x1 | BUCK1 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep (Force PFM mode) | | |
| 0x3 | n/a | | | | | | |
| BUCK1_MCTL2 | [5:4] | RW OTP | 0x1 | BUCK1 mode when in M_CTL mode == 10. See Unknown Register: BUCK1MCTL3 for details | | | |
| BUCK1_MCTL1 | [3:2] | RW OTP | 0x1 | BUCK1 mode when in M_CTL mode == 01. See Field: BUCK1_MCTL3 (Reg: BUCK1_MCTL [0x0060]) for details | | | |
| BUCK1_MCTL0 | [1:0] | RW OTP | 0x1 | BUCK1 mode when in M_CTL mode == 00. See Field: BUCK1_MCTL3 (Reg: BUCK1_MCTL [0x0060]) for details | | | |

Table 163: Register BUCK2_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|------------------------|-------------|----------|
| 0x0061 | BUCK2_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK2_MCTL3 | | BUCK2_MCTL2 | | BUCK2_MCTL1 | | BUCK2_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK2_MCTL3 | [7:6] | RW OTP | 0x1 | BUCK2 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep (Force PFM mode) | | |
| 0x3 | n/a | | | | | | |
| BUCK2_MCTL2 | [5:4] | RW OTP | 0x1 | BUCK2 mode when in M_CTL mode == 10. See Unknown Register: BUCK2MCTL3 for details | | | |
| BUCK2_MCTL1 | [3:2] | RW OTP | 0x1 | BUCK2 mode when in M_CTL mode == 01. See Field: BUCK2_MCTL3 (Reg: BUCK2_MCTL [0x0061]) for details | | | |
| BUCK2_MCTL0 | [1:0] | RW OTP | 0x1 | BUCK2 mode when in M_CTL mode == 00. See Field: BUCK2_MCTL3 (Reg: BUCK2_MCTL [0x0061]) for details | | | |

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Table 164: Register BUCK3_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|------------------------|-------------|----------|
| 0x0062 | BUCK3_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK3_MCTL3 | | BUCK3_MCTL2 | | BUCK3_MCTL1 | | BUCK3_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK3_MCTL3 | [7:6] | RW OTP | 0x1 | BUCK3 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep (Force PFM mode) | | |
| 0x3 | n/a | | | | | | |
| BUCK3_MCTL2 | [5:4] | RW OTP | 0x1 | BUCK3 mode when in M_CTL mode == 10. See Unknown Register: BUCK3MCTL3 for details | | | |
| BUCK3_MCTL1 | [3:2] | RW OTP | 0x1 | BUCK3 mode when in M_CTL mode == 01. See Field: BUCK3_MCTL3 (Reg: BUCK3_MCTL [0x0062]) for details | | | |
| BUCK3_MCTL0 | [1:0] | RW OTP | 0x1 | BUCK3 mode when in M_CTL mode == 00. See Field: BUCK3_MCTL3 (Reg: BUCK3_MCTL [0x0062]) for details | | | |

Table 165: Register BUCK4_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|------------------------|-------------|----------|
| 0x0063 | BUCK4_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK4_MCTL3 | | BUCK4_MCTL2 | | BUCK4_MCTL1 | | BUCK4_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK4_MCTL3 | [7:6] | RW OTP | 0x1 | BUCK4 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep (Force PFM mode) | | |
| 0x3 | n/a | | | | | | |
| BUCK4_MCTL2 | [5:4] | RW OTP | 0x1 | BUCK4 mode when in M_CTL mode == 10. See Unknown Register: BUCK4MCTL3 for details | | | |
| BUCK4_MCTL1 | [3:2] | RW OTP | 0x1 | BUCK4 mode when in M_CTL mode == 01. See Field: BUCK4_MCTL3 (Reg: BUCK4_MCTL [0x0063]) for details | | | |
| BUCK4_MCTL0 | [1:0] | RW OTP | 0x1 | BUCK4 mode when in M_CTL mode == 00. See Field: BUCK4_MCTL3 (Reg: BUCK4_MCTL [0x0063]) for details | | | |

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Table 166: Register BUCK5_MCTL

| Address | Name | POR value | | | | | |
|-------------|------------|-------------|----------|--|------------------------|-------------|----------|
| 0x0064 | BUCK5_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK5_MCTL3 | | BUCK5_MCTL2 | | BUCK5_MCTL1 | | BUCK5_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK5_MCTL3 | [7:6] | RW OTP | 0x1 | BUCK5 mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | Sleep (Force PFM mode) | | |
| 0x3 | n/a | | | | | | |
| BUCK5_MCTL2 | [5:4] | RW OTP | 0x1 | BUCK5 mode when in M_CTL mode == 10. See Unknown Register: BUCK5MCTL3 for details | | | |
| BUCK5_MCTL1 | [3:2] | RW OTP | 0x1 | BUCK5 mode when in M_CTL mode == 01. See Field: BUCK5_MCTL3 (Reg: BUCK5_MCTL [0x0064]) for details | | | |
| BUCK5_MCTL0 | [1:0] | RW OTP | 0x1 | BUCK5 mode when in M_CTL mode == 00. See Field: BUCK5_MCTL3 (Reg: BUCK5_MCTL [0x0064]) for details | | | |

Table 167: Register BUCK_RF_MCTL

| Address | Name | POR value | | | | | |
|---------------|--------------|---------------|----------|--|--------------------|---------------|----------|
| 0x0065 | BUCK_RF_MCTL | 0x55 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCK_RF_MCTL3 | | BUCK_RF_MCTL2 | | BUCK_RF_MCTL1 | | BUCK_RF_MCTL0 | |
| Field name | Bits | Type | POR | Description | | | |
| BUCK_RF_MCTL3 | [7:6] | RW OTP | 0x1 | BUCK_RF mode when in M_CTL mode == 11. | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | Off | | |
| | | | | 0x1 (POR) | On | | |
| | | | | 0x2 | n/a | | |
| 0x3 | n/a | | | | | | |
| BUCK_RF_MCTL2 | [5:4] | RW OTP | 0x1 | BUCK_RF mode when in M_CTL mode == 10. See Field: BUCK_RF_MCTL3 (Reg: BUCK_RF_MCTL [0x0065]) for details | | | |
| BUCK_RF_MCTL1 | [3:2] | RW OTP | 0x1 | BUCK_RF mode when in M_CTL mode == 01. See Field: BUCK_RF_MCTL3 (Reg: BUCK_RF_MCTL [0x0065]) for details | | | |
| BUCK_RF_MCTL0 | [1:0] | RW OTP | 0x1 | BUCK_RF mode when in M_CTL mode == 00. See Field: BUCK_RF_MCTL3 (Reg: BUCK_RF_MCTL [0x0065]) for details | | | |

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Table 168: Register GPADC_MCTL

| Address | Name | POR value |
|---------|------------|-----------|
| 0x0066 | GPADC_MCTL | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|-------------|---|-------------|---|-------------|---|
| GPADC_MCTL3 | | GPADC_MCTL2 | | GPADC_MCTL1 | | GPADC_MCTL0 | |

| Field name | Bits | Type | POR | Description | |
|-------------|-------|-----------|-----|--|--------------------------------------|
| GPADC_MCTL3 | [7:6] | RW OTP | 0x0 | GPADC mode when in M_CTL mode == 11. | |
| | | | | Value | Description |
| | | | | 0x0 (POR) | Off |
| | | | | 0x1 | On if already enabled |
| | | | | 0x2 | Sleep - 20ms mode if already enabled |
| 0x3 | n/a | | | | |
| GPADC_MCTL2 | [5:4] | RW OTP | 0x0 | GPADC mode when in M_CTL mode == 10. See Field: GPADC_MCTL3 (Reg: GPADC_MCTL [0x0066]) for details | |
| GPADC_MCTL1 | [3:2] | RW OTP | 0x0 | GPADC mode when in M_CTL mode == 01. See Field: GPADC_MCTL3 (Reg: GPADC_MCTL [0x0066]) for details | |
| GPADC_MCTL0 | [1:0] | RW OTP | 0x0 | GPADC mode when in M_CTL mode == 00. See Field: GPADC_MCTL3 (Reg: GPADC_MCTL [0x0066]) for details | |

Table 169: Register MISC_MCTL

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x0067 | MISC_MCTL | 0xFF |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|-------------------|-------------------|-------------------|----------------|----------------|----------------|----------------|
| DIG_CLK_M CTL3 | DIG_CLK_M CTL2 | DIG_CLK_M CTL1 | DIG_CLK_M CTL0 | BBAT_M CTL3 | BBAT_M CTL2 | BBAT_M CTL1 | BBAT_M CTL0 |

| Field name | Bits | Type | POR | Description |
|---------------|------|-----------|-----|--|
| DIG_CLK_MCTL3 | [7] | RW OTP | 0x1 | Disable Digital clock when in M_CTL mode == 11 |
| DIG_CLK_MCTL2 | [6] | RW OTP | 0x1 | Disable Digital clock when in M_CTL mode == 10 |
| DIG_CLK_MCTL1 | [5] | RW OTP | 0x1 | Disable Digital clock when in M_CTL mode == 01 |
| DIG_CLK_MCTL0 | [4] | RW OTP | 0x1 | Disable Digital clock when in M_CTL mode == 00 |
| BBAT_MCTL3 | [3] | RW OTP | 0x1 | BBAT enable when in M_CTL mode == 11 |
| BBAT_MCTL2 | [2] | RW OTP | 0x1 | BBAT enable when in M_CTL mode == 10 |
| BBAT_MCTL1 | [1] | RW OTP | 0x1 | BBAT enable when in M_CTL mode == 01 |
| BBAT_MCTL0 | [0] | RW OTP | 0x1 | BBAT enable when in M_CTL mode == 00 |

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Table 170: Register VBUCK1_MCTL_RET

| Address | Name | POR value | |
|---------|-----------------|-----------|--|
| 0x0068 | VBUCK1_MCTL_RET | 0x0C | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|------------|---|---|---|---|---|---|
| Reserved | VBUCK1_RET | | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|--|
| VBUCK1_RET | [6:0] | RW OTP | 0xc | Buck 1 retention (sleep) voltage. See VBuck1 for voltage mapping |

Table 171: Register VBUCK4_MCTL_RET

| Address | Name | POR value | |
|---------|-----------------|-----------|--|
| 0x0069 | VBUCK4_MCTL_RET | 0x0C | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|------------|---|---|---|---|---|
| Reserved | Reserved | VBUCK4_RET | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|-----------|-----|---|
| VBUCK4_RET | [5:0] | RW OTP | 0xc | Buck4 retention voltage. See VBuck4 for voltage mapping |

System PMIC for Dual/Quad-Core Processors

A.6 Control

Table 172: Register WAIT_CONT

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x006A | WAIT_CONT | 0x3B |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------|-----------|--------|------------|---|---|---|
| WAIT_DIR | RTC_CLOCK | WAIT_MODE | EN_32K | DELAY_TIME | | | |

| Field name | Bits | Type | POR | Description | |
|------------|------|-----------|-----|---|--|
| WAIT_DIR | [7] | RW OTP | 0x0 | Value Description | |
| | | | | 0x0 (POR) | 0: Wait during Power-Up Sequence |
| | | | | 0x1 | 1: Wait during Power-Up and Power-Down Sequence |
| RTC_CLOCK | [6] | RW OTP | 0x0 | Value Description | |
| | | | | 0x0 (POR) | 0: No Gating of RTC Calendar Clock |
| | | | | 0x1 | 1: Clock to RTC Counter is Gated until WAIT is Asserted (depends on WAIT_MODE) |
| WAIT_MODE | [5] | RW OTP | 0x1 | OUT32K and RTC internal clock enable mode | |
| | | | | Value Description | |
| | | | | 0x0 | 0: Wait for GPIO1 to be Active |
| EN_32K | [4] | RW OTP | 0x1 | Enable OUT_32K from power-up | |
| | | | | Value Description | |
| | | | | 0x0 | 0: Wait for out_32k_pd |
| | | | | 0x1 (POR) | 1: output 32K from OTP_load |

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| Field name | Bits | Type | POR | Description | |
|------------|--------------|-----------|-----|--|--------------------|
| DELAY_TIME | [3:0] | RW OTP | 0xb | OUT32K and RTC internal clock delay when in timer mode | |
| | | | | Value | Description |
| | | | | 0x0 | 0000: 0usec |
| | | | | 0x1 | 0001: 540us |
| | | | | 0x2 | 0010: 1.0msec |
| | | | | 0x3 | 0011: 2.0msec |
| | | | | 0x4 | 0100: 4.1msec |
| | | | | 0x5 | 0101: 8.2msec |
| | | | | 0x6 | 0110: 16.4msec |
| | | | | 0x7 | 0111: 32.8msec |
| | | | | 0x8 | 1000: 65.5msec |
| | | | | 0x9 | 1001: 131msec |
| | | | | 0xA | 1010: 262msec |
| | | | | 0xB | 1011: 524msec |
| | | | | 0xC | 1100: 1.0sec |
| | | | | 0xD | 1101: 2.1sec |
| 0xE | 1110: 4.2sec | | | | |
| 0xF | 1111: 8.4sec | | | | |

Table 173: Register ONKEY_CONT1

| Address | Name | POR value |
|---------|-------------|-----------|
| 0x006B | ONKEY_CONT1 | 0x19 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|------------|---|---|---|
| NONKEY_DEB | | | | PRESS_TIME | | | |

| Field name | Bits | Type | POR | Description | |
|------------|-------|-----------|-----|----------------------------|--------------------|
| NONKEY_DEB | [7:4] | RW OTP | 0x1 | nONKEY short debounce time | |
| | | | | Value | Description |
| | | | | 0x0 | None |
| | | | | 0x1 (POR) | 10ms |
| | | | | 0x2 | 20ms |
| | | | | ... | ... |
| | | | | 0xB | 110ms |
| | | | | 0xC | 120ms |
| | | | | 0xD | 240ms |
| | | | | 0xE | 360ms |
| 0xF | 480ms | | | | |

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| Field name | Bits | Type | POR | Description | |
|------------|--------|-----------|-----|-----------------------------|--------------------|
| PRESS_TIME | [3:0] | RW OTP | 0x9 | Long (shutdown) nONKEY time | |
| | | | | Value | Description |
| | | | | 0x0 | 3.0 s |
| | | | | 0x1 | 3.5 s |
| | | | | ... | ... |
| | | | | 0x8 | 7.0 s |
| | | | | 0x9 (POR) | 7.5 s |
| | | | | 0xA | 8.0 s |
| | | | | & | & |
| 0xF | 10.5 s | | | | |

Table 174: Register OUT2_32K_ONKEY_CONT

| Address | Name | POR value |
|---------|---------------------|-----------|
| 0x006C | OUT2_32K_ONKEY_CONT | 0x11 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---------------------|---|---|----------|--------------------|---|---|
| OUT2_32K_EN | NONKEY_HOLD_OFF_DEB | | | Reserved | NONKEY_HOLD_ON_DEB | | |

| Field name | Bits | Type | POR | Description | |
|---------------------|-------|-----------|-----|---|--------------------|
| OUT2_32K_EN | [7] | RW OTP | 0x0 | Enable for second 32kHz Output | |
| NONKEY_HOLD_OFF_DEB | [6:4] | RW OTP | 0x1 | nONKEY hold to request shutdown debounce time | |
| | | | | Value | Description |
| | | | | 0x0 | 0.5s |
| | | | | 0x1 (POR) | 1.0s |
| | | | | ... | ... |
| | | | | 0x5 | 3.0s |
| | | | | 0x6 | 3.5s |
| 0x7 | 4.0s | | | | |
| NONKEY_HOLD_ON_DEB | [2:0] | RW OTP | 0x1 | nONKEY hold on time (causes POC wakeup). Same enumeration as Field: NONKEY_HOLD_OFF_DEB (Reg: OUT2_32K_ONKEY_CONT [0x006C]) | |

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Table 175: Register POWER_CONT

| Address | Name | POR value | |
|---------|------------|-----------|--|
| 0x006D | POWER_CONT | 0x08 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------|-------------|------------|------------|------------------|------------|------------|----------|
| NJIG_MCTRL_WAKE_DIS | RTC_AUTO_EN | Reserved 0 | Reserved 0 | BBAT_ILIM_IGNORE | Reserved 0 | Reserved 0 | MCTRL_EN |

| Field name | Bits | Type | POR | Description | | | | | | |
|---------------------|---|-----------|-----|---|-------|-------------|-----------|--|-----|---|
| NJIG_MCTRL_WAKE_DIS | [7] | RW | 0x0 | Disable MCTL_wakeup by nJIG_ON when set to 1 | | | | | | |
| RTC_AUTO_EN | [6] | RW | 0x0 | Enter RTC mode when in POWER_DOWN | | | | | | |
| BBAT_ILIM_IGNORE | [3] | RW OTP | 0x1 | When this bit is set active (1) it allows the backup battery charger to be ON even when the current limit is reached. | | | | | | |
| MCTRL_EN | [0] | RW OTP | 0x0 | Enable the use of M_CTL pins (only in Active) <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Mode Control pins MCTRL[1:0] Disabled</td> </tr> <tr> <td>0x1</td> <td>1: Mode Control pins MCTRL[1:0] Enabled in ACTIVE state</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Mode Control pins MCTRL[1:0] Disabled | 0x1 | 1: Mode Control pins MCTRL[1:0] Enabled in ACTIVE state |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Mode Control pins MCTRL[1:0] Disabled | | | | | | | | | |
| 0x1 | 1: Mode Control pins MCTRL[1:0] Enabled in ACTIVE state | | | | | | | | | |

Table 176: Register VDDFAULT

| Address | Name | POR value | |
|---------|----------|-----------|--|
| 0x006E | VDDFAULT | 0x2B | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|---------------|---|---|---|--------------|---|
| Reserved | Reserved | vdd_fault_adj | | | | vdd_hyst_adj | |

| Field name | Bits | Type | POR | Description |
|---------------|-------|-----------|-----|--|
| vdd_fault_adj | [5:2] | RW OTP | 0xa | Modifies the threshold voltage for VDD, default setting of 1010 gives value if 2.90v. |
| vdd_hyst_adj | [1:0] | RW OTP | 0x3 | Modifies the hysteresis in the comparator. The default value of 11 sets an upper voltage limit of 3.222V |

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Table 177: Register BBAT_CONT

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x006F | BBAT_CONT | 0xFF |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---|---|---|---------------|---|---|---|
| BCHARGER_ISET | | | | BCHARGER_VSET | | | |

| Field name | Bits | Type | POR | Description | |
|---------------|-----------|-----------|-----|--------------------------------|--------------------|
| BCHARGER_ISET | [7:4] | RW OTP | 0xf | Backup battery charger current | |
| | | | | Value | Description |
| | | | | 0x0 | 0000: 0 uA |
| | | | | 0x1 | 0001: 100uA |
| | | | | 0x2 | 0010: 200uA |
| | | | | 0x3 | 0011: 300uA |
| | | | | 0x4 | 0100: 400uA |
| | | | | 0x5 | 0101: 500uA |
| | | | | 0x6 | 0110: 600uA |
| | | | | 0x7 | 0111: 700uA |
| | | | | 0x8 | 1000: 800uA |
| | | | | 0x9 | 1001: 900uA |
| | | | | 0xA | 1010: 1mA |
| | | | | 0xB | 1011: 2mA |
| | | | | 0xC | 1100: 3mA |
| | | | | 0xD | 1101: 4mA |
| 0xE | 1110: 5mA | | | | |
| 0xF | 1111: 6mA | | | | |

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| Field name | Bits | Type | POR | Description | |
|---------------|------------|-----------|-----|--------------------------------|--------------------|
| BCHARGER_VSET | [3:0] | RW OTP | 0xf | Backup battery charger voltage | |
| | | | | Value | Description |
| | | | | 0x0 | 0000: 1.8V |
| | | | | 0x1 | 0001: 1.9V |
| | | | | 0x2 | 0010: 2.0V |
| | | | | 0x3 | 0011: 2.1V |
| | | | | 0x4 | 0100: 2.2V |
| | | | | 0x5 | 0101: 2.3V |
| | | | | 0x6 | 0110: 2.4V |
| | | | | 0x7 | 0111: 2.5V |
| | | | | 0x8 | 1000: 2.6V |
| | | | | 0x9 | 1001: 2.7V |
| | | | | 0xA | 1010: 2.8V |
| | | | | 0xB | 1011: 2.9V |
| | | | | 0xC | 1100: 3.0V |
| | | | | 0xD | 1101: 3.1V |
| 0xE | 1110: 3.2V | | | | |
| 0xF | 1111: 3.3V | | | | |

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A.7 ADC

Table 178: Register ADC_MAN

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|---|--|---|---|
| 0x0070 | ADC_MAN | 0x80 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ISRC_50U | Reserved | Reserved | MAN_CONV | MUX_SEL | | | |
| Field name | Bits | Type | POR | Description | | | |
| ISRC_50U | [7] | RW OTP | 0x1 | Use a 50uA current source for TBAT1 and TBAT2 rather than 10uA. | | | |
| MAN_CONV | [4] | RW VOL | 0x0 | Perform Manual Conversion. (reset to 0 when conversion is complete) | | | |
| MUX_SEL | [3:0] | RW OTP | 0x0 | ADC multiplexer channel select for manual conversions | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | 0000: VBAT_S pin (Channel A0) Selected | | |
| | | | | 0x2 | 0010: TEMP1 pin (Channel A1) Selected | | |
| | | | | 0x4 | 0100: VF pin (Channel A3) Selected | | |
| | | | | 0x5 | 0101: ADCIN pin (Channel A4) Selected | | |
| | | | | 0x6 | 0110: TEMP2 pin (Channel A2) Selected | | |
| | | | | 0x8 | 1000: internal TJUNC (Channel A6) Selected | | |

Table 179: Register ADC_CONT

| Address | Name | POR value | | | | | |
|---------------|----------|---------------|------------|------------------------------------|---|------------|--------------|
| 0x0071 | ADC_CONT | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_AUTO_EN | ADC_MODE | TEMP1_ISRC_EN | VF_ISRC_EN | TEMP2_ISRC_EN | AUTO_AIN_EN | AUTO_VF_EN | AUTO_VBAT_EN |
| Field name | Bits | Type | POR | Description | | | |
| ADC_AUTO_EN | [7] | RW OTP | 0x0 | ADC Auto Measurements Enabled | | | |
| ADC_MODE | [6] | RW OTP | 0x0 | Value | Description | | |
| | | | | 0x0 (POR) | 0: Measurement Sequence Interval 20ms (economy mode) | | |
| | | | | 0x1 | 1: Measurement Sequence Interval 2ms | | |
| TEMP1_ISRC_EN | [5] | RW OTP | 0x0 | TEMP1 50uA Current Source Enabled: | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | 0: Enabled One Slot Before Measurement (disabled after measurement) | | |
| | | | | 0x1 | 1: Permanently Enabled | | |

System PMIC for Dual/Quad-Core Processors

| Field name | Bits | Type | POR | Description | | | | | | |
|---------------|---|-----------|-----|---|-------|-------------|--------------|---|-----|---|
| VF_ISRC_EN | [4] | RW OTP | 0x0 | VF 50uA Current Source Enabled: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0:Disabled</td> </tr> <tr> <td>0x1</td> <td>1: Permanently Enabled in Manual mode. Dynamic in Auto mode</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0:Disabled | 0x1 | 1: Permanently Enabled in Manual mode. Dynamic in Auto mode |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0:Disabled | | | | | | | | | |
| 0x1 | 1: Permanently Enabled in Manual mode. Dynamic in Auto mode | | | | | | | | | |
| TEMP2_ISRC_EN | [3] | RW OTP | 0x0 | TEMP2 50uA Current Source Enabled: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Enabled One Slot Before Measurement (disabled after measurement)</td> </tr> <tr> <td>0x1</td> <td>1: Permanently Enabled</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Enabled One Slot Before Measurement (disabled after measurement) | 0x1 | 1: Permanently Enabled |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Enabled One Slot Before Measurement (disabled after measurement) | | | | | | | | | |
| 0x1 | 1: Permanently Enabled | | | | | | | | | |
| AUTO_AIN_EN | [2] | RW OTP | 0x0 | ADCIN Auto Measurements Enabled | | | | | | |
| AUTO_VF_EN | [1] | RW OTP | 0x0 | VF Auto Measurements Enabled | | | | | | |
| AUTO_VBAT_EN | [0] | RW OTP | 0x0 | VDDOUT Auto Measurements Enabled | | | | | | |

Table 180: Register ADC_CONT2

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x0072 | ADC_CONT2 | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|----------|----------|-------------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | AD5_ISRC_EN |

| Field name | Bits | Type | POR | Description | | | | | | |
|--------------|---|-----------|-----|---|-------|-------------|--------------|------------|-----|---|
| AD5_ISRC_EN | [0] | RW OTP | 0x0 | ADCIN 50uA Current Source Enabled: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0:Disabled</td> </tr> <tr> <td>0x1</td> <td>1: Permanently Enabled in Manual mode. Dynamic in Auto mode</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0:Disabled | 0x1 | 1: Permanently Enabled in Manual mode. Dynamic in Auto mode |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0:Disabled | | | | | | | | | |
| 0x1 | 1: Permanently Enabled in Manual mode. Dynamic in Auto mode | | | | | | | | | |

Table 181: Register ADC_RES_L

| Address | Name | POR value |
|---------|-----------|-----------|
| 0x0073 | ADC_RES_L | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|----------|----------|-------------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | ADC_RES_LSB |

| Field name | Bits | Type | POR | Description |
|-------------|-------|------|-----|--|
| ADC_RES_LSB | [3:0] | RO | 0x0 | 12 Bit Manual Conversion Result (4 LSBs) |

System PMIC for Dual/Quad-Core Processors

Table 182: Register ADC_RES_H

| Address | Name | POR value | | | | | |
|-------------|-----------|-----------|-----|--|---|---|---|
| 0x0074 | ADC_RES_H | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ADC_RES_MSB | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| ADC_RES_MSB | [7:0] | RO | 0x0 | 12 Bit Manual Conversion Result (8 MSBs) | | | |

Table 183: Register VBAT_RES

| Address | Name | POR value | | | | | |
|--------------|----------|-----------|-----|--|---|---|---|
| 0x0075 | VBAT_RES | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBAT_RES_MSB | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| VBAT_RES_MSB | [7:0] | RO | 0x0 | Auto VBAT_S Conversion Result (8 MSBs) 00000000 corresponds to 2.5V 11111111 corresponds to 4.5V | | | |

Table 184: Register VDDOUT_MON

| Address | Name | POR value | | | | | |
|------------|------------|-----------|-----|---------------------------|---|---|---|
| 0x0076 | VDDOUT_MON | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VDDOUT_MON | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| VDDOUT_MON | [7:0] | RW OTP | 0x0 | Battery Monitor threshold | | | |

Table 185: Register TEMP1_RES

| Address | Name | POR value | | | | | |
|------------|-----------|-----------|-----|--|---|---|---|
| 0x0077 | TEMP1_RES | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBAT1_RES | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TBAT1_RES | [7:0] | RO | 0x0 | Auto TEMP1 Conversion Result (8 MSBs) 00000000 - 11111111 | | | |

System PMIC for Dual/Quad-Core Processors

Table 186: Register TEMP1_HIGHP

| Address | Name | POR value | | | | | |
|-------------|-------------|-----------|-----|----------------------|---|---|---|
| 0x0078 | TEMP1_HIGHP | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMP1_HIGHP | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TEMP1_HIGHP | [7:0] | RW OTP | 0x0 | TEMP1 High threshold | | | |

Table 187: Register TEMP1_HIGHN

| Address | Name | POR value | | | | | |
|-------------|-------------|-----------|-----|----------------------|---|---|---|
| 0x0079 | TEMP1_HIGHN | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMP1_HIGHN | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TEMP1_HIGHN | [7:0] | RW OTP | 0x0 | TEMP1 High threshold | | | |

Table 188: Register TEMP1_LOW

| Address | Name | POR value | | | | | |
|------------|-----------|-----------|------|---------------------|---|---|---|
| 0x007A | TEMP1_LOW | 0xFF | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMP1_LOW | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TEMP1_LOW | [7:0] | RW OTP | 0xff | TEMP1 Low threshold | | | |

Table 189: Register T_OFFSET

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----|--|---|---|---|
| 0x007B | T_OFFSET | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| T_OFFSET | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| T_OFFSET | [7:0] | RW OTP | 0x0 | Offset Calibration TJUNC measurement 10000000 - 01111111 (signed 2's compliment) | | | |

System PMIC for Dual/Quad-Core Processors

Table 190: Register VF_RES

| Address | Name | POR value | | | | | |
|------------|--------|-----------|-----|---|---|---|---|
| 0x007C | VF_RES | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VF_RES_MSB | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| VF_RES_MSB | [7:0] | RO | 0x0 | Auto VF Conversion Result (8 MSBs) 00000000 - 11111111 | | | |

Table 191: Register VF_HIGH

| Address | Name | POR value | | | | | |
|------------|---------|-----------|------|-------------------|---|---|---|
| 0x007D | VF_HIGH | 0xFF | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VF_HIGH | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| VF_HIGH | [7:0] | RW OTP | 0xff | VF High threshold | | | |

Table 192: Register VF_LOW

| Address | Name | POR value | | | | | |
|------------|--------|-----------|-----|------------------|---|---|---|
| 0x007E | VF_LOW | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VF_LOW | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| VF_LOW | [7:0] | RW OTP | 0x0 | VF Low threshold | | | |

Table 193: Register AIN_RES

| Address | Name | POR value | | | | | |
|-------------|---------|-----------|-----|--|---|---|---|
| 0x007F | AIN_RES | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AIN_RES_MSB | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| AIN_RES_MSB | [7:0] | RO | 0x0 | Auto ADCIN Conversion Result (8 MSBs) 00000000 - 11111111 | | | |

System PMIC for Dual/Quad-Core Processors

Table 194: Register TEMP2_RES

| Address | Name | POR value | | | | | |
|------------|-----------|-----------|-----|--|---|---|---|
| 0x0082 | TEMP2_RES | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TBAT2_RES | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TBAT2_RES | [7:0] | RO | 0x0 | Auto TEMP2 Conversion Result (8 MSBs) 00000000 - 11111111 | | | |

Table 195: Register TEMP2_HIGHP

| Address | Name | POR value | | | | | |
|-------------|-------------|-----------|-----|----------------------|---|---|---|
| 0x0083 | TEMP2_HIGHP | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMP2_HIGHP | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TEMP2_HIGHP | [7:0] | RW OTP | 0x0 | TEMP2 High threshold | | | |

Table 196: Register TEMP2_HIGHN

| Address | Name | POR value | | | | | |
|-------------|-------------|-----------|-----|----------------------|---|---|---|
| 0x0084 | TEMP2_HIGHN | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMP2_HIGHN | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TEMP2_HIGHN | [7:0] | RW OTP | 0x0 | TEMP2 High threshold | | | |

Table 197: Register TEMP2_LOW

| Address | Name | POR value | | | | | |
|------------|-----------|-----------|------|---------------------|---|---|---|
| 0x0085 | TEMP2_LOW | 0xFF | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMP2_LOW | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TEMP2_LOW | [7:0] | RW OTP | 0xff | TEMP2 Low threshold | | | |

System PMIC for Dual/Quad-Core Processors

Table 198: Register TJUNC_RES

| Address | Name | POR value | | | | | |
|------------|-----------|-----------|-----|--|---|---|---|
| 0x0086 | TJUNC_RES | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TJUNC_RES | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TJUNC_RES | [7:0] | RO | 0x0 | Auto TJUNC Conversion Result (8 MSBs) 00000000 - 11111111 | | | |

Table 199: Register ADC_RES_AUTO1

| Address | Name | POR value | | | | | |
|---------------|---------------|-----------|-----|-------------------------------|---|---|---|
| 0x0087 | ADC_RES_AUTO1 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TEMP1_RES_LSB | | | | VBAT_RES_LSB | | | |
| Field name | Bits | Type | POR | Description | | | |
| TEMP1_RES_LSB | [7:4] | RO | 0x0 | Auto TEMP1 Conversion Result | | | |
| VBAT_RES_LSB | [3:0] | RO | 0x0 | Auto VBAT_S Conversion Result | | | |

Table 200: Register ADC_RES_AUTO2

| Address | Name | POR value | | | | | |
|-------------|---------------|-----------|-----|------------------------------|---|---|---|
| 0x0088 | ADC_RES_AUTO2 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AIN_RES_LSB | | | | VF_RES_LSB | | | |
| Field name | Bits | Type | POR | Description | | | |
| AIN_RES_LSB | [7:4] | RO | 0x0 | Auto ADCIN Conversion Result | | | |
| VF_RES_LSB | [3:0] | RO | 0x0 | Auto VF Conversion Result | | | |

Table 201: Register ADC_RES_AUTO3

| Address | Name | POR value | | | | | |
|---------------|---------------|-----------|-----|------------------------------|---|---|---|
| 0x0089 | ADC_RES_AUTO3 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TJUNC_RES_LSB | | | | TEMP2_RES_LSB | | | |
| Field name | Bits | Type | POR | Description | | | |
| TJUNC_RES_LSB | [7:4] | RO | 0x0 | Auto TJUNC Conversion Result | | | |
| TEMP2_RES_LSB | [3:0] | RO | 0x0 | Auto TEMP2 Conversion Result | | | |

System PMIC for Dual/Quad-Core Processors

A.8 RTC

Table 202: Register COUNT_S

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----|---|---|---|---|
| 0x008A | COUNT_S | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | COUNT_SEC | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| COUNT_SEC | [5:0] | RW | 0x0 | 0x00 - 0x3B: RTC SECONDS. When read, latches data in COUNT_MIN - COUNT_YEAR | | | |

Table 203: Register COUNT_MI

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----|--------------------------|---|---|---|
| 0x008B | COUNT_MI | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | COUNT_MIN | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| COUNT_MIN | [5:0] | RW | 0x0 | 0x00 - 0x3B: RTC MINUTES | | | |

Table 204: Register COUNT_H

| Address | Name | POR value | | | | | |
|------------|----------|-----------|------------|------------------------|---|---|---|
| 0x008C | COUNT_H | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | COUNT_HOUR | | | | |
| Field name | Bits | Type | POR | Description | | | |
| COUNT_HOUR | [4:0] | RW | 0x0 | 0x00 - 0x17: RTC HOURS | | | |

Table 205: Register COUNT_D

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----------|-----------------------|---|---|---|
| 0x008D | COUNT_D | 0x01 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | COUNT_DAY | | | | |
| Field name | Bits | Type | POR | Description | | | |
| COUNT_DAY | [4:0] | RW | 0x1 | 0x01 - 0x1F: RTC DAYS | | | |

System PMIC for Dual/Quad-Core Processors

Table 206: Register COUNT_MO

| Address | Name | POR value | | | | | |
|-------------|----------|-----------|----------|-------------------------|---|---|---|
| 0x008E | COUNT_MO | 0x01 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | Reserved | COUNT_MONTH | | | |
| Field name | Bits | Type | POR | Description | | | |
| COUNT_MONTH | [3:0] | RW | 0x1 | 0x01 - 0x0C: RTC MONTHS | | | |

Table 207: Register COUNT_Y

| Address | Name | POR value | | | | | |
|------------|---|------------|-----|--|--|---|---|
| 0x008F | COUNT_Y | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | MONITOR | COUNT_YEAR | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| MONITOR | [6] | RW | 0x0 | RTC Status: | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | 0: Read-out - RTC Clock/Counters OFF (RTC not started or reset after power loss) | | |
| 0x1 | 1: Read-out - Clock ON / Time OK (set to 1 when Setting Time to start the RTC and arm the monitor function) | | | | | | |
| COUNT_YEAR | [5:0] | RW | 0x0 | 0x00 - 0x3F: RTC YEARS (0 corresponds to year 2000) A write to this register latches the registers COUNT_SEC to COUNT_MONTH into the current RTC calendar counter | | | |

Table 208: Register ALARM_S

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----|------------------------------------|---|---|---|
| 0x0090 | ALARM_S | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | ALARM_SEC | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| ALARM_SEC | [5:0] | RW | 0x0 | 0x00 - 0x3B: Alarm SECONDS Setting | | | |

System PMIC for Dual/Quad-Core Processors

Table 209: Register ALARM_MI

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----------|------------------------------------|---------------|---|---|
| 0x0091 | ALARM_MI | 0x80 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TICK_TYPE | Reserved | ALARM_MIN | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TICK_TYPE | [7] | RW | 0x1 | Tick Alarm Interval: | | | |
| | | | | Value | Description | | |
| | | | | 0x0 | 0: One Second | | |
| | | | 0x1 (POR) | 1: One Minute | | | |
| ALARM_MIN | [5:0] | RW | 0x0 | 0x00 - 0x3B: Alarm MINUTES Setting | | | |

Table 210: Register ALARM_H

| Address | Name | POR value | | | | | |
|------------|----------|-----------|------------|----------------------------------|---|---|---|
| 0x0092 | ALARM_H | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | ALARM_HOUR | | | | |
| Field name | Bits | Type | POR | Description | | | |
| ALARM_HOUR | [4:0] | RW | 0x0 | 0x00 - 0x17: Alarm HOURS Setting | | | |

Table 211: Register ALARM_D

| Address | Name | POR value | | | | | |
|------------|----------|-----------|-----------|---------------------------------|---|---|---|
| 0x0093 | ALARM_D | 0x01 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | ALARM_DAY | | | | |
| Field name | Bits | Type | POR | Description | | | |
| ALARM_DAY | [4:0] | RW | 0x1 | 0x01 - 0x1F: Alarm DAYS Setting | | | |

Table 212: Register ALARM_MO

| Address | Name | POR value | | | | | |
|-------------|----------|-----------|----------|-----------------------------------|---|---|---|
| 0x0094 | ALARM_MO | 0x01 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | Reserved | ALARM_MONTH | | | |
| Field name | Bits | Type | POR | Description | | | |
| ALARM_MONTH | [3:0] | RW | 0x1 | 0x01 - 0x0C: Alarm MONTHS Setting | | | |

System PMIC for Dual/Quad-Core Processors

Table 213: Register ALARM_Y

| Address | Name | POR value | |
|---------|---------|-----------|--|
| 0x0095 | ALARM_Y | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|----------|------------|---|---|---|---|---|
| TICK_ON | ALARM_ON | ALARM_YEAR | | | | | |

| Field name | Bits | Type | POR | Description |
|------------|-------|------|-----|--|
| TICK_ON | [7] | RW | 0x0 | Enable tick function. Interval set by TICK_TYPE |
| ALARM_ON | [6] | RW | 0x0 | Enable alarm function |
| ALARM_YEAR | [5:0] | RW | 0x0 | 0x00 - 0x3F: Alarm YEAR Setting (0 corresponds to year 2000). A write to this register latches the registers ALARM_SEC to ALARM_MONTH |

System PMIC for Dual/Quad-Core Processors

A.9 OTP Config

Table 214: Register CHIP_ID

| Address | Name | POR value | | | | | |
|------------|---------|-----------|-----|---|-------------|---|---|
| 0x0096 | CHIP_ID | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| MRC | | | | TRC | | | |
| Field name | Bits | Type | POR | Description | | | |
| MRC | [7:4] | RO | 0x0 | Read back of Mask Revision Code (MRC) | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | AA | | |
| | | | | 0x1 | AB | | |
| TRC | [3:0] | RO OTP | 0x0 | Read back of OTP Trimming Release Code (TRC) - starts with code 0 | | | |

Table 215: Register CONFIG_ID

| Address | Name | POR value | | | | | |
|------------|------------|------------|------------|--|------------|---------|---|
| 0x0097 | CONFIG_ID | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 | CONF_ID | |
| Field name | Bits | Type | POR | Description | | | |
| CONF_ID | [2:0] | RO OTP | 0x0 | ID for Customer Variant of Start-up Voltages and Sequencer Configuration | | | |

Table 216: Register OTP_CONT

| Address | Name | POR value | | | | | |
|--------------|---------------|-------------|----------|------------------------------|---|--------|--------------|
| 0x0098 | OTP_CONT | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GP_WRITE_DIS | OTP_CONF_LOCK | OTP_GP_LOCK | Reserved | OTP_CONF | OTP_GP | OTP_RP | OTP_TRANSFER |
| Field name | Bits | Type | POR | Description | | | |
| GP_WRITE_DIS | [7] | RW OTP | 0x0 | GP_ID Registers Write Access | | | |
| | | | | Value | Description | | |
| | | | | 0x0 (POR) | 0: Enables Write Access to GP_ID Registers | | |
| | | | | 0x1 | 1: Read Only GP_ID Registers Note: Write access for fusing only, control state is loaded from OTP defaults after POR | | |

System PMIC for Dual/Quad-Core Processors

| Field name | Bits | Type | POR | Description | | | | | | |
|---------------|--|-----------|-----|---|-------|-------------|--------------|---|-----|--|
| OTP_CONF_LOCK | [6] | RW OTP | 0x0 | OTP Lock Control: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: OTP Registers R10 to R106 Not Locked after Programming (only for unmarked evaluation samples)</td> </tr> <tr> <td>0x1</td> <td>1: OTP registers R10 to R106 Locked during Programming (set for all marked parts, no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: OTP Registers R10 to R106 Not Locked after Programming (only for unmarked evaluation samples) | 0x1 | 1: OTP registers R10 to R106 Locked during Programming (set for all marked parts, no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: OTP Registers R10 to R106 Not Locked after Programming (only for unmarked evaluation samples) | | | | | | | | | |
| 0x1 | 1: OTP registers R10 to R106 Locked during Programming (set for all marked parts, no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR | | | | | | | | | |
| OTP_GP_LOCK | [5] | RW OTP | 0x0 | GP_OTP Lock Status: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: OTP Not Locked after Programming</td> </tr> <tr> <td>0x1</td> <td>1: OTP Locked during Programming (no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: OTP Not Locked after Programming | 0x1 | 1: OTP Locked during Programming (no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: OTP Not Locked after Programming | | | | | | | | | |
| 0x1 | 1: OTP Locked during Programming (no further fusing possible) Note: Write access for fusing only, control state is loaded from OTP defaults after POR | | | | | | | | | |
| OTP_CONF | [3] | RW | 0x0 | <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: No Action</td> </tr> <tr> <td>0x1</td> <td>1: Transfer Includes Configuration R10 to R106 (plus OTP_CONF_LOCK)</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: No Action | 0x1 | 1: Transfer Includes Configuration R10 to R106 (plus OTP_CONF_LOCK) |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: No Action | | | | | | | | | |
| 0x1 | 1: Transfer Includes Configuration R10 to R106 (plus OTP_CONF_LOCK) | | | | | | | | | |
| OTP_GP | [2] | RW | 0x0 | <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: No Action</td> </tr> <tr> <td>0x1</td> <td>1: Transfer Includes Configuration Registers R132 to R142 (plus GP_WRITE_DIS and OTP_GP_LOCK)</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: No Action | 0x1 | 1: Transfer Includes Configuration Registers R132 to R142 (plus GP_WRITE_DIS and OTP_GP_LOCK) |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: No Action | | | | | | | | | |
| 0x1 | 1: Transfer Includes Configuration Registers R132 to R142 (plus GP_WRITE_DIS and OTP_GP_LOCK) | | | | | | | | | |
| OTP_RP | [1] | RW | 0x0 | OTP Transfer Type: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Read</td> </tr> <tr> <td>0x1</td> <td>1: Programming (Write)</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Read | 0x1 | 1: Programming (Write) |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Read | | | | | | | | | |
| 0x1 | 1: Programming (Write) | | | | | | | | | |
| OTP_TRANSFER | [0] | RW | 0x0 | OTP Status Indicator: <table border="1"> <thead> <tr> <th>Value</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>0x0 (POR)</td> <td>0: Read-out - No Transfer in Progress (writing 1 to this bit initiates the fusing of selected OTP cells with the content from corresponding</td> </tr> <tr> <td>0x1</td> <td>1: Read-out - Transfer in Progress</td> </tr> </tbody> </table> | Value | Description | 0x0 (POR) | 0: Read-out - No Transfer in Progress (writing 1 to this bit initiates the fusing of selected OTP cells with the content from corresponding | 0x1 | 1: Read-out - Transfer in Progress |
| Value | Description | | | | | | | | | |
| 0x0 (POR) | 0: Read-out - No Transfer in Progress (writing 1 to this bit initiates the fusing of selected OTP cells with the content from corresponding | | | | | | | | | |
| 0x1 | 1: Read-out - Transfer in Progress | | | | | | | | | |

System PMIC for Dual/Quad-Core Processors

Table 217: Register OSC_TRIM

| Address | Name | POR value | | | | | |
|------------|--------------------|-----------|----------|-----------------------------------|---------------------------------|----------|----------|
| 0x0099 | OSC_TRIM | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TRIM_32K | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| TRIM_32K | [7:0] | RW OTP | 0x0 | 32K Oscillator Frequency Control: | | | |
| | | | | Value | Description | | |
| | | | | 0x80 | 10000000: -244.1ppm | | |
| | | | | ... | ... | | |
| | | | | 0xFF | 11111111: -1.9ppm | | |
| | | | | 0x0 (POR) | 00000000: OFF | | |
| | | | | 0x1 | 00000001: 1.9ppm (1/(32768*16)) | | |
| | | | | ... | ... | | |
| 0x7F | 01111111: 242.2ppm | | | | | | |

Table 218: Register GP_ID_0

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|--|----------|----------|----------|
| 0x009A | GP_ID_0 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GP_0 | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| GP_0 | [7:0] | RW OTP | 0x0 | General Purpose Data from Fuse Array (OTP) | | | |

Table 219: Register GP_ID_1

| Address | Name | POR value | | | | | |
|------------|----------|-----------|----------|--|----------|----------|----------|
| 0x009B | GP_ID_1 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GP_1 | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| GP_1 | [7:0] | RW OTP | 0x0 | General Purpose Data from Fuse Array (OTP) | | | |

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Table 220: Register GP_ID_2

| Address | Name | POR value | | | | | |
|------------|---------|-----------|-----|--|---|---|---|
| 0x009C | GP_ID_2 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GP_2 | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| GP_2 | [7:0] | RW OTP | 0x0 | General Purpose Data from Fuse Array (OTP) | | | |

Table 221: Register GP_ID_3

| Address | Name | POR value | | | | | |
|------------|---------|-----------|-----|--|---|---|---|
| 0x009D | GP_ID_3 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GP_3 | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| GP_3 | [7:0] | RW OTP | 0x0 | General Purpose Data from Fuse Array (OTP) | | | |

Table 222: Register GP_ID_4

| Address | Name | POR value | | | | | |
|------------|---------|-----------|-----|--|---|---|---|
| 0x009E | GP_ID_4 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GP_4 | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| GP_4 | [7:0] | RW OTP | 0x0 | General Purpose Data from Fuse Array (OTP) | | | |

Table 223: Register GP_ID_5

| Address | Name | POR value | | | | | |
|------------|---------|-----------|-----|--|---|---|---|
| 0x009F | GP_ID_5 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| GP_5 | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| GP_5 | [7:0] | RW OTP | 0x0 | General Purpose Data from Fuse Array (OTP) | | | |

System PMIC for Dual/Quad-Core Processors

A.10 Audio

Table 224: Register AUDIO_REG_DFLT_0

| Address | Name | POR value |
|---------|------------------|-----------|
| 0x00A0 | AUDIO_REG_DFLT_0 | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| AUD_REG_0 | | | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|-------|-----------|-----|-------------|---------------------|
| AUD_REG_0 | [7:0] | RW OTP | 0x0 | Value | Description |
| | | | | 2:0 | Codec Slave address |
| | | | | 3:3 | pc_resync_auto |
| | | | | 5:4 | gain_ramp_rate |
| | | | | 7:6 | PLL_MODE[1:0] |

Table 225: Register AUDIO_REG_DFLT_1

| Address | Name | POR value |
|---------|------------------|-----------|
| 0x00A1 | AUDIO_REG_DFLT_1 | 0x00 |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| AUD_REG_1 | | | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|---------------|-----------|-----|---------------------------|----------------|
| AUD_REG_1 | [7:0] | RW OTP | 0x0 | Audio Register 1 Defaults | |
| | | | | Value | Description |
| | | | | 0:0 | PLL_MODE[2] |
| | | | | 6:1 | cp_thresh_vdd2 |
| 7:7 | dmic_data_sel | | | | |

System PMIC for Dual/Quad-Core Processors

Table 226: Register AUDIO_REG_DFLT_2

| Address | Name | POR value | |
|---------|------------------|-----------|--|
| 0x00A2 | AUDIO_REG_DFLT_2 | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| AUD_REG_2 | | | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|-----------------|-----------|-----|---------------------------|--------------------|
| AUD_REG_2 | [7:0] | RW OTP | 0x0 | Audio Register 2 Defaults | |
| | | | | Value | Description |
| | | | | 0:0 | dmic_samplephase |
| | | | | 1:1 | dmic_clk_rate |
| | | | | 3:2 | aux_l_amp_bias |
| | | | | 5:4 | mic_l_amp_bias |
| 7:6 | mic_bias1_level | | | | |

Table 227: Register AUDIO_REG_DFLT_3

| Address | Name | POR value | |
|---------|------------------|-----------|--|
| 0x00A3 | AUDIO_REG_DFLT_3 | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| AUD_REG_3 | | | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|------------------------|-----------|-----|---------------------------|--------------------|
| AUD_REG_3 | [7:0] | RW OTP | 0x0 | Audio Register 3 Defaults | |
| | | | | Value | Description |
| | | | | 0:0 | micbias1_en |
| | | | | 2:1 | micbias2_level |
| | | | | 3:3 | micbias2_en |
| | | | | 4:4 | micbias3_en |
| | | | | 6:5 | mixin_l_amp_bias |
| 7:7 | adc_bias_trim[6,4,2,0] | | | | |

System PMIC for Dual/Quad-Core Processors

Table 228: Register AUDIO_REG_DFLT_4

| Address | Name | POR value | |
|---------|------------------|-----------|--|
| 0x00A4 | AUDIO_REG_DFLT_4 | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| AUD_REG_4 | | | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|------------------|-----------|-----|---------------------------|------------------------|
| AUD_REG_4 | [7:0] | RW OTP | 0x0 | Audio Register 4 Defaults | |
| | | | | Value | Description |
| | | | | 0:0 | adc_bias_trim[7,5,3,1] |
| | | | | 3:1 | dac_l_bias |
| | | | | 5:4 | mixout_l_amp_bias |
| | | | | 6:6 | mixout_l_mix_tie_off |
| 7:7 | hp_l_amp_bias[0] | | | | |

Table 229: Register AUDIO_REG_DFLT_5

| Address | Name | POR value | |
|---------|------------------|-----------|--|
| 0x00A5 | AUDIO_REG_DFLT_5 | 0x00 | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| AUD_REG_5 | | | | | | | |

| Field name | Bits | Type | POR | Description | |
|------------|---------------|-----------|-----|---------------------------|--------------------|
| AUD_REG_5 | [7:0] | RW OTP | 0x0 | Audio Register 5 Defaults | |
| | | | | Value | Description |
| | | | | 0:0 | hp_l_amp_bias[1] |
| | | | | 1:1 | hp_amp_ems_en |
| | | | | 2:2 | unused |
| | | | | 4:3 | ep_amp_bias |
| | | | | 6:5 | sp_amp_bias |
| 7:7 | bias_level[0] | | | | |

System PMIC for Dual/Quad-Core Processors

Table 230: Register AUDIO_REG_DFLT_6

| Address | Name | POR value | | | | | |
|------------|------------------|-----------|----------|---------------------------|---------------------|----------|----------|
| 0x00A6 | AUDIO_REG_DFLT_6 | 0x00 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| AUD_REG_6 | | | | | | | |
| Field name | Bits | Type | POR | Description | | | |
| AUD_REG_6 | [7:0] | RW OTP | 0x0 | Audio Register 6 Defaults | | | |
| | | | | Value | Description | | |
| | | | | 0:0 | bias_level[1] | | |
| | | | | 1:1 | io_voltage_level | | |
| | | | | 3:2 | ldo_level_select | | |
| | | | | 4:4 | ldo_en | | |
| | | | | 6:5 | ADD_SLAVE_ADDR[1:0] | | |
| | | | | 7:7 | PMIC_POR_DISABLE | | |

A.11 RF Supplies Control

Table 231: Register BUCK2_5_CONF1

| Address | Name | POR value | | | | | |
|--------------------|--------------------|-------------------|----------|------------------------------------|------------|------------|------------|
| 0x00DF | BUCK2_5_CONF1 | 0x80 | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| buck_6_ext_ctrl_en | buck_5_ext_ctrl_en | ldo18_ext_ctrl_en | Reserved | Reserved 0 | Reserved 0 | Reserved 0 | Reserved 0 |
| Field name | Bits | Type | POR | Description | | | |
| buck_6_ext_ctrl_en | [7] | RW OTP | 0x1 | Buck 6 external pin control enable | | | |
| buck_5_ext_ctrl_en | [6] | RW OTP | 0x0 | Buck 5 external pin control enable | | | |
| ldo18_ext_ctrl_en | [5] | RW OTP | 0x0 | ldo18 external pin control enable | | | |
| | | | | | | | |

System PMIC for Dual/Quad-Core Processors

Appendix B Audio Register Descriptions

B.1 Common Registers

Table 232: Common1 Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|----------------|------|-----|------------|---------|--------------------|--|
| CIF_CTRL | 0x01 | 0 | lat_rw | 0b0 | CIF_I2C_WRITE_MODE | 2-wire interface write mode: 0 = page mode, register address is auto incremented after first write. 1 = repeat mode, register address and data is sent for each write. |
| | | 7 | reg_rw_clr | 0b0 | CIF_REG_SOFT_RESET | Software reset which returns all the registers back to the default. Writing to this bit causes all the registers to reset. |
| SR | 0x02 | 3:0 | reg_rw | 0b1010 | SR | Sample rate control: 0001 = 8.000 kHz 0010 = 11.025 kHz 0011 = 12.000 kHz 0101 = 16.000 kHz 0110 = 22.050 kHz 0111 = 24.000 kHz 1001 = 32.000 kHz 1010 = 44.100 kHz 1011 = 48.000 kHz 1110 = 88.200 kHz 1111 = 96.000 kHz |
| PC_COUNT | 0x03 | 0 | lat_rw | 0b0 | PC_FREERUN | Enables the filter operation when AIF is not enabled or no AIF clocks are available (ADC to DAC processing path): 0 = Filters synchronized to the AIF 1 = Filters free running |
| | | 1 | lat_rw_otp | 0b0 | PC_RESYNC_AUTO | PC resync mode:- 0 = no resync - just double sample or skip sample if the clocks drift 1 = autoresync upon detection of AIF drift wrt to system clock |
| GAIN_RAMP_CTRL | 0x04 | 1:0 | lat_rw_otp | 0b00 | GAIN_RAMP_RATE | Controls the gain slew rate for all parts of the system when ramping the gain: 0 = nominal rate 1 = nominal rate * 4 (faster) 2 = nominal rate * 8 (fastest) 3 = nominal rate / 8 (slowest) |

Table 233: Common2 Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|---------------|------|-----|-------------|---------|---------------|------------------------------|
| CHIP_ID2 | 0x82 | 7:0 | dat_ro_data | 0x53 | CHIP_ID2 | Chip ID second two numbers |
| CHIP_REVISION | 0x83 | 3:0 | dat_ro_data | 0x0 | CHIP_MINOR | Chip minor revision |
| | | 7:4 | dat_ro_data | 0x0 | CHIP_MAJOR | Chip major revision |
| SPARE1 | 0x84 | 7:0 | reg_rw | 0x00 | SPARE1 | Spare registers of flop type |
| STATUS1 | 0x85 | 7:0 | dat_ro_data | 0x00 | STATUS_SPARE1 | Spare status registers |

System PMIC for Dual/Quad-Core Processors

B.2 System Registers

Table 234: System Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------------|------|-----|-------------|---------|-------------|--|
| SYSTEM_STATUS | 0x08 | 0 | dat_ro_data | 0b0 | SC1_BUSY | Indicates the current status of the system controller: 0 = complete 1 = busy |
| | | 1 | dat_ro_data | 0b0 | SC2_BUSY | Indicates the current status of the system mode controller: 0 = complete 1 = busy |
| SYSTEM_MODES_CFG1 | 0x09 | 0 | reg_rw_clr | 0b0 | MODE_SUBMIT | Causes both the ADC_MODE and DAC_MODE to become active |
| | | 7:1 | lat_rw | 0x00 | MODE_CFG1 | preconfigured system modes (input side): [2] = MIC_L [3] = MIC_R [4] = MIXEXT [5] = MICBIAS1 [6] = MICBIAS2 [7] = MICBIAS3 |
| SYSTEM_MODES_CFG2 | 0x0a | 0 | duplicate | 0b0 | MODE_SUBMIT | Mirrored function of MODE_SUBMIT. |
| | | 7:1 | lat_rw | 0x00 | MODE_CFG2 | preconfigured system modes (output side): [1] = [2] = AUX_L [3] = AUX_R [4] = MIXIN_L [5] = MIXIN_R [6] = ADC_L [7] = ADC_R |
| SYSTEM_MODES_CFG3 | 0x0b | 0 | duplicate | 0b0 | MODE_SUBMIT | Mirrored function of MODE_SUBMIT. |
| | | 7:1 | lat_rw | 0x00 | MODE_CFG3 | preconfigured system modes (output side): [1] = [2] = EP [3] = RCVR [4] = HP_L [5] = HP_R [6] = DAC_L [7] = DAC_R |

System PMIC for Dual/Quad-Core Processors

B.3 ADC Filter

Table 235: ADC Filter Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|--------------|------|-----|--------|---------|--------------------------|--|
| ADC_FILTERS1 | 0x1c | 2:0 | lat_rw | 0b000 | ADC_VOICE_HPF_CO RNER | Voice (8 kHz) High pass 3 dB cutoff at: 000 = 2.5 Hz 001 = 25 Hz, 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz |
| | | 3 | lat_rw | 0b0 | ADC_VOICE_EN | ADC voice filter enable 0 = disable 1 = enable |
| | | 5:4 | lat_rw | 0b00 | ADC_AUDIO_HPF_CO RNER | High-pass filter at 48 kHz the 3 dB cutoff is at: 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = 16 Hz For other sample rates the corner scales. |
| | | 7 | lat_rw | 0b1 | ADC_HPF_EN | ADC high-pass filter enable 0 = disable 1 = enable |
| ADC_FILTERS2 | 0x1d | 3:0 | lat_rw | 0b1000 | ADC_EQ_BAND1 | Gain of ADC 5-band EQ band 1: 0000 = -10.5 dB in 1.5dB steps 0111 = 0 dB 1111 = 12 dB |
| | | 7:4 | lat_rw | 0b1000 | ADC_EQ_BAND2 | Gain of ADC 5-Band EQ band 2. Settings as band 1. |
| ADC_FILTERS3 | 0x1e | 3:0 | lat_rw | 0b1000 | ADC_EQ_BAND3 | Gain of ADC 5-Band EQ band 3. Settings as band 1. |
| | | 7:4 | lat_rw | 0b1000 | ADC_EQ_BAND4 | Gain of ADC 5-Band EQ band 4. Settings as band 1. |
| ADC_FILTERS4 | 0x1f | 3:0 | lat_rw | 0b1000 | ADC_EQ_BAND5 | Gain of ADC 5-Band EQ band 5. Settings as band 1. |
| | | 5:4 | lat_rw | 0b00 | ADC_EQ_GAIN | Overall gain of ADC 5 Band EQ: 00: 0 dB 01: -6 dB 10: -12 dB 11: Reserved |
| | | 7 | lat_rw | 0b0 | ADC_EQ_EN | ADC 5-band EQ enable: 0 = equalizer disabled 1 = equalizer enabled |

System PMIC for Dual/Quad-Core Processors

B.4 DAC Filter

Table 236: DAC Filter Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|--------------|------|-----|--------|---------|----------------------|--|
| DAC_FILTERS1 | 0x24 | 2:0 | lat_rw | 0b000 | DAC_VOICE_HPF_CORNER | Voice (8 kHz) High-pass 3 dB cutoff at: 000 = 2.5 Hz 001 = 25 Hz, 010 = 50 Hz 011 = 100 Hz 100 = 150 Hz 101 = 200 Hz 110 = 300 Hz 111 = 400 Hz |
| | | 3 | lat_rw | 0b0 | DAC_VOICE_EN | DAC voice filter 0 = disable 1 = enable overrides ADC_EQ5B_EN |
| | | 5:4 | lat_rw | 0b00 | DAC_AUDIO_HPF_CORNER | High-pass filter at 48 kHz the 3 dB cutoff is at: 00 = 2 Hz 01 = 4 Hz 10 = 8 Hz 11 = 16 Hz For other sample rates the corner scales. |
| | | 7 | lat_rw | 0b1 | DAC_HPF_EN | DAC high-pass filter enable 0 = disable 1 = enable |
| DAC_FILTERS2 | 0x25 | 3:0 | lat_rw | 0b1000 | DAC_EQ_BAND1 | Gain of DAC 5-band EQ band 1: 0000 = -10.5 dB in 1.5 dB steps 0111 = 0 dB 1111 = 12 dB |
| | | 7:4 | lat_rw | 0b1000 | DAC_EQ_BAND2 | Gain of DAC 5-band EQ band 2. Settings as band 1. |
| DAC_FILTERS3 | 0x26 | 3:0 | lat_rw | 0b1000 | DAC_EQ_BAND3 | Gain of DAC 5-band EQ band 3. Settings as band 1. |
| | | 7:4 | lat_rw | 0b1000 | DAC_EQ_BAND4 | Gain of DAC 5-band EQ band 4. Settings as band 1. |
| DAC_FILTERS4 | 0x27 | 3:0 | lat_rw | 0b1000 | DAC_EQ_BAND5 | Gain of DAC 5-band EQ band 5. Settings as band 1. |
| | | 7 | lat_rw | 0b0 | DAC_EQ_EN | DAC 5-band EQ enable: 0 = equalizer disabled 1 = equalizer enabled |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|--------------|------|-----|--------|---------|-------------------|---|
| DAC_FILTERS5 | 0x28 | 6:4 | lat_rw | 0b000 | DAC_SOFTMUTE_RATE | Softmute gain update rate (samples per 0.1875dB): 000 = 1 001 = 2 010 = 4 ... 110 = 64 111 = reserved |
| | | 7 | lat_rw | 0b0 | DAC_SOFTMUTE_EN | DAC softmute enable causing both channels to mute: 0 = disable 1 = enable |

B.5 ALC

Table 237: ALC Registers

| Register | Addr | Bit | Type | Default | Name | Description |
|-----------|------|-----|-------------|---------|--------------------|--|
| ALC_CTRL1 | 0x2c | 0 | lat_rw | 0b0 | ALC_OFFSET_EN | |
| | | 1 | lat_rw | 0b0 | ALC_SYNC_MODE | |
| | | 2 | lat_rw | 0b0 | ALC_CALIB_MODE | Calibration mode 0: Automatic calibration 1: Manual calibration |
| | | 3 | lat_rw | 0b0 | ALC_L_EN | Enables the ALC operation on the left ADC channel: 0 = Disabled 1 = Enabled |
| | | 4 | reg_rw_clr | 0b0 | ALC_AUTO_CALIB_EN | Automatic calibration enable(self clearing bit) |
| | | 5 | dat_ro_data | 0b0 | ALC_CALIB_OVERFLOW | Offset overflow during calibration |
| | | 6 | lat_rw | 0b0 | ALC_EXT_MIC_MODE | Microphone selection in hybrid mode: 0: MIC1 for left channel MIC2 for right channel 1: EXT_MIC for left channel if ALC_L_EN = 1 EXT_MIC for right channel if ALC_R_EN = 1 |
| | | 7 | lat_rw | 0b0 | ALC_R_EN | Enables the ALC operation on the left ADC channel: 0 = Disabled 1 = Enabled |
| ALC_CTRL2 | 0x2d | 3:0 | lat_rw | 0x0 | ALC_ATTACK | Sets the ALC attack rate: the speed at which the ALC can change the gain down by 6 dB. 0 = fs/44 (0.917 μs@48 kHz) 1 = fs/88 (1.8 ms@48 kHz) ... 12-15 = fs/180224 (3.75 s@48 kHz) |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Name | Description |
|----------------|------|-----|--------|---------|-------------------|---|
| | | 7:4 | lat_rw | 0x0 | ALC_RELEASE | Sets the ALC release rate: the speed at which the ALC can change the gain up by 6 dB. 0 = fs/172 (3.6 ms@48 kHz) 1 = fs/344 (7.3 ms@48 kHz) ... 10 to 15 = fs/176128 (3.7 s@48 kHz) |
| ALC_CTRL3 | 0x2e | 3:0 | lat_rw | 0x0 | ALC_HOLD | Sets the ALC hold time: the period at which the ALC waits before releasing. 0 = fs/62 (1.3 ms@48 kHz) 1 = fs/122 (2.6 ms@48 kHz) ... 15 = fs/2031616 (42.3 s@48 kHz) |
| | | 5:4 | lat_rw | 0b00 | ALC_INTEG_ATTACK | Sets the rate at which the input signal envelope is tracked as the signal gets larger: 0 = 1/4 1 = 1/16 2 = 1/256 3 = 1/65536 |
| | | 7:6 | lat_rw | 0b00 | ALC_INTEG_RELEASE | Sets the rate at which the input signal envelope is tracked as the signal gets smaller: 0 = 1/4 1 = 1/16 2 = 1/256 3 = 1/65536 |
| ALC_NOISE | 0x2f | 5:0 | lat_rw | 0x3f | ALC_NOISE | Sets the threshold below which input signals will not cause the ALC to change gain: 0 = 0 dBFS 1 = -1.5 dBFS ... 63 = -94.5 dBFS |
| ALC_TARGET_MIN | 0x30 | 5:0 | lat_rw | 0x3f | ALC_THRESHOLD_MIN | Sets the minimum amplitude of the ALC output signal before the ALC increases the gain. If the minimum attenuation level allowed is reached then the ALC will not increase the gain even if this threshold is breached: 0 = 0 dBFS 1 = -1.5 dBFS ... 63 = -94.5 dBFS |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Name | Description |
|---------------------|------|-----|--------|---------|--------------------|---|
| ALC_TARGET_MAX | 0x31 | 5:0 | lat_rw | 0x00 | ALC_THRESH_OLD_MAX | Sets the maximum amplitude of the ALC output signal before the ALC reduces the gain. If the maximum attenuation level allowed is reached then the ALC will not reduce the gain even if this threshold is exceeded: 0 = 0 dBFS 1 = -1.5 dBFS ... 63 = -94.5 dBFS |
| ALC_GAIN_LIMITS | 0x32 | 3:0 | lat_rw | 0xf | ALC_ATTEN_MAX | Sets the maximum amount of attenuation that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold: 0 = 0 dB 1 = 6 dB ... 63 = 90 dB |
| | | 7:4 | lat_rw | 0xf | ALC_GAIN_MAX | Sets the maximum amount of gain that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold: 0 = 0 dB 1 = 6 dB ... 63 = 90 dB |
| ALC_ANA_GAIN_LIMITS | 0x33 | 2:0 | lat_rw | 0b001 | ALC_ANA_GAIN_MIN | Sets the minimum amount of analog gain that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold (mixed analog and digital gain mode only): 0 = reserved 1 = 0 dB 2 = 6 dB ... 7 = 36 dB |
| | | 6:4 | lat_rw | 0b111 | ALC_ANA_GAIN_MAX | Sets the maximum amount of analog gain that can be applied to the input signal by the ALC when the input signal is large relative to the maximum threshold (mixed analog and digital gain mode only): 0 = reserved 1 = 0 dB 2 = 6 dB ... 7 = 36 dB |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Name | Description |
|---------------------|------|-----|----------------|---------|---------------------|---|
| ALC_ANTICLIP_CTRL | 0x34 | 7 | lat_rw | 0b0 | ALC_ANTICLIP_EN | Enables the ALC signal clip prevention mechanism: 0 = Disabled 1 = Enabled |
| ALC_ANTICLIP_LEVEL | 0x35 | 6:0 | lat_rw | 0x00 | ALC_ANTICLIP_LEVEL | Sets the threshold above which the ALC enters anti-clip operation: 00 = 0.0039 FS 01 = 0.0078 FS 7F = 1.0000 FS |
| ALC_OFFSET_AUTO_M_L | 0x36 | 7:0 | dat_ro_data | 0x00 | ALC_OFFSET_AUTO_M_L | Offset correction (automatic mode) for the left channel; bits[15:8] (RO) |
| ALC_OFFSET_AUTO_U_L | 0x37 | 3:0 | dat_ro_data | 0x00 | ALC_OFFSET_AUTO_U_L | Offset correction (automatic mode) for the left channel; bits[19:16] (RO) |
| ALC_OFFSET_MAN_M_L | 0x39 | 7:0 | lat_rw | 0x00 | ALC_OFFSET_MAN_M_L | Offset correction (manual mode) for the left channel; bits[15:8] |
| ALC_OFFSET_MAN_U_L | 0x3a | 3:0 | lat_rw | 0x0 | ALC_OFFSET_MAN_U_L | Offset correction (manual mode) for the left channel; bits[19:16] |
| ALC_OFFSET_AUTO_M_R | 0x3b | 7:0 | dat_ro_data | 0x00 | ALC_OFFSET_AUTO_M_R | Offset correction (automatic mode) for the right channel; bits[15:8] (RO) |
| ALC_OFFSET_AUTO_U_R | 0x3c | 3:0 | dat_ro_data | 0x00 | ALC_OFFSET_AUTO_U_R | Offset correction (automatic mode) for the right channel; bits[19:16] (RO) |
| ALC_OFFSET_MAN_M_R | 0x3e | 7:0 | lat_rw | 0x00 | ALC_OFFSET_MAN_M_R | Offset correction (manual mode) for the right channel; bits[15:8] |
| ALC_OFFSET_MAN_U_R | 0x3f | 3:0 | lat_rw | 0x0 | ALC_OFFSET_MAN_U_R | Offset correction (manual mode) for the right channel; bits [19:16] |
| ALC_CIC_OP_LVL_CTRL | 0x40 | 1:0 | lat_rw_writing | 0x0 | ALC_CIC_OP_CTRL | ALC CIC output level read control: 0 = capture ALC_CIC_OP_LVL_DATA 1 = select bottom 8 bits for read back on ALC_CIC_OP_LVL_DATA 2 = select middle 8 bits for read back on ALC_CIC_OP_LVL_DATA 3 = select top 8 bits for read back on ALC_CIC_OP_LVL_DATA |
| | | 7 | lat_rw | 0b0 | ALC_CIC_OP_CHANNEL | ALC CIC output channel select: 0 = left channel 1 = right channel |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Name | Description |
|---------------------|------|-----|-------------|---------|------------|---|
| ALC_CIC_OP_LVL_DATA | 0x41 | 7:0 | dat_ro_data | 0x00 | ALC_CIC_OP | ALC CIC output data as selected by the control register |

B.6 Digital Router

Table 238: Digital Router Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-----------------|------|-----|--------|---------|------------|---|
| DIG_ROUTING_AIF | 0x44 | 1:0 | lat_rw | 0b00 | AIF_L_SRC | Data select for the AIF left output stream: 0 = ADC left 1 = ADC right 2 = AIF input left data 3 = AIF input right data |
| | | 5:4 | lat_rw | 0b01 | AIF_R_SRC | Data select for the AIF right output stream: 0 = ADC left 1 = ADC right 2 = AIF input left data 3 = AIF input right data |
| DIG_ROUTING_DAC | 0x45 | 1:0 | lat_rw | 0b10 | DAC_L_SRC | Data select to the DAC_L path: 0 = ADC left output 1 = ADC right output 2 = AIF input left / AIF left mono mix 3 = AIF input right / AIF right mono mix |
| | | 3 | lat_rw | 0b0 | DAC_L_MONO | AIF left input stream is replaced with a mono mix of left and right |
| | | 5:4 | lat_rw | 0b11 | DAC_R_SRC | Data select to the DAC_L path: 0 = adc left output 1 = adc right output 2 = AIF input left / AIF mono mix 3 = AIF input right / AIF mono mix |
| | | 7 | lat_rw | 0b0 | DAC_R_MONO | AIF right input stream is replaced with a mono mix of left and right |
| DIG_CTRL | 0x46 | 3 | lat_rw | 0b0 | DAC_L_INV | AIF left input stream is inverted |
| | | 7 | lat_rw | 0b0 | DAC_R_INV | AIF right input stream is inverted |

System PMIC for Dual/Quad-Core Processors

B.7 AIF

Table 239: AIF Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|--------------|------|-----|--------|---------|--------------------|--|
| AIF_CTRL | 0x48 | 1:0 | lat_rw | 0b00 | AIF_FORMAT | AIF data format: 0 = I ² S mode 1 = left justified mode 2 = right justified mode 3 = DSP mode |
| | | 3:2 | lat_rw | 0b10 | AIF_WORD_LENGTH | AIF data word length: 0 = 16 bits per channel 1 = 20 bits per channel 2 = 24 bits per channel 3 = 32 bits per channel |
| | | 4 | lat_rw | 0b0 | AIF_MONO_MODE_EN | AIF mono mode enable. In mono mode only the data from the AIF left output stream is transmitted: 0 = AIF stereo mode 1 = AIF mono mode |
| | | 5 | lat_rw | 0b0 | AIF_TDM_MODE_EN | AIF TDM mode enable. In TDM mode the output is high impedance when not actively driving data to allow other devices to share the DATOUT line: 0 = AIF normal mode 1 = AIF TDM mode |
| | | 6 | lat_rw | 0b0 | AIF_OE | AIF output enable: 0 = AIF DATOUT pin is high impedance 1 = AIF DATOUT pin is driven when required |
| | | 7 | lat_rw | 0b0 | AIF_EN | AIF enable: 0 = AIF disabled; no data transferred 1 = AIF enabled; input and output data streams transferred |
| AIF_OFFSET | 0x49 | 7:0 | lat_rw | 0x00 | AIF_OFFSET | AIF data offset with respect to WCLK. 0 = no offset relative to the normal formatting. |
| AIF_CLK_MODE | 0x4a | 1:0 | lat_rw | 0b01 | AIF_BCLKS_PER_WCLK | AIF master mode BCLK number per WCLK period: 0 = #BCLK = 32 1 = #BCLK = 64 2 = #BCLK = 128 3 = #BCLK = 256 |
| | | 2 | lat_rw | 0b0 | AIF_CLK_POL | AIF clock polarity: 0 = normal polarity 1 = inverted polarity |
| | | 3 | lat_rw | 0b0 | AIF_WCLK_POL | AIF word clock polarity: 0 = normal polarity 1 = inverted polarity |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|----------|------|-----|--------|---------|------------|---|
| | | 7 | reg_rw | 0b0 | AIF_CLK_EN | AIF master mode enable: 0 = slave mode (BCLK/WCLK inputs) 1 = master mode (BCLK/WCLK outputs) |

B.8 PLL

Table 240: PLL Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|--------------|------|-----|-----------------|---------|--------------------|---|
| PLL_CTRL | 0x4c | 3:2 | lat_rw | 0b11 | PLL_INDIV | PLL reference input clock (MCLK) rate: 0 = 2 MHz to 4.5 MHz 1 = 4.5 MHz to 9 MHz 2 = 9 MHz to 18 MHz 3 = 18 MHz to 36 MHz 4 = 36 MHz to 54 MHz |
| | | 4 | lat_rw | 0b0 | PLL_MCLK_SQR_EN | 0 = squarer disabled 1 = squarer enabled |
| | | 5 | | | | Reserved |
| | | 6 | lat_rw | 0b0 | PLL_SRM_EN | PLL sample rate tracking enable: 0 = PLL rate is reference * PLL_FBDIV 1 = PLL rate is locked to AIF WCLK |
| | | 7 | lat_rw | 0b0 | PLL_EN | PLL enable: 0 = system clock is MCLK 1 = system clock is PLL output |
| PLL_FRAC_TOP | 0x4d | 4:0 | lat_rw_otp | 0x00 | PLL_FBDIV_FRAC_TOP | PLL fractional division value (top bits) |
| PLL_FRAC_BOT | 0x4e | 7:0 | lat_rw_otp | 0x00 | PLL_FBDIV_FRAC_BOT | PLL fractional division value (bottom bits) |
| PLL_INTEGER | 0x4f | 6:0 | lat_rw_otp_wrig | 0x20 | PLL_FBDIV_INTEGER | PLL integer division value. Note that writing this register causes the entire PLL_FBDIV value (PLL_INTEGER, PLL_FRAC_TOP, PLL_FRAC_BOT) to be updated. |
| PLL_STATUS | 0x50 | 0 | dat_ro_data | 0b0 | PLL_LOCK | Indicates if the PLL is locked to the reference clock |
| | | 1 | dat_ro_data | 0b0 | PLL_SRM_LOCK | Indicates if the SRM is locked to the reference signal |
| | | 2 | dat_ro_data | 0b0 | PLL_MCLK_STATUS | Indicates if the frequency on MCLK is greater than 1 MHz. |
| | | 3 | dat_ro_data | 0b0 | PLL_BYPASS_ACTIVE | Indicates whether the PLL is in bypass mode. |

System PMIC for Dual/Quad-Core Processors

B.9 DAC Noise Gate

Table 241: DAC Noise Gate Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|----------------------|------|-----|--------|---------|----------------------|---|
| DAC_NG_CTRL | 0x54 | 7 | lat_rw | 0b0 | DAC_NG_EN | DAC noise gate enable: 0 = disabled 1 = enabled |
| DAC_NG_SETUP_TIME | 0x55 | 1:0 | lat_rw | 0x0 | DAC_NG_SETUP_TIME | Time for which the largest signal through the DACs must be below DAC_NG_ON_THRESHOLD for the noise gate to mute the data. 0 = 256 samples 1 = 512 samples 2 = 1024 samples 3 = 2048 samples |
| | | 2 | lat_rw | 0b0 | DAC_NG_RAMPUP_RATE | |
| | | 3 | lat_rw | 0b0 | DAC_NG_RAMPDN_RATE | |
| DAC_NG_OFF_THRESHOLD | 0x56 | 2:0 | lat_rw | 0x0 | DAC_NG_OFF_THRESHOLD | Threshold above which the noise gate will be deactivated: 0 = -90 dB 1 = -84 dB ... 7 = -48 dB |
| DAC_NG_ON_THRESHOLD | 0x57 | 2:0 | lat_rw | 0x0 | DAC_NG_ON_THRESHOLD | Threshold below which the noise gate will start to activate (see DAC_NG_OFF_THRESHOLD for levels) |

B.10 Charge Pump

Table 242: Charge Pump Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|----------|------|-----|--------|---------|-----------------|--|
| CP_CTRL | 0x5c | 1:0 | lat_rw | 0b01 | CP_ANALOGUE_LVL | Charge pump analog feedback control mode: 0 = no feedback 1 = low voltage indicator boosts charge pump 2 = low voltage indicator restarts charge pump cycle |
| | | 3:2 | lat_rw | 0b00 | CP_MOD | Charge pump manual mode level control: 0 = standby 1 = reserved 2 = CPVDD/2 3 = CPVDD/1 |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------------|------|-----|------------|---------|-------------------------|---|
| | | 5:4 | lat_rw | 0b10 | CP_MCHANGE | Charge pump tracking mode select: 0 = voltage level is controlled by cp_mod 1 = voltage level is controlled by the largest output volume level 2 = voltage level is controlled by the DAC output signal magnitude 3 = voltage level is controlled by the analog output signal magnitude and the programmed gain setting |
| | | 6 | lat_rw | 0b1 | CP_SMALL_SWITCH_FREQ_EN | Charge pump low-load low-power mode enable: 0 = off 1 = on |
| | | 7 | lat_rw | 0b0 | CP_EN | Charge pump enable: 0 = off 1 = on |
| CP_DELAY | 0x5d | 2:0 | lat_rw | 0b101 | CP_FCONTROL | Charge pump nominal clock rate. Lower rates provide lower power but can drive less load: 0 = 1 MHz 1 = 500 kHz 2 = 250 kHz 3 = 125 kHz 4 = 63 kHz 5 = 0 kHz (analog feedback control only) 6,7 = reserved |
| | | 5:3 | lat_rw | 0b010 | CP_TAU_DELAY | Charge pump voltage decay rate control measured (all values are rounded): 0 = 0 ms 1 = 2 ms 2 = 4 ms 3 = 16 ms 4 = 64 ms 5 = 128 ms 6 = 256 ms 7 = 512 ms |
| | | 7:6 | lat_rw | 0b10 | CP_ONOFF | Charge pump limiter enable: 0 = limiter on 1 = limiter off 2 = limiter automatically enabled when required |
| CP_DETECTOR | 0x5e | 1:0 | lat_rw | 0b00 | CPDET_DROP | Charge pump maximum voltage droop: 0 = 25 mV 1 = 50 mV 2 = 75 mV 3 = 100 mV |
| CP_VOL_THRESHOLD1 | 0x5f | 5:0 | lat_rw_otp | 0x32 | CP_THRESH_VDD2 | Threshold at and below which the charge pump can use the CPVDD/2 rail. |

System PMIC for Dual/Quad-Core Processors

B.11 Digital Microphone

Table 243: Digital Microphone Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|------------|------|-----|------------|---------|------------------|---|
| MIC_CONFIG | 0x68 | 0 | lat_rw_otp | 0b0 | DMIC_DATA_SEL | DMIC channel select 0 = {rising L, falling R} 1 = {falling L, rising R} |
| | | 1 | lat_rw_otp | 0b0 | DMIC_SAMPLEPHASE | 0 = sample on DMICCLK edges 1 = sample between DMICCLK edges. |
| | | 2 | lat_rw_otp | 0b0 | DMIC_CLK_RATE | 0 = 3 MHz 1 = 1.5 MHz |

B.12 Accessory Detect

Table 244: Accessory Detect Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|---------------|------|-----|-------------|---------|----------------------|---|
| ACCDET_CONFIG | 0x6C | 1:0 | lat_rw | 0b0 | ACCDET_MODE | Accessory detect power optimisation mode: 0 = Automatic power optimisation 1 = Low power, simple button detect 2 = Higher power, low latency 3 = Microphone externally biased |
| | | 3 | lat_rw | 0b0 | ACCDET_JACK_EN | Accessory detect jack detection : 0 = Disabled 1 = Enabled |
| | | 7 | lat_rw | 0b0 | ACCDET_BTN_EN | Accessory detect button detection: 0 = Disabled 1 = Enabled |
| ACCDET_STATUS | 0x6d | 7:0 | dat_ro_data | 0x00 | ACCDET_BTN_STATUS | Measured impedance of the button. |
| ACCDET_CFG1 | 0x6e | 1:0 | lat_rw | 0b10 | ACCDET_JACK_BOOST | Set the current level used for jack detection: 0 = 50 μ A 1 = 100 μ A 2 = 150 μ A 3 = 200 μ A |
| | | 3:2 | lat_rw | 0b01 | ACCDET_JACK_DEBOUNCE | Number of samples taken by the jack det before a decision is made: 0 = 1 sample 1 = 2 samples 2 = 3 samples 3 = 4 samples |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------|------|-----|-------------|---------|-------------------------------|---|
| | | 7:4 | lat_rw | 0b0100 | ACCDET_NO_JACK_RATE | Time between jack detection updates when no jack is present: 0 = 0.256 ms 1 = 0.512 ms doubling each setting up to 10 = 262.144 ms 11 to 15 = reserved |
| ACCDET_CFG2 | 0x6f | 3:0 | lat_rw | 0b1000 | ACCDET_THREE_POLE_JACK_RATE | Time between jack detection updates when a 3-pole jack is present: Timings as accdet_no_jack_rate |
| | | 7:4 | lat_rw | 0b0100 | ACCDET_FOUR_POLE_JACK_RATE | Time between jack detection updates when a 4-pole jack is present. Timings as accdet_no_jack_rate |
| ACCDET_CFG3 | 0x70 | 1:0 | lat_rw | 0b00 | ACCDET_BTN_BOOST | Set the current level used for button detection: 0 = 50uA 1 = 100uA 2 = 150uA 3 = 200uA |
| | | 3:2 | lat_rw | 0b00 | ACCDET_ADC_DEBOUNCE | Number of samples taken by the button det before a decision is made: 0 = 1 sample 1 = 2 samples 2 = 3 samples 3 = 4 samples |
| | | 5:4 | lat_rw | 0b00 | ACCDET_TIMEOUT | Number of samples taken by the button det before a decision is made: 0 = 1 sample 1 = 2 samples 2 = 3 samples 3 = 4 samples |
| | | 7:6 | dat_ro_data | 0b00 | ACCDET_JACK_MODE | AUX_R amplifier enable: 0 = disable 1 = enable |
| ACCDET_CFG5 | 0x72 | 0 | lat_rw | 0b0 | ACCDET_ADC_FORCE_FLOAT_IN_MSK | 0: Normal 1: Masks off force_float |
| | | 1 | lat_rw | 0b0 | ACCDET_ADC_PD_MICBIAS_MSK | 0: Normal 1: Masks off pd_micbias |
| | | 2 | lat_rw | 0b1 | ACCDET_ISOOURCE_JACK_FRC_EN | 0: Normal 1: Force the accdet isource on (arm, jackdet_en) |
| | | 3 | lat_rw | 0b0 | ACCDET_ISOOURCE_MIC_FRC_EN | 0: Normal 1: Force the accdet isource on (arm, micdet_en) |
| | | 4 | lat_rw | 0b0 | ACCDET_JACKDET_FRC_EN | 0: Normal 1: Force jackdet_en |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|----------------|------|-----|--------|---------|------------------------|--|
| | | 5 | lat_rw | 0b1 | ACCDET_JACKDET_HYST_EN | 0: No hysteresis in Jackdet 1: En hysteresis in Jackdet |
| | | 6 | lat_rw | 0b0 | ACCDET_ADC_FORCE_EN | 0: Normal 1: Force adc_en |
| ACCDET_THRESH1 | 0x76 | 7:0 | lat_rw | 0x00 | ACCDET_JACK_THR1 | 3/4 pole jack detection threshold for 1 bit ADC |
| ACCDET_THRESH2 | 0x77 | 7:0 | lat_rw | 0x00 | ACCDET_JACK_THR2 | 3/4 pole jack detection threshold for 8 bit ADC |
| ACCDET_THRESH3 | 0x78 | 7:0 | lat_rw | 0x00 | ACCDET_BTN_THR1 | Button detection threshold for 1 bit ADC |
| ACCDET_THRESH4 | 0x79 | 7:0 | lat_rw | 0x00 | ACCDET_BTN_THR2 | Button detection threshold for 1 bit ADC |

B.13 Speaker THD/Power Limiter

Table 245: Speaker THD/Power Limiter Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|---------------|------|-----|--------|---------|----------------------|---|
| LIMITER_CTRL1 | 0x88 | 2:0 | lat_rw | 0b000 | SP_PWR_THD_ATK_RATE | SP amplifier power/THD limit attack rate: 000 = 30 μ s/dB 001 = 60 μ s/dB 010 = 120 μ s /dB 011 = 250 μ s/dB 100 = 500 μ s/dB 101 = 1 ms/dB 110 = 2 ms/dB 111 = TBD |
| | | 5:3 | lat_rw | 0b000 | SP_PWR_THD_REL_RATE | SP amplifier power/THD limiter release rate: 000 = 20 ms/dB 001 = 50 ms/dB 010 = 100 ms/dB 011 = 200 ms/dB 100 = 400 ms/dB 101 = 700 ms/dB 110 = 1000 ms/dB 111 = 30 μ s/dB |
| | | 7:6 | lat_rw | 0b0 | SP_PWR_THD_HOLD_TIME | 0 = 30 μ s 1 = 500 ms 2 = 1 s 3 = 2 s |
| LIMITER_CTRL2 | 0x89 | 0 | lat_rw | 0b0 | SP_PWR_EN | The power limiter limits the peak power that can be transmitted to the Speaker/Headphone driver. Designed for maximizing power output |
| | | 1 | lat_rw | 0b0 | SP_THD_EN | Non-Clip Enable: Non-clip limit tracks supply voltage. As battery starts to droop the limit will be reduced. The limiter is designed to maximize THD with a failing battery |
| | | 2 | lat_rw | 0b0 | SP_PWR_HYST_DIS | 0 = Normal Operation 1 = Remove hysteresis from Power Limiter |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|-----------------|------|-----|--------|---------|--------------------------|--|
| | | 3 | lat_rw | 0b0 | SP_THD_HYST_DIS | 0 = Normal Operation 1 = Remove hysteresis from Non-Clip Limiter |
| | | 6:4 | lat_rw | 0b000 | SP_LIM_FINE_GAIN_FRC_VAL | The PGA fine gain value when sp_pwr_lim_fine_gain_frc_en is high |
| | | 7 | lat_rw | 0b0 | SP_LIM_FINE_GAIN_FRC_EN | Override Fine Gain calculated by the limiter 0 = fine_gain_tx uses the gain calculated by the limiter 1 = fine_gain_tx uses the value in sp_pwr_limit_fine_gain_frc_val register |
| LIMITER_PWR_LIM | 0x8a | 5:0 | lat_rw | 0b0 | SP_PWR_LIM | Speaker Power Limits Setting |
| LIMITER_THD_LIM | 0x8b | 5:0 | lat_rw | 0b0 | SP_THD_LIM | Speaker THDS Limits Setting 000000 : No Clipping 000001 : 000010 : 000011 : ... 111111 : 20 % |
| NG_CTRL1 | 0x8c | 1:0 | lat_rw | 0b00 | SP_NG_ATT | 00: -24 dB 01: -24 dB 10: -24 dB 11: -12 dB |
| | | 7 | lat_rw | 0b0 | SP_NG_EN | Noise gate enable |
| NG_CTRL2 | 0x8d | 2:0 | lat_rw | 0b000 | SP_ATK_RATE | SP noise gate attack time |
| | | 5:3 | lat_rw | 0b000 | SP_REL_RATE | SP noise gate release time |
| | | 7:6 | lat_rw | 0b00 | SP_HLD_TIME | SP noise gate hold time |

System PMIC for Dual/Quad-Core Processors

B.14 AUX Input

Table 246: AUX Input Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------------|------|-----|-------------|----------|-----------------------|---|
| AUX_L_CTRL | 0x90 | 3:2 | lat_rw | 0b01 | AUX_L_AMP_ZC_SEL | Selects where the zero cross detection on the AUX_L input is measured: 0 = Input of AUX_L amplifier 1 = input of AUX_L amplifier if gain <= 4.5 dB otherwise on the output 2 = Neither (no zero cross possible) 3 = Output of AUX_L amplifier |
| | | 4 | lat_rw | 0b0 | AUX_L_AMP_ZC_EN | AUX_L amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | AUX_L_AMP_RAMP_EN | AUX_L amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | AUX_L_AMP_MUTE_EN | AUX_L amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | AUX_L_AMP_EN | AUX_L amplifier enable: 0 = disable 1 = enable |
| AUX_L_GAIN | 0x91 | 5:0 | lat_rw | 0b110101 | AUX_L_AMP_GAIN | 00000 = 010001 = -54 dB 010010 = -52.5 dB 110101 = 0 dB 111111 = +15 dB |
| AUX_L_GAIN_STATUS | 0x92 | 5:0 | dat_ro_data | 0b000000 | AUX_L_AMP_GAIN_STATUS | Contains the presently active gain setting. See AUX_L_GAIN register for values. |
| AUX_R_CTRL | 0x93 | 3:2 | lat_rw | 0b01 | AUX_R_AMP_ZC_SEL | Selects where the zero cross detection on the AUX_R input is measured: 0 = Input of AUX_R amplifier 1 = input of AUX_R amplifier if gain <= 4.5 dB otherwise on the output 2 = Neither (no zero cross possible) 3 = Output of AUX_R amplifier |
| | | 4 | lat_rw | 0b0 | AUX_R_AMP_ZC_EN | AUX_R amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | AUX_R_AMP_RAMP_EN | AUX_R amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | AUX_R_AMP_MUTE_EN | AUX_R amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------------|------|-----|-------------|----------|-----------------------|---|
| | | 7 | lat_rw | 0b0 | AUX_R_AMP_EN | AUX_R amplifier enable: 0 = disable 1 = enable |
| AUX_R_GAIN | 0x94 | 5:0 | lat_rw | 0b110101 | AUX_R_AMP_GAIN | 000000 = 010001 = -54 dB 010010 = -52.5 dB 110101 = 0 dB 111111 = +15 dB |
| AUX_R_GAIN_STATUS | 0x95 | 5:0 | dat_ro_data | 0b000000 | AUX_R_AMP_GAIN_STATUS | Contains the presently active gain setting. See AUX_R_GAIN register for values. |

B.15 MIC Input

Table 247: MIC Input Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------------|------|-----|-------------|---------|-----------------------|---|
| MIC_L_CTRL | 0x98 | 3:2 | lat_rw | 0b00 | MIC_L_AMP_IN_SEL | MIC1_P/N input source select: 00 = differential 01 = MIC1_P single-ended 10 = MIC1_N single-ended 11 = reserved |
| | | 6 | lat_rw | 0b1 | MIC_L_AMP_MUTE_EN | MIC1 amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | MIC_L_AMP_EN | MIC1 amplifier enable: 0 = disable 1 = enable |
| MIC_L_GAIN | 0x99 | 2:0 | lat_rw | 0b001 | MIC_L_AMP_GAIN | 000 = -6 dB 001 = 0 dB 010 = 6 dB ... 111 = 36 dB |
| MIC_L_GAIN_STATUS | 0x9a | 2:0 | dat_ro_data | 0b001 | MIC_L_AMP_GAIN_STATUS | Contains the presently active gain setting. See MIC_L_GAIN register for values. |
| MIC_R_CTRL | 0x9b | 3:2 | lat_rw | 0b00 | MIC_R_AMP_IN_SEL | MIC2_P/N input source select: 00 = differential 01 = MIC2_P single-ended 10 = MIC2_N single-ended 11 = reserved |
| | | 6 | lat_rw | 0b1 | MIC_R_AMP_MUTE_EN | MIC2 amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | MIC_R_AMP_EN | MIC2 amplifier enable: 0 = disable 1 = enable |

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| Register | Addr | Bit | Type | Default | Field | Description |
|---------------------|------|-----|-------------|---------|-------------------------|---|
| MIC_R_GAIN | 0x9c | 2:0 | lat_rw | 0b001 | MIC_R_AMP_GAIN | 000 = -6 dB 001 = 0 dB 010 = 6 dB ... 111 = 36 dB |
| MIC_R_GAIN_STATUS | 0x9d | 2:0 | dat_ro_data | 0b001 | MIC_R_AMP_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |
| MIC_EXT_CTRL | 0x9e | 3:2 | lat_rw | 0b00 | MIC_EXT_AMP_IN_SEL | MIC3_P/N input source select: 00 = differential 01 = MIC3_P single-ended 10 = MIC3_N single-ended 11 = reserved |
| | | | lat_rw | 0b1 | MIC_EXT_AMP_MUTE_EN | MIC3 amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | MIC_EXT_AMP_EN | MIC3 amplifier enable: 0 = disable 1 = enable |
| MIC_EXT_GAIN | 0x9f | 2:0 | lat_rw | 0b001 | MIC_EXT_AMP_GAIN | 000 = -6 dB 001 = 0 dB 010 = 6 dB ... 111 = 36 dB |
| MIC_EXT_GAIN_STATUS | 0xa0 | 2:0 | dat_ro_data | 0b001 | MIC_EXT_AMP_GAIN_STATUS | Contains the presently active gain setting. See MIC_EXT_GAIN register for values. |

B.16 MICBIAS

Table 248: MICBIAS Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|---------------|------|-----|------------|---------|----------------|---|
| MICBIAS1_CTRL | 0xa1 | 7 | lat_rw_otp | 0b0 | MICBIAS1_EN | Microphone bias1 enable: 0 = disable 1 = enable |
| MICBIAS2_CTRL | 0xa2 | 1:0 | lat_rw_otp | 0b01 | MICBIAS2_LEVEL | Microphone bias2 level: 0 = 1.6 V 1 = 2.2 V 2 = 2.5 V 3 = 3.0 V |
| | | 7 | lat_rw_otp | 0b0 | MICBIAS2_EN | Microphone bias2 enable: 0 = disable 1 = enable |
| MICBIAS3_CTRL | 0xa3 | 1:0 | lat_rw_otp | 0b01 | MICBIAS3_LEVEL | Microphone bias3 level: 0 = 1.6 V 1 = 2.2 V 2 = 2.5 V 3 = 3.0 V |

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| Register | Addr | Bit | Type | Default | Field | Description |
|----------|------|-----|------------|---------|-------------|---|
| | | 7 | lat_rw_otp | 0b0 | MICBIAS3_EN | Microphone bias3 enable: 0 = disable 1 = enable |

B.17 Input Mixers

Table 249: MIXIN Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|---------------------|------|-----|-------------|---------|-------------------------|--|
| MIXIN_L_CTRL | 0xa8 | 3 | lat_rw | 0b0 | MIXIN_L_MIX_EN | MIXIN_L mixer enable. When disabled all inputs are deselected: 0 = mixer disabled 1 = mixer enabled |
| | | 4 | lat_rw | 0b0 | MIXIN_L_AMP_ZC_EN | MIXIN_L amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | MIXIN_L_AMP_RAMP_EN | MIXIN_L amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | MIXIN_L_AMP_MUTE_EN | MIXIN_L amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | MIXIN_L_AMP_EN | MIXIN_L amplifier enable: 0 = amplifier disabled 1 = amplifier enabled |
| MIXIN_L_GAIN | 0xa9 | 3:0 | lat_rw | 0b0011 | MIXIN_L_AMP_GAIN | 0000 = -4.5 dB 0001 = -3 dB 0010 = -1.5 dB 1111 = 18.0 dB |
| MIXIN_L_GAIN_STATUS | 0xaa | 3:0 | dat_ro_data | 0b0000 | MIXIN_L_AMP_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |
| MIXIN_L_SELECT | 0xab | 4:0 | lat_rw | 0b00000 | MIXIN_L_MIX_SELECT | MIXIN_L mixer inputs: [0] = AUX_L [1] = MIC_L [2] = MIC_R [3] = MIC_EXT [4] = reserved |
| | | 7 | lat_rw | 0b0 | DMIC_L_EN | Enable the left dmic input: 0 = disabled 1 = enabled |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|---------------------|------|-----|-------------|---------|-------------------------|--|
| MIXIN_R_CTRL | 0xac | 3 | lat_rw | 0b0 | MIXIN_R_MIX_EN | MIXIN_R mixer enable. When disabled all inputs are deselected: 0 = mixer disabled 1 = mixer enabled |
| | | 4 | lat_rw | 0b0 | MIXIN_R_AMP_ZERO_EN | MIXIN_R amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | MIXIN_R_AMP_RAMP_EN | MIXIN_R amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | MIXIN_R_AMP_MUTE_EN | MIXIN_R amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | MIXIN_R_AMP_ENABLE | MIXIN_R amplifier enable: 0 = amplifier disabled 1 = amplifier enabled |
| MIXIN_R_GAIN | 0xad | 3:0 | lat_rw | 0b0011 | MIXIN_R_AMP_GAIN | 0000 = -4.5 dB 0001 = -3 dB 0010 = -1.5 dB 1111 = 18.0 dB |
| MIXIN_R_GAIN_STATUS | 0xae | 3:0 | dat_ro_data | 0b0000 | MIXIN_R_AMP_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |
| MIXIN_R_SELECT | 0xaf | 4:0 | lat_rw | 0b00000 | MIXIN_R_MIX_SELECT | MIXIN_R mixer inputs: bit 0 = AUX_R bit 1 = MIC_R bit 2 = MIC_L bit 3 = MIC_EXT bit 4 = MIXIN_L |
| | | 6 | lat_rw | 0b0 | MIC_BIAS_OUTPUT_SELECT | Selects which of the two MICBIAS pins acts as the bias source: 0 = MICBIAS1 1 = MICBIAS2 |
| | | 7 | lat_rw | 0b0 | DMIC_R_EN | Enable the right dmic input: 0 = disabled 1 = enabled |

System PMIC for Dual/Quad-Core Processors

B.18 ADC

Table 250: ADC Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------------|------|-----|-------------|---------|---------------------------|---|
| ADC_L_CTRL | 0xb4 | 5 | lat_rw | 0b0 | ADC_L_RAMP_EN | ADC_L digital gain ramping enable. 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | ADC_L_MUTE_EN | ADC_L mute enable: 0 = ADC_L unmuted 1 = ADC_L muted |
| | | 7 | lat_rw | 0b0 | ADC_L_EN | ADC_L enable: 0 = ADC_L disabled 1 = ADC_L enabled |
| ADC_L_GAIN | 0xb5 | 6:0 | lat_rw | 0x6f | ADC_L_DIGITAL_GAIN | ADC_L digital gain: 00 = -83.25 dB ... 6F = 0 dB ... FE = 11.25 dB FF = 12 dB |
| ADC_L_GAIN_STATUS | 0xb6 | 6:0 | dat_ro_data | 0x00 | ADC_L_DIGITAL_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |
| ADC_R_CTRL | 0xb8 | 5 | lat_rw | 0b0 | ADC_R_RAMP_EN | ADC_R digital gain ramping enable. 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | ADC_R_MUTE_EN | ADC_R mute enable: 0 = ADC_R unmuted 1 = ADC_R muted |
| | | 7 | lat_rw | 0b0 | ADC_R_EN | ADC_R enable: 0 = ADC_R disabled 1 = ADC_R enabled |
| ADC_R_GAIN | 0xb9 | 6:0 | lat_rw | 0x6f | ADC_R_DIGITAL_GAIN | ADC_R digital gain: 00 = -83.25 dB ... 6F = 0 dB ... FE = 11.25 dB FF = 12 dB |
| ADC_R_GAIN_STATUS | 0xba | 6:0 | dat_ro_data | 0x00 | ADC_R_DIGITAL_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |

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B.19 DAC

Table 251: DAC Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-------------------|------|-----|-------------|---------|---------------------------|--|
| DAC_L_CTRL | 0xbc | 5 | lat_rw | 0b0 | DAC_L_RAMP_EN | DAC_L digital gain ramping enable. 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | DAC_L_MUTE_EN | DAC_L mute enable: 0 = DAC_L unmuted 1 = DAC_L muted |
| | | 7 | lat_rw | 0b0 | DAC_L_ENABLE | DAC_L enable: 0 = DAC_L disabled 1 = DAC_L enabled |
| DAC_L_GAIN_AIN | 0xbd | 6:0 | lat_rw | 0x6F | DAC_L_DIGITAL_GAIN | DAC_L digital gain: 00 = 07 = mute 08 = -78 dB ... 6F = 0 dB ... FE = 11.25 dB FF = 12 dB |
| DAC_L_GAIN_STATUS | 0xbe | 6:0 | dat_ro_data | 0x00 | DAC_L_DIGITAL_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |
| DAC_R_CTRL | 0xbf | 5 | lat_rw | 0b0 | DAC_R_RAMP_EN | DAC_R digital gain ramping enable. 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | DAC_R_MUTE_EN | DAC_R mute enable: 0 = DAC_R unmuted 1 = DAC_R muted |
| | | 7 | lat_rw | 0b0 | DAC_R_ENABLE | DAC_R enable: 0 = DAC_R disabled 1 = DAC_R enabled |
| DAC_R_GAIN_AIN | 0xc0 | 6:0 | lat_rw | 0x6F | DAC_R_DIGITAL_GAIN | DAC_R digital gain: 00 = 07 = mute 08 = -78 dB ... 6F = 0 dB ... FE = 11.25 dB FF = 12 dB |
| DAC_R_GAIN_STATUS | 0xc1 | 6:0 | dat_ro_data | 0x00 | DAC_R_DIGITAL_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |

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B.20 Output Mixers

Table 252: MIXOUT Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-----------------|------|-----|--------|---------|----------------------|---|
| MIXOUT_L_CTRL | 0xc4 | 3 | lat_rw | 0b0 | MIXOUT_L_MIX_EN | MIXOUT_L mixer enable. When disabled all inputs are deselected: 0 = mixer disabled 1 = mixer enabled |
| | | 4 | lat_rw | 0b1 | MIXOUT_L_SOFTMIX_EN | MIXOUT_L soft mixing enable: 0 = disabled 1 = enabled |
| | | 7 | lat_rw | 0b0 | MIXOUT_L_AMP_EN | MIXOUT_L mixer amp enable: 0 = disabled 1 = enabled |
| MIXOUT_L_SELECT | 0xc5 | 6:0 | lat_rw | 0x00 | MIXOUT_L_MIX_SELECT | Output mixer left channel selection, [0] => aux_l, [1] => mixin_l, [2] => mixin_r, [3] => dac_l [4] => aux_l inverted, [5] => mixin_l inverted, [6] => mixin_r inverted |
| MIXOUT_R_CTRL | 0xc6 | 3 | lat_rw | 0b0 | MIXOUT_R_MIX_EN | MIXOUT_R mixer enable. When disabled all inputs are deselected: 0 = mixer disabled 1 = mixer enabled |
| | | 4 | lat_rw | 0b1 | MIXOUT_R_SOFTMIX_EN | MIXOUT_R soft mixing enable: 0 = disabled 1 = enabled |
| | | 7 | lat_rw | 0b0 | MIXOUT_R_AMP_EN | MIXOUT_R mixer amp enable: 0 = disabled 1 = enabled |
| MIXOUT_R_SELECT | 0xc7 | 6:0 | lat_rw | 0x00 | MIXOUT_R_MIX_SELECT | Output mixer right channel selection, [0] => aux_r, [1] => mixin_r, [2] => mixin_l, [3] => dac_r [4] => aux_r inverted, [5] => mixin_r inverted, [6] => mixin_l inverted |
| MIXOUT_SP_CTRL | 0xc8 | 3 | lat_rw | 0b0 | MIXOUT_SP_MIX_EN | MIXOUT_SP mixer enable. When disabled all inputs are deselected: 0 = mixer disabled 1 = mixer enabled |
| | | 4 | lat_rw | 0b1 | MIXOUT_SP_SOFTMIX_EN | MIXOUT_SP soft mixing enable: 0 = disabled 1 = enabled |
| | | 7 | lat_rw | 0b0 | MIXOUT_SP_AMP_EN | MIXOUT_SP mixer amp enable: 0 = disabled 1 = enabled |

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| Register | Addr | Bit | Type | Default | Field | Description |
|----------------------|------|-----|--------|---------|--------------------------|--|
| MIXOUT_S P_SELECT | 0xc9 | 6:0 | lat_rw | 0x00 | MIXOUT_SP_ MIX_SELECT | MIXOUT_SP channel selection, [0] => aux_r, [1] => mixin_r, [2] => mixin_l, [3] => dac_r [4] => aux_r inverted, [5] => mixin_r inverted, [6] => mixin_r inverted |

B.21 Headphones

Table 253: Headphone Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|-----------|------|-----|--------|---------------|------------------------------|--|
| HP_L_CTRL | 0xcc | 2 | lat_rw | 0b0 | HP_L_AMP_ MIN_GAIN_ EN | HP_L amplifiers gain held at the minimum value: 0 = Normal gain operation 1 = Minimum gain only |
| | | 3 | lat_rw | 0b0 | HP_L_AMP_ OE | HP_L amplifier output enable: 0 = output is high impedance 1 = output is driven |
| | | 4 | lat_rw | 0b0 | HP_L_AMP_ ZC_EN | HP_L amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | HP_L_AMP_ RAMP_EN | HP_L amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | HP_L_AMP_ MUTE_EN | HP_L amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | HP_L_AMP_ EN | HP_L amplifier enable: 0 = amplifier disabled 1 = amplifier enabled |
| HP_L_GAIN | 0xcd | 6:0 | lat_rw | 0b11100 10 | HP_L_AMP_ GAIN | HP_L_GAIN -> Sets the gain level for the left headphone channel: 00-03 = -56.0 dB 04-07 = -54.0 dB ... 60-63 = -26.0 dB 64-65 = -24.0 dB 66-67 = -23.0 dB 68-69 = -22.0 dB ... 98-99 = -7.0 dB 100 = -6 dB 101 = -5.5 dB 102 = -5.0 dB ... 112 = 0.0 dB ... 123 = 5.5 dB 124-127 = 6.0 dB |

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| Register | Addr | Bit | Type | Default | Field | Description |
|------------------|------|-----|-------------|-----------|-----------------------|--|
| HP_L_GAIN_STATUS | 0xce | 6:0 | dat_ro_data | 0b000000 | HP_L_AMP_GAIN_STAT_US | Contains the presently active gain setting. See previous register for values. |
| HP_R_CTRL | 0xcf | 2 | lat_rw | 0b0 | HP_R_AMP_MIN_GAIN_EN | HP_R amplifiers gain held at the minimum value: 0 = Normal gain operation 1 = Minimum gain only |
| | | 3 | lat_rw | 0b0 | HP_R_AMP_OE | HP_R amplifier output enable: 0 = output is high impedance 1 = output is driven |
| | | 4 | lat_rw | 0b0 | HP_R_AMP_ZC_EN | HP_R amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | HP_R_AMP_RAMP_EN | HP_R amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | HP_R_AMP_MUTE_EN | HP_R amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | HP_R_AMP_EN | HP_R amplifier enable: 0 = amplifier disabled 1 = amplifier enabled |
| HP_R_GAIN | 0xd0 | 6:0 | lat_rw | 0b1110010 | HP_R_AMP_GAIN | HP_R_GAIN -> Sets the gain level for the left headphone channel: 00 to 03 = -56.0 dB 04 to 07 = -54.0 dB ... 60 to 63 = -26.0 dB 64 to 65 = -24.0 dB 66 to 67 = -23.0 dB 68 to 69 = -22.0 dB ... 98 to 99 = -7.0 dB 100 = -6 dB 101 = -5.5 dB 102 = -5.0 dB ... 112 = 0.0 dB ... 123 = 5.5 dB 124 to 127 = 6.0 dB |
| HP_R_GAIN_STATUS | 0xd1 | 6:0 | dat_ro_data | 0b000000 | HP_R_AMP_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |
| HP_TEST | 0xd2 | 0 | lat_rw_otp | 0b0 | HP_AMP_EMS_EN | EMS additional components enable: 0 = Disabled 1 = Enabled |

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B.22 Earpiece

Table 254: Earpiece Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|----------------|------|-----|-------------|-----------|--------------------|--|
| EP_CTRL | 0xd4 | 1:0 | lat_rw_otp | 0b00 | EP_AMP_BIAS | TBD |
| | | 2 | lat_rw | 0b0 | EP_AMP_MIN_GAIN_EN | EP amplifier gain held at the minimum value: 0 = Normal gain operation 1 = Minimum gain only |
| | | 3 | lat_rw | 0b0 | EP_AMP_OE | EP amplifier output enable: 0 = output is high impedance 1 = output is driven |
| | | 4 | lat_rw | 0b0 | EP_AMP_ZC_EN | EP amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | EP_AMP_RAM_P_EN | EP amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped between |
| | | 6 | lat_rw | 0b1 | EP_AMP_MUTE_EN | EP amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | EP_AMP_EN | EP amplifier enable: 0 = amplifier disabled 1 = amplifier enabled |
| EP_GAIN | 0xd5 | 6:0 | lat_rw | 0b1110010 | EP_AMP_GAIN | EP_GAIN -> Sets the gain level for the left headphone channel: 00 to 03 = -56.0 dB 04 to 07 = -54.0 dB ... 60 to 63 = -26.0 dB 64 to 65 = -24.0 dB 66 to 67 = -23.0 dB 68 to 69 = -22.0 dB ... 98 to 99 = -7.0 dB 100 = -6 dB 101 = -5.5 dB 102 = -5.0 dB ... 112 = 0.0 dB ... 123 = 5.5 dB 124 to 127 = 6.0 dB |
| EP_GAIN_STATUS | 0xd6 | 6:0 | dat_ro_data | 0b0000000 | EP_AMP_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |

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B.23 Speakers

Table 255: Speaker Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|----------------|------|-----|-------------|----------|----------------------|---|
| SP_CTRL | 0xd8 | 2 | lat_rw | 0b0 | SP_AMP_MIN_GAIN_EN | SP amplifier gain held at the minimum value: 0 = Normal gain operation 1 = Minimum gain only |
| | | 4 | lat_rw | 0b0 | SP_AMP_ZERO_CROSS_EN | SP amplifier zero cross gain update mode enable: 0 = gain changes are instant 1 = gain changes are performed when the data crosses zero |
| | | 5 | lat_rw | 0b0 | SP_AMP_RAMPING_EN | SP amplifier gain ramping enable, this overrides zero crossing: 0 = gain changes are instant 1 = gain changes are ramped |
| | | 6 | lat_rw | 0b1 | SP_AMP_MUTE_EN | SP amplifier mute enable: 0 = amplifier unmuted 1 = amplifier muted |
| | | 7 | lat_rw | 0b0 | SP_AMP_ENABLE | SP amplifier enable: 0 = amplifier disabled 1 = amplifier enabled |
| SP_GAIN | 0xd9 | 5:0 | lat_rw | 0b110011 | SP_AMP_GAIN | 000000 = -24.0 dB 011010 = -24.0 dB 011011 = -24.0 dB 011100 = -23.0 dB ... 110011 = 0.0 dB ... 111111 = 12.0 dB |
| SP_GAIN_STATUS | 0xda | 5:0 | dat_ro_data | 0b000000 | SP_AMP_GAIN_STATUS | Contains the presently active gain setting. See previous register for values. |
| SP_CFG1 | 0xdb | 7:0 | lat_rw | 0x0 | SP_AMP_CONFIG1 | SP amplifier P drive RF control [0] = increased bias [1] = PWM deglitch disable [2] = ON_Sup_p [3] = Min_Drv_p_en [4] = LS_Drv_RT_p [5] = LS_Drv_FT_p [6] = HS_Drv_RT_p [7] = HS_Drv_FT_p |
| SP_CFG2 | 0xdc | 7:0 | lat_rw | 0x0 | SP_AMP_CONFIG2 | SP amplifier M drive RF control [1:0] = spare [2] = ON_Sup_m [3] = Min_Drv_m_en [4] = LS_Drv_RT_m [5] = LS_Drv_FT_m [6] = HS_Drv_RT_m [7] = HS_Drv_FT_m |

System PMIC for Dual/Quad-Core Processors

| Register | Addr | Bit | Type | Default | Field | Description |
|-----------|------|-----|-------------|---------|---------------|--|
| SP_STATUS | 0xde | 7:0 | dat_ro_data | 0x0 | SP_AMP_STATUS | SP amplifier status [0] = PWM oscillator OK [1] = HiZ flag [2] = overtemp [3] = overvoltage [4] = HiZ_HP [5] = HiZ_HM [7:6] = spare |

B.24 Voltage References

Table 256: References Registers

| Register | Addr | Bit | Type | Default | Field | Description |
|------------|------|-----|------------|---------|---------------------|--|
| REFERENCES | 0xe4 | 3 | lat_rw | 0b0 | BIAS_EN | master bias enable: 0 = master bias disabled 1 = master bias enabled |
| | | 4 | lat_rw | 0b0 | VMID_FAST_CHARGE | VMID reference fast charge enable: 0 = low noise slow charge mode 1 = high noise fast charge mode |
| | | 5 | lat_rw | 0b0 | VMID_FAST_DISCHARGE | VMID reference fast discharge enable: 0 = low noise slow discharge mode 1 = high noise fast discharge mode |
| | | 7 | lat_rw | 0b0 | VMID_EN | VMID reference enable: 0 = disabled 1 = enabled |
| IO_CTRL | 0xe5 | 0 | lat_rw_otp | 0b0 | IO_VOLTAGE_LEVEL | Digital I/O voltage range: 0 = 1.2 V to 2.8 V 1 = 2.5 V to 3.6 V |
| LDO_CTRL | 0xe6 | 5:4 | lat_rw_otp | 0b00 | LDO_LEVEL_SELECT | Audio sub-system digital LDO level select: 0 = 1.05 V 1 = 1.10 V 2 = 1.20 V 3 = 1.40 V |
| | | 7 | lat_rw_otp | 0b0 | LDO_EN | Audio sub-system digital LDO control. The master bias must be enabled for the LDO to operate: 0 = LDO bypassed (digital operates from LDO5) 1 = LDO active |

System PMIC for Dual/Quad-Core Processors

Status Definitions

| Revision | Datasheet Status | Product Status | Definition |
|----------|------------------|----------------|--|
| 1.<n> | Target | Development | This datasheet contains the design specifications for product development. Specifications may be changed in any manner without notice. |
| 2.<n> | Preliminary | Qualification | This datasheet contains the specifications and preliminary characterization data for products in pre-production. Specifications may be changed at any time without notice in order to improve the design. |
| 3.<n> | Final | Production | This datasheet contains the final specifications for products in volume production. The specifications may be changed at any time in order to improve the design, manufacturing and supply. Major specification changes are communicated via Customer Product Notifications. Datasheet changes are communicated via www.dialog-semiconductor.com . |
| 4.<n> | Obsolete | Archived | This datasheet contains the specifications for discontinued products. The information is provided for reference only. |

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System PMIC for Dual/Quad-Core Processors

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