D2-3(S) Audio SOC

Intelligent Digital Amplifier and Sound Processor

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The D2-3(S) family (D2-92633-LR, D2-92634-LR, D2-92643-LR, D2-92683-QR, D2-92684-QR) of the D2-3 and D2-3S Digital Audio Processor devices are complete System on Chip (SoC) multi-channel digital sound processors and Class-D amplifier controllers.

The integrated DSP provides efficient and configurable audio signal path processing including equalization, dynamic range compression, mixing, and filtering that is completely configurable using the D2 Audio Customization GUI v3 high level programming interface. The integrated PWM engine supports programmable and dynamic control of audio output, enabling a variety of multi-channel output configurations and output power capacity. Internal noise shaping, an embedded asynchronous sample rate converter, dynamic level-dependent timing, and high resolution operation support power stage audio performances with SNR >110dB and THD+N <0.01%.

The D2-3(S) devices are provided in two package and feature configurations which include the 128 Ld D2-3 family and the 72-pin D2-3S family. Both the D2-3 and D2-3S family provide identical performance and enable an extremely flexible platform for feature rich and cost-affordable quality audio solutions, which benefit from the addition of Class-D amplifiers and DSP audio processing.

The 12 integrated digital PWM controllers can be used in a variety of multi-channel audio system configurations, supporting powered as well as line outputs. Fully protected amplifier control provides efficient and clean Class-D power output support.

Applications

- DTV and Blu-ray Soundbar
- DVD and Blu-ray Home Theater Systems
- Home Theater in a Box (HTiB)
- Audio Video Receiver (AVR)
- Multi-Channel Multi-Media (MM) Systems
- Multi-Room Distributed Audio (MRDA)
- Powered speaker systems
- Automotive trunk/amplified solutions

Features

- Advanced D2-3 family Digital Audio Processor IC family
  - D2-3 family pin compatible and function/feature compatible with the D2 Audio DSP D2-6 device family
  - D2-3S family - identical D2-3 family performance, in a 72 Ld QFN package
- Integrated Digital Sound Processing (DSP)
  - Customizable audio path sound processing
  - Fully configurable and routable audio signal paths and hardware function assignment
  - Fully supported with the D2 Audio Customization GUI v3 Design Tool
- Flexible audio input and output configurations
  - 12 independent PWM engine channels
  - Four independent asynchronous I^2S digital inputs
  - Integrated high-performance stereo ADC (D2-3 family only)
  - S/PDIF™ digital audio inputs supporting linear IEC-61958 PCM or compressed IEC-61937 audio
  - S/PDIF digital audio PCM output
- Embedded 8-channel sample rate converter
- Real-time amplifier control and monitoring
  - Supports bridged, half-bridged, and Bridge-Tied Load (BTL) topologies, using discrete or integrated power stages
  - Complete fault protection with automatic recovery
- D2 Audio DSP Sound Enhancement Algorithms and virtualization
- Enhanced audio processing decoders and virtualization
  - Dolby® Digital/AC3

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Ordering Information

PART NUMBER (Notes 3, 4)	DEVICE FAMILY	PART MARKING	AUDIO PROCESSING FEATURE SET SUPPORT (Note 1)	PACKAGE (RoHS Compliant)	PKG. DWG. #	CARRIER TYPE (Note 2)	TEMP. RANGE (°C)
D2-92633-LR	D2-3	D2-92633-LR	See Table 1	128 Ld LQFP	Q128.14x14	Tray	-10 to +85
D2-92634-LR	D2-3	D2-92634-LR					
D2-92643-LR	D2-3	D2-92643-LR					-40 to +125
D2-92683-QR	D2-3S	D2-92683-QR		72 Ld QFN	L72.10x10F	Tube	-10 to +85
D2-92683-QR-T	D2-3S					3k	
D2-92684-QR	D2-3S	D2-92684-QR				Tube	
D2-92684-QR-T	D2-3S					3k	

NOTES:

1. The D2-3(S) devices support multiple audio processing algorithms and decoders, and support is device-dependent. See Table 1 on page 5 for the supported features for each device part number.
2. See TB347 for details about reel specifications.
3. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). The Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), see the D2-92633, D2-92634, D2-92643, D2-92683, D2-92684 device pages. For more information on MSL, see TB363.

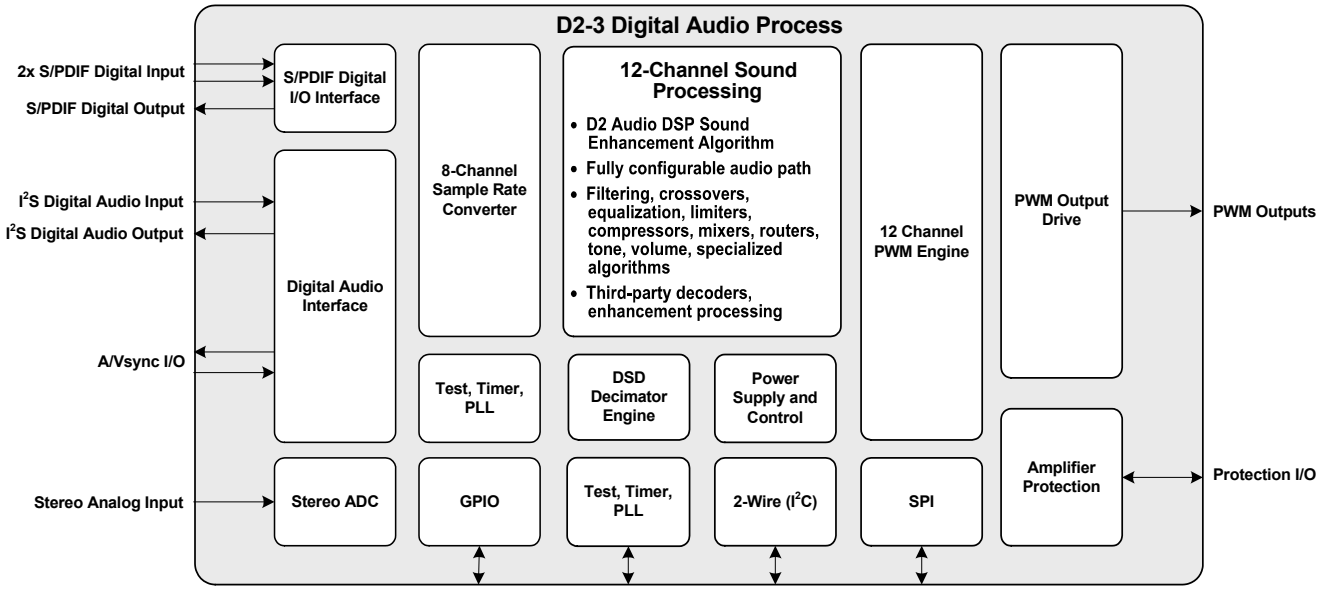


FIGURE 1. D2-3 DIGITAL AUDIO PROCESSOR

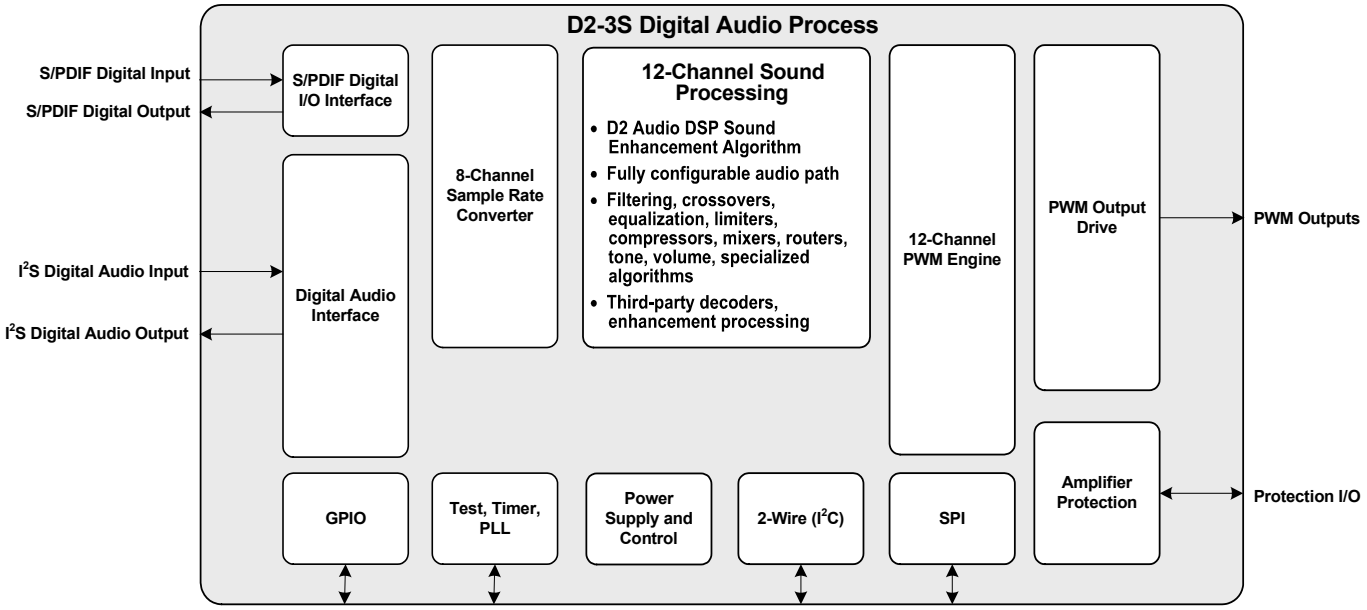


FIGURE 2. D2-3S DIGITAL AUDIO PROCESSOR

D2-3 Family Device Feature Set Offering

The D2-3(S) family has specific part numbers to specify the features and algorithms supported in the device. All devices of the D2-3 family include eight audio input processing channels, up to 12 PWM output channels, an embedded 8-channel Sample Rate Converter (SRC), and are fully supported with the D2 Audio Customization GUI v3 design tool software. Additional features within each D2-3 family part number are shown in Table 1.

TABLE 1. D2-3 DEVICE PART NUMBERS AND FEATURES

PART NUMBER	FAMILY	FEATURES	LICENSED ALGORITHM SUPPORT (Note 5)
D2-92633-LR	D2-3 128 Ld Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs 8 Channels of I^2S or Left Justified Serial Digital Audio Outputs 2 S/PDIF Digital Inputs 1 S/PDIF Digital Output 2 ADC Analog Audio Inputs	D2 Audio DSP Sound Enhancement Algorithms
D2-92634-LR	D2-3 128 Ld Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs 8 Channels of I^2S or Left Justified Serial Digital Audio Outputs 2 S/PDIF Digital Inputs 1 S/PDIF Digital Output 2 ADC Analog Audio Inputs	D2 Audio DSP Sound Enhancement Dolby Digital/AC3 Decoder
D2-92643-LR	D2-3 128 Ld Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs 8 Channels of I^2S or Left Justified Serial Digital Audio Outputs 2 S/PDIF Digital Inputs 1 S/PDIF Digital Output 2 ADC Analog Audio Inputs	D2 Audio DSP Sound Enhancement Algorithms
D2-92683-QR	D2-3S 72 Ld Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs, or 6 Channels of I^2S or Left Justified Serial Digital Audio Inputs plus 2 Channels of I^2S or Left Justified Serial Digital Audio Outputs 1 S/PDIF Digital Input 1 S/PDIF Digital Output	D2 Audio DSP Sound Enhancement
D2-92684-QR	D2-3S 72 Ld Package	8 Channels of I^2S or Left Justified Serial Digital Audio Inputs, or 6 Channels of I^2S or Left Justified Serial Digital Audio Inputs plus 2 Channels of I^2S or Left Justified Serial Digital Audio Outputs 1 S/PDIF Digital Input 1 S/PDIF Digital Output	D2 Audio DSP Sound Enhancement Dolby Digital/AC3 Decoder

NOTE:

5. D2 Audio DSP Sound Enhancements are included with all D2-3 family devices with no additional licensing or royalties required. The D2-92634-LR and D2-92684-QR devices include Dolby Digital support and a third party license is required for these products.

Device Designations

This datasheet applies to the D2-3 device family, which includes both the D2-3 and D2-3S. Functional specifications apply to both designations of this family unless otherwise indicated.

Throughout this document the device names apply to all part numbers of their respective names as follows:

DEVICE NAME	DEVICE PART NUMBERS	PACKAGE PINS
D2-3	D2-92633-LR, D2-92634-LR, D2-92643-LR	128 Ld Package
D2-3S	D2-92683-QR, D2-92684-QR	72 Ld Package

Absolute Maximum Ratings (Note 10)

Supply Voltage
- RVDD, PWMVDD, ADCVDD ..... -0.3V to 4.0V
- CVDD, PLLVDD ..... -0.3V to 2.4V

Input Voltage
- Any Input but XTALI .....-0.3V to RVDD +0.3V
- XTALI .....-0.3V to PLLVDD +0.3V

Input Current, Any Pin but Supplies ..... ±10mA

ESD Rating
- Human Body Model (Tested per JESD22-A114F)..... 2kV
- Machine Model (Tested per JESD22-A115C) 200V
- Charged Device Model (Tested per JESD22-C101E) 750V

Latch-Up
- (Pins 2, 4, 6, 7, 8, 9, 37 (72 Ld Package only)
- Tested per JESD78D, Class II, Level B) 50mA
- (All Other Pins Tested per JESD78D Class II, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
128 Ld LQFP Package (Notes 6, 8)	39	6.5
72 Ld QFN Package (Notes 7, 9)	22	0.80

Maximum Storage Temperature ..... -55°C to +150°C

Pb-Free Reflow Profile ..... see TB493

Recommended Operating Conditions

Temperature Range .....-10°C to +85°C

Temperature Range (D2-92643) .....-40°C to +125°C

Digital I/O Supply Voltage, PWMVDD 3.3V

Core Supply Voltage, CVDD 1.8V

Analog Supply Voltage, PLLVDD 1.8V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
7. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board with direct attach of exposed pad to PCB.
8. For θ_{JC}, the “case temp” location is taken at the package top center.
9. For θ_{JC}, the “case temp” is measured on bottom of exposed pad.
10. Absolute Maximum parameters are not tested in production.

Electrical Specifications

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Digital Input High Logic Level (Note 11)	V_{IH}	Relative to RVDD	2.0	-	-	V
Digital Input Low Logic Level (Note 11)	V_{IL}	Relative to RVDD	-	-	0.8	V
High Level Output Drive Voltage I_{OUT} at - Pin Drive Strength Current. See “Pin Description, D2-3 Family (128 Ld)” on page 13, and “Pin Description D2-3S Family (72 Ld)” on page 18	V_{OH}		RVDD - 0.4	-	-	V
Low Level Output Drive Voltage I_{OUT} at + Pin Drive Strength Current. See “Pin Description, D2-3 Family (128 Ld)” on page 13, and “Pin Description D2-3S Family (72 Ld)” on page 18	V_{OL}		-	-	0.4	V
High Level Input Drive Voltage XTALI Pin	VIHX		0.7	-	PLLVDD	V
Low Level Input Drive Voltage XTALI Pin	VILX		-	-	0.3	V
Input Leakage Current (Note 12)	I_{IN}		-	-	±10	µA
Input Capacitance	C_{IN}		-	9	-	pF
High Level Output Drive Voltage OSCOUT Pin	VOHO		PLLVDD - 0.3	-	-	V
Low Level Output Drive Voltage OSCOUT Pin	VOLO		-	-	0.3	V
Output Capacitance	C_{OUT}		-	9	-	pF
nRESET Pulse Width	t_{RST}		-	10	-	ns
Typical Digital I/O Pad Ring Supply (Voltage)	R_{VDD}		3.0	3.3	3.6	V
(Current, Active)			-	10	-	mA
(Current, Power-Down)			-	<1	-	mA
Typical PWM I/O Pad Ring Supply (Voltage)	PWM_{VDD}		3.0	3.3	3.6	V
(Current, Active)			-	5	-	mA
(Current, Power-Down)			-	<1	-	mA

Electrical Specifications T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Typical Core Supply (Voltage)	CVDD		1.7	1.8	1.9	V
(Current, Active)			-	300	-	mA
(Current, Power-Down)			-	15	-	mA
Typical PLL Analog Supply (Voltage)	PLLVDD		1.7	1.8	1.9	V
(Current, Active)			-	25	-	mA
(Current, Power-Down)			-	10	-	mA
Typical ADC Analog Supply (Voltage)	ADCVDD		3.0	3.3	3.6	V
(Current, Active, Power-Down)			-	12	-	mA
CRYSTAL OSCILLATOR						
Crystal Frequency (Fundamental Mode Crystal)	Xo		20	24.576	24.822 (24.576+1%)	MHz
Duty Cycle	Dt		40	-	60	%
Start-Up Time (Start-Up Time is Oscillator Enabled (with Valid Supply) to Stable Oscillation)	t_{START}		-	5	20	ms
PLL						
VCO Frequency	F_{VCO}		80.00	294.912	297.86	MHz
Input Reference Frequency	F_{IN}		20	-	24.822 (24.576+1%)	MHz
Feedback Dividers (Integer)			4	12	15	
PLL Lock Time from any Input Change			-	2	-	ms
1.8V POWER-ON RESET						
Reset Enabled Voltage Level	V_{EN}		0.9	1.1	1.4	V
POR Pulse Width Rejection (Note 14)	t_{REJ}		-	150	500	µs
POR Minimum Output Pulse Width	t_{DIS}		-	5	-	µs
1.8V BROWNOUT DETECTION						
Detect Level			1.4	1.5	1.6	V
Pulse Width Rejection	t_{BOD1}			100	-	ns
Minimum Output Pulse Width	t_{O1}		20	-	-	ns
3.3V BROWNOUT DETECTION						
Detect Level			2.5	2.7	2.9	V
Pulse Width Rejection	t_{BOD3}			100	-	ns
Minimum Output Pulse Width	t_{O3}		20	-	-	ns
ADC PERFORMANCE SPECIFICATIONS (D2-3 only)						
ADCREF DC Level	V_{REF}		1.3	1.4	1.5	V
ADCREF Load Current	I_{REF}		-	-	±20	µA
Analog Input Level	V_{AIN}		V_{REF} - 0.6	-	V_{REF} + 0.6	V
ADC Dynamic Range and SNR (Note 15) (ADC + ADC Decimator performance only, DSP inactive, no digital audio processing, PWM outputs off, no pPWM switching)		1.0V_{P-P} 1kHz sine wave input reference level, using firmware from D2 Audio Customization GUI v3 rev 3.1.4 or newer.	-	94	-	dB
ADC Dynamic Range and SNR (Note 15) (DSP active and processing audio data, PWM active and driving audio outputs, measurements using typical system-level amplifier equivalent as measurement environment)			-	83	-	dB

Electrical Specifications

T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground. PLL at 294.912MHz, OSC at 24.576MHz, core running at 147.456MHz with typical audio data traffic. Minimum supply currents are measured in full power down configuration. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
THD+N			-	-80	-	dB
Gain Mismatch			-	0.1	-	dB
Crosstalk			-	-80	-	dB
Power Supply Rejection			-	-70	-	dB

NOTES:

11. All input pins except XTALI.
12. Input leakage applies to all pins except XTALO.
13. Power-down is with device in reset and clocks stopped.
14. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
15. Analog performance is system-design dependent and is affected by factors that include PCB layout, shielding and routing of analog traces, additional components within the analog input path, and power supply isolation.

Serial Audio Interface Port Timing

(Figure 3) T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

DESCRIPTION	SYMBOL	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
SCKRx Frequency - SCKR0, SCKR1	tc_{SCLK}			12.5	MHz
SCKRx Pulse Width (High and Low) - SCKR0, SCKR1	tw_{SCLK}	40			ns
LRCKRx Set-Up to SCLK Rising - LRCKR0, LRCKR1	ts_{LRCLK}	20			ns
LRCKRx Hold from SCLK Rising - LRCKR0, LRCKR1	th_{LRCLK}	20			ns
SDINx Set-Up to SCLK Rising - SDIN0, SDIN1	ts_{SDI}	20			ns
SDINx Hold from SCLK Rising - SDIN0, SDIN1	th_{SDI}	20			ns
SDOUTx Delay from SCLK Falling	t_{dSDO}			20	ns

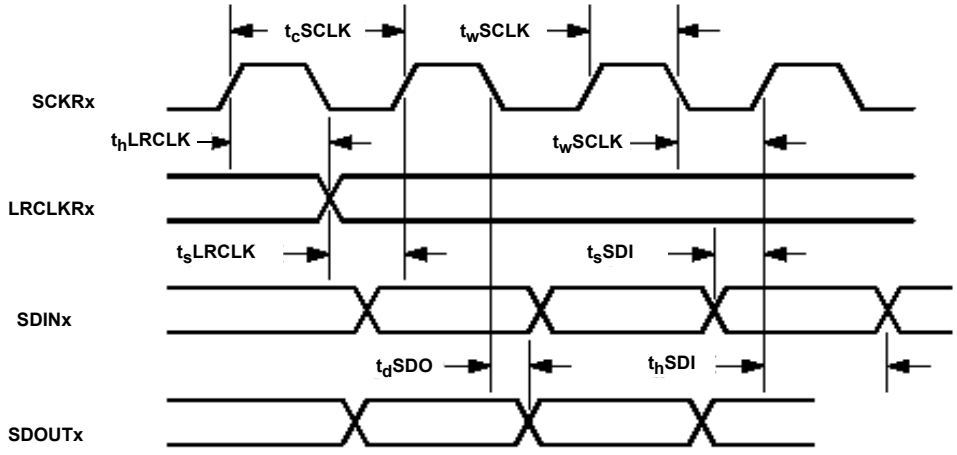


FIGURE 3. SERIAL AUDIO INTERFACE PORT TIMING

Two-Wire (I^2C) Interface Port Timing

(Figure 4) T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN (Note 14)	MAX (Note 14)	UNIT
f_{SCL}	SCL Frequency		100	kHz
t_{buf}	Bus Free Time Between Transmissions	4.7		µs
$tw_{lowSCLx}$	SCL Clock Low	4.7		µs
$tw_{highSCLx}$	SCL Clock High	4.0		µs
ts_{STA}	Set-Up Time For a (Repeated) Start	4.7		µs
th_{STA}	Start Condition Hold Time	4.0		µs
th_{SDAx}	SDA Hold From SCL Falling (Note 16)	0		µs
ts_{SDAx}	SDA Set-Up Time to SCL Rising	250		ns
td_{SDAx}	SDA Output Delay Time From SCL Falling		3.5	µs
t_r	Rise Time of Both SDA and SCL		1	µs
t_f	Fall Time of Both SDA and SCL		300	ns
ts_{STO}	Set-Up Time For a Stop Condition	4.7		µs

NOTE:

16. Data must be held sufficient time to bridge the 300ns transition time of SCL.

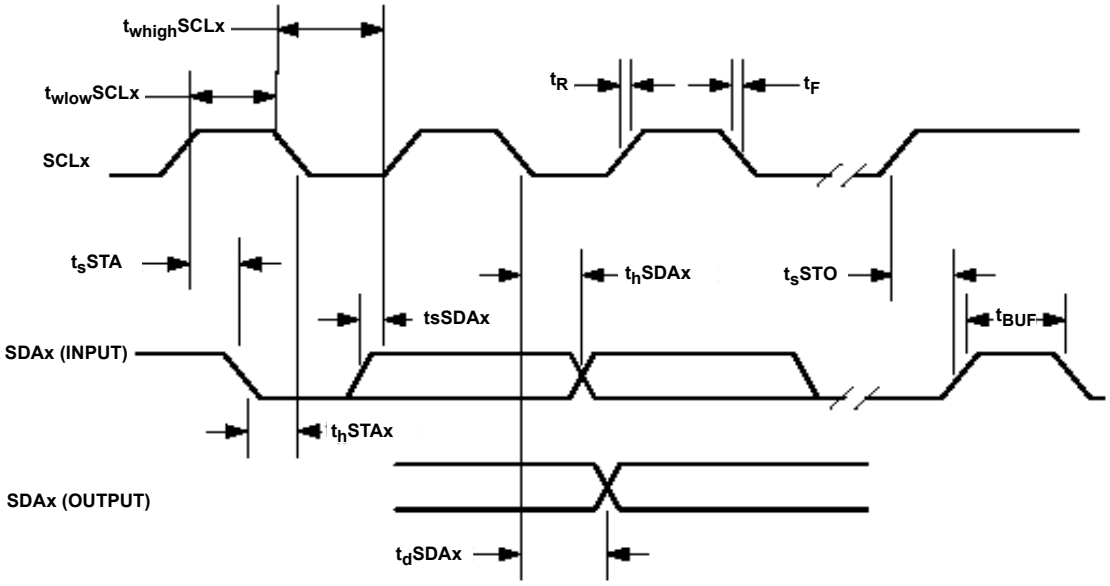


FIGURE 4. I^2C INTERFACE TIMING

SPI™ Interface Port Timing

(Figure 5) T_A = +25°C, CVDD = PLLVDD = 1.8V ±5%, RVDD = PWMVDD = 3.3V ±10%. All grounds at 0.0V. All voltages referenced to ground.

SYMBOL	DESCRIPTION	MIN (Note 14)	MAX (Note 14)	UNIT
SPI MASTER MODE TIMING				
t_V	MOSI Valid From Clock Edge		8	ns
t_S	MISO Set-Up to Clock Edge	2		ns
t_H	MISO Hold From Clock Edge	2		ns
t_{WI}	nCS Minimum Width	3		3 system clocks + 2ns
SPI SLAVE MODE TIMING				
t_V	MISO Valid From Clock Edge		8	ns
t_S	MOSI Set-Up to Clock Edge	2		ns
t_H	MOSI Hold From Clock Edge	2		ns
t_{WI}	nCS Minimum Width	3		3 system clocks + 2ns

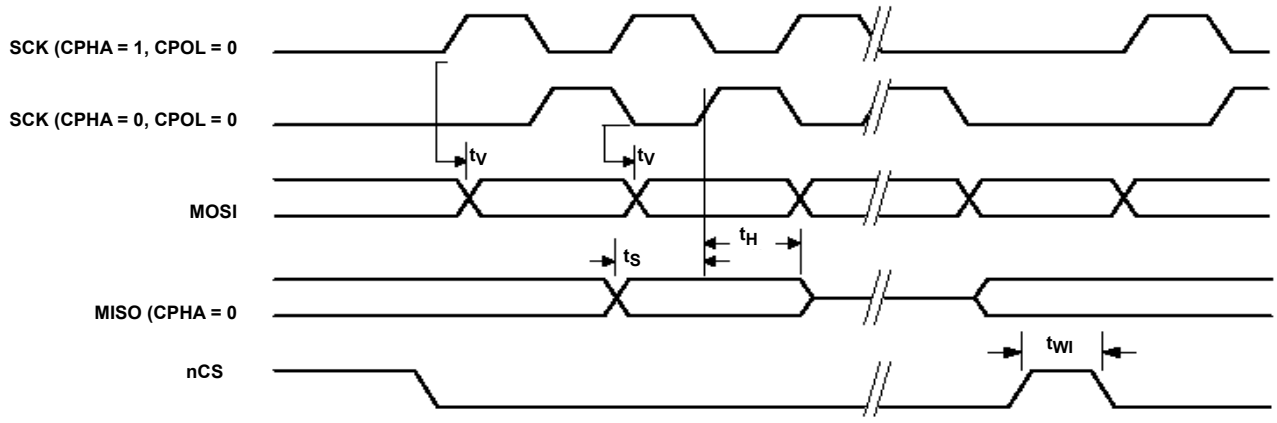
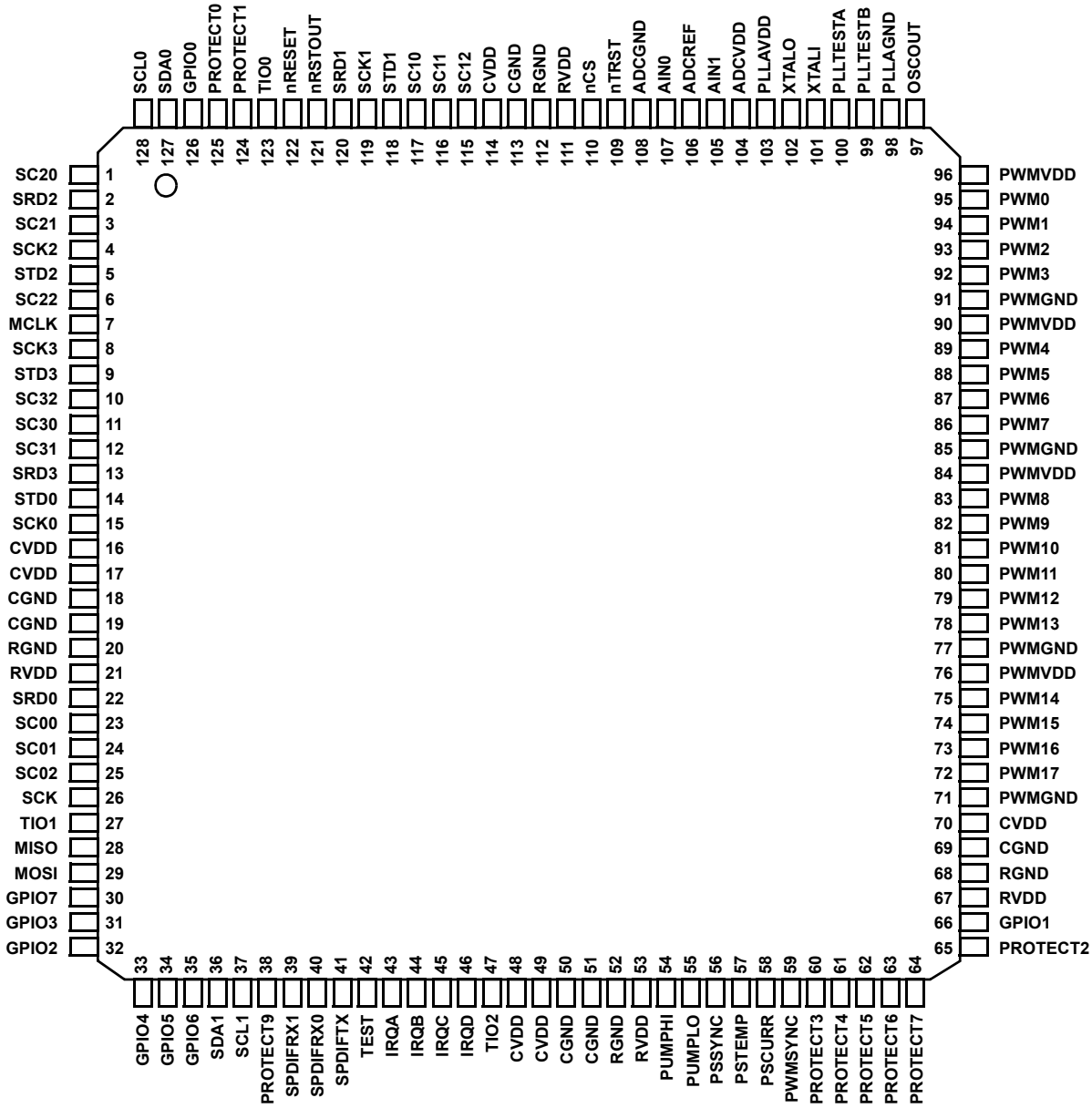


FIGURE 5. SPI TIMING

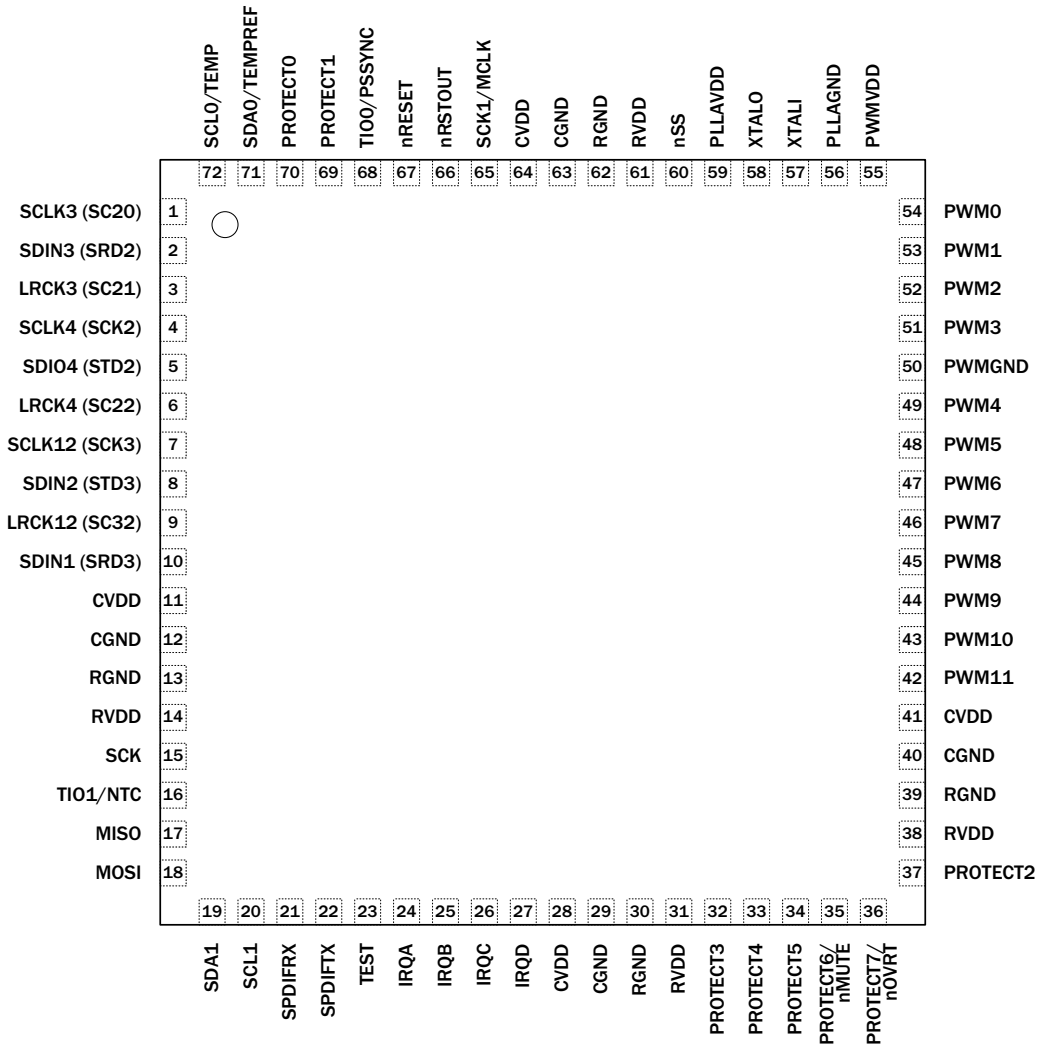
Pin Configuration D2-3 Family (128 Ld Package)

D2-92633, D2-92634, D2-92643
(128 LD LQFP)
TOP VIEW



Pin Configuration D2-3S Family (72 Ld Package)

D2-92683, D2-92684
(72 LD QFN)
TOP VIEW



NOTE:

17. All pins pass JEDEC II 100mA at +85°C, with exception of pins 2, 4, 6, 7, 8, 9, 37, which pass 50mA at +85°C.

Pin Description, D2-3 Family (128 Ld)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
1	SC20	I/O	3.3	8	Serial Audio Interface 2, I^2S0 SCLK
2	SRD2	I/O	3.3	4	Serial Audio Interface 2, I^2S0 SDIN
3	SC21	I/O	3.3	8	Serial Audio Interface 2, I^2S0 LRCK
4	SCK2	I/O	3.3	8	Serial Audio Interface 2, I^2S1 SCLK
5	STD2	I/O	3.3	8	Serial Audio Interface 2, I^2S1 SDIN
6	SC22	I/O	3.3	4	Serial Audio Interface 2, I^2S1 LRCK
7	MCLK	O	3.3	16	I^2S Serial Audio Master Clock output for external ADC/DAC components, drives low on reset and is enabled by firmware assignment.
8	SCK3	I/O	3.3	8	Serial Audio Interface 3, I^2S3 SCLK
9	STD3	I/O	3.3	8	Serial Audio Interface 3, I^2S3 SDIN
10	SC32	I/O	3.3	8	Serial Audio Interface 3, I^2S3 LRCK
11	SC30	I/O	3.3	8	Serial Audio Interface 3, I^2S2 SCLK
12	SC31	I/O	3.3	8	Serial Audio Interface 3, I^2S2 LRCK
13	SRD3	I/O	3.3	4	Serial Audio Interface 3, I^2S2 SDIN
14	STD0	I/O	3.3	8	Serial Audio Interface 0, I^2S SDAT0
15	SCK0	I/O	3.3	8	Serial Audio Interface 0, I^2S LRCK0
16	CVDD	P	3.3		Core power, 1.8V
17	CVDD	P	3.3		Core power, 1.8V
18	CGND	P	3.3		Core ground
19	CGND	P	3.3		Core ground
20	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
21	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
22	SRD0	I/O	3.3	4	Serial Audio Interface 0, SDIO, Defaults to input, and can be configured as GPIO by firmware.
23	SC00	I/O	3.3	8	Serial Audio Interface 0, SDIO, Defaults to input, and can be configured as GPIO by firmware.
24	SC01	I/O	3.3	8	Serial Audio Interface 0, I^2S SDAT1
25	SC02	I/O	3.3	8	Serial Audio Interface 0, I^2S LRCK1
26	SCK	I/O	3.3	4	SPI clock I/O with hysteresis input.
27	TIO1	I/O	3.3	16	Timer I/O Port 1. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
28	MISO	I/O	3.3	4	SPI master input, slave output data signal.
29	MOSI	I/O	3.3	4	SPI master output, slave input data signal.
30	GPIO7	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
31	GPIO3	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
32	GPIO2	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
33	GPIO4	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)

Pin Description, D2-3 Family (128 Ld) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
34	GPIO5	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
35	GPIO6	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
36	SDA1	I/O	3.3	8 - OD	Two-Wire Serial data Port 1. Bidirectional signal used by both the master and slave controllers for data transport.
37	SCL1	I/O	3.3	8 - OD	Two-Wire Serial clock Port 1. Bidirectional signal is used by both the master and slave controllers for clock signaling.
38	PROTECT9	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
39	SPDIFRX1	I	3.3		S/PDIF Digital audio data input 1
40	SPDIFRX0	I	3.3		S/PDIF Digital audio data input 0
41	SPDIFTX	O	3.3	4	S/PDIF Digital audio output. (Audio content and audio processing signal flow is dependent upon firmware, driving stereo output up to 192kHz.)
42	TEST	I	3.3		Factory test use only. Must be tied low.
43	IRQA	I	3.3		Interrupt request Port A, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.
44	IRQB	I	3.3		Interrupt request Port B, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.
45	IRQC	I	3.3		Interrupt request Port C, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.
46	IRQD	I	3.3		Interrupt request Port D, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.
47	TIO2	I/O	3.3	16	Timer I/O Port 2. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
48	CVDD	P	3.3		Core power, 1.8V
49	CVDD	P	3.3		Core power, 1.8V
50	CGND	P	3.3		Core ground
51	CGND	P	3.3		Core ground
52	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
53	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
54	PUMPHI	I/O	3.3	16	Assignable I/O. Function and operation defined by firmware.
55	PUMPLO	I/O	3.3	16	Assignable I/O. Function and operation defined by firmware.
56	PSSYNC	I/O	3.3	16	Synchronizing output signal to switching power supply. (Operates under specification of firmware and resets to high impedance inactive state when not used.)
57	PSTEMP	I/O	3.3	4	Assignable I/O. Function and operation defined by firmware.
58	PSCURR	I/O	3.3	4	Assignable I/O. Function and operation defined by firmware.
59	PWMSYNC	I/O	3.3	16	PWM synchronization port. (Function and operation is defined by firmware.)
60	PROTECT3	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)

Pin Description, D2-3 Family (128 Ld) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
61	PROTECT4	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
62	PROTECT5	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
63	PROTECT6	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
64	PROTECT7	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
65	PROTECT2	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
66	GPIO1	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
67	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
68	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
69	CGND	P	3.3		Core ground
70	CVDD	P	3.3		Core power, 1.8V
71	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
72	PWM17	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
73	PWM16	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
74	PWM15	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
75	PWM14	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
76	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
77	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
78	PWM13	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
79	PWM12	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
80	PWM11	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
81	PWM10	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
82	PWM9	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
83	PWM8	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
84	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
85	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
86	PWM7	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)

Pin Description, D2-3 Family (128 Ld) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
87	PWM6	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
88	PWM5	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
89	PWM4	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
90	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
91	PWMGND	P	3.3		PWM output pin ground. Internally connected to RGND.
92	PWM3	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
93	PWM2	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
94	PWM1	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
95	PWM0	I/O	3.3	8 or 16	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)
96	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
97	OSCOUT	P	1.8		Analog oscillator output to slave D2-3(S) devices. OSCOUT drives a buffered version of the crystal oscillator signal from the XTALI pin.
98	PLLAGND	P	1.8		PLL Analog ground
99	PLLTESTB	O	1.8		Factory test use only. Must be tied low.
100	PLLTESTA	O	1.8		Factory test use only. Must be tied low.
101	XTALI	P	1.8		Crystal oscillator analog input port. An external clock source would be driven into the this port. In multi-D2-3(S) systems, the OSCOUT from the master D2-3(S) would drive the XTALI pin.
102	XTALO	P	1.8		Crystal oscillator analog output port. When using an external clock source, this pin must be open. XTALO does not have a drive strength specification.
103	PLLAVDD	P	1.8		PLL Analog power, 1.8V
104	ADCVDD	P	3.3		Analog power for internal ADC, 3.3V
105	AIN1	I	3.3		Analog input 1 to internal ADC
106	ADCREF	O	3.3		Analog voltage reference output. Must be decoupled to analog ground with 1µF capacitor.
107	AIN0	I	3.3		Analog input 0 to internal ADC
108	ADCGND	P	3.3		Analog ground for internal ADC
109	nTRST	I	3.3		Factory test only. Must be tied high at all times.
110	nCS	I/O	3.3	4	SPI slave select I/O.
111	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
112	RGND	P	3.3		Digital pad ring ground. Internally connected to PWMGND.
113	CGND	P	3.3		Core ground
114	CVDD	P	3.3		Core power, 1.8V
115	SC12	I/O	3.3	8	Serial Audio Interface 1, LRCK
116	SC11	I/O	3.3	8	Serial Audio Interface 1, SDAT3

Pin Description, D2-3 Family (128 Ld) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
117	SC10	I/O	3.3	8	Serial Audio Interface 1, data (assignment by firmware control.)
118	STD1	I/O	3.3	8	Serial Audio Interface 1, SDAT2
119	SCK1	I/O	3.3	8	Serial Audio Interface 1, SCK
120	SRD1	I/O	3.3	4	Serial Audio Interface 1, data (assignment by firmware control.)
121	nRSTOUT	O	3.3	16 - OD	Active low open-drain reset output. Pin drives low from POR generator, 3.3V brownout detector going active, or from 1.8V brownout detector going active. This output should be used to initiate a system reset to the nRESET pin upon brownout event detection.
122	nRESET	I	3.3		Active low reset input with hysteresis. Activates system level reset when pulled low, initializing all internal logic and program operations. System latches boot mode selection of the IRQ input pins on the rising edge.
123	TIO0	I/O	3.3	16	Timer I/O Port 0. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
124	PROTECT1	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
125	PROTECT0	I/O	3.3	4	PWM protection input with hysteresis. (One of nine protection inputs. Specific function and channel assignment is defined by firmware.)
126	GPIO0	I/O	3.3	16	General purpose I/O Bidirectional GPIO port. (One of eight GPIO. Resets to input port. Operation and assignment is defined by product application's firmware.)
127	SDA0	I/O	3.3	8 - OD	Two-Wire Serial data Port 0. Bidirectional signal used by both the master and slave controllers for data transport.
128	SCL0	I/O	3.3	8 - OD	Two-Wire Serial clock Port 0. Bidirectional signal is used by both the master and slave controllers for clock signaling.

NOTES:

18. Unless otherwise specified, all pin names are active high. Those that are active low have an “n” prefix.
19. All power and ground pins of same names are to be tied together to all other pins of their same name. (that is, CVDD pins to be tied together, CGND pins to be tied together, RVDD pins to be tied together, and RGND pins to be tied together.) CGND and RGND are to be tied together on board. RGND and PWMGND pins are also internally connected and are to be tied together.

Pin Description D2-3S Family (72 Ld)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
1	SCLK3 (SC20)	In	3.3	8	Bit clock, I2S Port 3, audio input channels 5-6. (I2S Port 3 is 1 of 3 input-only ports, providing channels 5-6 input audio content.)
2	SDIN3 (SRD2)	In	3.3	4	Audio data, I2S Port 3, audio input channels 5-6 (I2S Port 3 is 1 of 3 input-only ports, providing channels 5-6 input audio content.)
3	LRCK3 (SC21)	In	3.3	8	L/R clock, I2S Port 3, audio input channels 5-6 (I2S Port 3 is 1 of 3 input-only ports, providing channels 5-6 input audio content.)
4	SCLK4 (SCK2)	In	3.3	8	Bit clock, I2S Port 4, audio input channels 7-8, or audio output channels 1-2. (I2S Port 4 is either an I2S input port, or and I2S output port. Selection of input or output is defined by firmware. When used as input, Port 4 provides channel 7-8 input audio content. When used as an output, Port 4 provides the 2 channels of I2S output audio.)
5	SDIO4 (STD2)	I/O	3.3	8	Audio data, I2S Port 4, input channels 7-8, or output channels 1-2. (I2S Port 4 is either an I2S input port, or and I2S output port. Selection of input or output is defined by firmware. When used as input, Port 4 provides channel 7-8 input audio content. When used as an output, Port 4 provides the 2 channels of I2S output audio.)
6	LRCK4 (SC22)	In	3.3	4	L/R clock, I2S Port 4, audio input channels 7-8, or audio output channels 1-2. (I2S Port 4 is either an I2S input port, or and I2S output port. Selection of input or output is defined by firmware. When used as input, Port 4 provides channel 7-8 input audio content. When used as an output, Port 4 provides the 2 channels of I2S output audio.)
7	SCLK12 (SCK3)	In	3.3	8	Bit clock, I2S ports 1 and 2, audio input channels 1-4 (I2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
8	SDIN2 (STD3)	In	3.3	8	Audio data, I2S Port 2, audio input channels 3-4 (I2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
9	LRCK12 (SC32)	In	3.3	8	L/R clock, I2S ports 1 and 2, audio input channels 1-4 (I2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
10	SDIN1 (SRD3)	In	3.3	8	Audio data, I2S Port 1, audio input channels 1-2 (I2S ports 1 and 2 are 2 of the 3 input-only ports, providing channels 1-4 input audio content.)
11	CVDD	P	3.3		Core power, 1.8V
12	CGND	G	3.3		Core ground
13	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
14	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers, except for the analog pads. Internally connected to PWMVDD.
15	SCK	I/O	3.3	4	SPI clock I/O with hysteresis input.
16	TIO1/NTC	I/O	3.3	16	Timer I/O Port 1, or assignable NTC temperature sensing common I/O. Operation and assignment is controlled by firmware. Leave unconnected when not in use.
17	MISO	I/O	3.3	4	SPI master input, slave output data signal.
18	MOSI	I/O	3.3	4	SPI master output, slave input data signal.
19	SDA1	I/O	3.3	8 - OD	Two-Wire Serial (I2C) data Port 1. Primary control interface data signal used for device boot and control. Bidirectional port for both master and slave controllers operation.
20	SCL1	I/O	3.3	8 - OD	Two-Wire Serial (I2C) clock Port 1. Primary control interface clock signal used for device boot and control. Bidirectional port for both master and slave controllers operation.
21	SPDIFRX	In	3.3		S/PDIF Digital audio data input
22	SPDIFTX	O	3.3		S/PDIF Digital audio output. (Audio content and audio processing signal flow is dependent upon firmware, driving stereo output up to 192kHz.)
23	TEST	In	3.3		Factory test use only. Must be tied low.
24	IRQA	In	3.3		Interrupt request Port A, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.

Pin Description D2-3S Family (72 Ld) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
25	IRQB	In	3.3		Interrupt request Port B, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.
26	IRQC	In	3.3		Interrupt request Port C, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.
27	IRQD	In	3.3		Interrupt request Port D, Boot Mode Select. One of four IRQ pins. Connects to logic high (3.3V) or to ground and High/Low logic status establishes boot mode selection upon deassertion of reset (nRESET) cycle.
28	CVDD	P	3.3		Core power, 1.8V
29	CGND	G	3.3		Core ground
30	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
31	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers. Internally connected to PWMVDD.
32	PROTECT3	In	3.3	4	PWM protection input with hysteresis. (One of eight protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
33	PROTECT4	In	3.3	4	PWM protection input with hysteresis. (One of eight protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
34	PROTECT5	In	3.3	4	PWM protection input with hysteresis. (One of eight protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
35	PROTECT6 /nMUTE	I/O	3.3	4	PWM protection input with hysteresis, or optional mute output. (One of eight protection inputs. Specific function, channel assignment, and/or optional GPIO is defined by firmware.)
36	PROTECT7 /nOVRT	In	3.3	4	PWM protection input with hysteresis, or optional over-temperature monitor input. (One of eight protection inputs. Specific function, channel assignment, and/or optional GPIO is defined by firmware.)
37	PROTECT2	In	3.3	4	PWM protection input with hysteresis. (One of eight protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
38	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers. Internally connected to PWMVDD.
39	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
40	CGND	G	3.3		Core ground
41	CVDD	P	3.3		Core power, 1.8V
42	PWM11	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
43	PWM10	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
44	PWM9	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
45	PWM8	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
46	PWM7	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)

Pin Description D2-3S Family (72 Ld) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
47	PWM6	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
48	PWM5	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
49	PWM4	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
50	PWMGND	O	3.3		PWM output pin power ground
51	PWM3	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
52	PWM2	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
53	PWM1	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
54	PWM0	O	3.3	8 or 16	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)
55	PWMVDD	P	3.3		PWM output pin power. This 3.3V supply is used for the PWM pad drivers. Internally connected to RVDD.
56	PLLAGND	G	1.8		PLL Analog ground
57	XTALI	In	1.8		Crystal oscillator analog input port. When using an external clock source, the external clock is driven into the this port.
58	XTALO	O	1.8		Crystal oscillator analog output port. When using an external clock source, this pin must be open. XTALO does not have a drive strength specification.
59	PLLAVDD	P	1.8		PLL Analog power, 1.8V
60	nSS	O	3.3	4	SPI slave select I/O.
61	RVDD	P	3.3		Digital pad ring power, 3.3V. This 3.3V supply is used for all the digital I/O pad drivers and receivers. Internally connected to PWMVDD.
62	RGND	G	3.3		Digital pad ring ground. Internally connected to PWMGND.
63	CGND	G	3.3		Core ground
64	CVDD	P	3.3		Core power, 1.8V
65	SCK1 /MCLK	I/O	3.3	8	Assignable general purpose I/O, or MCLK output. Operation and assignment is controlled by firmware. Assigns as default output for MCLK when enabled through firmware.
66	nRSTOUT	O	3.3	16 - OD	Active low open drain reset output. Pin drives low from POR generator, 3.3V brownout detector going active, or from 1.8V brownout detector going active. This output should be used to initiate a system reset to the nRESET pin upon brownout event detection.
67	nRESET	In	3.3		Active low reset input with hysteresis. Activates system level reset when pulled low, initializing all internal logic and program operations. System latches boot mode selection of the IRQ input pins on the rising edge.
68	TIO0 /PSSYNC	I/O	3.3	16	Timer I/O Port 0, or power supply sync output. Operation and assignment is controlled by firmware. Leave unconnected when not in use.

Pin Description D2-3S Family (72 Ld) (Continued)

PIN	PIN NAME (Note 18)	TYPE	VOLTAGE LEVEL (V)	DRIVE STRENGTH (mA)	DESCRIPTION
69	PROTECT1	In	3.3	4	PWM protection input with hysteresis. (One of eight protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
70	PROTECT0	In	3.3	4	PWM protection input with hysteresis. (One of eight protection inputs. Specific function, channel assignment, and optional GPIO is defined by firmware.)
71	SDA0 /TEMPREF	I/O	3.3	8 - OD	Two-Wire Serial data Port 0, or assignable I/O. Available for NTC temperature sensing reference as assignable I/O. Function is assigned by firmware.
72	SCL0 /TEMP	I/O	3.3	8 - OD	Two-Wire Serial clock Port 0, assignable I/O. Available for NTC temperature sensing reference as assignable I/O. Function is assigned by firmware.

NOTES:

20. Unless otherwise specified, all pin names are active high. Those that are active low have an “n” prefix.
21. All power and ground pins of same names are to be tied together to all other pins of their same name. (that is, CVDD pins to be tied together, CGND pins to be tied together, RVDD pins to be tied together, and RGND pins to be tied together.) CGND and RGND are to be tied together on board. RGND and PWMGND pins are also internally connected and are to be tied together.

Functional Block Diagram - D2-3

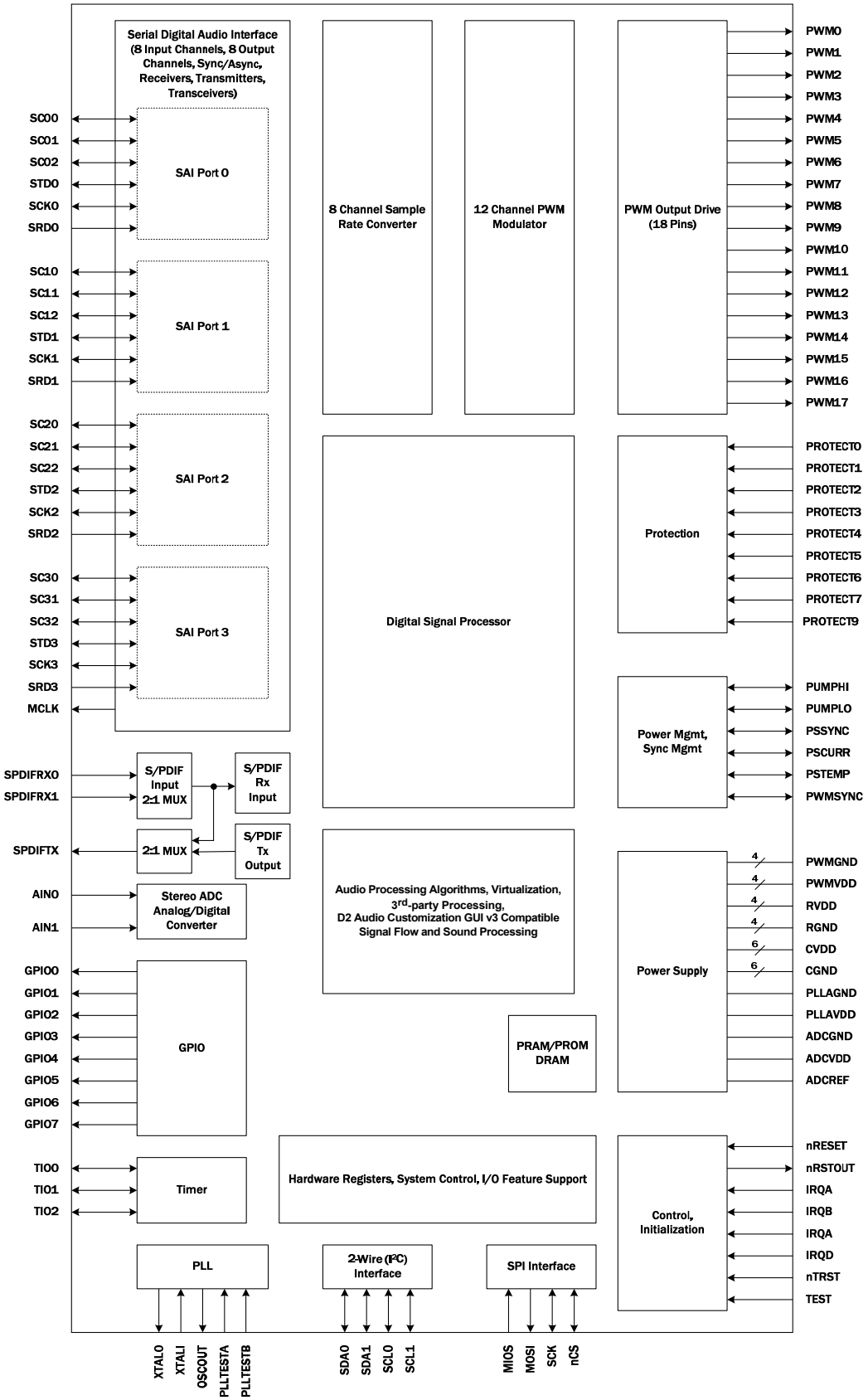


FIGURE 6. D2-3 IC FUNCTIONAL BLOCK DIAGRAM

Functional Block Diagram - D2-3S

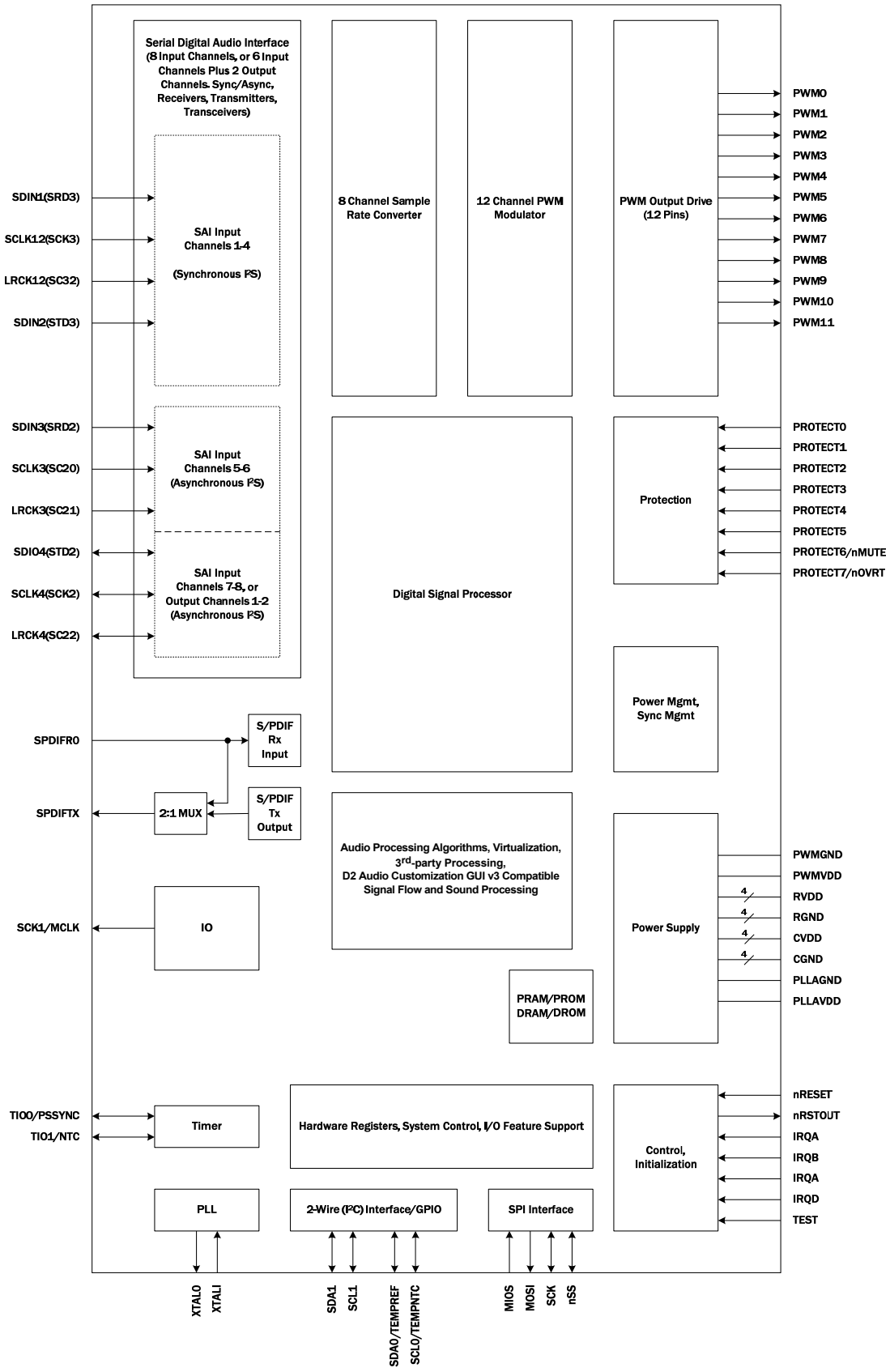


FIGURE 7. D2-3S IC FUNCTIONAL BLOCK DIAGRAM

Functional Description

Introduction

The D2-3 family of ICs provide the core functionality, amplifier control, and complete audio signal processing for D2 Audio DSP Class-D amplifier solutions. The devices are highly programmable with all system features and functionality totally defined by firmware, including complete definition of audio processing, signal flow, digital audio I/O, and amplifier hardware interface control.

The D2 Audio Customization GUI v3 software design tool supports building of the firmware for the D2-3 family devices. Using D2 Audio Customization GUI v3, the designer is able to fully define audio processing and hardware function features with I/O assignments, and build complete production-ready firmware for the D2-3 devices.

D2-3 DEVICE DESIGNATIONS

The D2-3 device family includes both the D2-3 and D2-3S ICs. Functional specifications are identical to both designations of this family unless otherwise indicated.

The family device names apply to these part numbers:

FAMILY DEVICE NAME	PART NUMBERS	PACKAGE PINS
D2-3	D2-92633-LR D2-92634-LR D2-92643-LR	128 Ld Package
D2-3S	D2-92683-QR D2-92684-QR	72 Ld Package

The D2-3 devices are completely pin-compatible with the D2-6 family devices, allowing full flexibility for function vs cost trade-off, providing cost-effective solutions for applications of varying end-user features and capabilities.

The D2-3S devices are identical to the D2-3 but are provided in a smaller 72 Ld package with features and I/O mapped to pins supported in that package.

D2 AUDIO CUSTOMIZATION GUI V3 SUPPORT

D2 Audio Customization GUI v3 is a powerful design tool that lets the designer define audio processing and build a signal flow customized to the user's specifications. It fully supports the D2-3 family including configuring the hardware I/O features and pin assignments. The designer can define the entire audio signal flow and architecture without signal flow limitations to any specific system. Capabilities include drag-and-drop of individual audio processing blocks that can be inserted into the signal flow, ability to connect and re-route signal flow, and live update capability to build and download the new audio architecture directly into the operating amplifier.

The D2-3 family of ICs supports a wide variety of signal flows and audio processing options that are fully programmable and are completely defined by the system firmware and system architecture.

The firmware is built by the D2 Audio Customization GUI v3 software, enabling full audio processing and amplifier hardware feature definition by the designer.

The D2-3 supports a Class-D amplifier system built around internal audio processing blocks and amplifier system hardware functions.

In addition to audio processing blocks and signal flow that are user-selectable, system functions of hardware are configurable that include PWM timing control, channel configuration and assignment, protection and monitoring features, clock configurations, and other audio system features. Choices and settings are defined using the D2 Audio Customization GUI v3 design tool software which builds the unique firmware for each particular system design.

DSP

The majority of the audio processing functions and hardware feature implementations operate through firmware running within the DSP core. The core is a 24-bit fixed-point Digital Signal Processor, with its own DMA, interrupt control, memory spaces, and control interfaces.

Sample Rate Converters (SRC)

The D2-3 family supports internal asynchronous sample rate conversion to align input audio streams to a single rate compatible with the DSP processing rate and PWM switch rate. The family has four independent rate estimators, allowing up to four asynchronous stereo inputs (eight channels) to be sample rate converted and processed simultaneously. The sample rate converter has a measured SNR that exceeds 140dB and a THD+N that exceeds -125dB.

Serial Digital Audio Interface

SERIAL DIGITAL AUDIO INPUTS

The D2-3 family includes four Serial Audio Interface (SAI) digital audio input ports supporting up to eight audio channels.

- The D2-3 supports four independent SAI ports. All four ports operate asynchronously to receive audio from four independent audio sources, and each of the four ports has its own clock and frame inputs. SAI Port 3 (the 4th port) of the D2-3 has multiplexed inputs to select that port's audio from the SAI input or from the on-chip ADC.
- The D2-3S devices support either four SAI input ports, or when its fourth port is used as an audio output, support three SAI input ports.

Each SAI port supports the digital audio industry I^2S standard which is capable of carrying up to 24-bit Linear PCM audio words per subframe IEC60958, or compressed digital audio (Dolby Digital, AAC, MPEG, etc.) packing per the IEC61937 specification. The SAI port also supports Left-Justified formatted Linear PCM or compressed digital audio. These ports support sample rates from 32kHz to 192kHz.

SAI data formats are shown in Figure 8 on page 25. For I2S format, the left channel data is read when LRCK is low. For the Left-Justified format, the left channel data is read when LRCK is high. Either format requires data to be valid on the rising edge of

SCLK and sent MSB-first on SDIN with 32 bits of data per channel. Each set of digital inputs runs asynchronously to the others and can accept different sample rates and formats.

Input audio can be received from the S/PDIF input for two audio input channels, concurrent with and asynchronous from audio that is also being presented to SAI inputs for other audio input channels. Routing through the SRC synchronizes this audio from multiple sources for synchronous audio processing within the D2-3 audio processing paths.

SERIAL DIGITAL AUDIO OUTPUTS

Up to four SAI ports (up to eight channels) are supported in the D2-3 families.

- The D2-3 supports four independent I^2S output ports for a total of eight channels of audio.
- the D2-3S supports 1 I^2S output port (two channels) and that port is configured to operate as either an input port or as an output port.

Use and channel assignment to the SAI outputs is configured using the D2 Audio Customization GUI v3 software. Any of the D2-3(S) device's 12 audio processing channels can be assigned to any of the available SAI output channels. D2 Audio Customization GUI v3 also assigns use of the fourth SAI port as in input or output for the D2-3S.

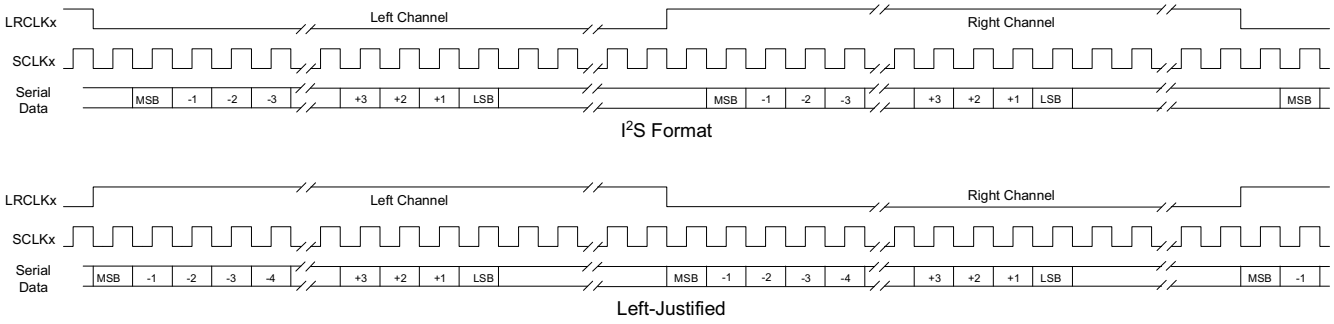


FIGURE 8. SAI PORT SUPPORTED DATA FORMATS FOR DELIVERY OF LINEAR PCM OR COMPRESSED AUDIO DATA

S/PDIF Digital Audio Interface

The device family includes an S/PDIF Digital receiver and transmitter.

- The D2-3 devices (128 pin packaged devices) include an on-chip multiplexer supporting switching of input from two different S/PDIF input pins. Input selection determines which pin routes to the S/PDIF receiver.
- The D2-3S devices (72 pin packaged devices) support one input pin only and do not use multiplex switching.

All of the devices in the family include a S/PDIF Digital transmitter.

S/PDIF RECEIVER

The S/PDIF receiver input pins are 3.3V CMOS input level compatible, requiring external circuitry to condition the serial input. The receiver contains an input transition detector, digital PLL clock recovery, and a decoder to separate audio, channel status, and user data. Only the first 24-channel status bits are supported. The receiver constantly monitors the incoming data stream to detect the IEC61937-1 packet headers, and if found, captures the Pc and Pd data words into registers. The receiver meets the jitter tolerance specified in IEC60958-4.

S/PDIF is typically used for receiving compressed (IEC61937-compliant) as well as stereo PCM (IEC60958-compliant) audio data. This interface also supports receipt of compressed audio data that is not compliant with the IEC61937 specification, but instead meets the IEC60958 specification.

S/PDIF receive data is routed through the SRC, providing a time synchronized audio input stream for use within any of the audio processing channels. Audio may be presented on the S/PDIF input asynchronous to audio also being presented to the I^2S Serial Digital inputs such that after routing through the SRC, are synchronous time aligned for internal audio processing.

S/PDIF TRANSMITTER

The transmitter complies with the consumer applications defined in IEC60958-3. The transmitter supports 24-bit audio data, 24-bit user data, and 30-bit channel status data. S/PDIF output is linear PCM only and is non-compressed. Routing of compressed audio that is presented to the inputs must be decoded by the D2-3 product and its firmware before the selected channels may be routed to the S/PDIF outputs.

Audio routing to the S/PDIF transmitter is defined by the signal flow built by the D2 Audio Customization GUI v3 software. That software supports assigning any of the audio processing channels to the two (L/R) channels of the S/PDIF output. Because all timing of the internal audio processing is synchronous to the internal DSP and processing channels, the S/PDIF audio output is also synchronous to that internal timing.

ADC input (D2-3 Devices Only)

The D2-3 devices contains a high-performance Analog-to-Digital Converter (ADC) that connects to input analog sources with a minimum of interface circuitry. The ADC is included in the D2-3 devices only. It is not supported in the D2-3S devices.

At a bandwidth of 20kHz at nominal voltage and temperature, the ADC input of the D2-3 provides a typical THD+N (unweighted) value of -81dB and a typical SNR/dynamic range of 83dB. These typical performances are based on a $1.0V_{P-P}$ 1kHz sine wave input reference level, using a representative system-level amplifier environment, processing digital audio data and producing PWM amplifier outputs.

Analog performance is affected by factors that include PCB layout, shielding and routing of analog traces, additional components within the analog input path, and proper power supply isolation techniques.

The ADC master clock is supplied from the low jitter PLL of the D2-3(S). The ADC operates synchronous to the DSP processing which minimizes noise pickup.

PWM Audio Amplifier Outputs

The D2-3 family devices include an integrated 12-channel PWM engine. Each engine is independently programmable for timing, output pin assignment, and audio processing path source.

PWM operation is defined by firmware. The D2 Audio Customization GUI v3 design tool provides the selection for audio channel assignment routing, protection enabling, timing, and PWM output pin mapping, then uses these selections to build the firmware that controls the PWM outputs. Some features such as dead-band timing are also adjustable in real-time through the control interface.

Programmability enables use of multiple PWM output topologies, which support system designs of a broad range of output stages. Output topologies include integrated power stages, or discrete implementations using N+N or P+N for half-bridge, full-bridge, or bridged-tied-load power stages. The PWM outputs can be used for powered outputs and can also be used for driving line-level or headphone outputs.

The 12 PWM channels are mapped to the PWM output pins by firmware register assignment. Both D2-3 and D2-3S include 12 PWM engines, and their available pins are:

- D2-3 - 18 assignable and mappable pins
- D2-3S- 12 assignable and mappable pins

Amplifier Protection

The core firmware that operates the D2-3 family devices supports protection options to prevent damage from faults present in class-D amplifier designs. This protection is also effective against user-induced faults such as clipping, output overload, or output shorts, including both shorted outputs or short-to-ground faults.

Protection features and their details are firmware dependent. The D2 Audio Customization GUI v3 program provides selection for assignment and use of certain protection methods, using the selections for building the system firmware.

GRACEFUL OVERCURRENT AND SHORT CIRCUIT

Per-channel PWM protection is supported through individual protection input pins. These PROTECT pins are primarily intended for protecting the PWM powered output stages and operation is firmware controlled. The protection input signal is typically generated by sensing circuits within power stages and can include sensing for detecting current, temperature, or voltage fault conditions.

Overcurrent sensing requires a current sensor in the power device to be protected, usually a powered PWM output. The typical sensor asserts its fault signal that is routed to the PROTECT pins of the device.

The D2-3(S) devices observe the overcurrent protection inputs and provide graceful protection for the assigned output stages. Hardware can be configured to provide immediate current reduction, cycle-by-cycle output clipping, output signal control, and output stage deactivation depending on the severity and duration of high current events. The combination of hardware features and firmware monitoring allows the system to differentiate between an overcurrent situation or a more serious short-circuit condition, and supports the managed protection within the amplifier systems.

THERMAL PROTECTION

Temperature monitoring can be used to provide warnings, shutdown, or managed output level reduction to attempt to reduce heating effects at high load power. Multiple thermal protection methods are supported within the D2-3 family firmware. User choice of method and operation is programmable, using the D2 Audio Customization GUI v3 software to configure settings and options.

Hardware I/O Features

The D2-3 and D2-3S provide programmable I/O pins used for various hardware functions of the system design. Pin functions are defined by the product firmware and configured with the D2 Audio Customization GUI v3 software.

GENERAL-PURPOSE I/O AND TIMERS

General Purpose I/O (GPIO) pins are available for system use with the D2-3 and are assignable by choice selection in the D2 Audio Customization GUI v3 software. The D2-3 supports pins assignable to various hardware features, while the D2-3S shares functions of some of its available device pins providing feature choices in a lower pin-count package.

Timers provide programmed I/O control of features that are event or timing dependent. Their hardware pins are assigned to system features, and operation is controlled through firmware. Timer pins are configurable based on the features supported within the system firmware. Choice and operation of their assigned features is selected through the D2 Audio Customization GUI v3 software that builds the firmware for the specific system project.

POWER SUPPLY SYNCHRONIZATION

The PSSYNC pin provides a power supply synchronization signal for switching power supplies. This synchronizing of power supply switching with the PWM switching rate eliminates audio output tones generated if the switching power supply is not locked to the amplifier switching.

Firmware settings configure PSSYNC to the desired frequency needed by the system switching regulator. The D2 Audio Customization GUI v3 software supports selection of use and frequency of this output.

Clocks and PLL

The PLL block operation is completely managed by the system firmware. The clock generation contains a low jitter PLL critical for low noise PWM output and a precise master clock source for the ADC, sample rate conversion, and the audio data paths.

The PLL block includes a low noise crystal oscillator, clock multipliers clock generation for all internal device timing, PWM engine timing, and clock reference for use with assignable clock outputs that include MCLK and PSSYNC outputs.

The system clock is provided by the crystal oscillator, using either a fundamental mode crystal or a clock input to the XTALI pin. If the clock input is used, it must be a 1.8V signal level. The input signal on the XTALI pin is analog buffered and driven onto the OSCOUT pin for use in driving the XTALI input of other D2-3(S) controllers, for supporting synchronous timing if multiple devices are used in a single application.

Reset and Initialization

The D2-3(S) must be reset after power-up to begin proper operation. In normal system hardware configurations, the reset occurs automatically through the reset hardware circuitry. The chip contains power rail sensors, brownout detectors, on the 3.3V and 1.8V power supplies. These brownout sensors will assert and hold an internal Power-on Reset which will disable the device until the power supplies are at a safe level for the DSP to start. These same brownout sensors will detect a power supply voltage droop while the system is active and provide a safe amplifier shutdown.

Power Sequencing

The CVDD and RVDD (including PWMVDD) supplies should be brought up together to avoid high current transients that could fold back a power supply regulator. The ADCVDD and PLLVDD can be brought up separately. The best practice would be for all supplies to feed from regulators with a common power source. Typically, this can be achieved by using a single 5V power source and regulating the 3.3V and 1.8V supplies from that 5V source.

Reset

D2-3(S) has one reset input: the nRESET pin. The nRESET input pin (active low, non-reset high) is effectively a power-on system reset. All internal state logic is initialized by nRESET. While reset is active, the system is held in the reset condition, which is defined as all internal reset signals being active, the crystal oscillator is running, and the PLL disabled. At the deassertion of nRESET, the chip will capture the boot mode selection from the IRQ[D:A] pins and begin the boot process.

The nRSTOUT pin is an active low open drain-reset output. This pin drives low from the internal power-on-reset generator, 3.3V brownout detector going active, or from the 1.8V brownout detector going active. This output should be used to initiate a system reset, and to also connect to the nRESET pin to initiate a reset upon brownout event detection.

Booting and Boot Modes

D2-3(S) includes a fully-programmable DSP with internal boot ROM. The boot ROM's primary function is to download a second-stage boot image from one of several possible sources.

The system requires external firmware to boot the internal DSP. Internal ROM within the D2-3 initiates the boot process to read the boot records and firmware, to load into the internal D2-3 memory. The boot ROM code is designed to handle both encrypted and non-encrypted boot images from any of the boot modes shown in Table 2.

The specific boot mode is selected based on the state of the IRQD, IRQC, IRQB, and IRQA pins at the time of reset deassertion. The mode is selected by a hardware pull-up or pull-down connection to each of the four boot mode (IRQ[D:A]) pins. (Modes not listed are reserved.)

Control Interfaces

I²C 2-WIRE INTERFACE

The D2-3(S) family ICs have two separate I²C 2-wire compatible ports. Port 1 is used as the external controller interface, and Port 0 is used for booting from an external EEPROMs or compatible chips. Both I²C interfaces are multi-master capable.

SERIAL PERIPHERAL INTERFACE (SPI)

The Serial Peripheral Interface (SPI) provides an alternate boot source interface such as an SPI Flash. The SPI port is used only for boot operation. Register control of the system firmware is not implemented through the SPI interface.

TABLE 2. BOOT MODES

MODE	IRQ[D:A]	M/S	XTALI RANGE	INTERFACE SPEED	DESCRIPTION
0	0000	Slave	N/A	per master	I²C Port 1 slave to external master, boot at address 88
1	0001	Master	24.576MHz	400kb/s	I²C Port 0 master to I²C EEPROM slave
2	0010	Master	24.576MHz	1.53MHz	SPI port master to SPI Flash slave
3-F	-	-	-	-	Reserved

Reading and Writing Control Registers

The control is provided through the I²C port, using registers and memory spaces that are defined within the firmware. After booting and initialization, this control port provides continuous read and write access for control and monitoring of the amplifier system. Register addresses are dynamic based on the audio path signal flow and hardware options selected for the particular project. Address locations are generated for each system through a header file from the D2 Audio Customization GUI v3 design tool that maps the address location to each parameter of the system.

The I²C port is used for reading and writing the control data. The highest-order byte of the register address (bits 23:16) determines the internal address space used for control read or write access, and the remaining 16 bits (bits 15:0) describe the actual address within that space.

All reads or writes to registers (shown in Figures 9 and 10) begin with a Start Condition, followed by the Device Address byte, three Register Address bytes, three Data bytes and a Stop Condition. Register writes through the I²C interface are initiated by setting the read/write bit that is within the device address byte. The device write function as shown in Figure 9, executes the following nine steps as the I²C bus master:

1. I²C START command
2. Transmit device I²C address with W
3. Transmit mode byte
4. Transmit upper memory address byte
5. Transmit lower memory address byte
6. Transmit data upper byte
7. Transmit data middle byte
8. Transmit data lower byte
9. I²C STOP command

All reads to registers require two steps. First, the master must send a dummy write which consist of sending a Start, followed by the device address with the write bit set, and three register address bytes. Next, the master must send a repeated Start, following with the device address with the read/write bit set to read, and then read the next three data bytes. The master must Acknowledge (ACK) the first two read bytes and send a Not Acknowledge (NACK) on the third byte received and a Stop condition to complete the transaction. The device's control interface acknowledges each byte by pulling SDA low on the bit immediately following each write byte. The device read function, as shown in Figure 10, executes the following 11 steps as the I²C bus master:

1. I²C START command
2. Transmit device I²C address with W
3. Transmit mode byte
4. Transmit upper memory address byte
5. Transmit lower memory address byte
6. Repeat START command
7. Transmit device I²C address with R
8. Receive data upper byte
9. Receive data middle byte
10. Receive data lower byte
11. I²C STOP command or NACK

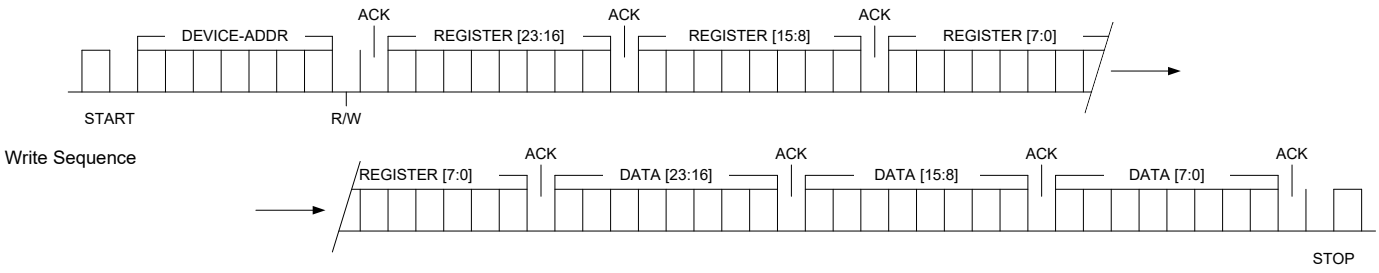


FIGURE 9. I²C WRITE SEQUENCE OPERATION

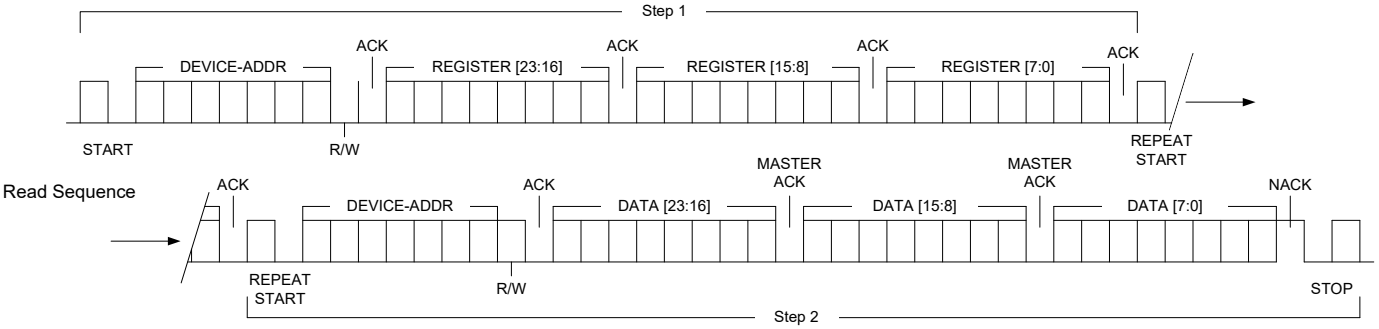


FIGURE 10. I²C READ SEQUENCE OPERATION

Audio Processing

Audio processing is totally defined by the system firmware and signal flow. Audio processing blocks are implemented using the D2 Audio Customization GUI v3 design tool software. This tool includes an extensive library of audio processing functions that are developed for operating in the D2-3 and D2-3S device families.

The D2 Audio Customization GUI v3 software provides the interface to define and build a complete audio sound processing system. Drag-and-drop inserting of its included audio processing blocks enables building a customized signal flow by placing audio algorithms into customized firmware for executing on the devices.

Audio Processing Algorithms

Audio processing algorithms include all of the following functions. Multiples of each are permitted, and there is no limit to the order or interconnect of the algorithm blocks. Upon completion of defining the audio processing path, the D2 Audio Customization GUI v3 software incorporates the blocks and builds the final system firmware for loading onto and running the devices.

Details and equations for each parameter are provided in the D2 Audio Customization GUI v3 User's Manual.

INPUT SOURCE SELECTION

A source selection register defines input channel assignment of audio presented to the device's audio input ports.

VOLUME

Volume control blocks provide level and trim adjustments within the signal flow. Continuous adjustment through programmable gain ranges supports attenuation to -100dB and gain to +24dB. A single 24-bit register value provides gain setting and also supports selectable audio phase inversion.

SHARED VOLUME

Shared Volume blocks implement multiple channels of level attenuation. The number of channels is configurable and a single 24-bit register value equally controls all channel levels. Volume is continuously adjustable from unity gain to -100dB.

MIXERS

Mixers provide individually-adjustable inputs that are summed together and passed to their output. Each input mixing level is controlled with its own 24-bit register that provides continuous adjustment from unity gain to -100dB, along with full audio path cut-off and optional input phase inversion supporting sum and difference mixers. Audio block choices include 2-input, 4-input, and configurable N-input mixers accommodating as many inputs as desired.

ROUTER

Routers perform independent channel routing assignment, connecting any input to any output. The number of channels is configurable with up to 64 inputs and 12 outputs.

STEREO A/B SWITCH

The A/B Switch provides stereo routing selection to switching either of two pairs of stereo inputs to its output. It operates as a double-pole, double-throw type of switch to the audio flow.

TONE CONTROL

Tone Controls are shelving filters providing independent of gain and frequency adjustment for bass and treble tone settings. Frequency and gain are continuously and independently adjustable for both the bass and treble settings, supporting gain ranges of -14 to +14 dB.

PARAMETRIC EQUALIZERS

Parametric Equalizer (EQ) blocks provide an adjustable bandpass or band-reject frequency response. With frequency-domain parameter settings of frequency, gain, and bandwidth or Q, parameters are continuously and independently adjustable. EQs are provided as individual audio blocks, and as blocks with groups of 3-Band and 5-Band EQs.

BIQUAD FILTER (FREQUENCY DOMAIN CONFIGURATION)

The Biquad block is a frequency-domain-parameter-entry biquad filter implemented as a second-order biquad algorithm, providing configurable high-pass, low-pass, and all-pass filtering functions. First or second filter order can be selected, and parameter setting entries of frequency and damping coefficient are continuously adjustable. Bypass and polarity phase inversion is also supported.

BIQUAD FILTER (Z-DOMAIN CONFIGURATION)

The Z-Domain Biquad is a second order biquad digital algorithm that operates from direct entry of z-transform coefficients. The filter supports individual user entry coefficients enabling nearly any second order filter synthesis per cascadable block.

CROSSOVER FILTER

The Crossover Filter blocks provide high-pass or low-pass filtering using frequency domain adjustment settings. Blocks are implemented from two cascaded second-order biquad elements, with selections that directly implement Linkwitz-Riley, Butterworth, or Bessel filter presets. The slope setting is adjustable from 6, 12, 18, or 24dB per octave, frequency and damping coefficients are continuously adjustable, and bypass, active or mute functions are supported.

FIR FILTER

The FIR filter is a configurable n-tap Finite Impulse Response (FIR) filter implementation. The number of taps and their coefficient values are defined in the audio signal flow simply through a user-generated list of tap coefficients for the FIR structure.

EXCURSION CONTROL

Excursion Control is a specialized algorithm that dynamically controls audio based on frequency and level. Excursion Control boosts the low frequency response to compensate for physically-limited low-frequency capabilities of small loudspeakers and subwoofers at low listening levels. As listening levels rise, it dynamically adjusts its boost, enabling an optimum subwoofer listening experience at all loudness levels.

DELAY

Delay Blocks introduce an adjustable delay of a channel's audio data. Buffer size is fully user-configurable, supporting adjustment over a range as small as milliseconds, to over 1 second.

COMPRESSOR

Compressors provide threshold-dependent level adjustments, implementing dynamic attenuation at configurable rates as the control signal level increases. Headroom level is configurable, supporting adjustable threshold ranges. Ratio, threshold, and attack/release times are also fully adjustable. Compressors incorporate a side chain input for algorithm control, supporting, compressing, or limiting operation from inputs independent of the processed channel audio signal flow.

COMPRESSOR/EXPANDER

The Expander Compressor implements dynamic low-level signal expansion, or an upward compression to audio levels. The Expander Compressor implements dynamic low-level signal expansion for an upward compression to audio levels. Adjustable settings include gate threshold and ratio, expansion threshold, ratio, and expansion gain limit, and attack and release times.

ENVELOPE VOLTAGE CONTROLLED AMPLIFIER (VCA)

The Envelope VCA processes its control input to establish an amplitude envelope signal representing the audio path input level. The Envelope VCA uses its side chain input to establish an amplitude envelope of the audio level. Controls are similar to that of the Compressor Block.

REVERB

The Reverb Block is a 2-channel stereo reverb processor. It provides adjustable reverb time and damping settings, and its built-in mixer includes adjustments for both dry and wet audio levels.

CHIME GENERATOR

The Chime Generator contains three oscillators, each with adjustable frequency and gain. When triggered, the oscillators initially produce full programmed output levels that then decrease at their programmable decay time rate.

RMS LEVEL METER

RMS Meters provide real-time indication of the signal levels through the audio processing path. Visible in the D2 Audio Customization GUI v3 signal flow, they provide continuous level indication. Measured data in the meter's registers can also be read by system controllers for monitoring levels in a final production system.

FADE-PAN

The Fade-Pan control provides level adjustment of four input channels to four output channels. Implementation includes a Rear/Front fade adjustment, and a Left/Right balance adjustment. Controls are continuously adjustable, providing unity gain at mid-point settings, and attenuating output levels of its channels, as the respective control is adjusted away from that channel's direction.

MONO MIXER

A Mono Mixer is a threshold-gating mixer that routes the sum of either or both of its two inputs into its output, based on a control level input. This threshold-controlled mixing supports processing of input audio that may be mono on both Left and Right, or containing content on only one of Left or Right. This summed audio then passes equally to stereo processing and output system channels.

DITHER GENERATOR

The Dither Block generates a random noise (dither) pattern at a shaped-spectrum low level. This noise is available to sum into the audio path using a mixer, pushing up low-order bits of low-level audio. This process enables improved uniform audio quality when digital bit depth truncation is required because of interfacing equipment. Audio signal flow data is normally processed and output in digital format as 24 bits from the channels assigned to the SAI digital outputs.

HARMONICS GENERATOR

The Harmonics Generator provides a harmonic spectrum content from audio presented to its input. Harmonic order and amplitude is programmable, supporting customized audio processing features.

Sound Enhancement Algorithm Processing

D2 Audio DSP Sound Enhancement Algorithm audio processing provides a full set of enhancements to audio that greatly add to the quality and listening experience of sound in wide scopes of consumer devices. The Sound Enhancement Algorithms use psycho-acoustic processing that creates a rich-sounding environment from small speakers, and synthesizes the sound and quality equivalent to more complex systems. It is especially suited to consumer products that include televisions, docking stations, and mini hi-fi stereo products. Sound Enhancement Algorithm Processing includes:

- 2 Channel stereo spatialization
- Bass Enhancement
- Content/configuration EQ presets
- Improved vocal clarity
- Automatic room audio setup/equalization/optimization
- Automatic loudspeaker setup/equalization/correction

D2 Audio DSP Sound Enhancement Algorithms are completely supported with all part numbers of the D2-3 and D2-3S families.

Third Party Virtualization and Enhancements

Enhancement processing and virtualization algorithms from third-party technology providers are available to add to D2 Audio Customization GUI v3. As permitted through license agreements from the providers, these algorithms are supplied to the designer where they integrate into the D2 Audio Customization GUI v3 software, and appear as additional audio block choices.

Depending on device part number and design-specific firmware definitions, the D2-3 device supports a variety of processing, decoding, virtualization, and pre/post processing feature sets. Features and processing support is shown in Table 1 on page 5.

Audio Processing Block Controls

Each audio processing block is assigned its own registers providing adjustment controls for the parameters associated with its audio function. Some blocks use one register only, while other blocks with multiple control settings may use multiple registers for each control. The parameter equations for all of the audio blocks are provided in the D2 Audio Customization GUI v3 User's Manual.

Dynamic Register Addressing Architecture

D2 Audio Customization GUI v3 supports building of any signal flow with no restriction of the order of occurrence of any audio block, or any limit to repeated deleting or addition during signal flow editing. As audio algorithm blocks are edited, added, or removed, the user-space memory addresses for each register will change. However, each instance of each block has its own unique label identifier where that identifier is clearly known and visible on the signal flow workspace.

Because each and every algorithm is assigned its own dedicated register for its parameter settings, the D2 Audio Customization GUI v3 generates a variable-to-address mapping for each build of each project. This mapping is provided as a text file in a header file format that can be directly included within a system controller's software build. As multiple iterations of a signal flow are created during the design process, a new header file is created matching each revision. Simply including the header file within the system controller compile automatically passes these new register addresses without need for repeated system code editing.

Hardware Feature Functions

In addition to the core firmware that runs the device to operate the amplifier, several feature-specific options are supported for use in the amplifier system. These optional features are configurable and may be chosen or bypassed. Configuration is set using the D2 Audio Customization GUI v3 software, where based on chosen settings, the firmware will include each function along with the hardware I/O assigned to its function.

The D2-3 supports pins assignable to various hardware features, while the D2-3S shares choices between functions with some of its available pins providing feature choices in a lower pin-count package.

These hardware feature algorithms include:

AM AVOIDANCE MODE

AM Avoidance Mode allows selecting the PWM switching frequency to move its harmonics away from the frequency of an AM radio station, reducing possible station interference. The algorithm is optional and selection is controlled through a register setting that is created with the system firmware.

MCLK CLOCK OUTPUT

The MCLK output provides the I^2S clock to external digital audio circuits or devices. The MCLK output is optional, and when enables is selectable between two frequencies.

PSSYNC CLOCK OUTPUT

The PSSYNC signal is used for synchronizing switching power converters used in the amplifier. Providing a synchronizing frequency that is a multiple or sub-multiple of the PWM switching rate eliminates possibility of in-band audio frequency generation from close but asynchronous clocks. The output is optional, and when enabled supports six frequency multiple choices.

AUDIO I/O CONFIGURATION

This configuration allows choice selection of which audio processing channels are assigned to the S/PDIF and I^2S digital outputs. It also supports choice of input port assignments to the audio input channels.

FAULT INDICATION

An optional output can be assigned to provide a control signal to a system controller or other hardware within the amplifier upon detection of protection or fault conditions. The feature can be enabled or disabled, and when enabled, allows choosing an available I/O pin for providing this output.

DECODER SELECTION

Third party decoding of compressed formats is supported based on the particular device part number. By default, when a device is used that supports the licensed technology, its supported decoding is enabled. Choices allow building of firmware to selectively include or exclude the available decoding algorithms.

FORMAT CHANGE NOTIFICATION

The Format Change Notification feature allows assigning an I/O pin to provide hardware indication when a change of decoded format types is detected. This supports dynamic audio path allocation by the system controller when audio content changes to or from PCM and an encoded format. The feature is disabled by default, but when enabled, allows assignment of the I/O pin to signal this state. An additional setting allows choosing an audio muting time delay between format changes.

IDLE POWER MANAGEMENT

The Idle Power Management feature allows controlled audio PWM output shutdown after a time period has elapsed with no audio detected above a threshold level. The feature is disabled by default and when enabled allows choice of threshold time and signal level, and assignment of an I/O pin that can be used to signal other operations in the amplifier.

MASTER VOLUME ENCODER

The Master Volume Encoder feature allows assigning of I/O pins to a quadrature-type encoder that can be used as a mechanical volume control. The feature is disabled by default, but when enabled, allows choice of volume control algorithm association in the audio signal flow, and choice of the I/O pins.

PWM OUTPUT CONFIGURATION

The PWM Output Configuration functions support assignment of PWM output pins to each of the 12 PWM engines. It allows pin polarity selection, and choice of enabling or disabling each PWM engine.

PWM OUTPUT TIMING

The PWM Output Timing controls enable per-channel adjustment of each PWM output timing. Controls included dead time, minimum pulse width, and stagger settings between channels.

POWER DOWN OUTPUT

The Power Down Output feature supports setting an output pin that can connect to power stages, for manually shutting down power stages during fault detection, and system startup. When enabled, the algorithm supports specification entry of the I/O pin to be used for the function.

TEMPERATURE SENSING

A thermal protection algorithm supports use of NTC resistors placed in heat-sensitive areas of the amplifier. The algorithms run and provide real-time temperature measurement. Temperature values are available in firmware registers for reading by a system controller, and set-points in the algorithm can be used to trigger a controlled-attenuation level reduction or fault shutdown.

THERMAL MANAGEMENT

An additional thermal protection algorithm supports a high temperature warning input to trigger controlled-attenuation level reduction. Rate of change and delay are programmable when the feature is enabled.

D2-3 and D2-3S Differences

The D2-3 device family includes both the D2-3 and D2-3S. Functional specifications are identical to both designations of this family. However, the D2-3S, provided in its smaller 72 Ld package, supports system and assignable functions that are mapped to the pins supported in that package. Complete pin functions of all pins of both devices of the D2-3 family are listed in the Pin Description Tables.

Pin Function Mapping Between Devices

Table 3 lists the pin numbers, names and functions for both the D2-3 and D2-3S devices, and provides a mapping of the pin functions between those devices.

TABLE 3. D2-3 AND D2-3S PIN AND I/O COMPARISON TABLE

PIN NUMBERS		PIN NAMES		DESCRIPTION AND FUNCTION	
D2-3	D2-3S	D2-3	D2-3S	D2-3	D2-3S
1	1	SC20	SCLK3 (SC20)	I^2S Input Port 1 SCLK	I^2S Port 3 Input Channels 5-6 SCLK
2	2	SRD2	SDIN3 (SRD2)	I^2S Data Port 1, Input Channels 1-2	I^2S Port 3 Input Channels 5-6 Audio Input Data
3	3	SC21	LRCK3 (SC21)	I^2S Input Port 1 LRCK	I^2S Port 3 Input Channels 5-6 LRCK
4	4	SCK2	SCLK4 (SCK2)	I^2S Input Port 2 SCLK	I^2S Port 4 Input Channels 7-8, or Output Channels 1-2 SCLK
5	5	STD2	SDIO4 (STD2)	I^2S Data Port 2, Input Channels 3-4	I^2S Port 4 Input Channels 7-8, or Output Channels 1-2 Audio Data
6	6	SC22	LRCK4 (SC22)	I^2S Input Port 2 LRCK	I^2S Port 4 Input Channels 7-8, or Output Channels 1-2 LRCK
8	7	SCK3	SCLK12 (SCK3)	I^2S Input Port 3 SCLK	I^2S Ports 1 and 2 Input Channels 1-4 SCLK
9	8	STD3	SDIN2 (STD3)	I^2S Data Port 4, Input Channels 7-8	I^2S Port 2 Input Channels 3-4 Audio Data
10	9	SC32	LRCK12 (SC32)	I^2S Input Port 4 LRCK	I^2S Ports 1 and 2 Input Channels 1-4 LRCK
13	10	SRD3	SDIN1 (SRD3)	I^2S Data Port 3, Input Channels 5-6	I^2S Port 1 Input Channels 1-2 Audio Data
36	19	SDA1	SDA1	2-Wire (I^2C) Data Port (Controller Port)	2-Wire (I2C) Data Port (Controller Port)
37	20	SCL1	SCL1	2-Wire (I^2C) Clock Port (Controller Port)	2-Wire (I2C) Clock Port (Controller Port)
119	65	SCK1	SCK1/ MCLK	I^2S Output Port SCLK	Assignable GPIO or MCLK Output
123	68	TIO0	TIO0/ PSSYNC	Timer I/O Port 0.	Timer I/O Port 0, or Assignable Power Supply Sync Output
127	71	SDA0	SDA0/ TEMPREF	2-Wire (I^2C) Data Port	Assignable I/O, NTC Temp Sense Reference
128	72	SCL0	SCL0/ TEMPNTC	2-Wire (I^2C) Clock Port	Assignable I/O, NTC Temp Sense NTC

TABLE 3. D2-3 AND D2-3S PIN AND I/O COMPARISON TABLE (Continued)

PIN NUMBERS		PIN NAMES		DESCRIPTION AND FUNCTION	
D2-3	D2-3S	D2-3	D2-3S	D2-3	D2-3S
27	16	TIO1	TIO1/NTC	Timer I/O Port 1, NTC Temp Sense Common	Assignable I/O, NTC Temp Sense Common
125	70	PROTECT0	PROTECT0	PWM Channel 0 Protect Input	PWM Channel 0 Protect Input
124	69	PROTECT1	PROTECT1	PWM Channel 1 Protect Input	PWM Channel 1 Protect Input
65	37	PROTECT2	PROTECT2	PWM Channel 2 Protect Input	PWM Channel 2 Protect Input
60	32	PROTECT3	PROTECT3	PWM Channel 3 Protect Input	PWM Channel 3 Protect Input
61	33	PROTECT4	PROTECT4	PWM Channel 4 Protect Input	PWM Channel 4 Protect Input
62	34	PROTECT5	PROTECT5	PWM Channel 5 Protect Input	PWM Channel 5 Protect Input
63	35	PROTECT6	PROTECT6 /nMUTE	PWM Channel 6 Protect Input	Assignable PWM Protect Input, or Mute Output
64	36	PROTECT7	PROTECT7 /nOVRT	PWM Channel 7 Protect Input	Assignable PWM Protect Input, or Over-Temperature Monitor Input
95	54	PWM0	PWM0	PWM output pin. (One of 18 PWM output pins. Channel and operation assignment is defined by firmware.)	PWM output pin. (One of 12 PWM output pins. Channel and operation assignment is defined by firmware.)

I/O Pin Function Assignment Comparison

Pin I/O functions and their assignments are supported through the D2 Audio Customization GUI v3 software that builds the D2-3 or D2-3S firmware. The designer has the option of choosing the offered features and allocating I/O pins to those features based on individual system design needs.

The differences of pin functions are shown in the preceding table, but the following provides additional detail to certain of these pins and functions as to their available features and assignment.

PWM OUTPUT PINS

- The D2-3 has 18 PWM pins that are assignable to any of the D2-3's 12 PWM channels.
- The D2-3S has 12 PWM pins that are assignable to any of the D2-3's 12 PWM channels.

I^2S DIGITAL INPUTS AND OUTPUTS

- The D2-3 supports eight audio INPUT channels through 4 I^2S serial digital audio input ports. Port assignments are established with the firmware built with the D2 Audio Customization GUI v3 software for the D2-3 devices.
- The D2-3 supports eight audio OUTPUT channels through 4 I^2S serial digital audio output ports. Port and channel assignments are established through user selection with the firmware built with the D2 Audio Customization GUI v3 software for the D2-3 devices.
- The D2-3S supports a user choice of either:
  - Eight audio INPUT channels through 4 I^2S serial digital audio input ports, and no I^2S OUTPUTS, or
  - Six INPUT channels through 3 I^2S ports with 1 I^2S OUTPUT supporting two audio channels.

MCLK

- The D2-3 uses a dedicated pin for the MCLK output. That pin is available only for MCLK. User selection determines if MCLK is present on this pin or if its output is off.
- The D2-3S provides a user selection to choose whether to enable the MCLK output. This pin (the SCK1/MCLK pin) becomes assigned to MCLK when MCLK is enabled. When MCLK is disabled, the SDK1/MCLK pin becomes available for assignment to other hardware I/O functions.

PROTECTION INPUT PINS

- The D2-3 provides nine protect input pins, in which the first eight are allocated to the first eight PWM engines. The last of the nine is a dedicated input for monitoring an over-temperature warning control signal from power stages or other monitoring switches.
- The D2-3S provides eight protect input pins. These pins are all assignable to be used as the protect input for their default PWM engine, or when not used for that protection become available for use with other pin-assignable hardware I/O functions. All selection is established through the user interface of the D2 Audio Customization GUI v3 design tool program.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

DATE	REVISION	CHANGE
Dec 12, 2024	4.02	Removed Dolby Virtual Speaker and DTS (SRS) information.
Oct 24, 2022	4.01	Removed Related Literature section. Updated links throughout. Updated ordering information formatting. Corrected part marking typo for D2-92643-LR. Removed Dolby Pro Logic IIx information throughout.
Apr 22, 2019	4.00	Changed the title to “D2-3(S) Audio SOC” Added D2-92643-LR to datasheet. Added Related Literature Ordering Information table - added D2-92683-QR-T and D2-92684-QR-T parts, tape and reel quantity column, and updated Note 2, and removed “Intersil” from note 3. Removed the following features from D2-92633 and D2-92643 in Table 1: - DTS(SRS) TruSurround HD4 - DTS(SRS) WOWHD4 - DTS(SRS) TruVolume Replaced all words named “D2AudioTM” to “D2 Audio DSP” ; “DAE-3” to “D2-3 Family”; “DAE-3HT” to “D2-3S Family”; “DAE-3 Family” to “D2-3 Family”; “D2-926xx” to “D2-926xx Family”; Replaced all words named “DAE-6” to “D2-6 Family” Replaced all words named “Digital Audio Engine” to “Digital Audio Processor”; “SoundSuite” to “Sound Enhancement Algorithm”; “Audio Canvas III” to “D2 Audio Customization GUI v3” Changed Sound Enhancement Algorithm 4 bullet points on page 31. Removed all DTS algorithms from “Licensed Algorithm Support” column for D2-92683-QR part number from Table 1 on page 5. Changed note 5 on page 5. Removed About Intersil section.
May 17, 2016	3.00	Updated entire datasheet applying Intersil’s new standards. Updated the Ordering Information table on page 3. Added Note 2. Replaced Products verbiage with About Intersil verbiage. Added Dolby and DTS disclaimers.
July 3, 2012	2.00	Complete datasheet rewrite to add DAE-3HT devices to the DAE-3 family. - Revisions and additions to accommodate additions for DAE-3HT to DAE-3/DAE-3HT family. - Complete rewrite of page 1 description and features, and complete rewrite of all functional description content. (Rewrites do not change function of DAE-3 devices, but provide more accurate explanation of device use.) - No changes to DAE-3 specifications other than: Addition and revision of ADC specifications and updates of supporting detail for ADC. All other DAE-3 specifications unless noted by DAE-3HT specific designations are identical to those of DAE-3. - Updates to DAE-3 high-level and detail block diagrams, and addition of diagrams for DAE-3HT. - Removal of ADC and DSD plots. - Removal of all HDA interface, HDMI interface, DSD, and SCI references and descriptions. - Removal of D2-92613-LR and D2-92625-LR part numbers which are being discontinued. (Their features are fully supported in the D2-92633-LR part number and the removed part numbers are not needed.) POD Q128.14x14 updated to latest revision - Changed title from “Thin Plastic Quad Flatpack Package (LQFP)” to “Low Plastic Quad Flatpack Package (LQFP)” POD L72.10x10F updated to latest revision - Changed bottom view to reflect correct pin 1 corner and pin numbering. Also cleaned up details Y and Z

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision. **(Continued)**

DATE	REVISION	CHANGE
May 3, 2011	1.00	Rewrite of datasheet. Fixes to incorrect (pin 109) connection description, removal of unnecessary descriptive content and structure. -Updated datasheet to latest corporate document format and applied standards as follows: Ordering information added audio processing column, added device support note, numbered notes, lead finish matching intrepid. Added Tjc to Thermal Information and corresponding note on page 5 Added Compliance note on page 6 referencing MIN and MAX columns of Electrical Spec Tables -Updated Block Diagram on page 1 - complete re-draw. -Removed D2-92643 part number from DAE-3 Device Feature Set Offering Table 1 on page 2 (this is not an available ordering part number) -Corrected pin 109 (nTRST) description error on page 14 to indicate that it must be pulled high at all times. (internally-requested error correction). Changed from: "Hardware test mode control. For D2Audio use only. Must be tied high or low." To: "Factory test only. Must be tied high at all times." -Removed outdated high level system diagrams, -Removed all (outdated and non-applicable) reference design examples, -Removed unnecessary HDA connection diagrams -Removed trademarks section/paragraph. Explicit listing not required/sufficiently covered through other means.
April 1, 2010	0.00	Initial release

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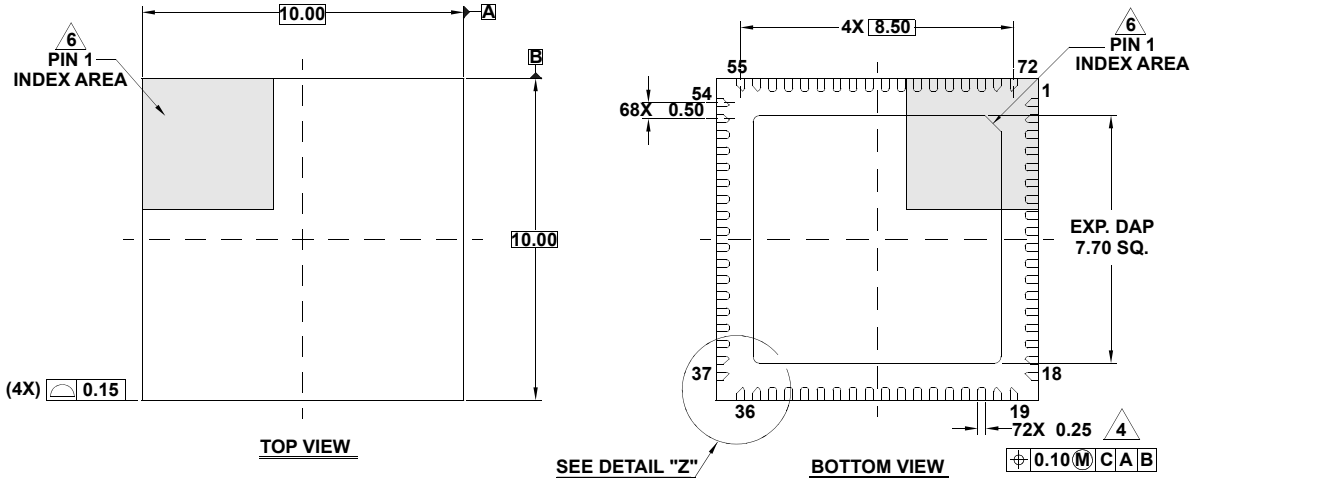
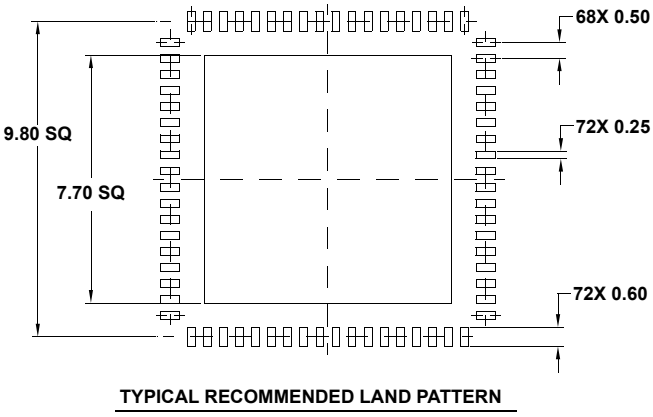
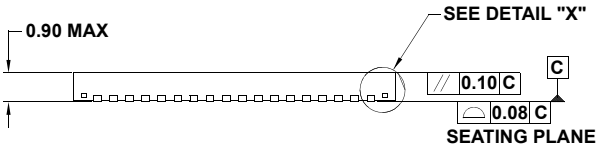
Package Outline Drawing

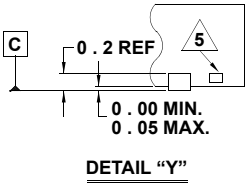
For the most recent package outline drawing, see L72.10x10F.

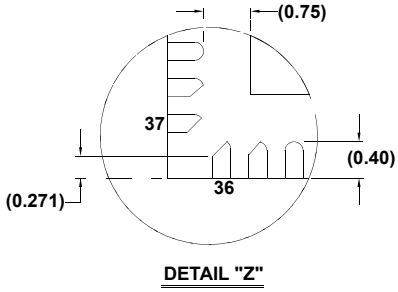
L72.10x10F
72 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 4/12











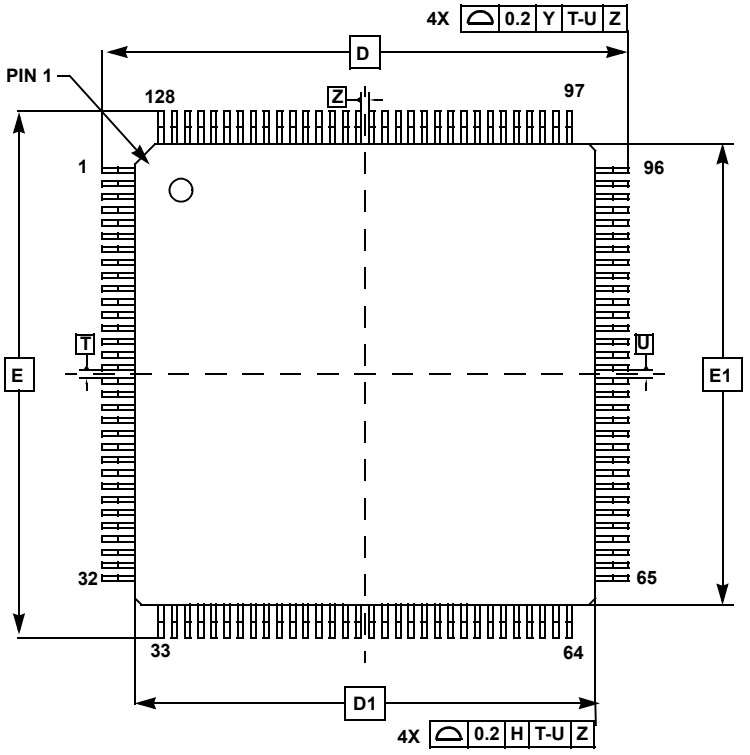
NOTES:

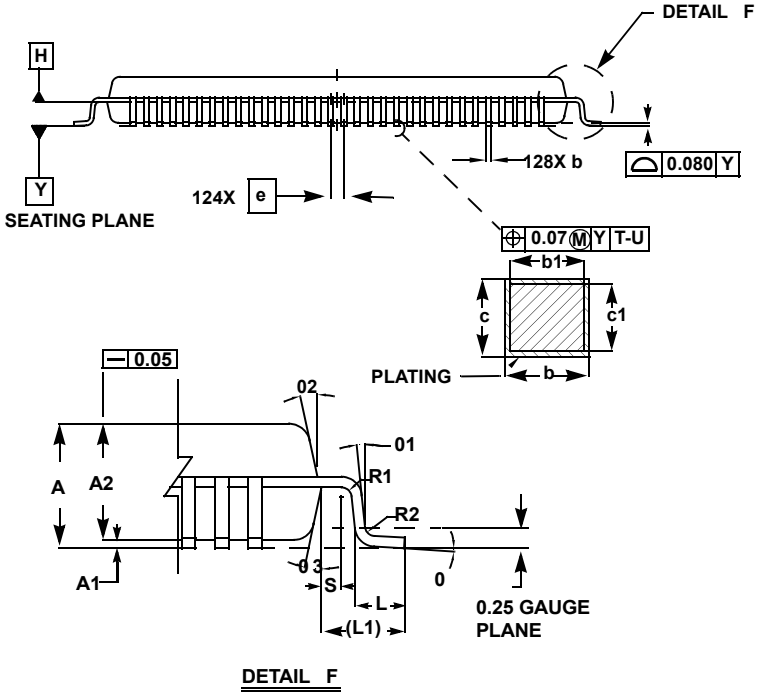
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Package outline compliant to JESD-MO220.

For the most recent package outline drawing, see Q128.14x14.

Q128.14x14

128 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE 0.4 MM PITCH





SYMBOL	MILLIMETERS			NOTES
	MIN	NOM	MAX	
A	-		1.60	-
A1	0.05		0.15	-
A2	1.35	1.40	1.45	-
b	0.13	0.16	0.23	4
b1	0.13	-	0.19	-
c	0.09	-	0.20	-
c1	0.09	-	0.16	-
D	16 BSC			-
D1	14 BSC			3
E	16 BSC			-
E1	14 BSC			3
L	0.45	0.60	0.75	-
L1	1.00 REF			-
R1	0.08	-	-	-
R2	0.08	-	0.20	-
S	0.20	-	-	-
0	0°	3.5°	7°	-
01	0°	-	-	-
02	11°	12°	13°	-
03	11°	12°	13°	-
N	128			-
e	0.40 BSC			-

Rev. 1 7/11

NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
2. Dimensions and tolerances per AMSEY14.5M-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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