CD4047BMS

CMOS Low-Power Monostable/Astable Multivibrator

FN3313
Rev 0.00
December 1992

Features

- **High Voltage Type (20V Rating)**
- **Low Power Consumption: Special CMOS Oscillator Configuration**
- **Monostable (One-Shot) or Astable (Free-Running) Operation**
- **True and Complemented Buffered Outputs**
- **Only One External R and C Required**
- **Buffered Inputs**
- **100% Tested for Quiescent Current at 20V**
- **Standardized, Symmetrical Output Characteristics**
- **5V, 10V and 15V Parametric Ratings**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Monostable Multivibrator Features

- **Positive or Negative Edge Trigger**
- **Output Pulse Width Independent of Trigger Pulse Duration**
- **Retriggerable Option for Pulse Width Expansion**
- **Internal Power-On Reset Circuit**
- **Long Pulse Widths Possible Using Small RC Components by Means of External Counter Provision**
- **Fast Recovery Time Essentially Independent of Pulse Width**
- **Pulse-Width Accuracy Maintained at Duty Cycles Approaching 100%**

Astable Multivibrator Features

- **Free-Running or Gatable Operating Modes**
- **50% Duty Cycle**
- **Oscillator Output Available**
- **Good Astable Frequency Stability: Frequency Deviation:**
  - **= ±2% + 0.03%/°C at 100kHz**
  - **= ±0.5% + 0.015%/°C at 10kHz (Circuits "Trimmed" to Frequency VDD = 10V ± 10%**

Applications

Digital equipment where low power dissipation and/or high noise immunity are primary design requirements

- **Envelope Detection**
- **Frequency Multiplication**
- **Frequency Division**
- **Frequency Discriminators**
- **Timing Circuits**
- **Time Delay Applications**

Description

CD4047BMS consists of a gatable astable multivibrator with logic techniques incorporated to permit positive or negative edge triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, -TRIGGER, ASTABLE, $\overline{\text{ASTABLE}}$, RETRIGGER, and EXTERNAL RESET. Buffered outputs are Q, $\overline{\text{Q}}$, and OSCILLATOR. In all modes of operation, an external capacitor must be connected between C-Timing and RC-Common terminals, and an external resistor must be connected between the R-Timing and RC-Common terminals.

Astable operation is enabled by a high level on the ASTABLE input or a low level on the $\overline{\text{ASTABLE}}$ input, or both. The period of the square wave at the Q and $\overline{\text{Q}}$ Outputs in this mode of operation is a function of the external components employed. "True" input pulses on the ASTABLE input or "Complement" pulses on the $\overline{\text{ASTABLE}}$ input allow the circuit to be used as a gatable multivibrator. The OSCILLATOR output period will be half of the Q terminal output in the astable mode. However, a 50% duty cycle is not guaranteed at this output.

The CD4047BMS triggers in the monostable mode when a positive going edge occurs on the +TRIGGER input while the -TRIGGER is held low. Input pulses may be of any duration relative to the output pulse.

If retrigger capability is desired, the RETRIGGER input is pulsed. The retriggerable mode of operation is limited to positive going edge. The CD4047BMS will retrigger as long as the RETRIGGER input is high, with or without transitions (See Figure 31)

An external countdown option can be implemented by coupling "Q" to an external "N" counter and resetting the counter with trigger pulse. The counter output pulse is fed back to the $\overline{\text{ASTABLE}}$ input and has a duration equal to N times the period of the multivibrator.

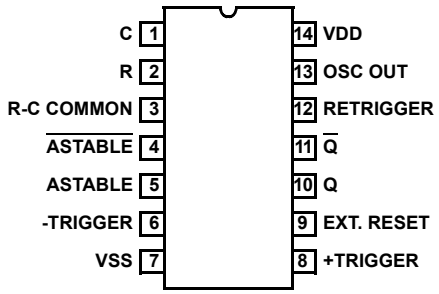
A high level on the EXTERNAL RESET input assures no output pulse during an "ON" power condition. This input can also be activated to terminate the output pulse at any time. For monostable operation, whenever VDD is applied, an internal power on reset circuit will clock the Q output low within one output period (tM).

The CD4047BMS is supplied in these 14-lead outline packages:

Braze Seal DIP	H4Q
Frit Seal DIP	H1B
Ceramic Flatpack	H3W

Pinout

CD4047BMS
TOP VIEW



Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Input Leakage Curent (Pin 3)	IIL	VDD = 24V, VIN = 11V or GND		1	+25°C	-300	-	nA
				2	+125°C	-10	-	µA
Input Leakage Current (Pin 3)	IIH	VDD = 26V, VIN = 13V or GND		1	+25°C	-	300	nA
				2	+125°C	-	10	µA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink) Q, $\overline{Q}$, OSC Out	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink) Q, $\overline{Q}$, OSC Out	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink) Q, $\overline{Q}$, OSC Out	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source) Q, $\overline{Q}$, OSC Out	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
Output Current (Sink)	IOL5RC	VDD = 5V, VOUT = 0.4V		1	+25°C	0.78	-	mA
Output Current (Sink)	IOL10RC	VDD = 10V, VOUT = 0.5V		1	+25°C	2.0	-	mA
Output Current (Sink)	IOL15RC	VDD = 15V, VOUT = 1.5V		1	+25°C	5.2	-	mA
Output Current (Source)	IOH5RC	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.78	mA
Output Current (Source)	IOH10RC	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-2	mA
Output Current (Source)	IOH15RC	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-5.2	mA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10μA	1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10μA	1	+25°C	0.7	2.8	V
Functional	F	VDD = 2.8V, VIN = VDD or GND	7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 20V, VIN = VDD or GND	7	+25°C			
		VDD = 18V, VIN = VDD or GND	8A	+125°C			
		VDD = 3V, VIN = VDD or GND	8B	-55°C			
Input Voltage Low (Note 2)	VIL	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)	VIH	VDD = 5V, VOH > 4.5V, VOL < 0.5V	1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2)	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V	1, 2, 3	+25°C, +125°C, -55°C	-	4	V
Input Voltage High (Note 2)	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V	1, 2, 3	+25°C, +125°C, -55°C	11	-	V

NOTES:

1. All voltages referenced to device GND, 100% testing being implemented
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max..

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay Astable, $\overline{\text{Astable}}$ to OSC	TPLH1	VDD = 5V, VIN = VDD or GND	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Propagation Delay Trigger to Q, $\overline{Q}$	TPHL3 TPLH3	VDD = 5V, VIN = VDD or GND	9	+25°C	-	1000	ns
			10, 11	+125°C, -55°C	-	1350	ns
Propagation Delay (Note 2) Astable or $\overline{\text{Astable}}$ to Q, $\overline{Q}$	TPLH2 TPLH2	VDD = 5V, VIN = VDD or GND	9	+25°C	-	700	ns
			10, 11	+125°C, -55°C	-	945	ns
Propagation Delay (Note 2) Retrigger to Q, $\overline{Q}$	TPHL4 TPLH4	VDD = 5V, VIN = VDD or GND	9	+25°C	-	600	ns
			10, 11	+125°C, -55°C	-	810	ns
Propagation Delay (Note 2) Reset to Q, $\overline{Q}$	TPLH5 TPLH5	VDD = 5V, VIN = VDD or GND	9	+25°C	-	500	ns
			10, 11	+125°C, -55°C	-	675	ns
Transition Time	TTHL TTLH	VDD = 5V, VIN = VDD or GND	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:

1. VDD = 5V, CL = 50pF, RL = 200K; input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low	VIL	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	-	3	V
Input Voltage High	VIH	VDD = 10V, VOH > 9V, VOL < 1V	1, 2	+25°C, +125°C, -55°C	+7	-	V
Propagation Delay Astable, $\overline{\text{Astable}}$ to OSC	TPLH1	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	160	ns
Propagation Delay Astable or $\overline{\text{Astable}}$ to Q, $\overline{Q}$	TPLH2 TPHL2	VDD = 10V	1, 2, 3	+25°C	-	350	ns
		VDD = 15V	1, 2, 3	+25°C	-	250	ns
Propagation Delay Trigger to Q, $\overline{Q}$	TPHL3 TPLH3	VDD = 10V	1, 2, 3	+25°C	-	450	ns
		VDD = 15V	1, 2, 3	+25°C	-	300	ns
Propagation Delay Retrigger to Q, $\overline{Q}$	TPHL4 TPLH4	VDD = 10V	1, 2, 3	+25°C	-	300	ns
		VDD = 15V	1, 2, 3	+25°C	-	200	ns
Propagation Delay Reset to Q, $\overline{Q}$	TPLH5 TPLH5	VDD = 10V	1, 2, 3	+25°C	-	200	ns
		VDD = 15V	1, 2, 3	+25°C	-	140	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Q or $\overline{Q}$ Deviation from 50% Duty Factor	QD	VDD = 5V	1, 2, 3	+25°C	-	±1	%
		VDD = 10V	1, 2, 3	+25°C	-	±1	%
		VDD = 15V	1, 2, 3	+25°C	-	±0.5	%
Minimum Pulse Width + Trigger - Trigger	TW	VDD = 5V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V	1, 2, 3	+25°C	-	160	ns
		VDD = 15V	1, 2, 3	+25°C	-	100	ns
Minimum Pulse Width Reset	TW	VDD = 5V	1, 2, 3	+25°C	-	200	ns
		VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	60	ns
Minimum Retrigger Pulse Width	TW	VDD = 5V	1, 2, 3	+25°C	-	600	ns
		VDD = 10V	1, 2, 3	+25°C	-	230	ns
		VDD = 15V	1, 2, 3	+25°C	-	150	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.7	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES:
1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 Note 1	1, 2, 10, 11, 13	3-9, 12	14			
Static Burn-In 2 Note 1	1, 2, 10, 11, 13	7	3-6, 8, 9, 12, 14			
Dynamic Burn-In Note 1	-	7, 9, 12	4, 5, 14	1, 2, 10, 11, 13	6, 8	3
Irradiation Note 2	1, 2, 10, 11, 13	7	3-6, 8, 9, 12, 14			

NOTE:

1. Each pin except VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V

TABLE 9. FUNCTIONAL TERMINAL CONNECTIONS

In all cases External resistor between terminals 2 and 3 (Note 1)
External capacitor between terminals 1 and 3 (Note 1)

FUNCTION	TERMINAL CONNECTIONS			OUTPUT PULSE FROM	OUTPUT PERIOD OR PULSE WIDTH
	TO VDD	TO VSS	INPUT TO		
ASTABLE MULTIVIBRATOR					
Free Running	4, 5, 6, 14	7, 8, 9, 12	-	10, 11, 13	T_A (10, 11) = 4.40 RC
True Gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	T_A (13) = 2.20 RC (Note 2)
Complement Gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	
MONOSTABLE MULTIVIBRATOR					
Positive Edge Trigger	4, 14	5, 6, 7, 9, 12	8	10, 11	tM (10, 11) = 2.48 RC
Negative Edge Trigger	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External Countdown (Note 3)	14	5, 6, 7, 8, 9, 12	-	10, 11	

NOTES:

1. See text.
2. First positive $^1/_2$ cycle pulse width = 2.48 RC. See note follow Monostable Mode Design Information.
3. Input Pulse to Reset of External Counting Chip External Counting Chip Output to Terminal 4.

Logic Diagrams

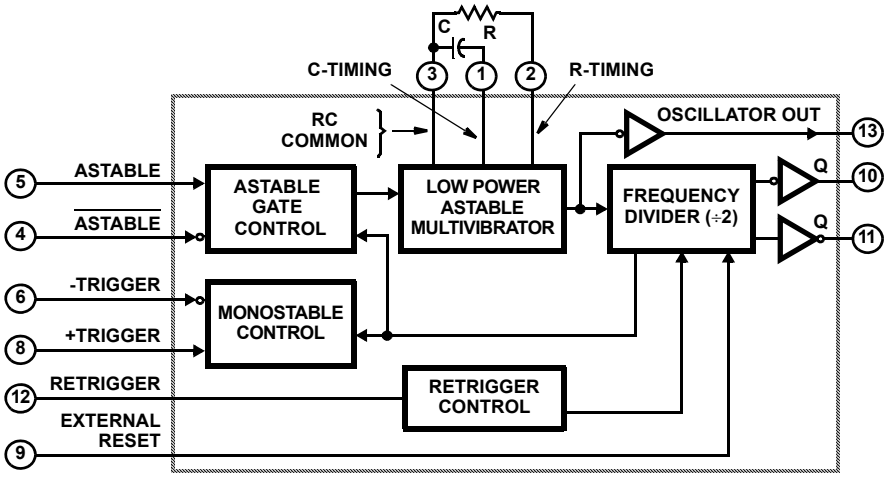


FIGURE 1. CD4047BMS LOGIC BLOCK DIAGRAM

Logic Diagrams (Continued)

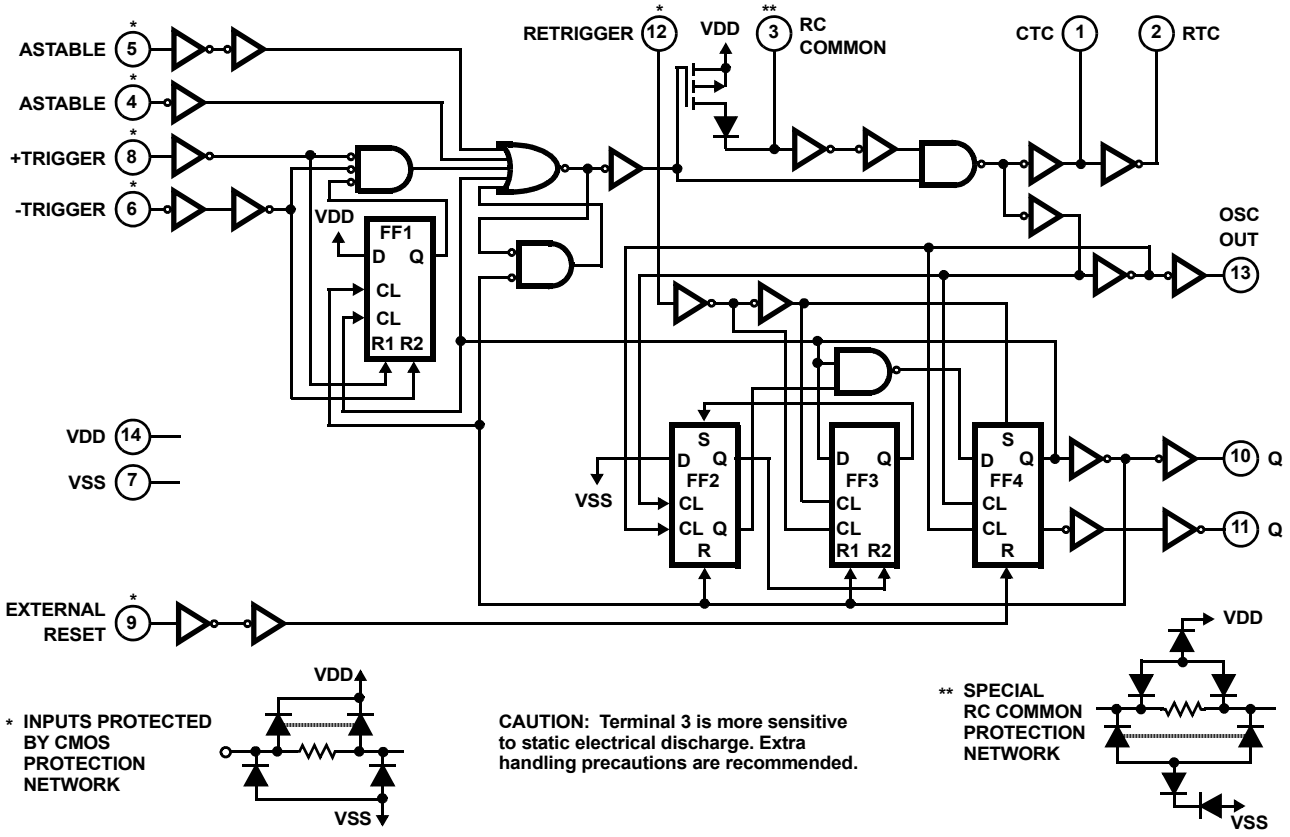


FIGURE 2. CD4047BMS LOGIC DIAGRAM

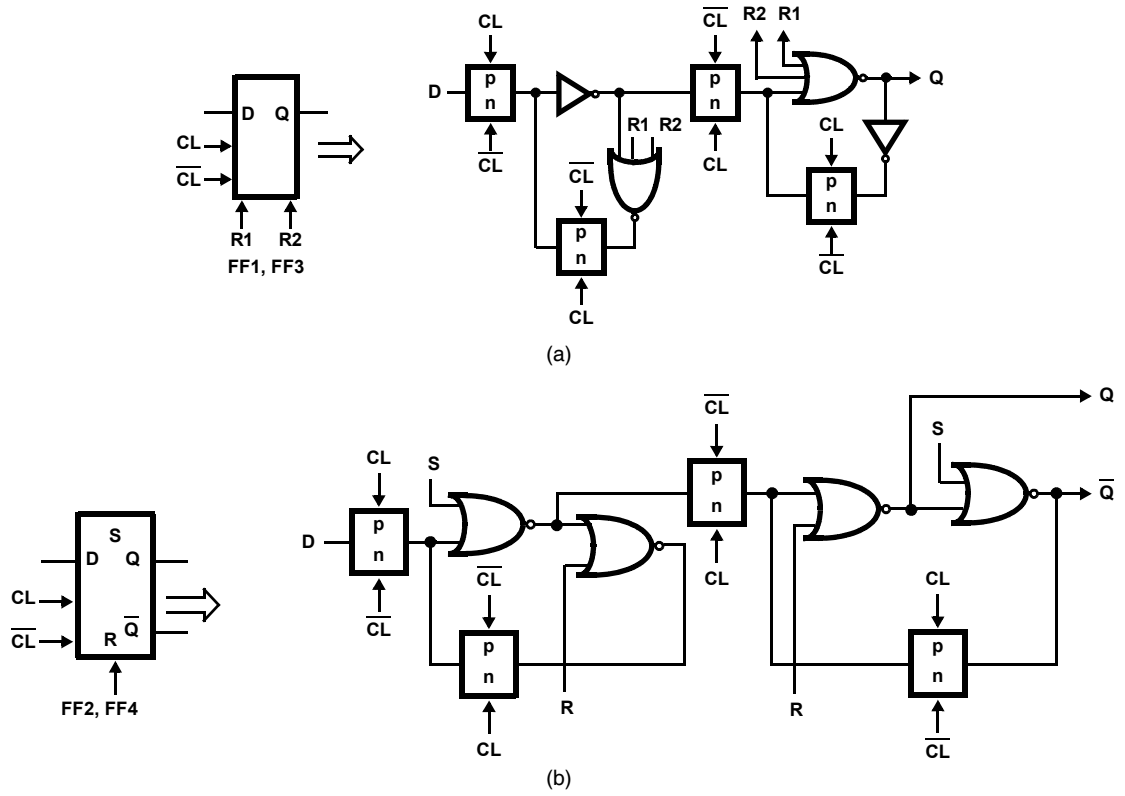


FIGURE 3. DETAIL LOGIC DIAGRAM FOR FLIP-FLOPS FF1 AND FF3 (a) AND FOR FLIP-FLOPS FF2 AND FF4 (b)

Typical Performance Characteristics

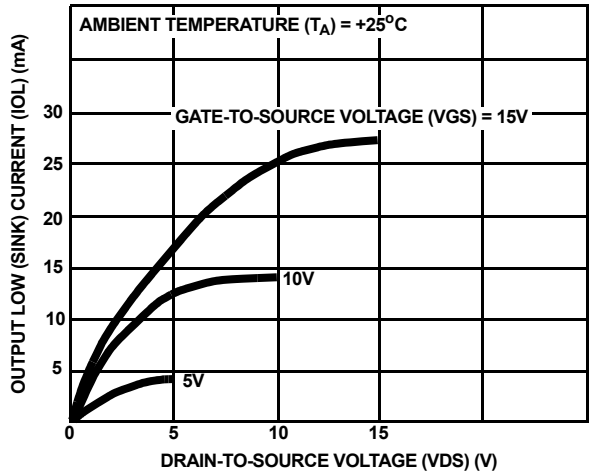


FIGURE 4. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

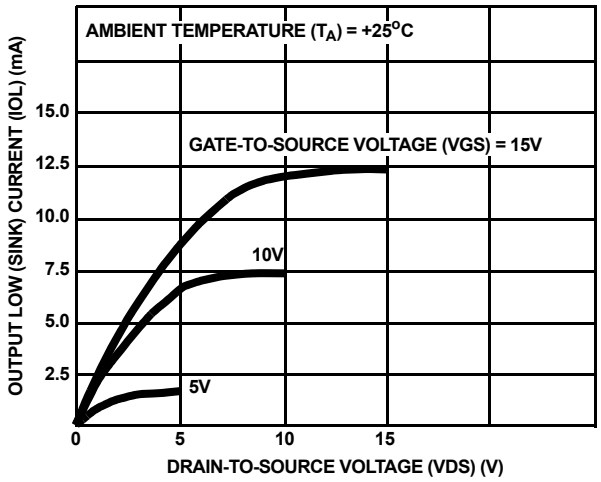


FIGURE 5. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

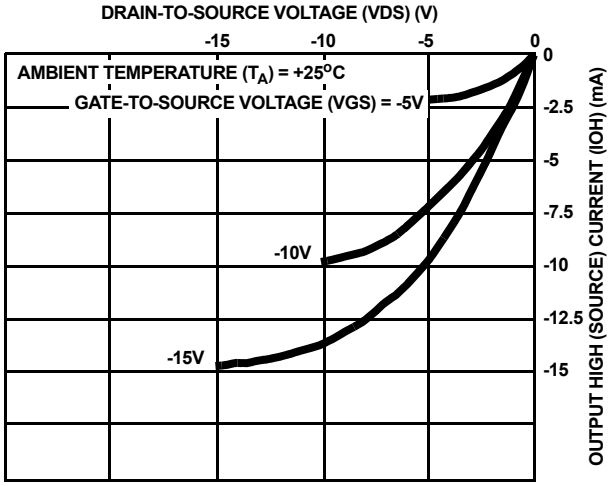


FIGURE 6. TYP. OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

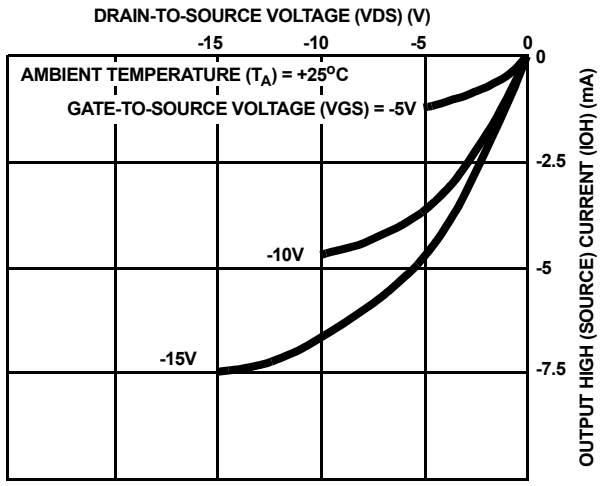


FIGURE 7. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

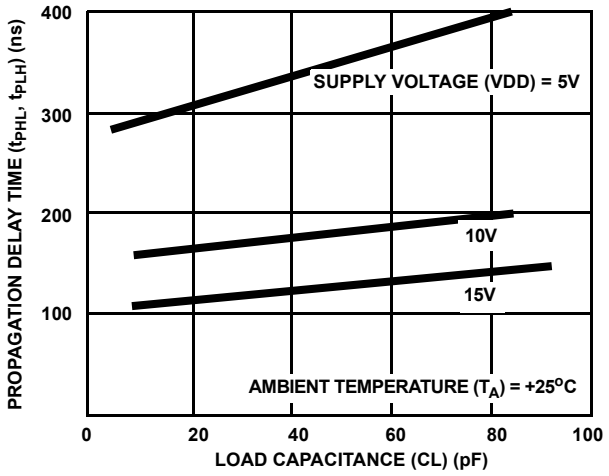


FIGURE 8. TYP. PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (ASTABLE, ASTABLE TO Q, $\overline{Q}$)

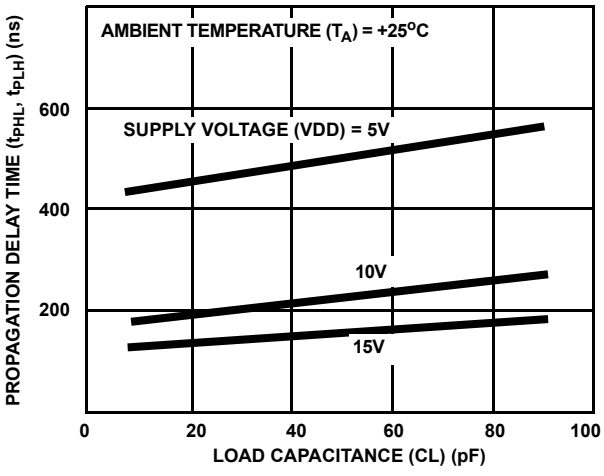


FIGURE 9. TYP. PROPAGATION DELAY TIME AS A FUNCTION OF LOAD CAPACITANCE (+ OR - TRIGGER TO Q, $\overline{Q}$)

Typical Performance Characteristics (Continued)

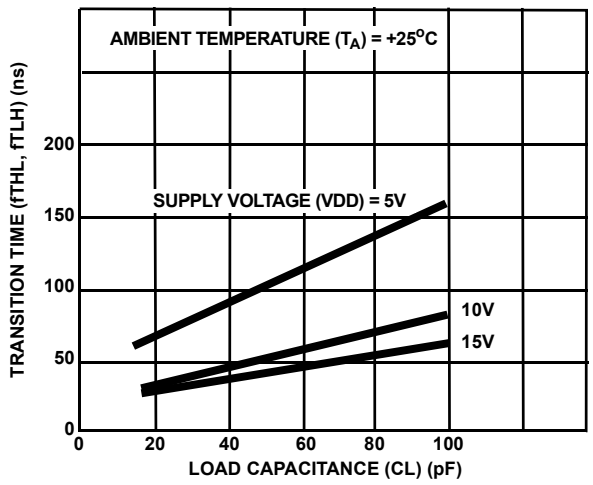


FIGURE 10. TYP. TRANSITION TIME AS A FUNCTION OF LOAD CAPACITANCE

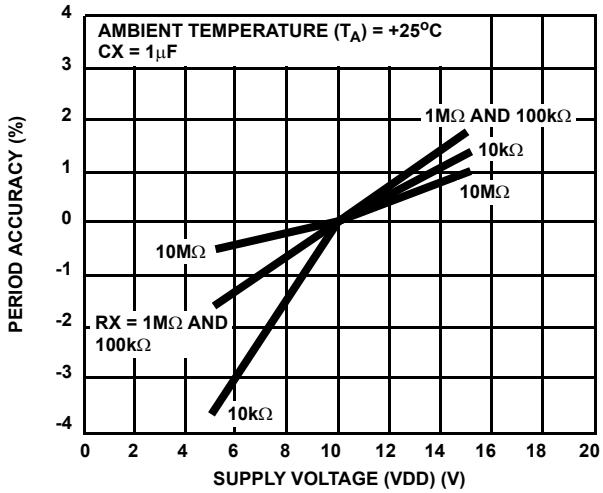


FIGURE 11. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs SUPPLY VOLTAGE

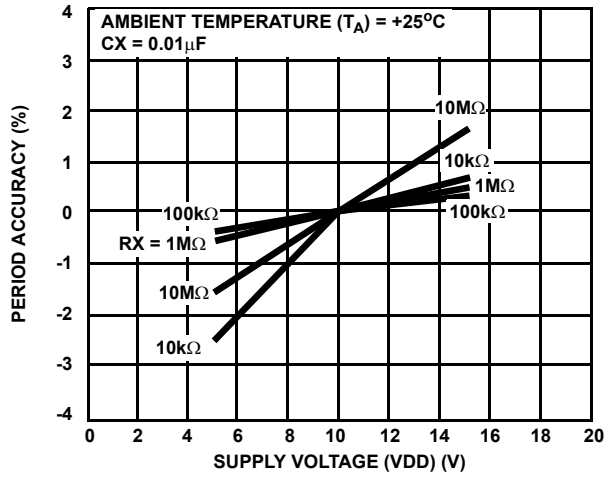


FIGURE 12. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs SUPPLY VOLTAGE

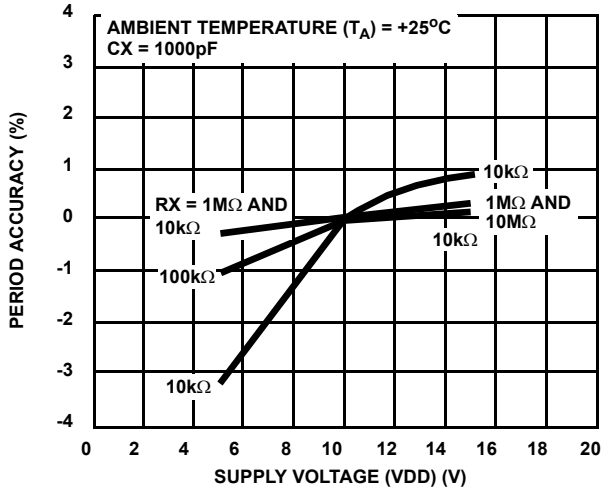


FIGURE 13. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs SUPPLY VOLTAGE

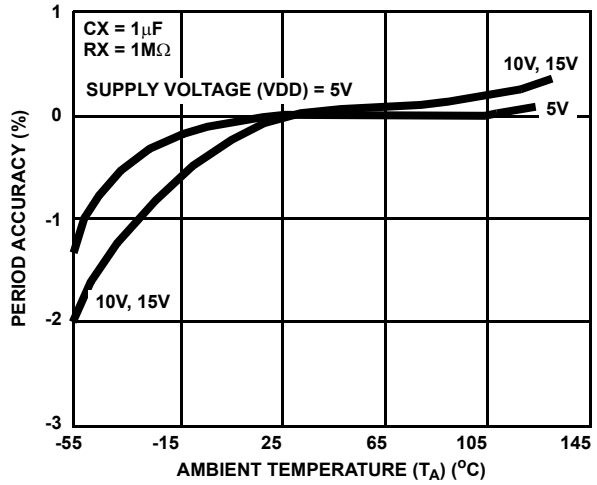


FIGURE 14. TYP. ASTABLE OSCILLATOR OR Q, Q PERIOD ACCURACY vs AMBIENT TEMPERATURE (ULTRA LOW FREQ.)

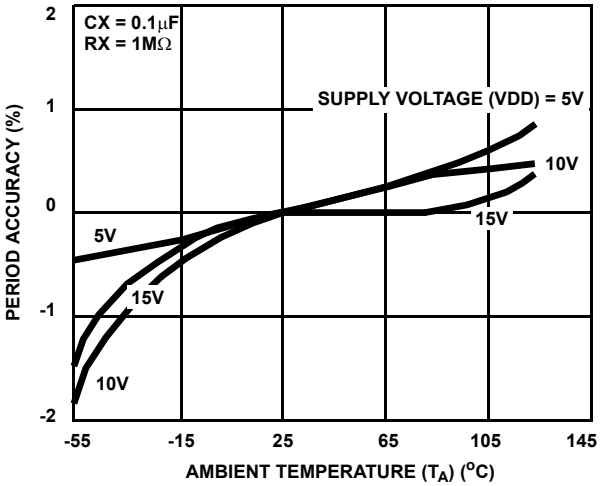


FIGURE 15. TYP. ASTABLE OSCILLATOR OR Q, Q PERIOD ACCURACY vs AMBIENT TEMPERATURE (LOW FREQ.)

Typical Performance Characteristics (Continued)

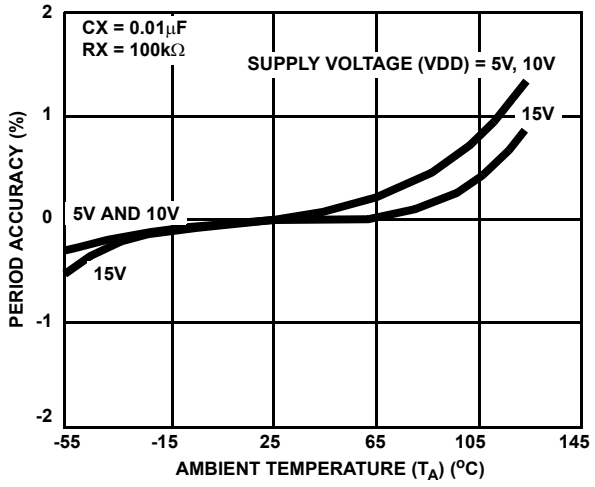


FIGURE 16. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs AMBIENT TEMPERATURE (MEDIUM FREQ.)

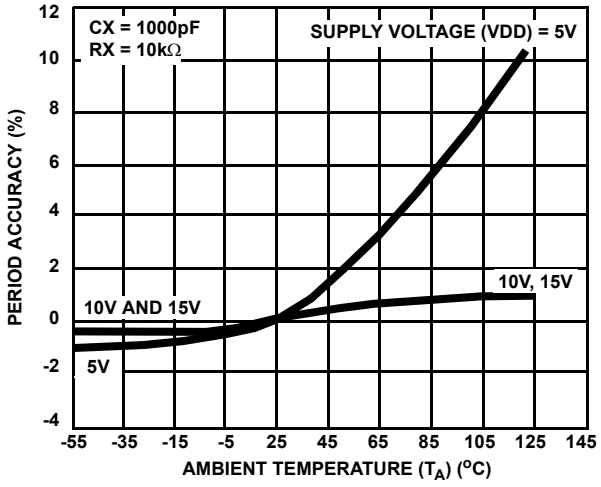


FIGURE 17. TYP. ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs AMBIENT TEMPERATURE (HIGH FREQ.)

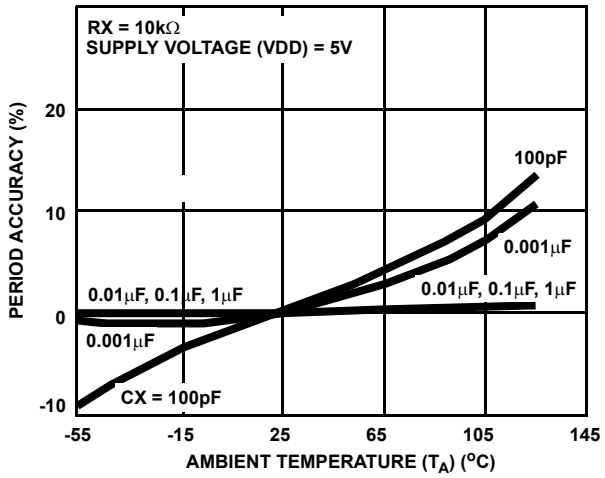


FIGURE 18. TYPICAL ASTABLE OSCILLATOR OR Q, $\overline{Q}$ PERIOD ACCURACY vs AMBIENT TEMPERATURE

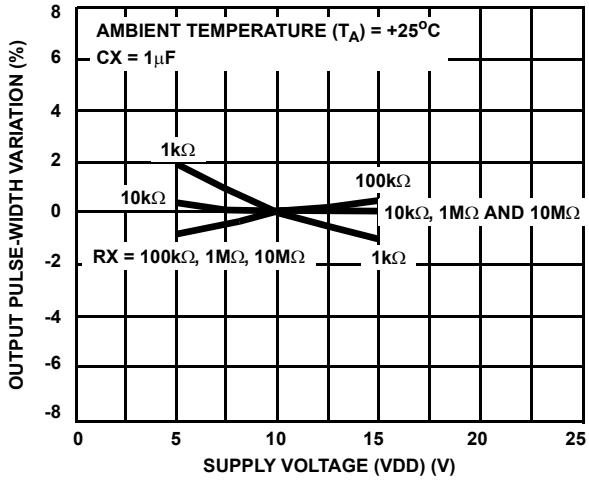


FIGURE 19. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs SUPPLY VOLTAGE

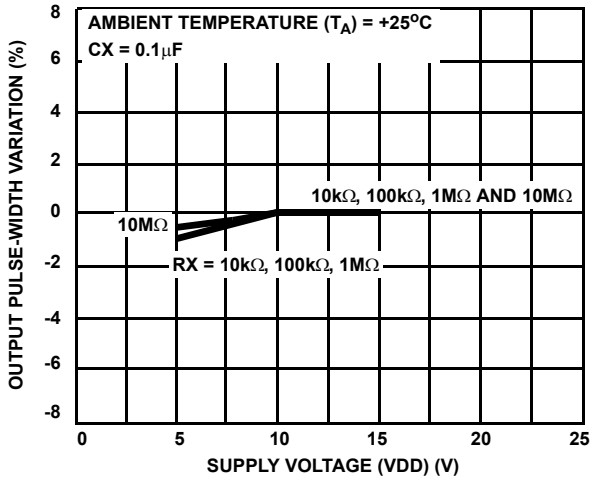


FIGURE 20. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs SUPPLY VOLTAGE

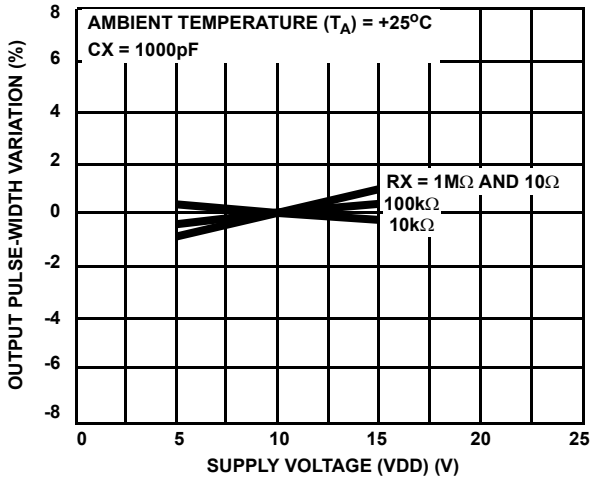


FIGURE 21. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs SUPPLY VOLTAGE

Typical Performance Characteristics (Continued)

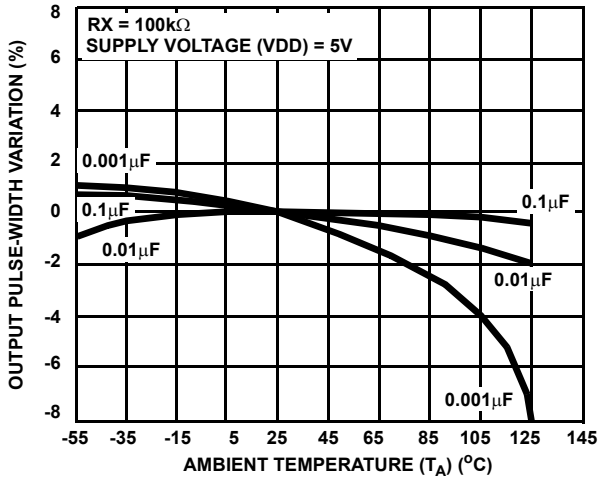


FIGURE 22. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

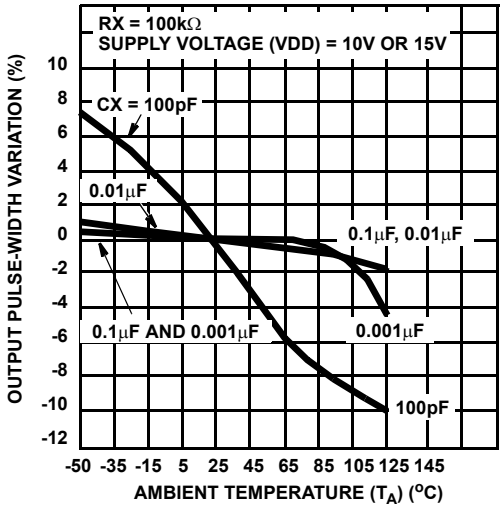


FIGURE 23. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

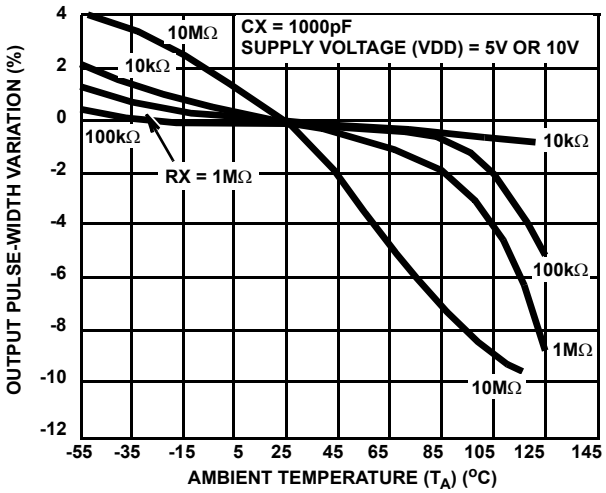


FIGURE 24. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

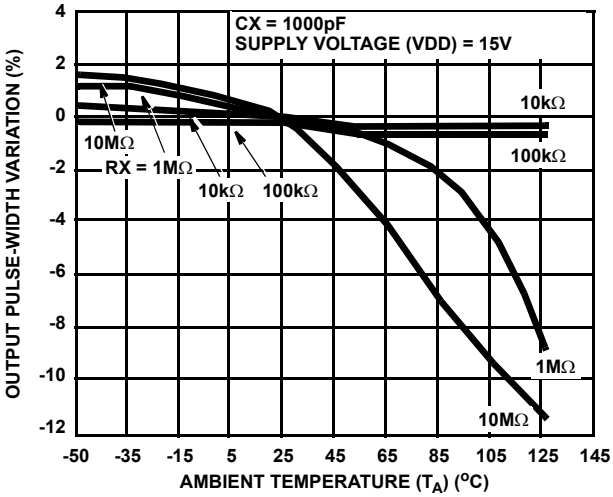


FIGURE 25. TYPICAL OUTPUT PULSE WIDTH VARIATIONS vs AMBIENT TEMPERATURE

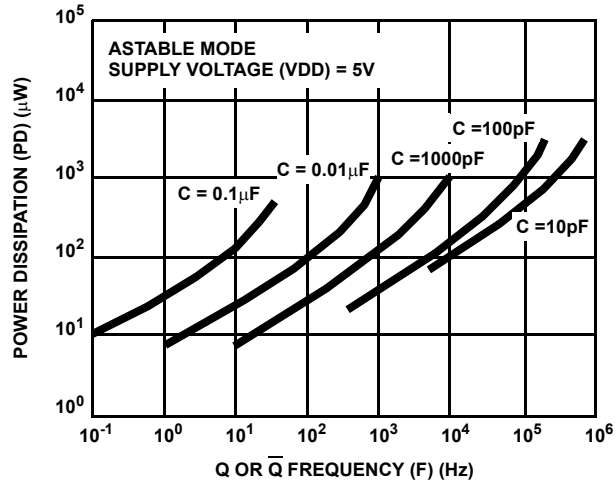


FIGURE 26. TYPICAL POWER DISSIPATION vs OUTPUT FREQUENCY (VDD = 5V)

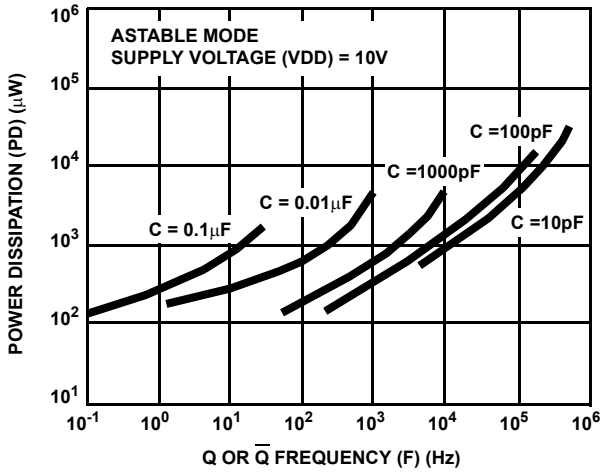


FIGURE 27. TYPICAL POWER DISSIPATION vs OUTPUT FREQUENCY (VDD = 10V)

Typical Performance Characteristics (Continued)

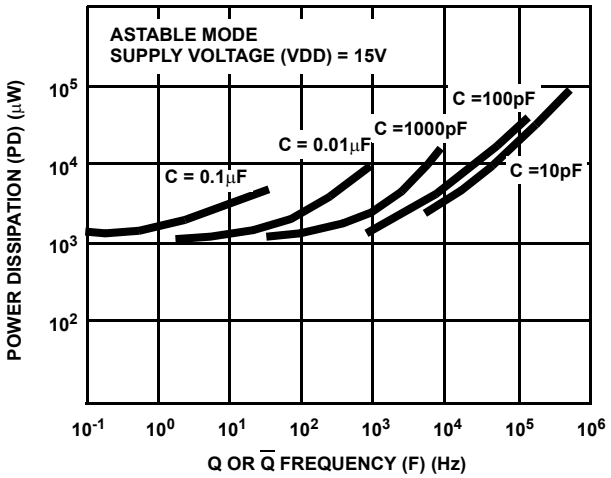


FIGURE 28. TYPICAL POWER DISSIPATION vs OUTPUT FREQUENCY (VDD = 15V)

Astable Mode Design Information

Unit-to-Unit Transfer Voltage Variations

The following analysis presents variations from unit to unit as a function of transfer voltage (VTR) shift (33%-67% VDD) for free running (astable) operation.

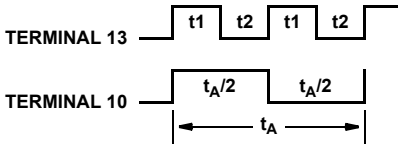


FIGURE 29. ASTABLE MODE WAVEFORMS

$$t1 = -RC \ln \frac{VTR}{VDD + VTR};$$

typically, t1 = 1.1RC

$$t2 = -RC \ln \frac{VDD - VTR}{2VDD - VTR};$$

typically, t2 = 1.1RC

$$t_A = 2(t1 + t2)$$

$$= -2RC \ln \frac{(VTR)(VDD - VTR)}{(VDD + VTR)(2VDD - VTR)}$$

Typ:	VTR = 0.5VDD	t_A = 4.40RC
Min:	VTR = 0.33VDD	t_A = 4.62RC
Max:	VTR = 0.67VDD	t_A = 4.62RC

thus if $\boxed{t_A = 4.40RC}$ is used, the variation will be +5%, -0% due to variations in transfer voltage.

Variations Due to VDD and Temperature Changes

In addition to variations from unit to unit, the astable period varies with VDD and temperature, Typical variations are presented in graphical form in Figures 11 to 18 with 10V as reference for voltage variations curves and +25°C as reference for temperature variations curves.

Monostable Mode Design Information

The following analysis presents variations from unit to unit as a function of transfer voltage (VTR) shift (33% - 67% VDD) for one shot (monostable) operation.

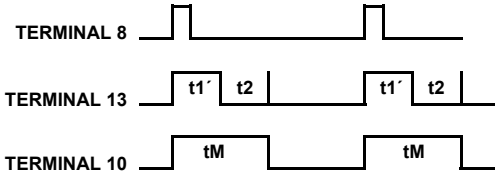


FIGURE 30. MONOSTABLE WAVEFORMS

$$t1' = -RC \ln \frac{VTR}{2VDD};$$

typically, t1´ = 1.38RC

$$tM = (t1' + t2)$$

$$tM = -RC \ln \frac{(VTR)(VDD - VTR)}{(2VDD - VTR)(2VDD)}$$

where tM = Monostable mode pulse width.
Values for tM are as follows:

Typ:	VTR = 0.5VDD	tM = 2.48RC
Min:	VTR = 0.33VDD	tM = 2.71RC
Max:	VTR = 0.67VDD	tM = 2.48RC

thus if $\boxed{tM = 2.48RC}$ is used, the variation will be +9.3%, -0% due to variations in transfer voltage.

NOTES:

1. In the astable mode, the first positive half cycle has a duration of tM; succeeding durations are t_A/s.
2. In addition to variations from unit to unit, the monostable pulse width varies with VDD and temperature. These variations are presented in graphical form in Figures 19 to 26 with 10V as reference for voltage variation curves and +25°C as reference for temperature variation curves.

Retrigger Mode Operation

The CD4047BMS can be used in the retrigger mode to extend the output pulse duration, or to compare the frequency of an input signal with that of the internal oscillator. In the retrigger mode the input pulse is applied to terminal 12, and the output is taken from terminal 10 or 11. As shown in Figure 31 normal monostable action is obtained when one retrigger pulse is applied. Extended pulse duration is obtained when more than one pulse is applied.

For two input pulses, tRE = t1´ + t1 + 2t2. For more than two pulses, the output pulse width is an integral number of time periods, with the first time period being t1´ + t2, typically, 2.48RC, and all subsequent time periods being t1 + t2, typically, 2.2RC.

External Counter Option

Time tM can be extended by any amount with the use of external counting circuitry. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Figure 32. The pulse duration at the output is

$$text = (N - 1)\ (t_A) + (tM + t_A/2)$$

where text = pulse duration of the circuitry, and N is the number of counts used.

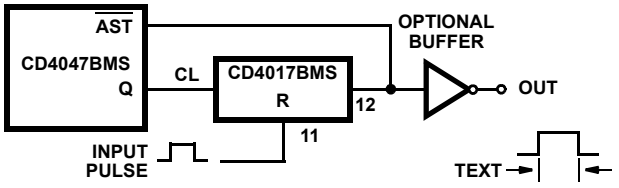


FIGURE 32. IMPLEMENTATION OF EXTERNAL COUNTER OPTION

Timing Component Limitations

The capacitor used in the circuit should be non polarized and have low leakage (i.e. the parallel resistance of the capacitor should be at least an order of magnitude greater than the external resistor used). There is no upper or lower limit for either R or C value to maintain oscillation.

However, in consideration of accuracy, C must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account). R must be much larger than the CMOS "ON" resistance in series with it, which typically is hundreds of Ω. In addition, with very large values of R, some short term instability with respect to time may be noted.

The recommended values for these components to maintain agreement with previously calculated formulas without trimming should be:

C ≥ 100pF, up to any practical value, for astable modes;

C ≥ 1000pF, up to any practical value for monostable modes.

10kΩ ≤ R ≤ 1MΩ

Power Consumption

In the standby mode (Monostable or Astable), power dissipation will be a function of leakage current in the circuit, as shown in the static electrical characteristics. For dynamic operation, the power needed to charge the external timing capacitor C is given by the following formula:

Astable Mode:

$$P = 2CV^2f.\ \text{(Output at terminal No. 13)}$$

$$P = 4CV^2f.\ \text{(Output at terminal Nos. 10 and 11)}$$

Monostable Mode:

$$P = \frac{(2.9CV^2)\ (\text{Duty Cycle})}{T}$$

(Output at terminal Nos. 10 to 11)

The circuit is designed so that most of the total power is consumed in the external components. In practice, the lower the values of frequency and voltage used, the closer the actual power dissipation will be to the calculated value.

Because the power dissipation does not depend on R, a design for minimum power dissipation would be a small value of C. The value of R would depend on the desired period (within the limitations discussed above). See Figures 26, 27, and 28 for typical power consumption in astable mode.

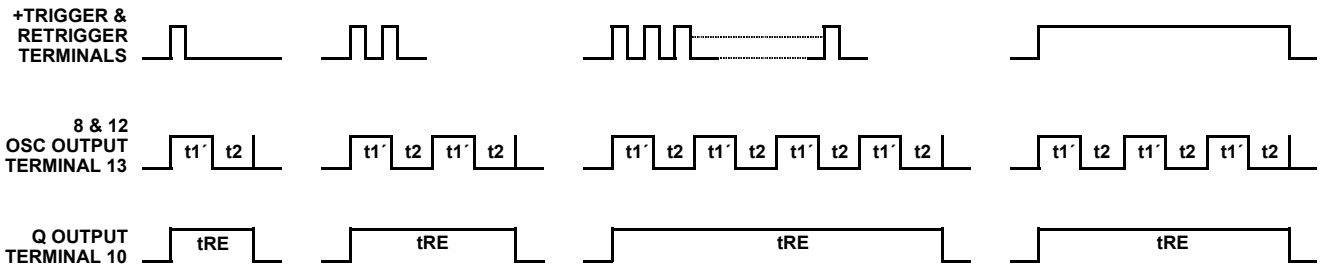
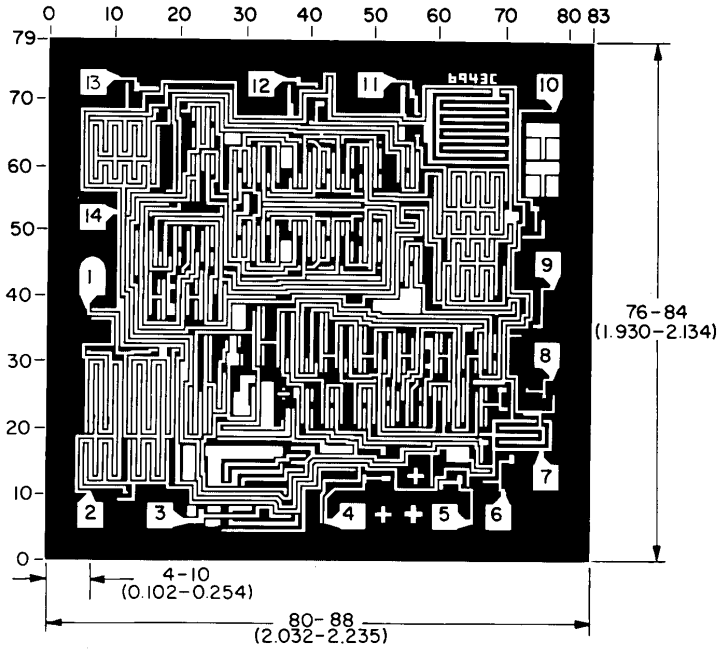


FIGURE 31. RETRIGGER MODE WAVEFORMS

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches