CCG9020

Power Control IC Datasheet

The CCG9020 is a 5-channel driver for external NMOS high-side switches with integrated charge-pump. It is intended for PWM operation controlled by an external uC.

A variety of configuration options can be selected via SPI, for example to optimize EMC performance.

The built-in 10-Bit ADC allows for measurements of channel currents, various interface voltages and the die temperature. An integrated programmable short-circuit protection, over- and under-voltage detection and overtemperature shut-down protect the chip and the load.

The IC is intended for operation in harsh environments including ground-shift, ground-loss, strong supply-transients, polarity reversal and a wiring-harness with significant inductance is supported.

A programmable high-voltage control-input and a high-voltage diagnosis-output or a LIN compatible I/O PHY provide connection to the environment. Low-power sleep mode and different selectable wake-up mechanisms help to reduce the system-level power consumption.

Key Features

- HV BCD process
- 5-channel operation available
- Integrated charge pump
- Short circuit shutdown
- Integrated 10-bit ADC
- Integrated current sensor
- Integrated die temperature sensor with over-temperature protection
- Integrated external uC interface, incl. LDO and Reset
- Suitable for Terminal 87 (T87) and Terminal 30 (T30) systems
- Low standby power

Applications

- Engine glow plug controller
- PTC heater controller for HVAC
- Seat heaters

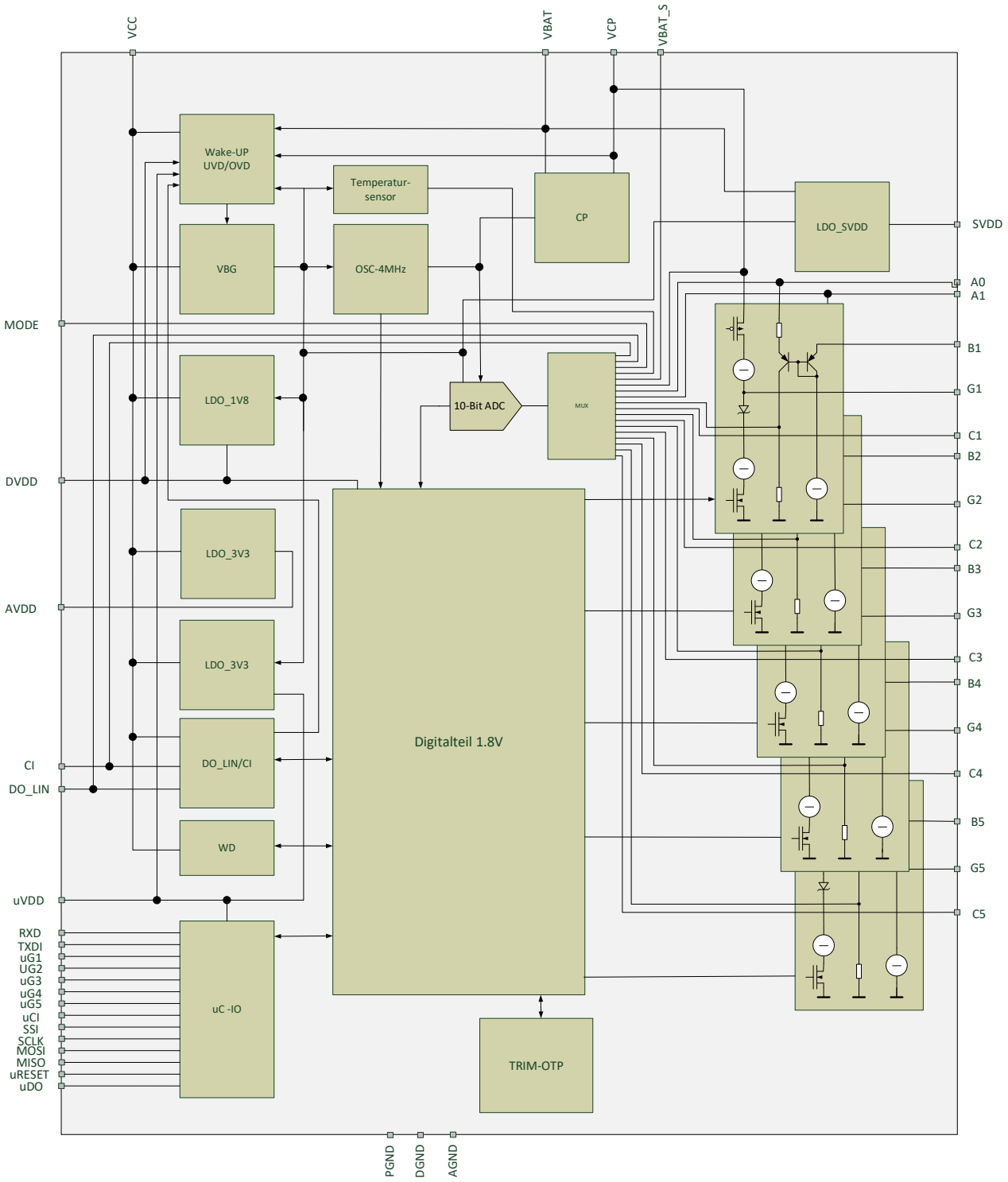

Figure 1. Block diagram

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1. Pinout

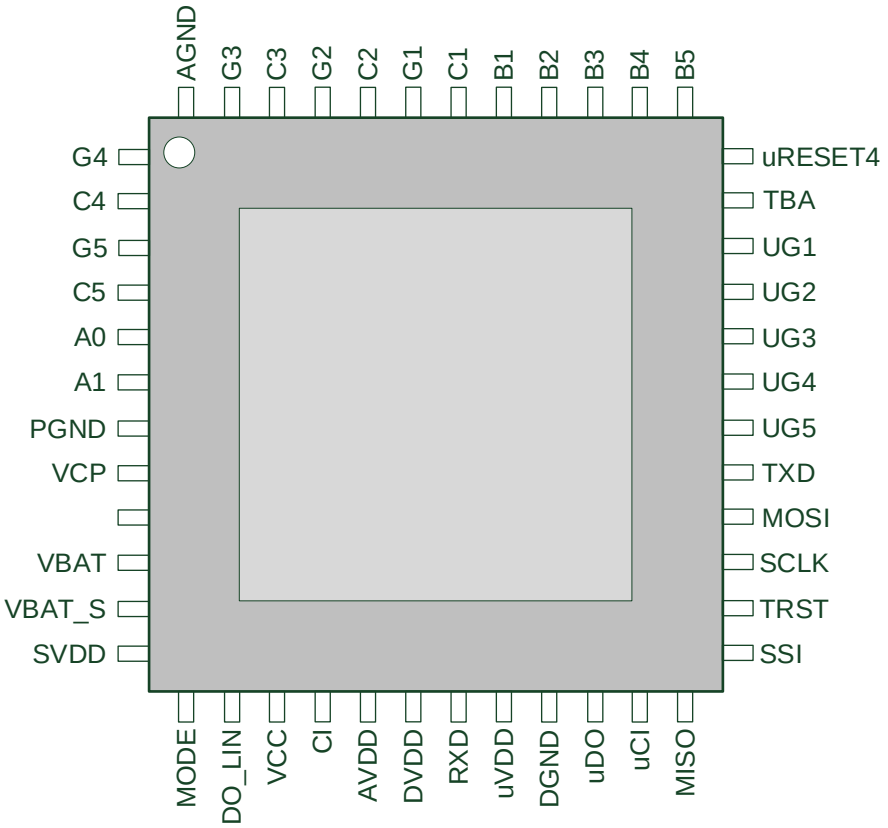


Figure 2. TQFP pinout diagram (Top view)

Table 1. Pin description

Pin #	Pin name	Type (Table 2)	Description
1	G4	O	Channel FET 4 gate control
2	C4	I	Channel FET 4 source
3	G5	O	Channel FET 5 gate driver
4	C5	I	Channel FET 5 source
5	A0	I	Channel 1/2 shunt high side
6	A1	I	Channel 3/4/5 shunt high side
7	PGND	GND	Charge pump and gate control ground
8	VCP	I/O	Cp bulk capacitor connection
9	-	-	Unassigned Wire to ground in application
10	VBAT	PWR	Power supply (T30)
11	VBAT_S	I	Sense input for T30 monitoring
12	SVDD	O	LDO output for powering channel amplifiers
13	MODE	I	T87/T30 configuration pin and T87 sense pin
14	DO_LIN	I/O	DIO_Bus/diagnostic output
15	VCC	PWR	Power supply (T87)
16	CI	I	PWM signal input
17	AVDD	O	LDO output for powering internal analog section

Pin #	Pin name	Type (Table 2)	Description
18	DVDD	O	LDO output for powering internal digital section
19	RXD	O	DIO_BUS data output to uC
20	uVDD	O	LDO output for powering external uC
21	DGND	GND	Digital section ground
22	uDO	I	Diagnostic data output from uC
23	uCI	O	Level-converted CI signal
24	MISO	O	SPI data output
25	SSI	I	SPI chip select
26	TRST	I	Test reset pin (JTAG) Wire to ground in application!
27	SCLK	I	SPI clock input
28	MOSI	I	SPI data input
29	TXD	I	DIO_BUS data input from uC
30	uG5	I	Channel 5 control signal input
31	uG4	I	Channel 4 control signal input
32	uG3	I	Channel 3 control signal input
33	uG2	I	Channel 2 control signal input
34	uG1	I	Channel 1 control signal input
35	TBA	I/O	Test Bus A Wire to ground in application!
36	uRESET	O	uC reset (active-low, open-drain)
37	B5	I	Channel 5 shunt low side (Channel FET 5 drain)
38	B4	I	Channel 4 shunt low side (Channel FET 4 drain)
39	B3	I	Channel 3 shunt low side (Channel FET 3 drain)
40	B2	I	Channel 2 shunt low side (Channel FET 2 drain)
41	B1	I	Channel 1 shunt low side (Channel FET 1 drain)
42	C1	I	Channel FET 1 source
43	G1	O	Channel FET 1 gate control
44	C2	I	Channel FET 2 source
45	G2	O	Channel FET 2 gate control
46	C3	I	Channel FET 3 source
47	G3	O	Channel FET 3 gate control
48	AGND	GND	Analog section ground
Exposed pad			Connected to AGND. Wire to ground in application

Table 2. Pin type definition

Pin Type	Description	Pin Type	Description
I	Input	O	Output
I/O	Input/Output	AO	Analog output
PWR	Power	GND	Ground

2. Characteristics

2.1 Absolute Maximum Ratings

V(AGND) = V(DGND) = V(PGND) = 0 V

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3. Absolute maximum ratings

Parameter	Description	Conditions	Min	Max	Unit
VBAT_DC	VBAT pin voltage	Note 2, Note 5	-0.3	30	V
VBAT_dyn	VBAT pin dynamic voltage	Note 3, Note 5	-0.7	45	V
IVBAT_dyn	VBAT pin dynamic injection current	Note 3	-50	0	mA
VCP_DC	VCP pin voltage	Note 2, Note 5	-0.3	40	V
VCP_dyn	VCP pin dynamic voltage	Note 3	-0.7	55	V
IVCP_dyn	VCP pin dynamic injection current	Note 3	-20	0	mA
Vai_DC	A0, A1 pin voltage		-0.3	V(VBAT)+2	V
Vai_dyn	A0, A1 pin dynamic voltage	Note 3	-0.7	V(VBAT)+2	V
IAi_dyn	A0, A1 pin dynamic injection current	Note 3	-2	0	mA
VBi_DC	B1, B2, B3, B4, B5 pin voltage	Note 2	-18	V(VBAT)+2	V
VBi_dyn	B1, B2, B3, B4, B5 pin dynamic voltage	Note 3	-25	V(VBAT)+2	V
VCi_DC	C1, C2, C3, C4, C5 pin voltage	Note 2	-18	30	V
VCi_dyn	C1, C2, C3, C4, C5 pin dynamic voltage	Note 3	-25	45	V
VGi_DC	G1, G2, G3, G4, G5 pin voltage	Note 2	-18	40	V
VGi_dyn	G1, G2, G3, G4, G5 pin dynamic voltage	Note 3	-25	55	V
VBAT_S_DC	VBAT_S pin voltage	Note 2	-0.3	30	V
VBAT_S_dyn	VBAT_S pin dynamic voltage	Note 3	-0.3	45	V
IVBAT_S_DC	VBAT_S pin injection current		-125	0	mA
IVBAT_S_dyn	VBAT_S pin dynamic injection current	Note 3	-200	0	mA
VSVDD_DC	SVDD pin voltage		VBAT-5	V(VBAT+0.3)	V
VCC_DC	VCC pin voltage	Note 2, Note 5, Note 6	-0.3	30	V
VCC_dyn	VCC pin dynamic voltage	Note 3, Note 5	-0.3	45	V
VDOLIN_DC	DO_LIN pin voltage		-27	40	V
VCI_DC	CI pin voltage	Note 2	-0.3	30	V
VCI_ dyn	CI pin dynamic voltage	Note 3	-0.3	45	V
ICI	CI pin injection current	Note 4	-5	0	mA
VMODE_DC	MODE pin voltage	Note 2, Note 5	-0.3	30	V
VMODE_dyn	MODE pin dynamic voltage	Note 3, Note 5	-0.7	45	V
IMODE_DC	MODE pin injection current		-14	0	mA
IMODE_dyn	MODE pin dynamic injection current	Note 3	-25	0	mA

Parameter	Description	Conditions	Min	Max	Unit
VAVDD, VuVDD	AVDD, uVDD pin voltage	Note 1	-0.3	5.0	V
VDVDD	DVDD pin voltage	Note 1	-0.3	2.0	V
VuCIO	RXD, TXD, uCI, uG1, uG2, uG3, uG4, uG5, SSI, SCLK, MOSI, MISO, TRST pin voltage		-0.3	V(uVDD)+0.3	V
VuDO	uDO pin voltage		-0.3	5.5	V
VuRESET	uRESET pin voltage		-0.3	VCC+0.3	V
VTBA	TBA pins voltage		-0.3	45	V
T_J	Junction temperature		-40	150 … 170 < TProt_s	°C
TI	Storage temperature		-40	150	°C

Note 1 Do not use an external power supply (UVDD can be powered externally to program the external uC provided UVDD does not exceed VCC, does not exceed 5.0 V and the internal LDO is enabled).

Note 2 DC value

Note 3 Dynamic value with pulse shape as per EMC requirements.

Note 4 Consider parameter PTOT.

Note 5 External reverse-polarity protection required.

Note 6 Refers to VSUP_NON_OP in ISO/DIS 17987-7

Component reliability refers to operation at the following temperatures.

The values are cumulative and total an overall operating time of 8,000 hours plus 14 years of standby operation at a T_J < 50 °C.

Table 4. Maximum voltage between pins

				DO_														Ci	Ai	Bi
ESD_H		0	0									0	0	0		0	0		2	2	2
ST(CI)		na										0 1)									
VCC			na		02)	02	02			02		0									
DO_LIN			45	na								27									
DVDD					na							0									
AVDD						na						0									
UVDD							Na	0	3	0		0									
µIO												0									
µDO									na			0									
µReset										na		0									
TBA											na	0									
XGND	45			40	2	5.5	6		6		45	0						55			
MODE												0 1)	N/A								
VBAT_S												0 1)		N/A							
VCP												0 1)			N/A	2					
VBAT												0 1)			15	N/A	0			2	2
SVDD												5				5	N/A				
Gj												25			55? OK PA55			55? OK PA55	10		
Cj												25						20			
Aj												0 1)					2				
Bj												25									

1):Injection currents at negative pin possible

2):Injection currents at positive pin possible

For each combination, the column lists the pin with the positive voltage.

For combinations with no entry, the max. differential voltage is 45 V provided no other adjacent path specifies a lower differential voltage.

µIO: uCI, MISO, SSI, TRST, SCLK, MOSI, TXD, RXD, uG5, uG4, uG3, uG2, uG1

The specified values factor in transient processes, particularly in case of fault, and do not apply to continuous operation.

2.2 Recommended Operating Conditions

V(AGND) = V(DGND) = V(PGND) = 0 V

Table 5. Recommended operating conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
VCC_1	VCC power supply to generate uVDD, operate the SPI interface, the internal digital section and for ADC metering	Note 1, Note 6	4.0		30	V
VCC_5	Cold-start VCC power supply	Note 7	4.5		30	V
VCC_2	VCC power supply to operate the DIO_BUS interface	Note 5	7.0		18	V
VCC_3	VCC power supply to operate the DO interface		4.0		22	V
VCC_4	VCC power supply for unrestricted ADC operation	Note 6	4.5		30	V
VBAT_1	VBAT power supply to generate uVDD (self-holding)	Note 1	6.0		26	V
VBAT_2	VBAT power supply to drive the FETs	Note 2	5.5		26	V
VBAT_3	VBAT power supply	Note 3	6.0		18	V
T_J_op	Junction temperature	Note 4	-40		150	°C
I_uVDD	uVDD current drain		-12.5		0	mA

Note 1 uVDD power can be operated as long as at least one of the two conditions (VCC_1 or VBAT_1) is met. ADC function is restricted (see section 3.9).

Note 2 Device functionality is given.

Note 3 In this voltage range, the specified values for the electrical parameters are reached.

Note 4 See Table 6.

Note 5 Refers to VSUP in ISO/DIS 17987-7

Note 6 See Note 4 of Table 24

Note 7 This supply voltage is required for approx. 10 ms after VCC is powered to enable startup. During this time, the fuse array in particular is read and the reference voltage trimmed.

Component reliability refers to operation at the following temperatures.

The values are cumulative and total an overall operating time of 8,000 hours plus 14 years of standby operation at a T_J < 50 °C.

Table 6. Temperature profile

Junction temperature	Operating time (h)
-40 °C	480
23 °C	1600
85 °C	5200
135 °C	640
150 °C	80

2.3 Electrostatic Discharge Ratings

Table 7. Electrostatic discharge ratings

Parameter	Description	Conditions	Value	Unit
V_{ESD_HBM}	Maximum ESD protection	Human body model (HBM) Note 1 AVDD pin Pin combinations with VCP and VGi All other pins	 ±1.5 ±0.5 ±2	kV

Note 1 According to ANSI/ESDA/JEDEC JS-001-2014

All pins are latchup-proof as per JESD78E.

2.4 Maximum Power Dissipation and Case Thermal Resistance

Table 8. Power dissipation

Parameter	Description	Conditions	Min	Typ	Max	Unit
P_{tot}	Max. power dissipation	40°C < T_J < 150°C			1	W
T_J	Max. junction temperature		-40		150	°C
$R_{th\_j\_epad}$	Junction-to-pad thermal resistance				10	K/W

2.5 Electrical Characteristics

Unless otherwise specified, the following data applies to the operating conditions in section 2.2.

2.5.1 Power Input

Table 9. Power input electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_op	Operating power input	I(VCC) + I(VBAT), w/o external load V(VCC) < 25 V V(VBAT) < 25 V			11	mA
I_stby_87_120	Standby power input in T87 application	I(VBAT), Standby mode V(VCC) = V(MODE) = 0 V V(VBAT) < 27 V V(Ci)>-1.5 V T_J < 120 °C			175	uA
I_stby_87_60	Standby power input in T87 application	I(VBAT), Standby mode V(VCC) = V(MODE) = 0 V, V(VBAT) < 27 V V(Ci)>-1.5 V, T_J < 60 °C			95	uA
I_stby_30	Standby power input in T30 application	I(VCC) + I(VBAT), Standby mode V(VCC) = V(VBAT_S) V(VBAT_S) < 27 V V(MODE) = 0 V V(ST) = V(VCC) V(DO_LIN) = V(VCC) T_J < 120 °C		40	190	uA

2.5.2 Under- and Over-Voltage Thresholds

Table 10. Under- and over-voltage thresholds electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
UVD_VCC_f	VCC UVD threshold (falling edge)	Note 1	3.2			V
UVD_VCC_s	VCC UVD threshold (rising edge)	Note 1			4.3	V
HYST_UVD_VCC	VCC UVD hysteresis			0.25		V
UVD_AVDD_f	AVDD UVD threshold (falling edge)		0.86x AVDD			
UVD_AVDD_s	AVDD UVD threshold (rising edge)	Note 3			0.97x AVDD	
HYST_UVD_AVDD	AVDD UVD hysteresis			0.06x AVDD		
UVD_DVDD_f	DVDD UVD threshold (falling edge)		0.88x DVDD			
UVD_DVDD_s	DVDD UVD threshold (rising edge)	Note 3			0.97x DVDD	
UVD_DVDD_start	DVDD UVD threshold (rising edge) on startup	Note 4	1.51		2.2	V
HYST_UVD_DVDD	DVDD UVD hysteresis			0.05x DVDD		
UVD_uVDD_f	uVDD UVD threshold (falling edge)	See sections 3.2 and 4.1.3	0.88x uVDD			
UVD_uVDD_start	uVDD UVD threshold (rising edge) on cold start	Note 4	2.79		3.9	V
UVD_uVDD_s	uVDD UVD threshold (rising edge)	See sections 3.2 and 4.1.3			0.97x uVDD	
HYST_UVD_uVDD	uVDD UVD hysteresis			0.05x uVDD		
UVD_SVDD_f	VBAT_SVDD UVD threshold (falling edge)		0.75x SVDD			
UVD_SVDD_s	VBAT_SVDD UVD threshold (rising edge)	Note 3			0.97x SVDD	
HYST_UVD_SVDD	VBAT_SVDD UVD hysteresis			0.05x SVDD		
UVD_VBAT_f	VBAT_S UVD threshold (falling edge)	See sections 3.2 and 4.1.3	4.5			V
UVD_VBAT_s	VBAT_S UVD threshold (rising edge)	See sections 3.2 and 4.1.3			5.6	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
HYST_UVD_VBAT	VBAT_S UVD hysteresis			0.6		V
OVD_VBAT_f0	VBAT_S OVD threshold (falling edge)	S_OVD 1.0 = 0 (see section 4.1.4)	25.7			V
OVD_VBAT_s0	VBAT_S OVD threshold (rising edge)	S_OVD 1.0 = 0 (see section 4.1.4)			31.0	V
HYST_OVD_VBAT_0	VBAT_S OVD hysteresis	S_OVD 1.0 = 0 (see section 4.1.4)		1.6		V
OVD_VBAT_f1	VBAT_S OVD threshold (falling edge)	S_OVD 1.0 = 1 (see section 4.1.4)	18.2			V
OVD_VBAT_s1	VBAT_S OVD threshold (rising edge)	S_OVD 1.0 = 1 (see section 4.1.4)			22.0	V
HYST_OVD_VBAT_1	VBAT_S OVD hysteresis	S_OVD 1.0 = 1 (see section 4.1.4)		0.9		V
OVD_VBAT_f2	VBAT_S OVD threshold (falling edge)	S_OVD 1.0 = 2 (see section 4.1.4)	17.3			V
OVD_VBAT_s2	VBAT_S OVD threshold (rising edge)	S_OVD 1.0 = 2 (see section 4.1.4) Note 6			21.0	V
HYST_OVD_VBAT_2	VBAT_S OVD hysteresis	S_OVD 1.0 = 2 (see section 4.1.4)		0.9		V
OVD_VBAT_f3	VBAT_S OVD threshold (falling edge)	S_OVD 1.0 = 3 (see section 4.1.4)	16.3			V
OVD_VBAT_s3	VBAT_S OVD threshold (rising edge)	S_OVD 1.0 = 3 (see section 4.1.4) Note 6			19.7	V
HYST_OVD_VBAT_3	VBAT_S OVD hysteresis	S_OVD 1.0 = 3 (see section 4.1.4)		0.9		V
UVD_VCP_VBAT	VCP-VBAT UVD threshold	Note 2, Note 5	4.5		5.4	V
UVD_VBAT_S, OVD_VBAT_S, VD_VCP_VBAT	Debounce time	See Table 36				

Note 1 Prolonged operation at this voltage range can trip the undervoltage detector at uVDD.

Note 2 No hysteresis

Note 3 This value only applies after the fuse array data has been read. For startup, see section 2.2.

Note 4 This value applies to startup after VCC is powered until the fuse array has been read (see section 2.2).

Note 5 Special characteristic as per VDA Vol. 2 or PPAP: S = safety

Note 6 Special characteristic as per VDA Vol. 2 or PPAP: F = functional

2.5.3 Voltage Regulator

Table 11. Voltage regulator electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
AVDD	AVDD w/o external load current	I(AVDD) = 0 A	3.4		4.0	V
AVDD_load	AVDD w/ external load current	I(AVDD) = -2 mA	3.4		4.0	V
DVDD	DVDD w/o external load current	I(DVDD) = 0 A	1.62		2.0	V
DVDD_load	DVDD w/ external load current	I(DVDD) = -2 mA	1.62		2.0	V
uVDD	uVDD w/o external load current	I(uVDD) = 0 A	3.1		3.75	V
uVDD_load	uVDD w/ external load current	I(uVDD) = -12.5 mA	3.1		3.75	V
SVDD	VBAT-SVDD w/o external load current	I(uVDD) = 0 A	3.6		4.6	V
SVDD_load	VBAT-SVDD w/ external load current	I(SVDD)=2 mA	3.6		4.6	V
I_AVDD	AVDD current limiting		-15			mA
I_DVDD	DVDD current limiting		-15			mA
I_uVDD	uVDD current limiting		-40			mA
I_SVDD	SVDD current limiting				15	mA
t_won	Wake-up time	Startup time between identified wake-up condition and deactivated uRESET		2	15	ms

2.5.4 uC Interface

Table 12. uC interface electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
VOH_uC	VOH	Pins RXD, uCI, MISO @ I = -1 mA	0.8x uVDD			
VOL_uC	VOL	Pins RXD, uCI, MISO, uRESET @ I = 1 mA			0.2x uVDD	
VIH_uC	VIH	Pins TXD, uGi, SSI, SCLK, MOSI, uDO			0.75x uVDD	
VIL_uC	VIL	Pins TXD, uGi, SSI, SCLK, MOSI, uDO	0.25x uVDD			
RPD_uC	PD resistor	Pins uGi, MOSI, SCLK, TRST Note 2	40		250	kOhm
RPU_uC	PU resistor	Pins SSI, TXD Note 2	40		250	kOhm
RPU_uC_uRESET	PU resistor (reset)	Pin uRESET	10		60	kOhm
fSPI	SPI frequency	See Figure 11			8	MHz
tsclkh	SCLK high time	See Figure 11	50			ns
tsclkl	SCLK low time	See Figure 11	50			ns
tSSIH	SSI high time	See Figure 11	180			ns
tSSIfSCLKf	SSI setup time	See Figure 11	10			ns
tSCLKrSSIr	SSI hold time	See Figure 11	10			ns
t_{MOSI_setup}	MOSI setup time	See Figure 11	10			ns
t_{MOSI_hold}	MOSI hold time	See Figure 11	10			ns
t_{MISO_valid}	MISO valid time	CL < 25 pF; see Figure 11			20	ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{min_reset}	Min. reset time	Note 1		100		us
I_{MISO_LEAK}	MISO pin leakage current	V_MISO = 0.5(uVDD)	-1		1	uA
I_{UDO_LEAK}	UDO pin leakage current	V_UDO = 5 V	-1		7	uA

Note 1 Subject to the tolerance of the oscillator frequency F_OSC

Note 2 The uDO pin has neither PU nor PD resistance. Therefore, it must be wired in all applications. (Exception: T30 application with wake-up via DIO_BUS.)

2.5.5 Internal Logic

Table 13. Internal logic electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_OSZ	Clock frequency		14.4	16	17.6	MHz

2.5.6 Charge Pump

Table 14. Charge pump electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
VCP_VBAT_2	VCP-VBAT under load	In VBAT_2 range, 0 > I(VCP_DC) > -150 µA, all gates on	5.4	10	15	V
VCP_VBAT_3	VCP-VBAT under load	In VBAT_3 range, 0 > I(VCP_DC) > -150 µA, all gates on	6.0	10	15	V
VCP_clamp	VCP–VBAT clamp voltage	I(VCP)=1 mA	11.0		16.0	V
ICP_Leak	VCP_leakage	VCP = VBAT + 10 V, VBAT = VBAT_S = 30 V CP_ON, no CP clock Gates 1–5 static-low	20		300	uA

2.5.7 Gate Control

Table 15. Gate control electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
TOL_IGATE_UP	Gate charging current tolerance	V(Gi) = V(VCP) - 2 V, see Table 50	-45		45	%
TOL_IGATE_DOWN	Gate discharge current tolerance	V(Gi) = 2 V, see Table 50	-45		45	%
Delta120,IF0,R0	Difference between gate discharge and gate charging current of two different channels IF0,x - IR0,y	Temperature ≤ 120 °C IR = IF = 0	-35		+39	uA
Delta150IF0,R0	Difference between gate discharge and gate charging current of two different channels across entire temperature	IR = IF = 0	-35		+85	uA

Parameter	Description	Conditions	Min	Typ	Max	Unit
	range IF0,x - IR0,y					
IGATE_DOWN_FAST	Fast discharge current	V(Gi) = V(VCP) - 2 V, See section 3.5	-2.8		-1.4	mA
RPU_GATE_15	Effective PU resistance	V(Gi) - V(Ci) > VTHRES_GATE, See section 3.5, Figure 5, R9 TR20 = 0, test condition: V(Gi) = V(VCP) - 2 V	2.5		8.0	kΩ
RPU_GATE_20	Effective PU resistance	V(Gi) - V(Ci) > VTHRES_GATE, See section 3.5, Figure 5, R9 TR20 = 1, test condition: V(Gi) = V(VCP) - 2 V	0.8		2.5	kΩ
Ishort_PU_15	High-side short circuit current	TR20=0, V(Gi)=0 Gate_charged	-1.4		-0.5	mA
Ishort_PU_20	High-side short circuit current	TR20=1, V(Gi)=0 Gate_charged	-4.0		-1.6	mA
RPD_GATE_STDBY	Effective PD resistance in STDBY	See section 3.5, Figure 5, R5 Test condition: V(Gi) = 2.0 V Device in STDBY	4.0		10	kΩ
tD_Gi	Gate control runtime	Rising and falling edge 0.75(uVDD) or 0.25(uVDD) and uGi up to 50% VCP at Gi Cload at Gi = 100 pF, VBAT = 12 V, IR[3:0] = IF[3:0] = 0x5 EN_DLY[5:0] = 0x0	4		10	us
VGS_clamp_p	Positive VGS clamp voltage	I(Gi) = 4.5 mA -25 V < V(Gi) < 35 V TR20=x	11.0		18	V
VGS_clamp_n	Negative VGS clamp voltage	I(Gi) = -4.5 mA -25 V < V(Gi) < 35 V TR20 = x	-18.0		-11	V
VGS_standoff	VGS standoff	I(Gi) = 100 µA Can only be measured in test mode	9.0			V
VC_shortGS_noBATS	V(Ci) to close gate source switch when VBAT_S low	VBAT_S = 0V V(Gi,Ci) < 600 mV @I(G) = 300 µA Note 1			-2.0	V
VC_shortGS_BATS	V(Ci) to close gate source switch	VBAT_S > 2 V V(Gi,Ci) < 600 mV @I(G) = 300 µA Gate Off Note 1			-1.5	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
C_LT_GND	Detection threshold for V_C lower than GND		-0.5		0.5	V

Note 1 Special characteristic as per VDA Vol. 2 or PPAP: S = safety

2.5.8 Short Circuit Power Shutdown

Table 16. Short Circuit power shutdown electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
TOL_ISC	Threshold tolerance	See Table 45 Note 1	-10		15	%

Note 1 Special characteristic as per VDA Vol. 2 or PPAP: S = safety

2.5.9 DIO_BUS

Table 17. DIO_BUS electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{BUS_LIM}	Dominant current limiting	VBUS =18 V	40		200	mA
$I_{BUS\_PAS\_dom}$	Driver off, bus dominant leakage current	Driver off, VBUS = 0 V, V(T87) = 12 V	-1			mA
$I_{BUS\_PAS\_rec}$	Driver off, bus recessive leakage current	Driver off, 8 V < VBUS < 18 V 8 V < V(T87) < 18 V VBUS > V(T87)			50	uA
$I_{BUS\_NO\_GND}$	Ground disconnect leakage current	VCC = 0 V V(KL87)-12 V < VBUS < V(KL87) + 6 V	-2.5		1	mA
$I_{BUS\_NO\_BAT}$	T87 disconnect leakage current	VCC=0 V 0 V < VBUS < 18 V			100	uA
V_{BUS_dom}	RX threshold dominant				0.4	VCC
V_{BUS_rec}	RX threshold recessive		0.6			VCC
V_{BUS_cnt}	RX mid-voltage	$V_{BUS\_cnt} = (V_{th\_dom} + V_{th\_rec}) / 2$ Note 1	0.475		0.525	VCC
V_{HYS}	RX hysteresis	$V_{HYS} = V_{th\_rec}-V_{th\_dom}$ Note 1			0.175	VCC
D1	DIO_BUS Duty Cycle 1	TH_{REC} = 0.744 x VCC TH_{dom}=0.581 x VCC 7.0 V < VCC < 18 V t_{Bit} = 50 µs D1 = t_{bus_rec} / (2 x tBit)	0.396			
D2	DIO_BUS Duty Cycle 2	TH_{REC} = 0.422 x VCC TH_{dom} = 0.284 x VCC) 7.6 V < VCC < 18 V t_{Bit} = 50 µs D2 = t_{bus_rec} / (2xt_{Bit})			0.581	
D3	DIO_BUS Duty Cycle 3	TH_{REC} = 0.788 x VCC TH_{dom} = 0.616 x VCC 7.0 V < VCC < 18 V t_{Bit} = 96 µs D3 = t_{bus_rec} / (2 x t_{Bit})	0.417			

Parameter	Description	Conditions	Min	Typ	Max	Unit
D4	DIO_BUS Duty Cycle 4	THREC = 0.389 x VCC THdom = 0.251 x VCC 7.6 V < VCC < 18 V tBit = 96 µs D4 = tbus_rec / (2xtBit)			0.590	
t_{rx_pd}	RX delay time				6	us
t_{rx_sym}	Symmetry trx_pd for rising and falling edge		-2		2	us
R_{SLAVE}	Bus pull-up		20		60	kΩ
I_{PU_STDBY}	Pull-up_power_source	Standby mode, wake-up condition: DIO_BUS V(VCC) > V(DO_LIN) > V(PGND)			60	uA
V_WU_DIO	DIO_BUS wake-up threshold		VCC-3.8 V		VCC-2 V	
T_WU_DIO	DIO_BUS wake-up debounce time		28		150	us
T_MAX_DOM	Max. dominant phase time at DIO-TX		6	9	12	ms

Note 1 V_{th_dom} and V_{th_rec} indicate the actual thresholds for V_{BUS_dom} and V_{BUS_rec}.

2.5.10 DO

Table 18. DO electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
VOL_DO_10	10 mA low-level DO	IDO_LIN = 10 mA			1.2	V
VOL_DO_2	2 mA low-level DO	IDO_LIN = 2 mA			0.7	V
I_DO_s	Output current limiting	Short circuit current limiting	11		33	mA
t_DO_f	Falling edge time	CDO = 4.7 nF, 0.8 x V(VCC) to 0.2 x V(VCC)			100	us
RPU_DO	Integrated pull-up		30		120	kΩ
I_{LEAK,DO_STDBY}	Leakage current: DO_LIN pin in standby mode	Standby mode, wake-up condition: CI V(VCC) > V(DO_LIN) > V(PGND)	-15		2	uA

2.5.11 ST

Table 19. ST electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Err_Thres_ST	ST threshold error (see Table 42)		-0.02x VCC		0.02x VCC	
WU_ST	ST wake-up threshold	Temp. ≤ 120 °C, higher temperatures can cause unintended wake-up if ST is selected as wake-up source	0.68x VCC		0.83x VCC	
T_WU_ST	ST wake-up debounce time		28		150	us
tD_CI	CI–uCI propagation delay, rising and falling edge (also to ST_TD0/1 in ST_CONFIG)	ST_Thres_up = ST_Thres_down = 50% Measured from 0.5 x V(VCC) to 0.5 x V(uVDD), Cload = 25 pF			7	us

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{CI_LEAK}	CI pin leakage current		-10		1	uA

2.5.12 Mode

Table 20. Mode electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_Th_MODE	Switching threshold (difference b/w T87/T30 application in standby)	See section 3.1	0.5		2.6	V
I_TEST	Test current to uDO	See section 3.1	-10		-1	uA
V_Th_UDO	Switching threshold to uDO pin to distinguish wake-up source (CI or DIO_BUS)		1.0		2.6	V

2.5.13 ADC

Table 21. ADC electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Vref	Reference voltage	Can be measured in test mode	1.232	1.25	1.268	V
E_TEMP	Temp. measurement error	After correcting by TASICOFFs Temp. ≥ 20 °C	-10		10	K
E_TEMP_LT	Temp. measurement error at low temp.	After correcting by TASICOFFs Temp. < 20 °C	-15		15	K
E_Gain_IGP	Channel current metering gain error Note 1	AD channels: IGPi	-1.5		1	%
E_Gain_HV	HV metering gain error Note 1	AD channels: UGPi, U30, U87, UCP, UCI	-1.5		1.5	%
E_Gain_LV	LV metering gain error Note 1	AD channel: uVDD	-1		1	%
E_Offset_IGP	Channel current metering offset error Note 1	AD channel: IGPi An offset measurement where I = 0 must be factored in	-1		20	LSB
E_Offset_HV	HV metering offset error Note 1	AD channels: UGPi, U30, U87, UCP, UCI The offset measurement via UHVofs must be factored in, reference is AGND	-8		5	LSB
E_Offset_LV	LV metering offset error Note 1	AD channel: uVDD The offset measurement via UVDDofs must be factored in, reference is AGND	-5		5	LSB
INL_IGP	Integrated channel current metering nonlinearity Note 1	AD channel: IGPi			5	LSB
INL_HV	Integrated HV metering nonlinearity Note 1	AD channels: UGPi, U30, U87, UCP, UCI			4	LSB
INL LV	Integrated LV metering nonlinearity Note 1	AD channel: uVDD			4	LSB

Note 1 Values refer to the deviation from the line of best fit.

2.5.14 Over-Temperature Shutdown

Table 22. Over-temperatur shutdown electrical characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
TProt_s	Over-temperature shutdown (rising edge) Note 1	Junction temperature	150		170	°C
TProt_f	Over-temperature shutdown (falling edge) Note 1	Junction temperature	130		150	°C
TProt_start	Over-temperature threshold on cold start Note 1	Junction temperature	140		185	°C

Note 1 The overtemperature shutdown function is indirectly tested in every component during manufacturing.

3. Functional Description

3.1 Power Supply, Startup and Shutdown

The device supports systems with T87 and T30 as well as those with only T30. In both cases, the load path is powered with the external FETs and the IPP from T30. In order to ensure the proper bootstrapping for the gate control in the event of transients in the power supply line, both the charge pump and the gate control circuit are powered in both system configurations from T30 (VBAT pin). In systems with only T30, the T87 connection is wired to T30 to ensure that VCC also receives uninterrupted power (see Figure 14 and Figure 15). Both system configurations require specific optimization for minimal standby power input. For this reason, the device distinguishes between an active mode and a standby mode. The overall system is only functional in active mode. In standby mode, only the parts of the circuit required for wake-up (transition to active mode) are powered. Wake-up is only possible when the VCC pin is powered. As long as either the VCC pin or the VBAT pin is powered, the device can be kept in active mode until the command to switch to standby mode is received from the SPI (see section 4.1.4).

In general, the device can be woken up via 3 conditions:

- High at MODE pin (T87)
- Low at ST pin
- Low pulse at DO_LIN pin

Which of these options is used in the actual system depends on the system's configuration:

In systems with T87, wake-up is only possible via a high at T87 (MODE pin). This means the standby power in T87 systems is considerably lower than in T30 systems.

In T30 systems - depending on the configuration (potential at the uDO pin) - wake-up is possible via a detected low state at CI or a high-low-high sequence at DO_LIN with a low phase of more than 150 µs.

As long as the voltage at T87 (and, based on this, the VCC voltage) is below the corresponding UVD threshold, the device cannot wake up. In this case, however, it is possible to keep the device in active mode as long as VBAT is powered (see below).

While the device is in standby mode, VCC is above the corresponding POR threshold and the MODE pin is low, the device sends a low test current (I_Test; see section 2.5) to the uDO pin to test whether this pin is wired to the uC. Since the device actively draws uVDD low in standby mode, it can be detected whether uDO is being kept low by the internal protective diode downstream of uVDD in the uC. In this case, the CI input is configured as the only wake-up source. Otherwise, the DIO_BUS becomes the only possible wake-up source. Note that uVDD is still charged when switching to sleep mode. This results in uDO initially being recognized as high when it is wired to the uC. This means that, even in an ST application, wake-up is only possible via the DIO_BUS immediately after switching to sleep mode (until uVDD is discharged). Although wake-up via the DIO_BUS is only possible with a sequence (falling edge, sufficiently long pause, rising edge), it is advisable in an ST configuration to set uDO to 1 before switching to sleep mode in order to avoid an inadvertent wake-up.

Table 23. Startup

VCC	MODE pin	uDO pin	
Not present	Ignored	Ignored	Wake-up not possible
Present	High	Ignored	Wake-up
Present	Low	Low	S1 open, S2 closed (Fig. 9), wake-up possible via CI
Present		High	S1 closed, S2 open (Fig. 9), wake-up possible via DIO_BUS

In active mode, the source of the last wake-up signal is stored in the State register (see section 4.1.3) and can be retrieved from there.

As long as the device is in active mode and both T30 (VBAT) and T87 (VCC) are powered, VCC is used to power the entire device except for the charge pump, gate control and Aj–Bi sense amplifier for channel current metering. The latter circuit blocks are always powered from T30 (VBAT).

It is possible to keep the device active after power to T87 is cut off and at minimum maintain power to the external uC as long as T30 has sufficient power. This self-holding requires the SH_ON bit be set in the Config register (see section 4.1.4).

In an application requiring self-holding, the software should therefore set the SH_ON bit during the startup routine, which will keep the uC on after T87 is shut down. The uC can detect this self-holding by measuring the voltage from T87. Once self-holding is complete, the uC writes the VDD_ON bit to low in the Config register, switching the device and itself to standby mode.

Note that the voltage drop with this self-holding (VBAT uVDD) is higher compared to the voltage drop during normal operation (VCC uVDD). Also note that, in self-holding the device feeds back the VCC pin from VBAT to approx. 4 V so Diode D4 (see Figure 16) is absolutely necessary to prevent excessive current at T87 from flowing back into the wiring harness.

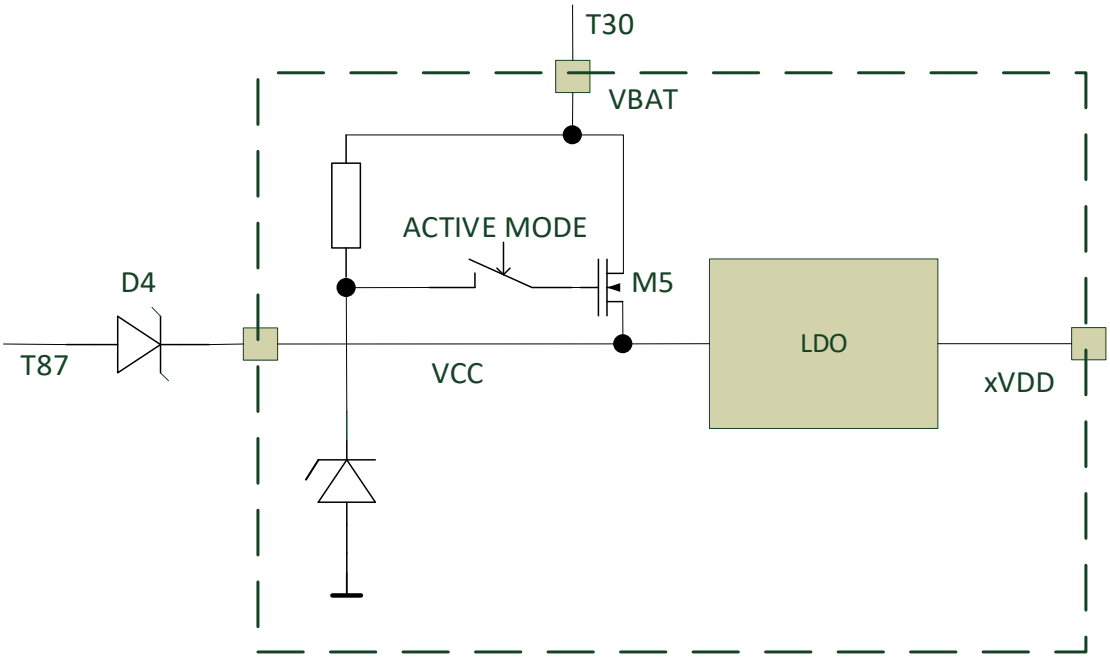


Figure 3. Power supply switch

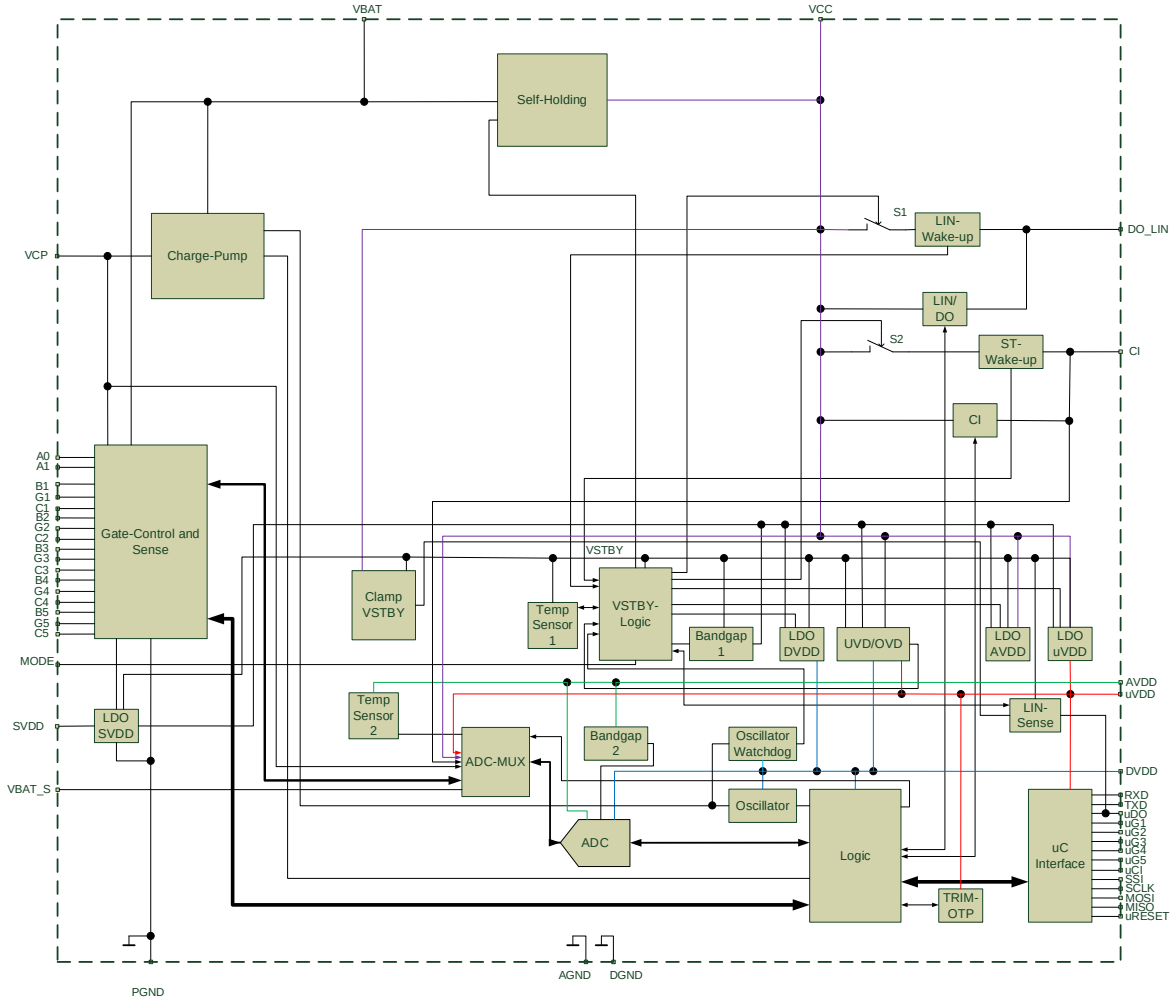


Figure 4. Power supply concept

The VSTBY voltage comes from VCC. This means it is always present when T87 is powered. This voltage is used to power the startup circuit. Startup therefore is only possible when VSTBY is present. On the other hand, the power input for the startup circuit is saved when VCC is not powered (T87 application).

VSTBY powers the VSTBY logic. This logic controls for example wake-up by monitoring the MODE pin. If a high is detected at the MODE pin, startup is initiated. As long as the MODE pin is low, the uDO pin is monitored as described above and, depending on the state, the wake-up circuit is enabled either at DIO_BUS or CI. These parts of the circuit draw static standby current depending on the state. Since VSTBY is drawn from VCC in standby mode, this standby current is not present in a T87-only application.

Once the device is woken up in the manner described above, the VSTBY logic enables the band gap, the UVD/OVD block and, where the VSTBY values are adequate, the LDO to generate DVDD and uVDD. At this point, there are no trim values yet. The band gap, and the regulator with it, start up with default values. These default values were selected to produce the highest possible band gap voltage (VBG) so that any later corrections (when trim values are available from the fuse array) always reduce VBG. This ensures that the UVDs do not inadvertently trip during the correction and trigger a reset. The transient overvoltage at DVDD and uVDD resulting from this process must be tolerated during every startup.

Once the UVD comparators at DVDD and uVDD signal valid voltage values, the oscillator is started up and the fuse array is read, then the corresponding corrections are made in the analog section. The other LDOs for AVDD and SVDD are then enabled. The fuse array has a fuse CRC checksum. The array is read repeatedly until the fuse CRC matches. In case of a permanent error, this means uRESET is not released.

The uRESET reset is only disabled after the UVD comparator at uVDD signals a valid voltage and the fuse array is read. After this time, the software can be used to set the SH_ON bit (see section 4.1.7) so self-holding remains guaranteed even when VCC breaks off.

For shutdown, the uC deletes the VDD_ON bit in the OUTCTR register (see section 4.1.4). This sets uRESET to low and all regulators are shut down.

The internal logic ensures that, after the VDD_ON bit is deleted, the uC always resets and all register values are reinitialized - even when a wake-up condition is met at the time VDD_ON is deleted (for example, MODE = high).

This method of control - especially of the LDOs - using the VDD_ON register bit in conjunction with emergency power from M5 ensures that self-holding is possible. This means the uC can still perform data postprocessing even after T87 is shut down and, in particular, save data to nonvolatile memory. Note, however, that heating and communication via DIO_BUS/DO are not possible during this self-holding. The voltage monitor in particular shuts off the corresponding functions when values drop below the proper thresholds at VCC, VBAT_S, VCP_VBAT/VBAT_SVDD. Also note when self-holding is enabled that the VDD_ON bit is only deleted once the voltage at the MODE pin has dropped below the wake-up threshold in order to prevent immediate wake-up.

3.2 Voltage and Temperature Monitoring

Operating voltages are not monitored at all in standby mode.

During startup, the series downstream of the voltages VSTBY, AVDD, DVDD, and uVDD are monitored in case a minimum value is exceeded. When the corresponding thresholds are met, a sequential wake-up occurs until uRESET is disabled (see section 3.11). If a value drops below one of the aforementioned UVD thresholds, uRESET is triggered.

Independently of the previously described functionality, VCC and VBAT-SVDD are monitored for undervoltage, and VBAT_S for under- and over-voltage (see UVD_SVDD, UVD_VCC, OVD_VBAT and UVD_VBAT in section 2.5.2). Device functionality is generally guaranteed within the specified voltage ranges. However, individual blocks may experience parametric restrictions (for example, DIO_BUS; see Table 5). The uC is responsible for monitoring the appropriate voltage ranges for compliance with certain specified parameters (see section 2.2).

If VBAT_S is outside the valid voltage range (VBAT_S < UVD_VBAT_S or VBAT_S > OVD_VBAT_Sx), the charge pump and gate control are shut down. If VCC is below the UVD threshold, DIO_BUS, DO, ST input, charge pump and gate control are disabled.

Since interactions with line inductances - particularly in the T30 lead - can result in major fluctuations in VBAT_S, a debounce time is implemented for monitoring VBAT_S for under-/over-voltage. It is also strongly recommended, depending on line inductance, to switch the individual channels on/off with a time delay of at least 300 µs.

In active mode, the IC junction temperature is continuously monitored. If this temperature exceeds a specific value (TProt_s), uRESET is set to low, DO_LIN becomes high-impedance and all potential sources of power dissipation are shut down (LDO_AVDD, LDO_VDD, LDO_uVDD, charge pump and gate drive). Only VSTBY and the connection parts of the circuit remain in operation. As soon as the temperature sensor detects that the temperature has dropped below the Tprot_f threshold, this block is disabled and the device wakes up as described above. Depending on the configuration, this requires the MODE pin to remain high, edges to continue at CI or the above DIO_BUS start sequence to take place at DO_LIN.

In active mode, the charge pump is enabled. The charge pump (VCP_VBAT) is regulated to a setpoint of approx. 10 V (see VCP_VBAT_2 and VCP_VBAT_3 in section 2.5.6). Additionally, VCP_VBAT is (passively) limited to < approx. 15 V. VCP_VBAT is also monitored for values dropping below the threshold UVD_VCP_VBAT (see section 2.5.2). If a value drops below this threshold, all gate drivers are disabled. When VCP_VBAT is valid once again, the gate drivers are reenabled (with each subsequent rising edge at uGi or after the F bit is reset in the Chctrl register).

The same applies analogously to VBAT-SVDD monitoring.

Of the cases described here, detected over-/under-voltage at VBAT_S, under-voltage from VBAT SVDD and VCP_VBAT_S under-voltage results in the E_ASIC bit being set in the State register (see section 4.1.3). The device never independently signals the error via DIO_BUS or DO.

For error handling, see section 4.1.3.

3.3 Oscillator Watchdog

The IC has a watchdog for monitoring the internal oscillator. When this watchdog is triggered, the charge pump and gate control are shut down. uRESET switches to low. This is signaled by the State register (see section 4.1.3), not via DO or DIO_BUS.

3.4 Short Circuit Shutdown

In addition to the error cases described in section 3.2, channels 1 to 5 are monitored for short circuits. The Aj - Bi voltage drop is recorded while the channel is on and compared to the thresholds configured in the ThShort register (section 4.1.8). This monitoring is independent of the channel current metering by the ADC (VAD register). Short circuits signaled when the corresponding channel is not enabled are ignored. If the measured voltage difference in a channel exceeds the specified threshold, the corresponding bit in the ChShort register is set to high and the channel is shut down. The other channels remain unaffected. The channel is only reenabled after the uC has deleted the corresponding bit (and only with the next rising edge at uGi or when the corresponding bit in the Chctrl register is reset). The device never independently signals the error via DIO_BUS or DO.

Since the various interference pulses as per ISO 7637 are present at VBAT, Aj, and Bi practically unfiltered, corresponding pulses result in the short circuit comparator malfunctioning. For this reason, an appropriate debounce time (see section 4.1.8) must be chosen to prevent the short circuit monitor from being inadvertently triggered by ISO pulse loads. This results in a corresponding delay in the short circuit shutdown. The FET in the load circuit must be large enough to withstand the load from the short circuit current for this delay time.

In the event of a short circuit shutdown, the gates for the external FETs are discharged using the fast discharge current IGATE_DOWN_FAST respectively pulled to GND.

3.5 Charge Pump and Gate Control

The device has an integrated charge pump for raising VBAT (T30). The pump works with internal pump capacitance and an external bulk capacitor. The charge pump frequency is F_OSC/4. The external bulk capacitor runs against VBAT in order to achieve a bootstrap effect when VBAT undergoes dynamic changes. The charge pump regulates to a VCP_VBAT setpoint of approx. 10 V.

The VCP_VBAT is monitored (see section 3.2).

The Gi outputs control the gates of the external FETs. These signals follow the logical state of uGi. A channel is only switched on - particularly after a detected error is rectified - following a rising edge at uGi (or the corresponding F bit being reset in the Chctrl register). The gates are generally controlled by current sources IS2 and IS3 (see Figure 5) with configurable currents (see “IRiseFall Register” in section 4.1.10). This current can be configured for all channels collectively but separately by rising and falling edge.

For the rising edge, a delay time TDLY,GUP between the input of the command to switch on a gate and the actuation of the gate can be configured. TDLY,GUP is defined in the Chconfig register by the EN_DLY[4:0] bits and applies to all channels.

250 µs after a gate is actuated with the configured charging/discharge current:

- the gate is discharged with the fast discharge current IS4 or held at GND (in case of switch-on).
- the charging current is disabled and the gate is drawn to VCP by the SW1 switch (in case of switch-on).

In standby mode, all gates are kept low by an internal resistor (RPD_GATE_STDBY) provided VCC has sufficiently high voltage.

The TR20 bit in the Chconfig register allows the value from R9 to be modified:

- If TR20 = low, a larger resistor is active.
- If TR20 = 1, a low-impedance resistor is chosen.

Comp3 detects when the FET source voltage drops below the device's local ground potential and then enables M9 so the gate continues to follow the source in order to block the external FET along with an external gate source resistor, including in the event of ground offset/loss of ground.

The M9 transistor can only be enabled when the corresponding gate is operated at low (uGi = 0) and the VCi voltage meets the parameters specified in section 2.5.7:

- VC_shortGS_noBATS for no or very low VBAT_S voltages
- VC_shortGS_BATS for sufficiently high VBAT_S voltages

In addition, M9 is enabled for a programmable time tav (see section 4.1.8) and disabled after a falling edge at uGi or F bit (see section 4.1.8) so the freewheeling of an inductive load can partially open the external FET via the source until the inductively stored energy dissipates. This avoids the FET's breakdown load. In conjunction,

the Gi gate is actively discharged until the GND voltage is reached. If a negative ground offset is present, the gate is actively discharged until V(Gi) = V(Ci).

Whenever uGi is low AND the corresponding Fi bit is low for a channel, Gi is disabled (low).

However, Gi is only set to Fi = high by a rising edge at uGi or write access to the Chctrl register. This means that Gi does not go to high on its own when Fi = high or uGi = high at the time an error condition (for example, over-temperature) ceases to exist.

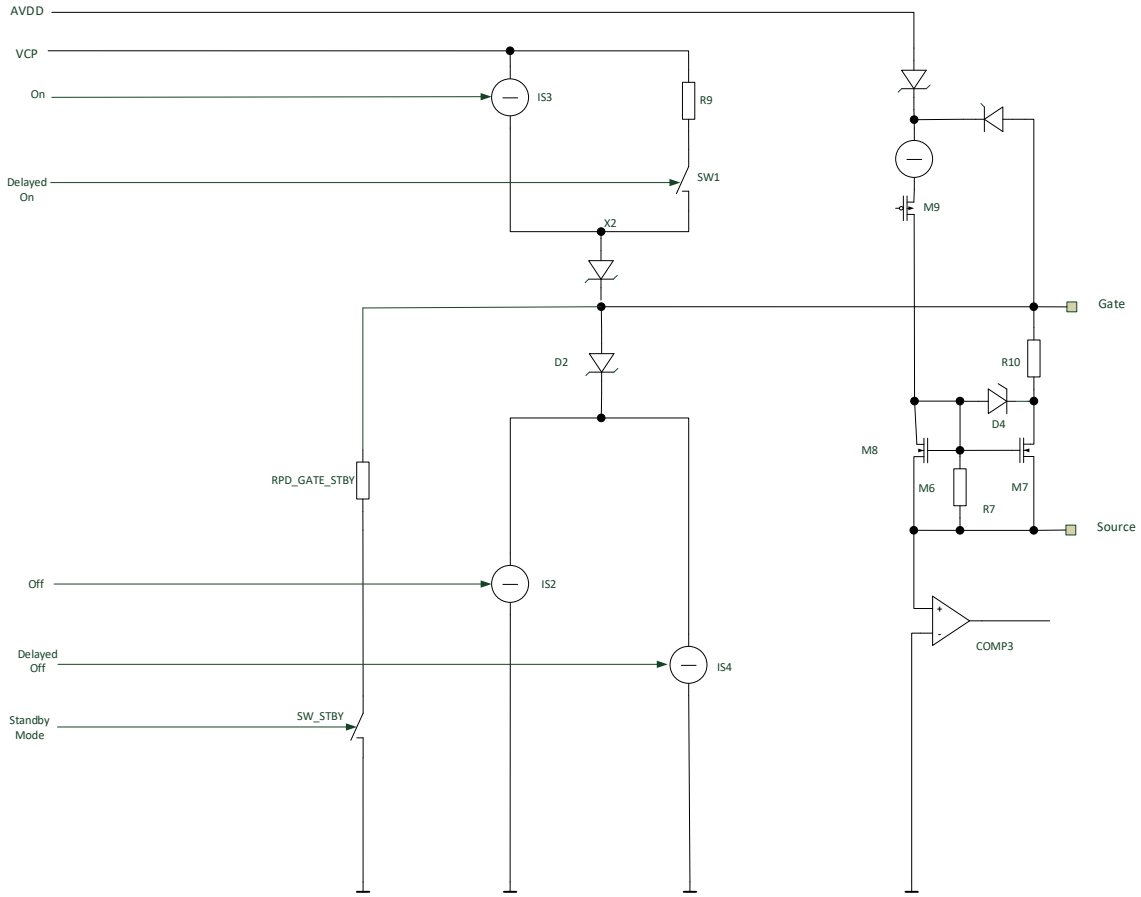


Figure 5. Simplified diagram of gate control

3.6 Reverse-Polarity Protection

Together with the application circuitry, the device protects against polarity reversal in the VBAT and T87 supply voltages. In Glow Plug applications, it also protects against positive and negative ground offset in the glow plug control unit compared to the ground of other control units or the glow plugs.

The reverse-polarity protection at T87 is an external Schottky diode.

Reverse-polarity protection at the ST input is guaranteed by an external series resistor of approx. 10 kΩ, which limits the injection current in the event polarity is reversed.

The DO_LIN pin is protected by an internal Schottky diode (see Figure 7); this prevents feedback from VCC in the device through this pin.

The voltage at the gate of the MIPP reverse-polarity protection FET is not monitored, so the application is responsible for enabling the MCH channel FETs only when MIPP is turned on.

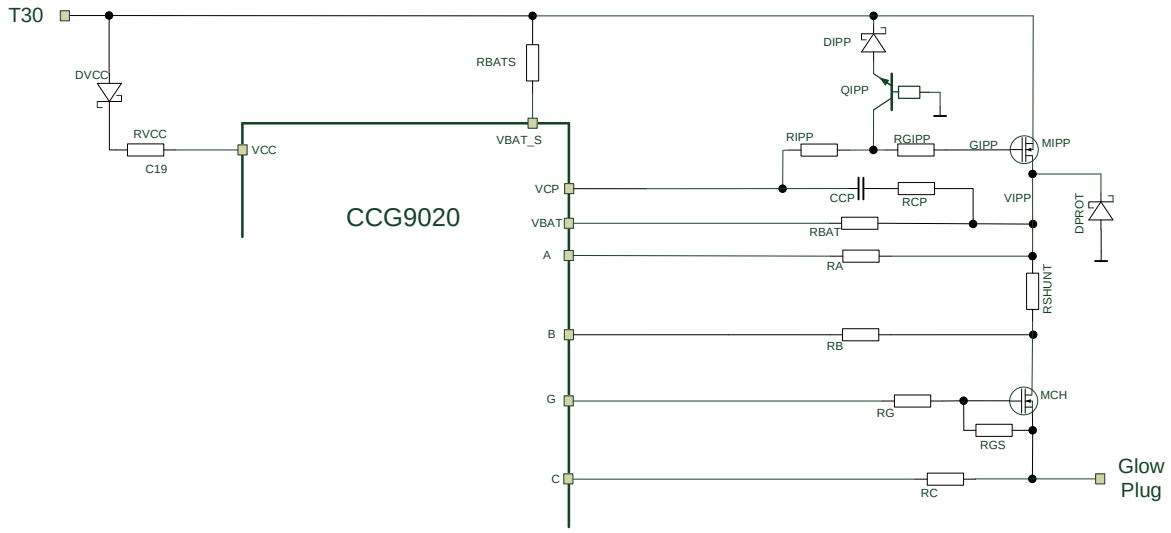


Figure 6. Simplified diagram of reverse polarity protection in the load path shows glow plug application

The principle of reverse-polarity protection in the load path is depicted in Figure 6. The load path is protected against reversed polarity by an external MIPP reverse-polarity FET. Since its source is connected to T30, its parasitic body diode also raises the VIPP node when T30 voltage is positive up to a diode voltage at the T30 level. This voltage remains at VBAT except for the voltage drop via RBAT. The charge pump's internal diode string also affects VCP and charges the external capacitor CCP.

During operation, VCP is pumped to VBAT + approx. 10 V and MIPP becomes low-impedance. Only now can a channel FET be activated to prevent the MIPP from being destroyed by the voltage drop through the body diode (and the resulting power dissipation).

In case V(T30) < V(GND), QIPP opens, short-circuiting GIPP against T30 via RGIPP (then the lowest potential). This locks MIPP, and VIPP as well as VBAT remain via GND.

The relatively high-impedance resistor RIPP limits the current from the VCP pin while also protecting the external bulk capacitor CCP from discharging too quickly from dynamic pulses.

As the only IC pin, VBAT_S is connected to T30 upstream of the reverse-polarity protection. This is protected by an adequately sized external series resistor for limiting injection current.

3.7 DIO_BUS/DO

The DO_LIN, RXD, TXD, and uDO pins refer to an integrated diagnostic/DIO_BUS block.

The DIO_BUS interface (bidirectional transceiver) is enabled by setting the DO_LIN bit in the Config register to 1. The DIO_BUS receives the data sent by the uC at the TXD pin. Received data is sent to the uC through the RXD pin. The DIO_BUS driver implements a low-side driver with slope regulation, short circuit current limiting and built-in series diode to protect the bus from ground offset. The DIO_BUS receiver implements the ratiometric thresholds to VCC.

When the DO_LIN bit in the Config register is set to 0, the DO_LIN pin acts as a pure low-side driver. The logic level received at uDO is output at DO_LIN. Also in this configuration, the DO_LIN pin has a regulated edge steepness, short circuit current limiting and a series diode to protect against ground offset. When DO_LIN = low, the level at TX is ignored and the RX state is high. In both modes, the DO_LIN pin has a chip-internal pull-up resistor against VCC. In standby, this resistor is disabled and is substituted by a pull-up power source provided VCC is powered and the DIO_BUS signal is selected as the wake-up condition.

In DIO_BUS mode, the duration of an output dominant level is limited to T_MAX_Dom. If TX stays low for an extended time, the DIO_BUS driver automatically switches to recessive until the next falling edge at TX.

The logic levels are relayed uninverted in both operating modes and in both directions (RX/TX), that is:

TXD/uDO = low => low-side driver enabled; TXD/uDO = high => DO_LIN high-impedance
DO_LIN = high => RXD = high (when DO_LIN = high); DO_LIN = low => RXD = low (when DO_LIN = high)
Depending on the state of the MODE pin and how the uDO pin is wired, the device can be woken up by a low level at DO_LIN (see section 3.1). This requires the DO_LIN detect low for a specified time at minimum (T_WU_DIO; see section 2.5.9).

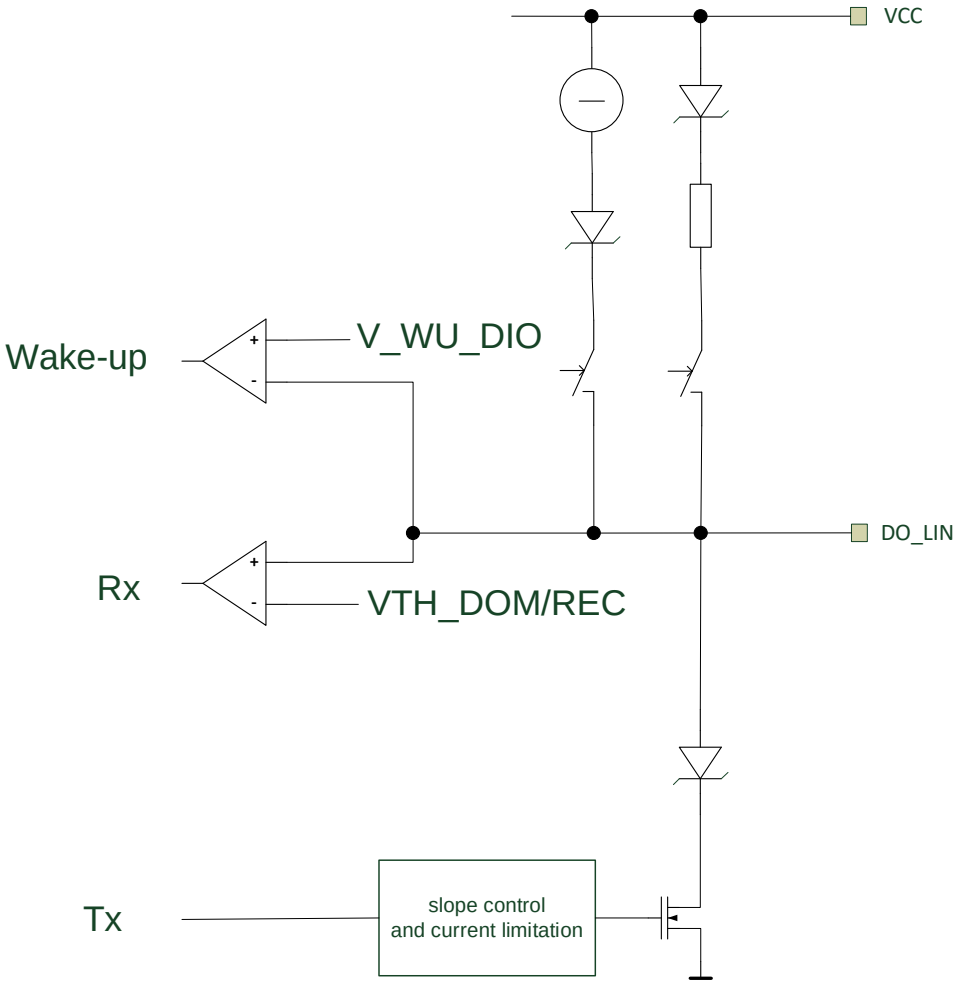


Figure 7. DIO_BUS/DO conceptual schematic

3.8 CI Input

The CI input receives the PWM signal from the engine control module (ECM) through the ST system pin.
The detected logic level is relayed uninverted to the uC through uCO.
Rising and falling edges at CI are debounced with a programmable time (ST_tdB; see section 4.1.7). A level change is only relayed when the signal remains stable without interruption for the recognized number of system cycles.
The CI input in the device is a high-impedance input. A series resistor prevents any feedback. The pull-up required at ST by the system must be supplied externally. In active mode, it is possible to measure the voltage at CI with the integrated ADC (see section 4.1.2).
Depending on the state of the MODE pin and how the uDO pin is wired, the device can be woken up by a low level at CI (see section 3.1). This requires the CI detect low for a specified time at minimum (T_WU_ST; see section 2.5.11).

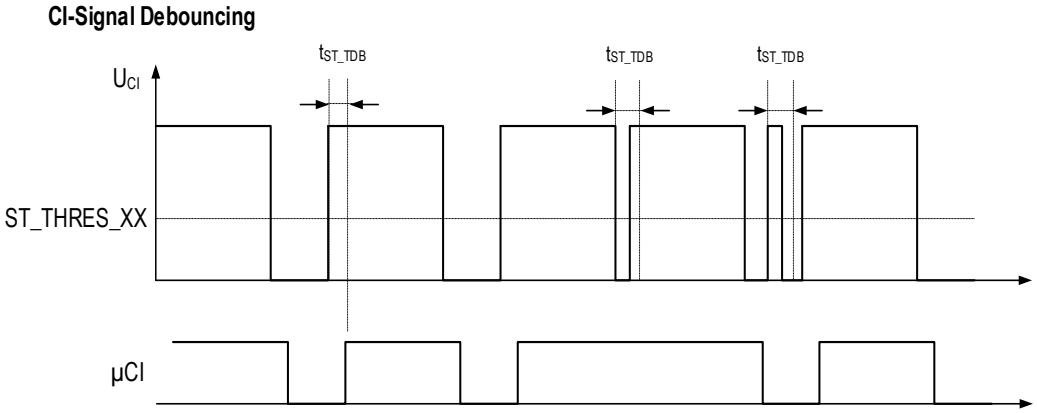


Figure 8. CI input debouncing

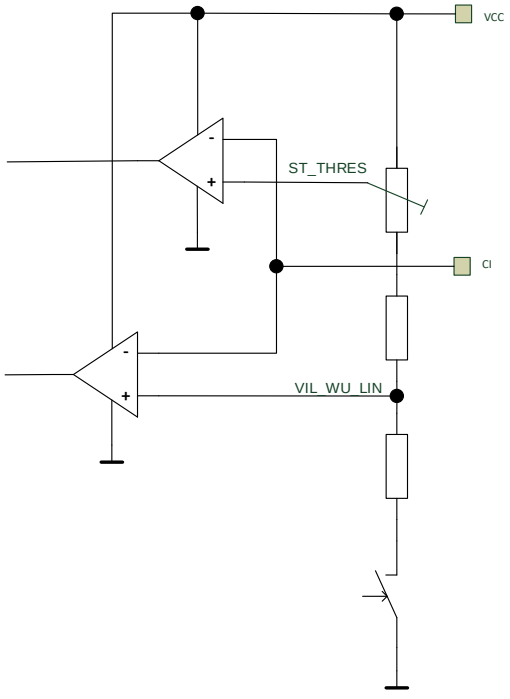


Figure 9. CI conceptual schematic

3.9 ADC

The device has a fully differential 10-bit ADC. The architecture is a two-step charge-balancing ADC. Readings are ordered by writing to one of the three VAD registers.

The conversion time is divided into 128 cycles at 8 MHz integration time, followed by 33 cycles at 8MHz fine-resolution time. The integration time is divided into 32 cycles of settling time (without integration), followed by 32 cycles in an initial integration phase. Then, the polarity of the internal offset compensation measurement channel is reversed, followed by another 32 cycles of a second settling time. This is followed by a second integration phase of 32 cycles. During the remaining 33 cycles at 8 MHz, the error from the first conversion is further resolved. During this second time, the conversion result is no longer influenced by a change in the measurement.

Once the entire conversion is complete (3 + 2 + 128 + 33 = 166 cycles at 8 MHz = 20.75 µs at typical oscillator frequency), the conversion result is stored and can be retrieved from the VAD register (see section 4.1.2).

The ADC uses the internal band gap as a reference. This means the VBG drift over temperature and life cycle is included in the conversion result.

The ADC has an internal channel multiplexer for measuring different voltages (see Table 33). Since the FSR, depending on the channel, extends well beyond the ADC's actual conversion range, internal voltage dividers are necessary. The resulting input impedance (see Table 24), together with the external series resistors, produces deviations that are factored in by the software. The FSR is designed so that, depending on the channel, even negative values are recorded in order to detect and be able to compensate for any system offsets. Offset measurements are included for this purpose (see Table 33). The recording of these offsets and their subtraction from the measurement can be used to increase measurement accuracy. Since the conversion time is completely controlled by the external uC, it is also possible to compensate for system offsets. For example, the measurement of voltage drop through a shunt in a channel that is off can be used also to compensate for external faults (for example, thermoelectric voltage).

Figure 10 shows the concept for the channel amplifier for measuring channel current and monitoring short circuits. The concept is based on the possibility of compensating for the amplifier offset by reversing the polarity of the amplifier and the measurement inputs halfway through the ADC’s integration time so the offset is canceled out at the end of the integration time. The switches S1 and S2 are used for this purpose. The source followers M1 and M2 realize the Aj and Bi inputs with as high of an impedance as possible so that, when S1 is switched, as few uncompensated errors as possible remain. They also ensure that the input voltages of OP1 and OP2 are so low that VBAT can produce effective negative feedback. OP1, OP2, M3 and M4 convert the differential voltage through the shunt into a proportional current. In turn, this current generates a differential voltage for the ADC in R5 and R6. The entire path is designed so that negative input voltages are included in the conversion range, even given the substantial offset voltages.

In addition to the (R5 + R6) to (R3 + R4) matching errors, the uncompensated amplification error in the circuit becomes dominantly affected through early voltage from M1 and M2.

In addition, a short circuit comparator (Comp1) is implemented (per channel). Due to the significantly lower accuracy requirements, this comparator is realized in an open-loop arrangement of two offsetting differential stages and a configurable reference voltage source (VTHRES). Chopper technology is also included here to compensate for the offset.

Since the ADC input and the short circuit comparator use the same switch S1 and the same source followers M1 and M2, the timings of the ADC and the short circuit comparators need to be coordinated with each other. This causes the starting of an ADC measurement (regardless of channel) to produce a delay in short circuit detection (see Table 46). If the started measurement is an offset measurement for the plug current of a channel, an additional delay occurs for this channel (see section 4.1.8).

The conversion result is stored in the VAD register as an unsigned integer with a value range of 0 to 1023 and the digital FSR (0 to 1023) is the FSR specified in Table 24. For a U30 measurement an LSB corresponds to a nominal change in input voltage of (32.8125 V - (-4.6875)) / 1024 = 36.62 mV. Since the digital offset from IC to IC can vary by the offset specified in Table 24, the lower/upper end of the analog FSR varies accordingly. This means the measuring range that is guaranteed to be usable by all ICs is smaller (see Table 24). Since a variation in offset concordantly affects both ends of the measuring range, the LSB is subject to a far lower variation. The impact of the varying offset can be greatly reduced by subtracting the result of an associated offset measurement (see Table 33) from the measured contents of the VAD register.

The actual ADC characteristic deviates from that of an ideal ADC in different ways (see section 2.5). This produces a deviation dM for the “true” measurement M that is close to the actual measurement. The actual measurement is the product of converting the numerical conversion result N (LSB), factoring in the typical FSR and offset values specified in section 3.9.

$$\text{Measurement M} = \frac{[\text{numerical conversion result N}]*[\text{full}-\text{scale range FSR}]}{1024} + [\text{analog offset}]$$

$$\text{Deviation dM} = \frac{\left(\left[\text{N x}\left[\text{error E}_{\text{gain}}\right] + \text{error E}_{\text{offset}}\right] + [\text{integral nonlinearity INL}]\right)\text{x FSR}}{1024} + \text{M x}\left(1 - \frac{\text{Vref}_{\text{current}}}{\text{Vref}_{\text{typical}}}\right)$$

Here, FSR describes the value interval (theoretically) assigned to the range 0 to 1023, for eample +156.3 mV - (-52.1 mV) = 208.4 mV for IGP1. Vref_current is the current Vref value at the time of measurement and Vref_typical is the typical Vref value (1.25 V) to which the FSR and offset in section 3.9 refer. The analog offset is the analog input corresponding to a digital value of 0. When the measurements are compensated by the measured offset, note that the result can be negative. This is why the software should have suitable arithmetic (16-bit signed).

The above formula for dM describes the actual error. For statistical expressions, the individual inputs can (depending on the assumption about correlation) be either added as absolutes (worst-case correlation) or added quadratically (no correlation). The above formula for dM also refers to a single measurement. When computing multiple measurements (for example, difference or quotient), the general error propagation methods should be applied. However, note that errors referring to the ADC characteristic in its entirety (for example, Vref, gain error, offset) do not change in the short term under identical conditions (in the same measurement channel). For example, the error in Vref factors out when calculating the quotient of two measurements taken close together.

The measurements taken with the ADC need to be averaged according to the software. This notably applies to the channel current.

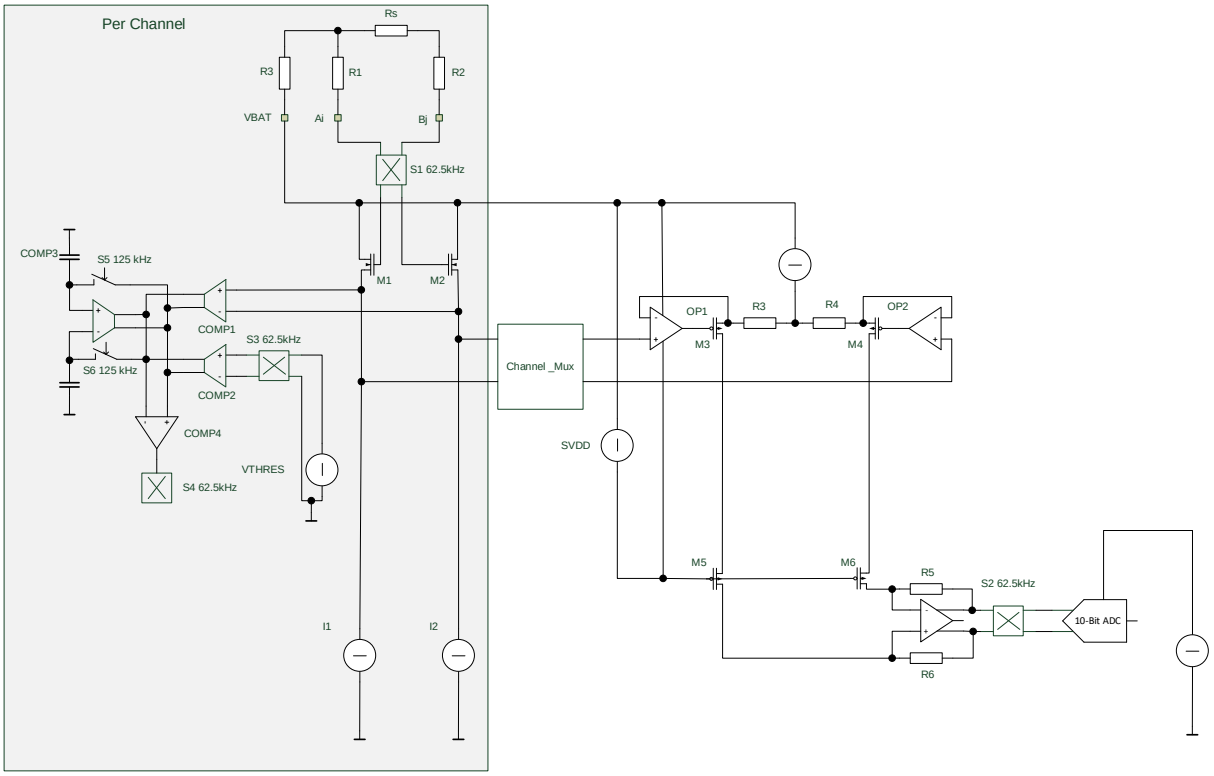


Figure 10. Simplified diagram of channel amplifier and short circuit comparators

Table 24. FSR of AD channels (see section 3.9)

AD channel	Typical FSR Note 2	Typical digital offset (Digital value when analog 0)	Typical input impedance/input current
IGP1…IGP5	(-¼ to ¾) x Vref ÷ 6 (-52.1 mV to 156.3 mV) Of which usable: (0 to ½) x Vref ÷ 6 0 to 104 mV Note 1	0 to 512, typically 256	>100 kΩ
IGP1ofs… IGP5ofs	(-¼ to ¾) x Vref ÷ 6 (-52.1 mV to 156.3 mV) Of which usable: (0 to ½) x Vref ÷ 6 0 to 104 mV Note 1	0 to 512, typically 256	>100 kΩ
UGP1…UGP5	(-15/4 to 105/4) x Vref -4.6875 V to 32.8125 V Of which usable: -3.9 V to 29 V Note 4	106 to 149, typically 128	Note 3
U30	(-15/4 to 105/4) x Vref -4.6875 V to 32.8125 V Of which usable: 0V to 29 V Note 4	106 to 149, typically 128	Note 3
U87	(-15/4 to 105/4) x Vref -4.6875 V to 32.8125 V Of which usable: 0 V to 29 V	106 to 149, typically 128	Note 3
UCP	(-15/4 to 105/4) x Vref -4.6875 V to 32.8125 V Of which usable: 0V to 29 V Note 4	106 to 149, typically 128	Note 3
UCI	(-15/4 to 105/4) x Vref -4.6875 V to 32.8125 V Of which usable: 0V to 29 V Note 4	106 to 149, typically 128	Note 3
HVofs	(-15/4 to 105/4) x Vref -4.6875 V to 32.8125 V Of which usable: -3.9 V to 29 V Note 4	106 to 149, typically 128	
UVDD	(-5/8 to 35/8) x Vref -0.78125 V to 5.46875 V Of which usable: -0.65V to 5.34V	107 to 148, typically 128	>35 kΩ
UVDDofs	(-5/8 to 35/8) x Vref -0.78125 V to 5.46875 V Of which usable: -0.65V to 5.34V	107 to 148, typically 128	

AD channel	Typical FSR Note 2	Typical digital offset (Digital value when analog 0)	Typical input impedance/input current
TASIC	-70 °C to 170 °C	Offset for 27 °C is in TASICofs	
TASICofs	See Table 33. ADC channels		

Note 1 Due to the channel amplifier's offset compensation concept (see Figure 10), the 25% at the top and bottom of the FSR are unusable.

Note 2 The figures refer to Vref = 1.25 V.

Note 3 During measurement, the voltage is approx. 1.8 V with a typical internal resistance of 300 kΩ. At an unselected input, a resistance of approx. 300 kΩ to XGND is effective.

Note 4 The full range is usable from VCC > VCC_4_min. For VCC_4_min > VCC > VCC_1_min, the measuring range saturates at approx. 16 V.

Clarification and Examples of ADC Temperature Measuring via TASIC and TASICofs

The device's junction temperature T_J can be measured with the ADC. The current temperature is detected as a 10-bit unsigned value when selecting the ADC channel TASIC. The following applies:

- Low values correspond to lower temperatures.
- High values correspond to higher temperatures.
- The 10-bit value is proportional to the temperature; the constant of proportionality is TEMPpc = 2.75 LSB/K.

In order to be able to compensate for fabrication-related tolerances as much as possible, the result of the temperature measurement for 27 °C is stored as TASICofs during the device end-of-line test.

The temperature currently measured is calculated as follows:

Measured temperature = (TASIC - TASICofs) / TEMPpc + 27 °C

Table 25. Example 1 of calculated measured temperature

TASIC binary	TASIC decimal	TASICofs binary	TASICofs decimal	TASIC - TASICofs decimal
01 0111 0100	372	01 0100 0100	324	48

Given these values:

Measured temperature = (TASIC - TASICofs) / TEMPpc + 27 °C = 48 / 2.75 LSB/K + 27 °C = 44.45 °C

Table 26. Example 2 of calculated measured temperature

TASIC binary	TASIC decimal	TASICofs binary	TASICofs decimal	TASIC - TASICofs decimal
00 1010 0000	160	01 0101 0000	336	-176

Given these values:

Measured temperature = (TASIC - TASICofs) / TEMPpc + 27 °C = -176 / 2.75 LSB/K + 27 °C = -37 °C

3.10 JTAG Interface

The device has a JTAG interface that, together with the pins TBA and TRST, are intended only for fabrication testing on the device. They have no functionality for the application or the module test, so the TRST and TBA pins should be hardwired to ground in any application. In addition to the TRST pin, the JTAG interface uses the SSI (TMS), SCLK (TCK), MOSI (TDI) and MISO (TDO) pins.

AVDD must be powered (possibly externally) in order to use the JTAG interface. The JTAG state machine is powered by VSTBY, meaning the JTAG interface is only functional when VSTBY is present (see section 3.1).

3.11 Digital Function

3.11.1 uRESET Pin

The uRESET pin is used to reset the external uC during startup or due to various error conditions (see section 4.1.3). The digital section ensures that an enabled reset is released no sooner than after t_min_reset (min. reset pulse length; see section 2.5.4).

3.11.2 SPI Interface

The SPI interface is for bidirectional communication with an external uC and is powered from uVDD. The external uC acts as a bus master. The clock polarity is clock idle high. Both modules - master and slave - modify the data (MOSI/MISO) after a falling edge at SCLK and sample the data with the rising edge. The max. data rate is 8 MHz. All access occurs in blocks at multiples of 16-bit and are MSB-first.

For write access, the data is applied to the addressed register at every 16th rising edge at SCLK. Any excess cycles are ignored.

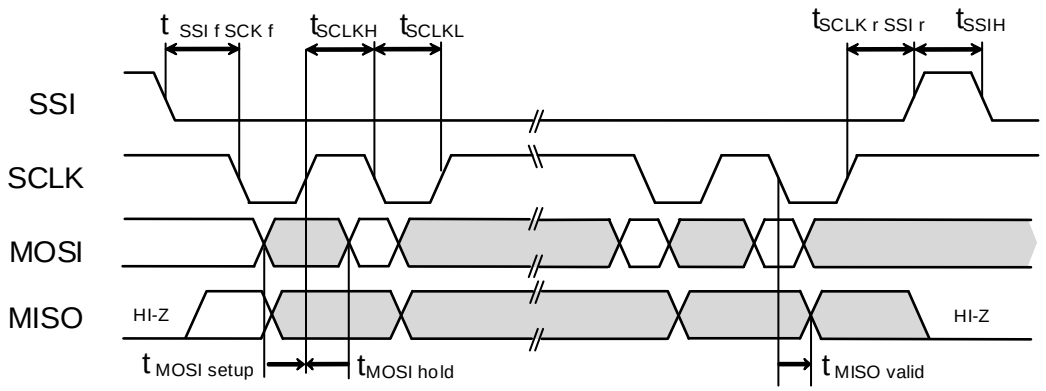


Figure 11. SPI timing

4. Register Definitions

4.1 Register Map

Every SPI access refers to the internal register map. The registers are arranged into 32 words with 10 bits of data each. Unless otherwise specified, all registers lose their stored data in standby mode.

Table 27. Register map

Register name	Address	R/W	Description
Version-Reg	0	R	Device version number
VAD_1	1	R/W	Virtual ADC register
VAD_2	2	R/W	Virtual ADC register
VAD_3	3	R/W	Virtual ADC register
State	4	R/W	Error status, wake-up status
Config	5	R/W	General configuration data
Chctrl	6	R/W	Static FET channel enabling
Chconfig	7	R/W	Gate control configuration
STconfig	8	R/W	CI interface configuration
ThShort	9	R/W	Short circuit detection threshold
ChShort	10	R/W	Short circuit detection
IRiseFall	11	R/W	Gate charging and discharge current from FET 1 to FET 5
TWdog	12	R/W	Software watchdog elapsed time
WdogReset	13	R/W	Watchdog reset by write access with magic number
DIOReg	14	R/W	DIO interface settings
Chip-ID1	15	R	Word High
Chip-ID2	16	R	Word Low

Every SPI access is initiated by the master (uC) and has the following pattern:

Table 28. SPI data format

D15–D11	D10	D9–D0
MOSI		
Register address	RW	Write data if RW = low,“don’t care” if RW = high
MISO		
Status	0	Read data if RW = high, “don’t care” if RW = low

RW = high, read access

RW = low, write access

When RW = high, the device responds at MISO with the contents of the register addressed by D15 to D11 (MOSI) in the same access.

The device outputs the 5-bit status word during every SPI access, which contains the following:

Table 29. Status data format

D15	D14	D13	D12	D11	D10
E_ASIC	K-Bit	AD_BUSY_3	AD_BUSY_2	AD_BUSY_1	0

E_ASIC bit — Copy of the corresponding bit from the State register (see section 4.1.3).

K bit — Or-ing of bits K1–K5 from the ChShort register (see section 4.1.9); signals the occurrence of a short circuit in at least one channel.

AD_BUSY_x — High: The assigned VAD register has been used to order a conversion that is not yet complete. Any further write access to the corresponding VAD register is ignored. Data retrieved from the assigned VAD register is invalid.

Low: The data from the last conversion is in the corresponding VAD register. New conversions can be ordered via write access.

4.1.1 Version Register

Table 30. Version register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	Major version					Minor version				
R/W	R	R	R	R	R	R	R	R	R	R

4.1.2 VAD Register

The device has three virtual ADC registers (VAD registers) for starting ADC measurements and retrieving the results. Every VAD register is assigned its own AD_BUSY bit in the status word.

The three VAD registers operate independently of one another, however, physically only one ADC is integrated. At the end of a successful write access to one of the three VAD registers, the corresponding AD_BUSY bit is set. If no conversion is active, the ADC begins a measurement that is assigned to the VAD register with an active AD_BUSY bit. If multiple VAD registers have an active BUSY bit, the next VAD register in line for writing with AD_BUSY = high is selected (FIFO principle). To order an AD measurement, the uC writes data as per Table 31 to one of the three VAD register addresses. When the AD_BUSY bit assigned to this channel is low during this write access, the order is accepted and the result can be retrieved later at the same address. Otherwise the order is rejected.

Table 31. VAD write access data format

D15–D11	RW	D9–D0
MOSI		
1, 2 or 3	0	ADC channel for the next conversion (“don’t care” if the AD_BUSY bit is high)
MISO		
Status	0	Result of the last conversion from this VAD register (“don't care” if the AD_BUSY bit is high)

Every time one of the three VAD registers is accessed (whether read or write), the device responds with the result of the last conversion ordered via this VAD register. Should the last conversion ordered not yet be complete, the corresponding AD_BUSY bit is high and the data on the MISO is ignored.

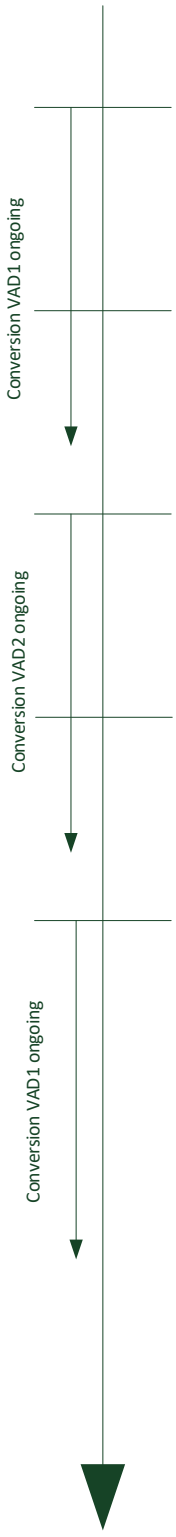
Table 32. VAD read access data format

D15–D11	RW	D9–D0
MOSI		
1, 2 or 3	0	“don't care”
MISO		
Status	0	Result of the last conversion from this VAD register (“don't care” if the AD_BUSY bit is high)

Table 33. ADC channels

AD channel	D9–D0 in VAD at MOSI	Measurement
IGP1	0	Voltage via Shunt 1 (FET 1 current)
IGP2	1	Voltage via Shunt 1 (FET 2 current)
IGP3	2	Voltage via Shunt 1 (FET 3 current)
IGP4	3	Voltage via Shunt 1 (FET 4 current)
IGP5	4	Voltage via Shunt 1 (FET 5 current)
IGP1ofs	5	FET 1 shunt offset voltage
IGP2ofs	6	FET 2 shunt offset voltage
IGP3ofs	7	FET 3 shunt offset voltage
IGP4ofs	8	FET 4 shunt offset voltage
IGP5ofs	9	FET 5 shunt offset voltage
UGP1	10	C1 pin voltage
UGP2	11	C2 pin voltage
UGP3	12	C3 pin voltage
UGP4	13	C4 pin voltage
UGP5	14	C5 pin voltage
U30	15	VBAT_S pin voltage
U87	16	MODE pin voltage
UCP	17	VCP pin voltage to ground
UCI	18	CI pin voltage
UHVofs	19	Offset for all measurements in 30 V range
UVDD	20	uVDD voltage
UVDDofs	21	uVDD offset voltage
TASIC	22	Device junction temperature (T_J)
TASICofs	23	T_J offset at 27 °C (stored in device end-of-line test)

For a detailed description of the ADC channels, see section 3.9.



MOSI	0x0803	Conversion from IGP4 in VAD1
MISO[15:11]	E,K,0,0,0	Status
MISO[10:0]	0xyyy	Result of an earlier Conversion at VAD1

MOSI	0x100f	Conversion from u30 in VAD2
MISO[15:11]	E,K,0,0,1	Status, VAD1 busy
MISO[10:0]	0xyyy	Result of an earlier Conversion at VAD2

MOSI	0x0802	Conversion from IGP3 in VAD1
MISO[15:11]	E,K,0,1,0	Status, VAD2 busy
MISO[10:0]	0x013	Order accepted, VAD2 busy IGP4:0x13

MOSI	0x1011	Conversion from Vcp in VAD2
MISO[15:11]	E,K,010	Status,VAD2 busy, Order NOT accepted
MISO[10:0]	0xyyy	Don't care

MOSI	0x1011	Conversion from Vcp in VAD2
MISO[15:11]	E,K,0,0,0	Status
MISO[10:0]	0x0027	U30: 0x27

Figure 12. Example of VAD register use

4.1.3 State Register

This register stores the cause of the last wake-up and internal device errors.

Table 34. State register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
4	E_ASIC	F-Err				WWdogH	WWdogS	WMode	WDIO	WCI
R/W	R/W	R	R		R	R/W	R/W	R	R	R
State after startup	1					Depending on wake-up/cause of reset				

Wake-up bits:

Bits D3–D0 show the cause of the last wake-up.

WMode: Wake-up due to high at MODE

WDIO: Wake-up due to DIO_BUS

WCI bit: Wake-up due to low at CI

The wake-up bits are only updated after a preceding standby mode, that is, when either VDD_ON was previously set to low or VSTBY was too low (because there was no sufficient VCC).

For details on the wake-up mechanism, see section 3.1.

Reset without another Wake-Up:

Of the errors that result in the uC and the internal logic being reset without another wake-up, only some are shown in special bits:

WWdogH: Reset due to hardware watchdog being triggered

WWdogS: Reset due to software watchdog being triggered

Other errors that result in the uC and the internal logic being reset without another wake-up but that are not signaled as separate errors in the State register:

- UVD at AVDD, DVDD or uVDD
- Over-temperature detection
- Fuse CRC error

The WWdogH and WWdogS software are latching and must be deleted by overwriting with 1.

Errors without Resetting the uC:

These bits signal internal errors that result in the drivers being shut down but not to the uC being reset. Device function starts automatically as soon as the error condition is rectified. The gate drivers, however, are only reenabled after another rising edge at uGi or after Fi is set again in the Chctrl register.

This can result in the error condition no longer existing by the time of the next uC scan (for example, because, in case of an F-Err, the Chctrl register had already been overwritten with correct data but the E_ASIC bit is still 1).

The E_ASIC bit is set in the event of the following:

- VCP_VBAT under-voltage
- VBAT_SVDD under-voltage
- VBAT_S under- or over-voltage
- Chctrl CRC error in the Chctrl register (combinational check)

The conditions for setting the E_ASCI bit also result in the charge pump being disabled but only as long as the condition is active. VCP_VBAT undervoltage itself does NOT result in the charge pump being disabled, rather to all gate drivers being disabled.

The E_ASCI bit is latching and must be actively reset by writing it to 1.

Note that, after a wake-up, the E_ASIC bit is set since VCP_VBAT_S is initially too low. This means it should be deleted by the CPU after a successful startup.

F-Err bit: This bit signals the occurrence of a Chctrl CRC error in the Chctrl register (the E_ASIC bit is also set).

Other errors that result in the drivers being shut down without the uC being reset and that are not signaled in the State register include the occurrence of a short circuit in a channel i.

This results in the Ki bit being set in the ChShort register and the affected channel being shut down but not to the E_ASIC bit or F-Err bit being set.

4.1.4 Config Register

This register allows the self-holding to be controlled and switching between DIO_BUS and DO.

The debounce time for voltage monitoring can also be selected.

The entire register permits write and read access.

Table 35. Config register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
5	TBD	WDW_1	WDW_0	Ptdb1	Ptdb0	S_OVD1	S_OVD0	DO_LIN	VDD_ON	SH_ON
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	1	1	0

VDD_ON This bit controls the LDOs. VDD_ON is set on startup. The LDOs stay active until this bit is written to low or until V(T87) AND (when SH_ON is set) VBAT drop too low.

SH_ON Setting this bit (self-holding) allows VCC to be powered from T30 if VCC is drops too low (for self-holding, see section 3.1).

DO_LIN High: DO acts as DIO_BUS; low: DO acts as a diagnostic output and is controlled by uDO. If DO_LIN = 1, the uDO input is disabled and can remain unwired.

S_OVDx These bits determine the OVD threshold at V_BAT_S (see section 2.5.2).

Ptdbx These bits determine the debounce time for UVD detection at MODE, VBAT_S and VCP_VBAT as well as for OVD detection at VBAT as per Table 36.

WDW_y These bits determine the start of the validity window for write access in the WDogReset register (see section 4.1.11).

Table 36. Programmable debounce times for voltage monitoring

Ptdb1	Ptdb0	UVD_SVDD debounce time (µs)	UVD_VBAT_S debounce time (µs)	UVD_VCP_VBAT debounce time (µs)	OVD_VBAT_S debounce time (µs)
0	0	100	200	100	350
0	1	100	400	200	700
1	0	100	800	400	1400
1	1	100	1600	800	2800

The times in Table 36 are subject to variations as per F_OSC.

Table 37. Programming the validity window for the software watchdog

WDW_1	WDW_0	Start of Validity Window
0	0	0% of software watchdog elapsed time
0	1	25% of software watchdog elapsed time
1	0	50% of software watchdog elapsed time
1	1	75% of software watchdog elapsed time

4.1.5 Chctrl Register

This register makes it possible to control individual channels independently of uGi.

Table 38. Chctrl register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
6	F5	F4	F3	F2	F1	CRC4	CRC3.	CRC2	CRC1	CRC0.
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	0	0	0

Fi Writing Fi to high enables the corresponding channel (regardless of the state of uGi).

CRCi In these bits, the uC must write the result of CRC $X^5 + X^2 + 1$ applied to the F5 to F0 data (see section 4.1.3).

4.1.6 Chconfig Register

This register makes it possible to configure the gate control functions globally for all channels.

Table 39. Chconfig register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
7	TR20	TBD	TBD	TBD	EN_DLY5	EN_DLY4	EN_DLY3	EN_DLY2	EN_DLY1	EN_DLY0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	0	0	0

The TR20 bit enables a smaller holding resistance between Gi and VCP. When TR20 is low, the holding resistance is greater.

The delay time TDLY_GUP is configured with the bits EN_DLY[5:0]. For EN_DLY[5:0] = 0, the delay is disabled; for the other values, the delay time is calculated using the following formula:

TDLY_GUP = (32 x EN_DLY - 1) ÷ F_OSC

For the typical oscillator frequency F_OSCtypical, this would result in, for example:

Table 40. Typcial oscillator frequency

EN_DLY5	EN_DLY4	EN_DLY3	EN_DLY2	EN_DLY1	EN_DLY0	
0	0	0	0	0	0	Delay disabled
0	0	0	0	0	1	1.94 µs
0	0	0	0	1	0	3.94 µs
0	0	0	0	1	1	5.94 µs
…	…	…	…	…	…	…
1	1	1	1	1	0	123.94 µs
1	1	1	1	1	1	125.94 µs

4.1.7 STConfig Register

This register is used to configure the CI input and permits write and read access.

Table 41. STconfig register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
8			ST_Thres_up			ST_Thres_down			ST_Tdb1	ST_Tdb0
R/W	R/W	R/W	R/W			R/W			R/W	R/W
State after startup	0	0	1	0	0	0	1	0	0	0

The bits ST_Thres_up and ST_Thres_down determine the VIH and VIL input levels at CI relative to VCC during operation (not for wake-up).

Table 42. Thresholds at ST (during operation)

ST_Thres_xx	Typical threshold
0	40% VCC
1	60% VCC
2	70% VCC
3	75% VCC
4	80% VCC
5	85% VCC
6	85% VCC
7	85% VCC

The software is responsible for ensuring that the threshold for the rising edge is greater than for the falling edge.

The threshold for wake-up via ST is 75% of VCC.

ST_Tdb1 and ST_Tdb0 define the debounce time for rising and falling edges at CI (see section 3.8).

Table 43. Debounce time coding at ST (during operation)

ST_Tdb	Typical debounce time (µs)
0	250
1	500
2	750
3	1000

A change of state is only relayed when the new state persists uninterrupted for the programmed debounce time.

4.1.8 ThShort Register

This register stores the thresholds for the short circuit shutdown.

The listed voltages specify the voltage drop between Aj and Bi (see section 3.4).

Table 44. ThShort register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
9	thres_3	thres_2	thres_1	thres_0	TAV2	TAV1	TAV0	Tdb2	Tdb1	Tdb0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	0	0	0

The bits thres_3 to thres_0 determine the short circuit threshold for channels 1 to 5.

In both cases, the thresholds are coded according to the following table:

Table 45. Short circuit threshold coding

thres_3 to thres_0	Typical threshold (Aj - Bi) Note 1
0	8/192 * Vref_int (52.0 mV)
1	9/192 * Vref_int (58.6 mV)
2	10/192 * Vref_int (65.1 mV)
3	11/192 * Vref_int (71.6 mV)
4	12/192 * Vref_int (78.1 mV)
5	13/192 * Vref_int (84.6 mV)
6	14/192 * Vref_int (91.1 mV)
7	15/192 * Vref_int (97.7 mV)

thres_3 to thres_0	Typical threshold (Aj - Bi) Note 1
8	16/192 * Vref_int (104 mV)
9	18/192 * Vref_int (117 mV)
10	20/192 * Vref_int (130 mV)
11	22/192 * Vref_int (143 mV)
12	24/192 * Vref_int (156 mV)
13	26/192 * Vref_int (169 mV)
14	29/192 * Vref_int (189 mV)
15	32/192 * Vref_int (208 mV)

Note 1 i (1–5) indicates the channel, j = (0, 1) – depending on which i: j = 0 for i = (1, 2), j = 1 for i = (3, 4, 5).

Note 2 Vref_int is nominally 1.25 V.

The bits Tbd2 to Tbd0 (debounce time) determine the digital debounce time for short-circuit detection globally for all channels. The short-circuit comparators typically deliver a new sample every 8 µs. Due to the prioritization of the ADC measurements, a cycle delay can occur after an AD conversion is started. As a result, every third comparator value may be delayed by no more than an additional 8 µs. If the started measurement is an offset measurement for the plug current of a channel, an additional delay occurs for this channel of up to 16 µs.

For this reason, an uninterrupted series of offset measurements for the plug current of one and the same channel results in the short-circuit detector for this channel being disabled for the duration of the offset measurements.

If a comparator sample is high (short-circuit threshold exceeded), an internal counter is incremented; if low, it is decremented. The short-circuit is detected when the counter reading programmed as per Table 46 is reached.

Factoring in the aforementioned cycle delay due to AD conversions (no offset measurement), the indicated trigger delays occur based on the value of Tbd0 to Tbd2 when the short circuit comparator responds without bouncing.

Table 46. Short circuit detector debounce times

Tdb2, Tdb1, Tdb0	No. samples for debouncing short-circuit detector	Trigger delay w/o bouncing (µs)
0	1	8 to 16
1	2	16 to 24
2	3	24 to 40
3	4	32 to 48
4	5	40 to 64
5	6	48 to 72
6	8	64 to 96
7	10	80 to 120

The time for deactivating the GS short-circuit on a falling edge (to avoid an avalanche breakdown) can also be selected (see section 3.5). The values can be configured globally for all channels in this register.

Table 47. VGS short circuit dead time on gate shutdown

TAV2–TAV0	Dead time [µs]
0	0
1	60
2	120
3	180
4	240
5	300
6	360
7	420

4.1.9 ChShort Register

This register makes it possible to read and reset the short-circuit detector.

Table 48. ChShort register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10	TBD	TBD	TBD	TBD	TBD	K5	K4	K3	K2	K1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	0	0	0

The bits K5–K1 are set by an overcurrent event in the respective channel. As long as a Ki bit is high, the corresponding channel is shut down. These bits are latching, that is, if they were set by an error condition, they are only reset by the uC overwriting with high or by activating standby mode.

The gate drivers, however, are only reenabled after another rising edge at uGi or after Fi is set again in the Chctrl register.

Bits K5 to to K1 are deleted via write access with high. Overwriting with low has no effect.

4.1.10 IRiseFall Register

In this register, the charging (IR3 to IR0) and discharge (IF3 to IF0) currents for controlling the channel FET gates are specified. The values apply globally to all channels.

Table 49. IRiseFall register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11	TBD	TBD	IF3	IF2	IF1	IF0	IR3	IR2	IR1	IR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	0	0	0

Table 50. Programming the gate control currents

IR3 to IR0 / IF3 to IF0	I rise/fall nominal value (µA)
0	150
1	200
2	250
3	300
4	400
5	500
6	600
7	800
8	1000
Other	150

4.1.11 TWdog Register

In this register, the software watchdog elapsed time is configured. The software watchdog is derived from the internal oscillator. The data refers to the nominal position of the oscillator frequency.

The software watchdog is reset by writing the WdogReset register (see section 4.1.12) with a magic number. Write access with the magic number that is not within the validity window triggers the watchdog. Write access with other data is ignored. The validity window begins at x% of the programmed elapsed time after the last reset. The percentage x is configured in the Config register (see section 4.1.4). When the programmed elapsed time since the last reset is reached, all channels are shut down and the uRESET pin is switched to low for 100 µs. The event is displayed in the State register (see section 4.1.3).

When the TWdog register is written to 0, the software watchdog is disabled.

To prevent the unintentional triggering of the watchdog when changing the elapsed time, it is recommended to first disable the watchdog by writing TWdog = 10'h000 and then setting the new value.

Table 51. TWdog register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	1	1	1	1	1	1	1	1	1	1

Table 52. Software watchdog elapsed time coding

T9–T0	Nominal elapsed time
0	Software watchdog disabled => no triggering
1	1 * 1 / 4 MHz * 32768 (8.192 ms)
2	2 * 1 / 4 MHz * 32768 (16.38 ms)
…	…
1021	1021 * 1 / 4 MHz * 32768 (8364 ms)
1022	1022 * 1 / 4 MHz * 32768 (8372 ms)
1023	2^30 * 1 / 4 MHz (268435 ms) (To ensure programming time for uC flashing process MEE fabrication)

4.1.12 WdogReset Register

The software watchdog is reset by writing this address with the magic number 0x2A5 as data

(D9–D0). This means 16'h6AA5 must be sent via MOSI overall. Write access with the magic number that is not within the validity window triggers the watchdog (see section 4.1.11).

The last value written is always read back.

Table 53. WdogReset register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
13										
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	0	0	0

4.1.13 DIOReg Register

In this register, settings for the DIO_BUS interface are configured (for example, debounce time setting during operation, not wake-up).

Table 54. DIOReg register

Address	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
14								DIOTdb2	DIOTdb1	DIOTdb0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
State after startup	0	0	0	0	0	0	0	0	0	0

Table 55. DIO_BUS debounce time coding

DIOTdb2–DIOTdb0	Debounce time [µs]
0	No digital debouncing
1	0.5
2	1.0
3	2.0
4	3.0

4.1.14 Chip-ID Registers, Address 15 and Address 16

These registers contain a common consecutive identification number (in encoded form, identification number = Chip_ID1 * 1024 + Chip_ID2) and are used for traceability. It is recommended to ensure the traceability of this identification number in the supply chain up to and including the vehicle identification number.

5. Package Information

5.1 Package Outline

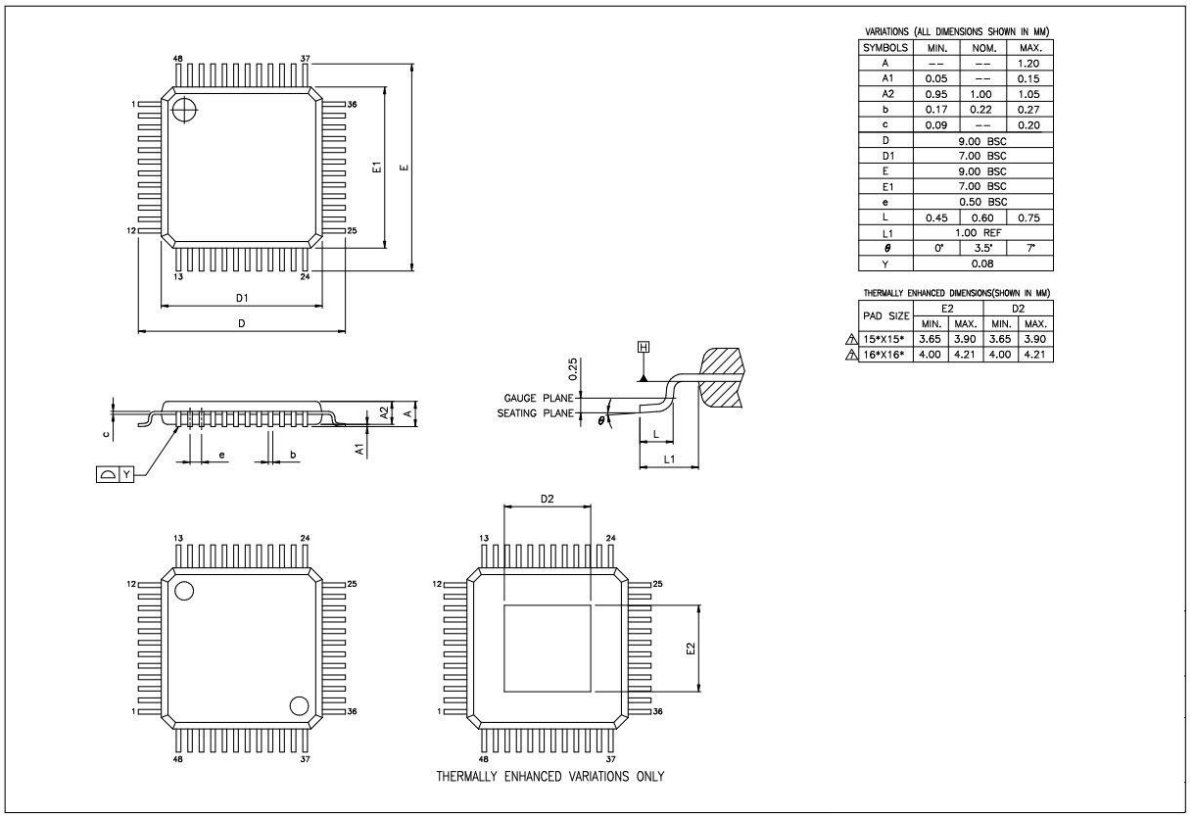


Figure 13. TQFP package outline drawing

The exposed pad used is 16 x 16.

The marking comprises the following:

Line 1: CCG9020.X.d
Line 2: YYWW (date code)
Line 3: Semiconductor manufacturer lot number

X: Major version of the photomask set starting with A
d: Minor version of the photomask set starting with 1

5.2 Moisture Sensitivity Level

The device meets the requirements according to MSL-3 of JEDEC standard J-STD-020E.

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in Table 56.

For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020E, which can be downloaded from http://www.jedec.org.

Table 56. MSL classification

MSL level	Floor lifetime	Conditions
MSL 4	72 hours	30°C/60% RH
MSL 3	168 hours	30°C/60% RH
MSL 2A	4 weeks	30°C/60% RH
MSL 2	1 year	30°C/60% RH
MSL 1	Unlimited	30°C/85% RH

6. Application Information

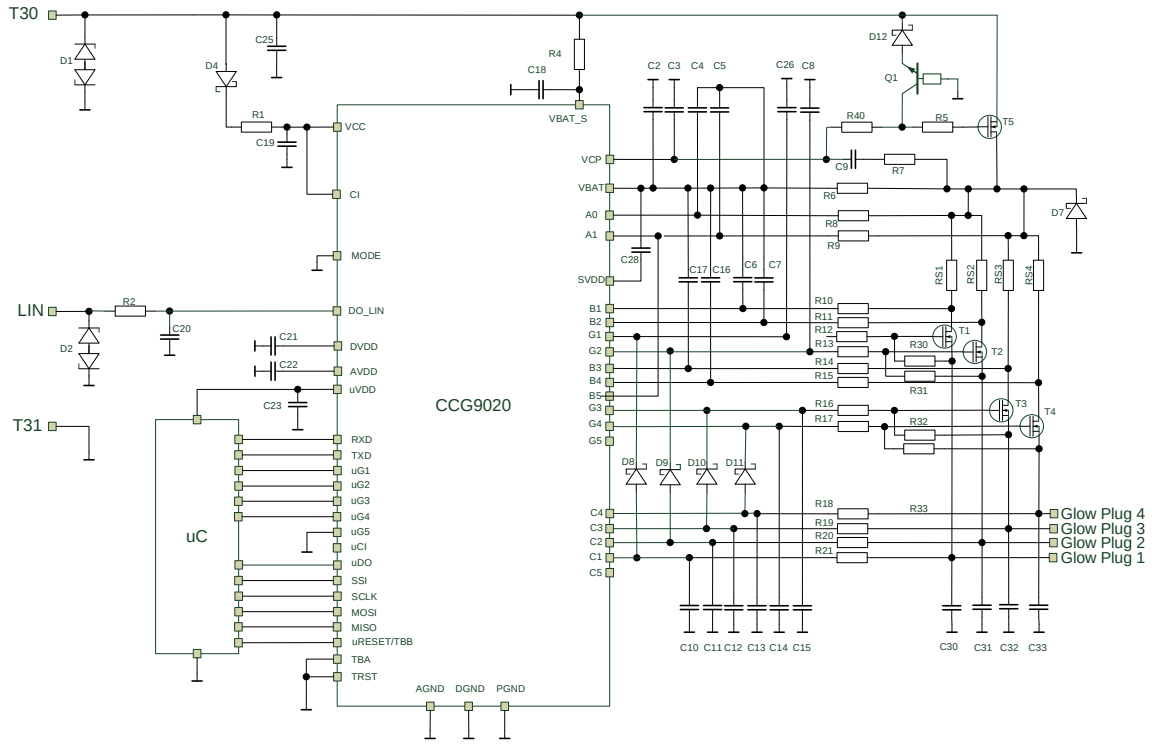


Figure 14. Sample wiring for a four-channel T30 application with DIO_BUS, glow plug application

Table 57. Sample sizing for a four-channel T30 application with DIO_BUS

Component	Value	Comment
R1	22 Ω	
R2	2.2 Ω	
R4	220 Ω	
R5	10 Ω up to 100 Ω	T5 gate must be able to be discharged with sufficient speed
R6	47.5 Ω	
R7	100 Ω	
R8, R9	1 kΩ	
R10, R11, R14, R15	1 kΩ	
R12, R13, R16, R17	1 kΩ	
R18, R19, R20, R21	100 Ω	
R30, R31, R32, R33	270 kΩ	
RS1, R2, RS2, RS3	1.3 mΩ	
R40	100 kΩ	
C1	1 nF	
C2	100 nF	
C3	1 nF	
C4, C5	470 pF	
C6, C7, C16, C17	470 pF	
C8, C14, C15, C26	100 pF	
C9	220 nF	
C10, C11, C12, C13	1 nF	
C18	10 nF	
C19	4.7 µF	
C20	220 pF	

Component	Value	Comment
C21	470 nF	
C22	470 nF	
C23	470 nF	
C25	220 nF	
C28	100 nF	
C30	47 nF	
C31	47 nF	
C32	47 nF	
C33	47 nF	
D1	SM6T27CAY	
D2	PESD1LIN	
D4	PMEG 6010	
D7	S1G	
D8, D9, D10, D11	1PS76SB70	Optional to ensure VCi < Vgi Leakage current must not overload CP
D12	1N4148	
T1, T2, T3, T4	STL120N4F6AG	
T5	NVMFS5C410NL	
Q1	PDTC143T	

Figure 14 shows an example of external wiring for a four-channel application without T87. In this example, wake-up and communication are exclusively through the DIO_BUS. Individual components may be omitted or may need to be added in the actual design, especially depending on EMC, reverse-polarity protection and pulse load requirements.

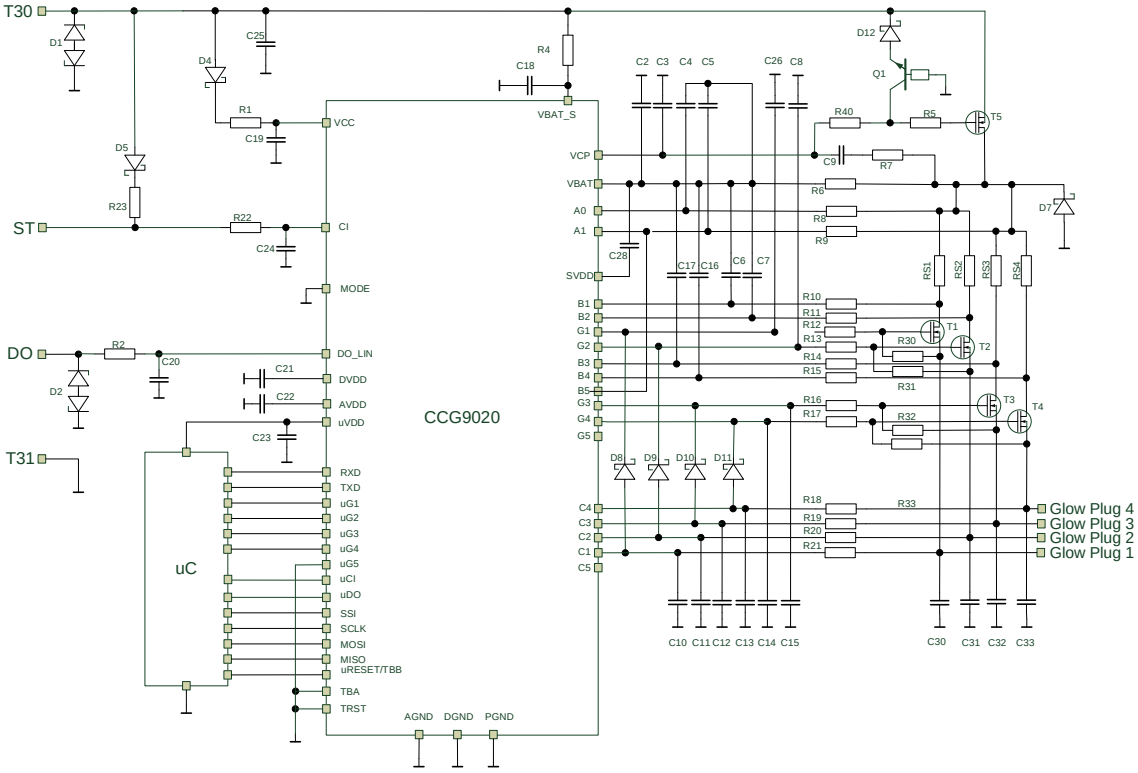


Figure 15. Sample wiring for a four-channel T30 application with ST, glow plug application

Table 58. Sample sizing for a four-channel T30 application with ST

Component	Value	Comment
R1	22 Ω	
R2	2.2 Ω	
R4	220 Ω	
R5	10 Ω up to 100 Ω	T5 gate must be able to be discharged with sufficient speed
R6	47.5 Ω	
R7	100 Ω	
R8, R9	1 kΩ	
R10, R11, R14, R15	1 kΩ	
R12, R13, R16, R17	1 kΩ	
R18, R19, R20, R21	100 Ω	
R30, R31, R32, R33	270 kΩ	
RS1, R2, RS2, RS3	1.3 mΩ	
R22	10 kΩ	
R23	2.2 kΩ	
R40	100 kΩ	
C1	1 nF	
C2	100 nF	
C3	1 nF	
C4, C5	470 pF	
C6, C7, C16, C17	470 pF	
C8, C14, C15, C26	100 pF	
C9	220 nF	
C10, C11, C12, C13	1 nF	
C18	10 nF	
C19	4.7 µF	
C20	470 pF	
C21	470 nF	
C22	470 nF	
C23	470 nF	
C24	1 nF	
C25	220 nF	
C28	100 nF	
C30	47 nF	
C31	47 nF	
C32	47 nF	
C33	47 nF	
D1	SM6T27CAY	
D2	PESD1LIN	
D5	1N4148	
D4	PMEG 6010	
D7	S1G	
D8, D9, D10, D11	1PS76SB70	Optional to ensure VCi < VG Leakage current must not overload CP
D12	1N4148	
T1, T2, T3, T4	STL120N4F6AG	
T5	NVMFS5C410NL	
Q1	PDTC143T	

Figure 15 shows an example of external wiring for a four-channel application without T87. In this example, wake-up is exclusively through ST. Communication through the DIO_BUS is also possible when the system is running. Individual components may be omitted or may need to be added in the actual design, especially depending on EMC, reverse-polarity protection and pulse load requirements.

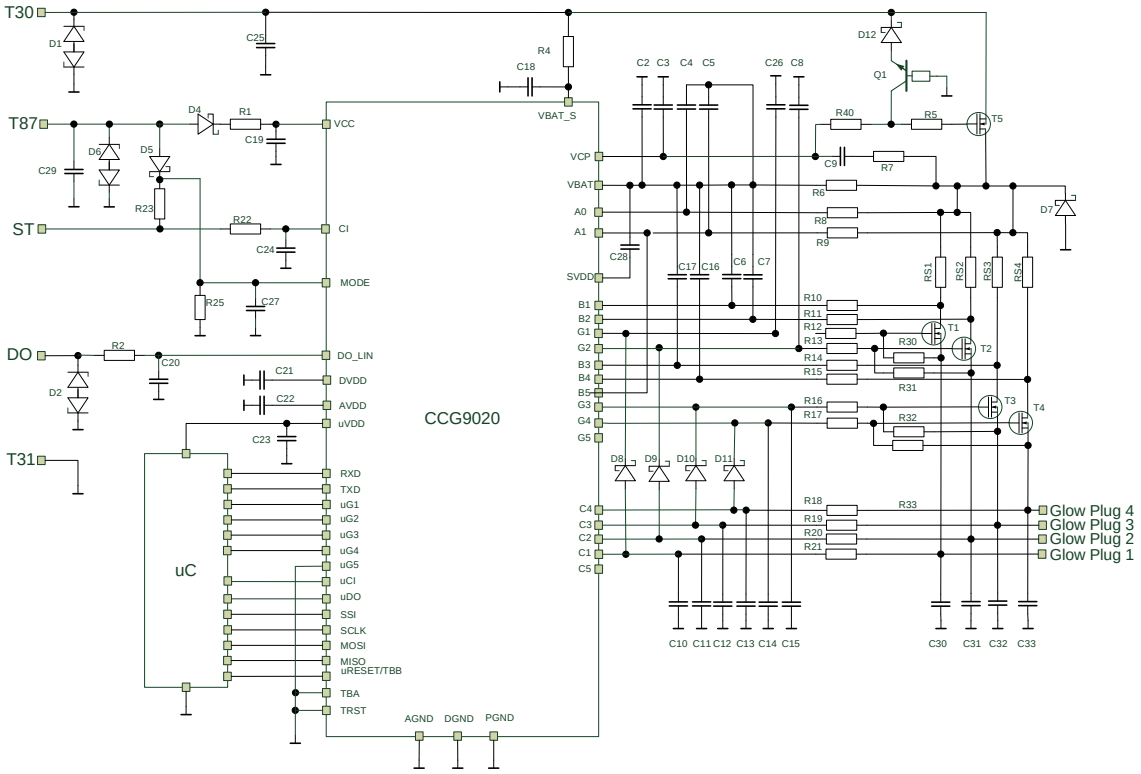


Figure 16. Sample wiring for a four-channel T87 application, glow plug application

Table 59. Sample sizing for a four-channel T87 application

Component	Value	Comment
R1	22 Ω	
R2	4.7 Ω	
R4	220 Ω	
R5	10 Ω up to 100 Ω	T5 gate must be able to be discharged with sufficient speed
R6	47.5 Ω	
R7	100 Ω	
R8, R9	1 kΩ	
R10, R11, R14, R15	1 kΩ	
R12, R13, R16, R17	1 kΩ	
R18, R19, R20, R21	100 Ω	
R30, R31, R32, R33	270 kΩ	
RS1, R2, RS2, RS3	1.3 mΩ	
R22	10 kΩ	
R23	2.2 kΩ	
R25	100 kΩ	
R40	100 kΩ	
C1	1 nF	
C2	100 nF	
C3	1 nF	
C4, C5	470 pF	
C6, C7, C16, C17	470 pF	

Component	Value	Comment
C8, C14, C15, C26	100 pF	
C9	220 nF	
C10, C11, C12, C13	1 nF	
C18	10 nF	
C19	4.7 µF	
C20	1.5 nF	
C21	470 nF	
C22	470 nF	
C23	470 nF	
C24	1 nF	
C25	220 nF	
C27	100 nF	
C28	100 nF	
C29	1.5 nF	
C30	47 nF	
C31	47 nF	
C32	47 nF	
C33	47 nF	
D1, D6	SM6T27CAY	
D2	PESD1LIN	
D4	PMEG 6010	
D5	1N4148	
D7	S1G	
D8, D9, D10, D11	1PS76SB70	Optional to ensure VCi < VGi Leakage current must not overload CP
D12	1N4148	
T1, T2, T3, T4	STL120N4F6AG	
T5	NVMFS5C410NL	
Q1	PDTC143T	

Figure 16 shows an example of external wiring for a four-channel application with T87. In this example, wake-up is exclusively through T87. Communication is also possible through the DIO_BUS when the system is running. Individual components may be omitted or may need to be added in the actual design, especially depending on EMC, reverse-polarity protection and pulse load requirements.

In Figure 14, Figure 15 and Figure 16, the diode D7 is used in each case to clamp the negative voltage at the channel FET drain, for example, in case T30 disconnects when the channel is active.

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