

## Bus Interface IC (Driver, Receiver)

### General Description

The CCA1224 is a bus interface IC with driver and receiver function. The bus driver provides two or combined inputs and a differential current bus output. The receiver uses the driver outputs as input and delivers the signal to an open collector output. This device is functional and pin compatible to the obsolete part no. HA12240.

Typical applications are automotive audio equipment controllers.

#### 1.1 FEATURES

- Two or combined data inputs (3.3 V and 5.0 V)
- Hysteresis input comparator
- Current drive output typ. 3.8 mA
- Hysteresis comparator for receiver
- Wide receiver common-mode input range of 0 to 5V typ.
- Open collector receiver output
- Operating VCC 5 V  $\pm$ 0.5 V
- Standby function (IVCC < 1  $\mu$ A)
- ESD protection 2 kV
- on all IO pins
- SOP8 package
- Automotive qualified (AECQ100)

#### 1.2 SCHEMATIC

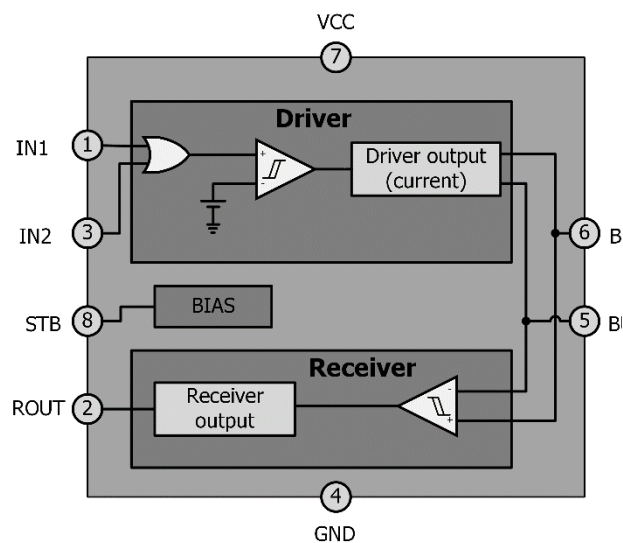


Figure 1: Block Diagram

Bus Interface IC (Driver, Receiver)

2 Pinout

2.1 PACKAGE

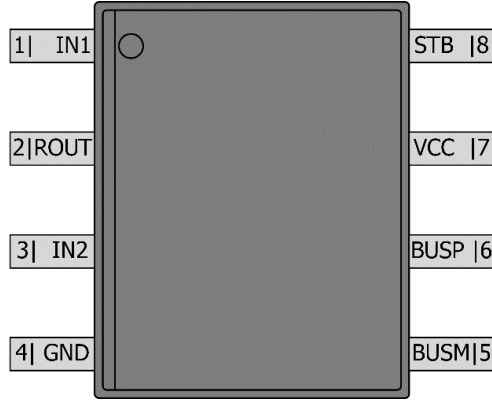


Figure 2: Package SOP8 (3.9x4.9mm)

2.2 PIN DESCRIPTIONS

Table 1: Pin Descriptions

Symbol	Pin no.	Type	Description	Schematic
IN1	1	IN	Data input 1	
ROUT	2	OUT	Receiver output (open collector)	
IN2	3	IN	Data input 2	
GND	4	PWR	Ground	
BUSM	5	IN/OUT	Minus bus driver output, receiver input	
BUSP	6	IN/OUT	Plus bus driver output, receiver input	
VCC	7	PWR	Voltage supply	
STB	8	IN	Stand by input: H => operating mode; L => standby mode	

## Bus Interface IC (Driver, Receiver)

### 3 Absolute Maximum Ratings

**Table 2: Absolute Maximum Ratings**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC	static	-0.7		36	V
Power dissipation QFN48	P <sub>TOT_QFN48</sub>	Multilayer PCB, Exp. Pad soldered, $\vartheta_{AMB} = 60^{\circ}\text{C}$			2	W
Power dissipation QFN24	P <sub>TOT_QFN24</sub>	Multilayer PCB, Exp. Pad soldered, $\vartheta_{AMB} = 60^{\circ}\text{C}$			1.5	W
Junction Temperature	$\vartheta_{JUNC}$				150	$^{\circ}\text{C}$
ESD-sensitivity	V <sub>ESD</sub>	Human Body Model EIA/JESD22-A114-B	2			kV
Storage Temperature	$\vartheta_{STORAGE}$		-55		155	$^{\circ}\text{C}$
Soldering Temperature	$\vartheta_{SOLDER}$	12 s max			260	$^{\circ}\text{C}$
FIT Rate					50	FIT

Functional operation is only guaranteed within operating conditions listed under “Electrical Characteristics”. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Exposure to conditions beyond those ratings may cause permanent damage to the device.

### 4 Electrical Characteristics

Electrical characteristics are valid for the whole specified temperature range and supply voltage range, if not otherwise noted.

#### 4.1 GENERAL PARAMETERS

**Table 3: General Parameters**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	VCC		4.5	5	5.5	V
Supply Current	I <sub>VCC</sub>		0.8		8.5	mA
Operating Temperature	$\vartheta_{AMB}$		-40		105	$^{\circ}\text{C}$
Thermal Resistance Ambient	$\vartheta_{JA\_SOPN-8}$	Junction to Ambient		100		K/W

## Bus Interface IC (Driver, Receiver)

### 4.2 DRIVER

Table 4: Driver

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage IN1	$V_{IHS1}$	$V1 = 0\text{ V} \rightarrow 5\text{ V}$ ; $V3 = 0\text{ V}$ ; $V6 - V5 = 110\text{ mV} \uparrow$	2.1			V
Low-level input voltage IN1	$V_{ILS1}$	$V1 = 5\text{ V} \rightarrow 0\text{ V}$ ; $V3 = 0\text{ V}$ ; $V6 - V5 = 30\text{ mV} \downarrow$			1.65	V
High-level input current IN1	$I_{IHS1}$	$V1 = 5\text{ V}$	-1	0	1	$\mu\text{A}$
Low-level input current IN1	$I_{ILS1}$	$V1 = 0\text{ V}$	-1	0.1	1	$\mu\text{A}$
High-level input voltage IN2	$V_{IHS2}$	$V3 = 0\text{ V} \rightarrow 5\text{ V}$ ; $V1 = 0\text{ V}$ ; $V6 - V5 = 110\text{ mV} \uparrow$	2.1			V
Low-level input voltage IN2	$V_{ILS2}$	$V3 = 5\text{ V} \rightarrow 0\text{ V}$ ; $V1 = 0\text{ V}$ ; $V6 - V5 = 30\text{ mV} \downarrow$			1.65	V
High-level input current IN2	$I_{IHS2}$	$V3 = 5\text{ V}$	-1	0	1	$\mu\text{A}$
Low-level input current IN2	$I_{ILS2}$	$V3 = 0\text{ V}$	-1	0.1	1	$\mu\text{A}$
High-level output voltage BUSP	$V_{OHDP}$	$V1$ or $V3 > 2.1\text{ V}$	1.8	2.5	3.2	V
Low-level output voltage BUSM	$V_{OHDM}$	$V1$ or $V3 > 2.1\text{ V}$	1.8	2.5	3.2	V
High-level output current (BUSP out; BUSM in)	$I_{OH}$	$V1$ or $V3 > 2.1\text{ V}$	3.1	3.8	4.5	mA
Low-level output voltage BUSP, BUSM	$V_{OLD}$	$V1$ and $V3 < 1.65\text{ V}$	2.3	2.5	2.7	V
Driver output resistance	$R_O$	$V1$ or $V3 > 2.1\text{ V}$ <b>Fehler!</b> <b>Verweisquelle konnte nicht gefunden werden..</b> 3; measure $I_{61}$ at $V6 = V_{OLD} + 0.3\text{ V}$ then measure $I_{62}$ at $V6 = V_{OLD} - 0.3\text{ V}$ ; $R_O = 0.6\text{ V} / (I_{61} - I_{62})$	5	10	15	k $\Omega$
Driver delay time low -> high	$T_{DDR}$	$V1 = 4.5\text{ V} \uparrow$ ; $V6 - V5 = 110\text{ mV} \uparrow$ ;		80	150	ns
Driver delay time high -> low	$T_{DDF}$	$V1 = 0.5\text{ V} \downarrow$ ; $V6 - V5 = 30\text{ mV} \downarrow$ ;		40	70	ns

### 4.3 RECEIVER

Table 5: Receiver

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High-level input voltage at low common-mode BUSP-BUSM	$V_{IH1}$	$V6 = 0\text{ V} \rightarrow 5\text{ V}$ ; $V5 = 0\text{ V}$ ; $V1 = 0\text{ V}$ ; $V3 = 0\text{ V}$ ; $V2 = 4\text{ V} \uparrow$ ; $V_{IH1} = V6 - V5$	45	80	110	mV
High-level input voltage at high common-mode BUSP-BUSM	$V_{IH2}$	$V6 = 0\text{ V} \rightarrow 5\text{ V}$ ; $V5 = 4.5\text{ V}$ ; $V1 = 0\text{ V}$ ; $V3 = 0\text{ V}$ ; $V2 = 4\text{ V} \uparrow$ ; $V_{IH2} = V6 - V5$	45	80	110	mV
Low-level input voltage at low common-mode BUSP-BUSM	$V_{IL1}$	$V6 = 5\text{ V} \rightarrow 0\text{ V}$ ; $V5 = 0\text{ V}$ ; $V1 = 0\text{ V}$ ; $V3 = 0\text{ V}$ ; $V2 = 1\text{ V} \downarrow$ ; $V_{IL1} = V6 - V5$	30	50	95	mV
High-level input voltage at high common-mode BUSP-BUSM	$V_{IL2}$	$V6 = 5\text{ V} \rightarrow 0\text{ V}$ ; $V5 = 4.5\text{ V}$ ; $V1 = 0\text{ V}$ ;	30	50	95	mV

## Bus Interface IC (Driver, Receiver)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
		V3 = 0 V; V2 = 1 V ↓; V <sub>IL2</sub> = V6 – V5				
Input hysteresis voltage at low common-mode BUSP-BUSM	V <sub>IHYS1</sub>	V <sub>IHYS1</sub> = V <sub>IH1</sub> - V <sub>IL1</sub>	15	30	45	mV
Input hysteresis voltage at high common-mode BUSP-BUSM	V <sub>IHYS2</sub>	V <sub>IHYS2</sub> = V <sub>IH2</sub> - V <sub>IL2</sub>	15	30	45	mV
High-level common-mode input voltage BUSM	V <sub>HCOM</sub>	V5 = 0 V → 5 V; V1 = 0 V; V3 = 0 V; V <sub>HCOM</sub> = V5 when V2 = 4 V ↓; V6 – V5 = 110 mV	4.5			V
Low-level common-mode input voltage BUSM	V <sub>LCOM</sub>	V5 = 0 V → 5 V; V1 = 0 V; V3 = 0 V; V <sub>HCOM</sub> = V5 when V4 = 1 V ↑; V6 – V5 = 30 mV	5			V
Receiver input resistance	R <sub>I</sub>	V1 and V3 < 1.65 V <b>Fehler!</b> <b>Verweisquelle konnte nicht gefunden werden..</b> 3; measure I <sub>63</sub> at V6 = V <sub>OLD</sub> + 0.3 V then measure I <sub>64</sub> at V6 = V <sub>OLD</sub> - 0.3 V; R <sub>I</sub> = 0.6 V / (I <sub>63</sub> - I <sub>64</sub> )	25	35	45	kΩ
High-level receiver output leakage current ROUT	I <sub>ROH</sub>	V1 = 5 V; V3 = 0 V; V2 = 5 V	-1	0	1	μA
Standby 1 receiver output leakage current ROUT	I <sub>ROS1</sub>	V1 = 0 V; V3 = 0 V; V8 = 0 V; VCC = 0 V; V2 = 5 V	-1	0	1	μA
Standby 2 receiver output leakage current ROUT	I <sub>ROS2</sub>	V1 = 0 V; V3 = 0 V; V8 = 0 V; V2 = 5 V	-1	0	1	μA
Low-level 1 receiver output voltage ROUT	V <sub>ROL1</sub>	V1 = 0 V; V3 = 0 V; I2 = 1.5 mA			0.6	V
Low-level 2 receiver output voltage ROUT	V <sub>ROL2</sub>	V1 = 0 V; V3 = 0 V; I2 = 200 μA			0.3	V
Receiver delay time low → high	T <sub>RDR</sub>	V6 – V5 = 110 mV ↑; V2 = 4.5 V ↑		600	700	ns
Receiver delay time high → low	T <sub>RDF</sub>	V6 – V5 = 30 mV ↓; V2 = 0.5 V ↓		110	150	ns

## 4.4 BIAS AND VCC

Table 6: BIAS and VCC

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent current high V <sub>CC</sub>	I <sub>CCH</sub>	V1 or V3 > 2.1 V	3		8.5	mA
Quiescent current low V <sub>CC</sub>	I <sub>CCL</sub>	V1 and V3 < 1.65 V	0.8		1.8	mA
Standby driver output leakage current BUSP	I <sub>DOS</sub>	V8 = 0 V; V1 or V3 > 2.1 V; V6 = 5 V	-1		1	μA
Standby supply leakage current V <sub>CC</sub>	I <sub>VCCS</sub>	V8 = 0 V; V1 or V3 > 2.1 V;	-1		1	μA
Standby high-level input voltage STB	V <sub>STBH</sub>	V8 = 0 V → 5 V; V1 = 0 V; V3 = 0 V; V <sub>STBH</sub> = V8 when V5, V6 = 2.3 V ↑	0.9		2	V
Standby low-level input voltage STB	V <sub>STBL</sub>	V8 = 5 V → 0 V; V1 = 5 V; V3 = 0 V; V <sub>STBH</sub> = V8 when I <sub>VCC</sub> = 1 μA ↓	0.9		2	V

Bus Interface IC (Driver, Receiver)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Standby high-level input current STB	I <sub>STBH</sub>	V <sub>8</sub> = 5 V; V <sub>1</sub> = 5 V; V <sub>3</sub> = 0 V;		50	100	μA
Standby low-level input current STB	I <sub>STBL</sub>	V <sub>8</sub> = 0 V; V <sub>1</sub> = 5 V; V <sub>3</sub> = 0 V;	-1	0	1	μA

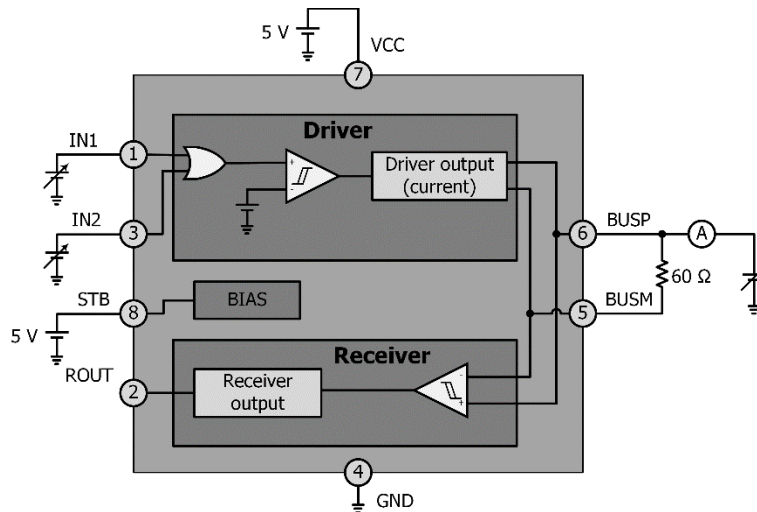


Figure 3: Measurement Circuits

## 5 Functional Description

### 5.1 DRIVER

The “Driver block” has two inputs and a differential current output. The inputs IN1 (Pin 1) and IN2 (Pin 3) are “or”-connected and their switching level and hysteresis are 3.3V and 5V compatible. The output BUSP (Pin 6) delivers a source current and BUSM (Pin 5) delivers a sink current of the same amount, so that with an external 60 Ohm Resistor between BUSP and BUSM the differential voltage is 230 mV (high) and 0 mV (low). The common-mode voltage is about 2.5 V, but the output can withstand external voltage up to VCC + 0.3V.

## Bus Interface IC (Driver, Receiver)

### 5.2 RECEIVER

The “Receiver block” has a differential voltage input and an open collector output. It share the Pins BUSP (Pin 6) and BUSM (Pin 5) with the driver block, but for the receiver block they are the differential voltage input. They have a large common-mode operating voltage from 0 V to 4.5 V and can withstand external voltage up to  $V_{CC} + 0.3V$ . The receiver output ROUT is open collector, so that the supply voltage for the external resistor at this Pin determines the following logic level.

### 5.3 BIAS

The “Bias block” delivers an internal reference voltage (2.5 V), several reference currents and the chance with the signal of Pin STB (Pin 8) to activate or deactivate the supply for all function blocks, so that in the standby mode ( $V(STB) < 0.9 V$ ) the power supply current falls to less than  $1\mu A$ .

## 6 Application notes

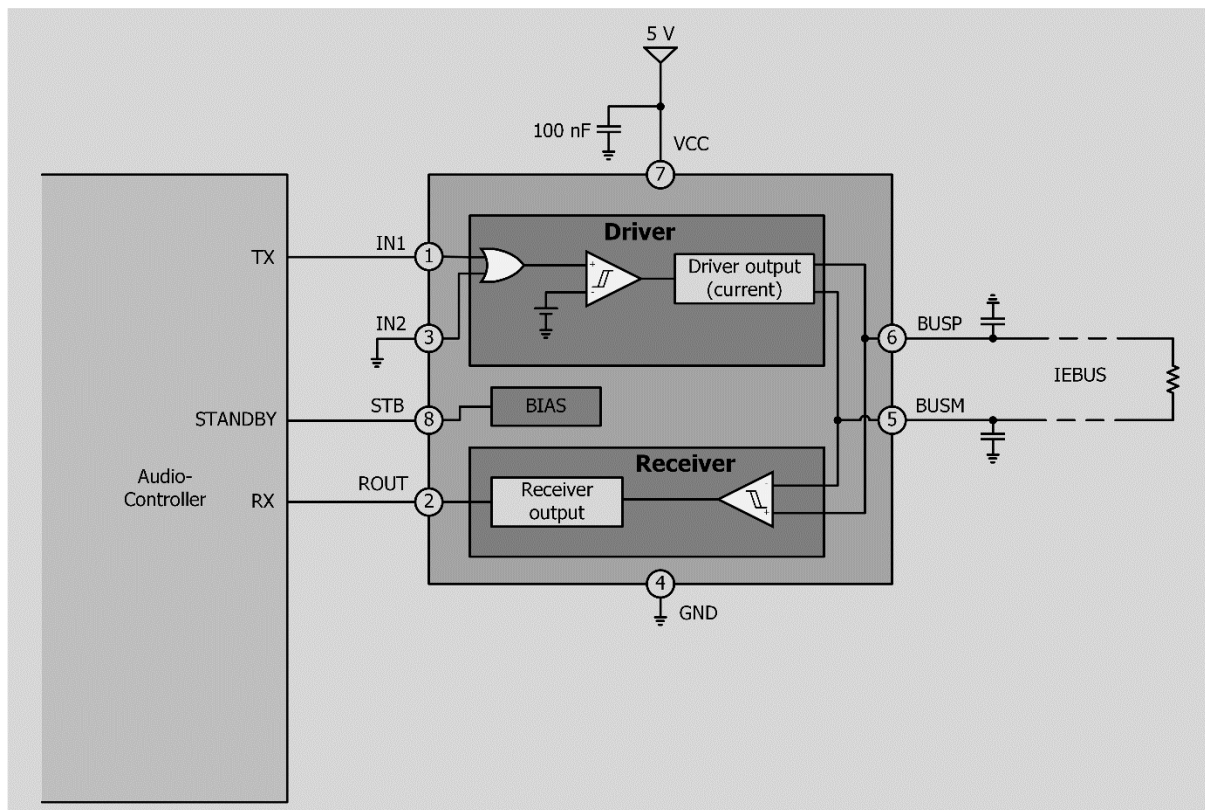


Figure 4: Application

Bus Interface IC (Driver, Receiver)

7 Package Outline

7.1 SOP8 Package

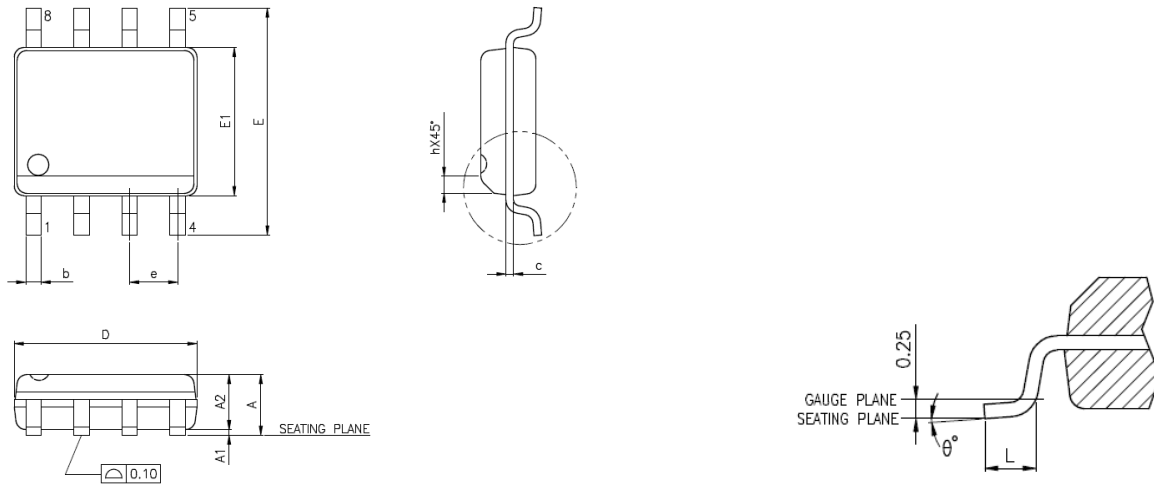


Figure 5: SOP8 Package

Symbol	A	A1	A2	b	C	D	E	E1	e	L	h	θ°
Min	--	0.10	1.25	0.31	0.10	4.90	6.00	3.90	1.27	0.40	0.25	5.15
Max	1.75	0.25	--	0.51	0.25	BSC.	BSC.	BSC.	BSC.	1.27	0.50	5.25

NOTES:

1. JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)  
MS-012 BA REV.F (THERMAL)
2. DIMENSIONS "d" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.



Bus Interface IC (Driver, Receiver)

8 Tape and Reel Information

8.1 TAPE INFORMATION

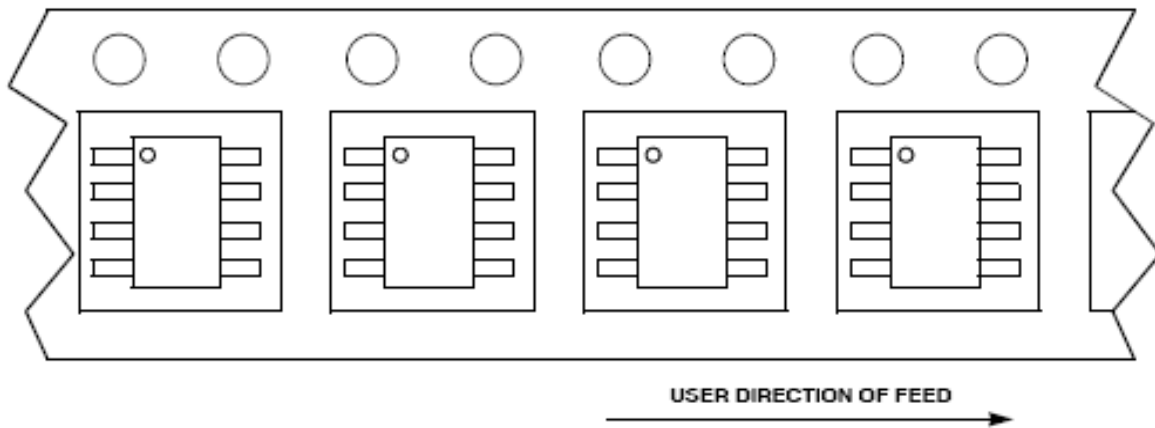
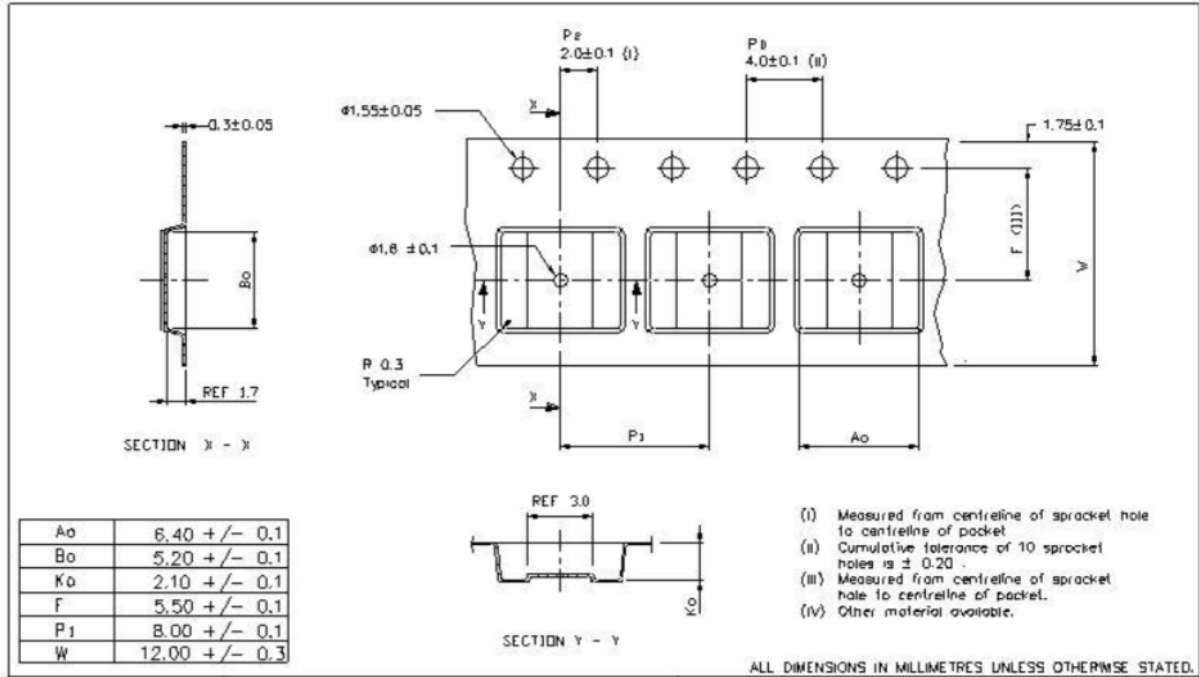
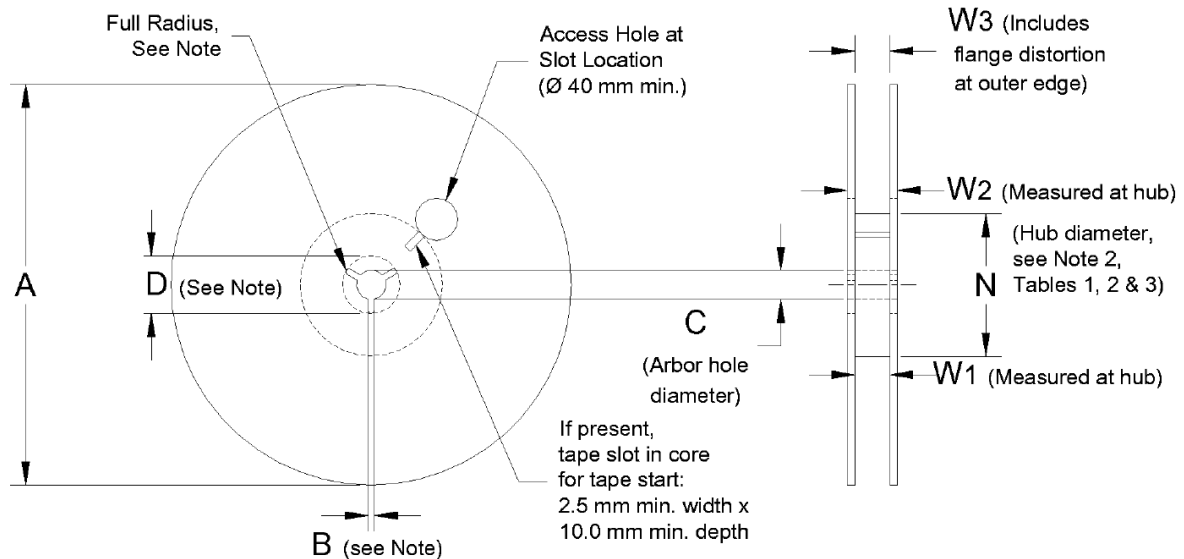


Figure 6: Tape Information

Bus Interface IC (Driver, Receiver)

8.2 Reel Information



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Figure 7: Reel Information

Symbol	A	B	C	D	W <sub>1</sub>
Minimal	-	1.5	12.8	20.2	13.25
Typical	-	-	13.0	-	-
Maximum	330	-	13.5	-	13.75

9 Ordering Information

Table 7: Ordering Information

Part	Order No.	Package	Delivery	Quantity
CCA1224	CCA1224_SO-P8	SOPN-8	Tape & Reel	3.800 parts per reel

## Bus Interface IC (Driver, Receiver)

### 10 Revision History

Revision	Date	Description
1.4	31-Oct-2019	Updated Template
1.3	24-Jul-2015	Updated Form
1.2	30-Apr-2015	Change of Part Number
1.1	25-Mar-2015	Changes in Timing and Bus
1.0	28-Aug-2014	Initial version

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**Bus Interface IC (Driver, Receiver)**

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**Contents**

General Description .....	1
1.1 Features .....	1
1.2 Schematic .....	1
2 Pinout .....	2
2.1 Package .....	2
2.2 Pin Descriptions .....	2
3 Absolute Maximum Ratings .....	3
4 Electrical Characteristics .....	3
4.1 General Parameters .....	3
4.2 Driver .....	4
4.3 Receiver .....	4
4.4 BIAS and VCC .....	5
5 Functional Description .....	6
5.1 Driver .....	6
5.2 Receiver .....	7
5.3 BIAS .....	7
6 Application notes .....	7
7 Package Outline .....	8
8 Tape and Reel Information .....	9
8.1 Tape Information .....	9
8.2 Reel Information .....	10
9 Ordering Information .....	10
10 Revision History .....	11
11 Disclaimer .....	11
Contents .....	12

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