AzureWave Technologies, Inc.

AW-CU429

Bluetooth 5.1 (LE ONLY) Stamp Module + Cortex M33 + Flash + Antenna

Datasheet

Rev. A

DF

FORM NO.: FR2-015_ A Responsible Depar
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Feature

Processor

- 32 kHz up to 96 MHz 32-bit ARM Cortex-M33 with 16 kBytes, 4-way associative cache and FPU Memory
- A flexible and configurable BLE MAC engine implementing the controller.
- A sensor node controller running uCode.
- Optimized power modes (Extended sleep, Deep sleep and Hibernation).

Flash

- 32Mbit SPI Flash

Memory

- 512 kB Data SRAM with retention capabilities
- 4 kB One-Time-Programmable (OTP) Memory.
- 16 kB Cache SRAM with retention capabilities.
- 128 kB ROM (including boot ROM and PKI routines for Flash image authentication).

- **Antenna**
  - Embedded Antenna

IO Interfaces

- Decrypt-on-the-fly QSPI FLASH interface.
- Separate QSPI PSRAM interface.
- Parallel/SPI LCD Controller with own DMA.
- 3 x UARTs up to 1 Mbps, one UART extended to support ISO7816.
- 2 SPI+™ controllers
- 2 I2C controllers at 100 kHz, 400 kHz or 3.4 MHz.
- PDM interface with HW sample rate converter.
- I2S/PCM master/slave interface up to 8 channels.
- USB 1.1 Full Speed device interface.
- 8-channel 10-bit SAR ADC, 3.4 M samples/sec.
- 8-channel 14-bit ΣΔ ADC, 1000 samples/sec.
- Haptic driver interface to LRA/ERM motors.
- 2 matched White LED drivers

Power input

- (2.4 V-4.75 V) Power Input

Package

- Stamp Module 19.6 mm x 15 mm x 2.45 mm

Certifications

- FCC/CE

Application

- Fitness trackers
- Sport watches
- Smartwatches
- Voice-controlled remote controls
- Rechargeable keyboards
- Toys.
- Consumer appliances
- Home automation
- Industrial automation

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Revision History

Document NO: R2-2429-DST-01

Version	Revision Date	DCN NO.	Description	Initials	Approved
Version 0.1	2019/1/31		Initial Version	Shihhua Huang	NC Chen
Version 0.2	2019/3/8		Modify chapter 1.4 info.	Shihhua Huang	NC Chen
Version 0.3	2019/4/16		Modify chapter 2 pin table info. Modify mechanical drawing	Shihhua Huang	NC Chen
Version 0.4	2019/6/5		Modify chapter 4 mechanical drawing	Shihhua Huang	NC Chen
Version 0.5	2019/7/22		Update Title BT5.0 to BT5.1 Update Specifications Table	Shihhua Huang	NC Chen
Version 0.6	2019/9/27		Update Pin define update Electrical Characteristics	Morris Huang	NC Chen
Version 0.7	2019/10/01		Update NOTE1 description.	Morris Huang	NC Chen
A	2019/10/03	DCN016409	● Update P0_15 pin define	Morris Huang	NC Chen

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1. Introduction

1.1 Product Overview

AzureWave presents **AW-CU429** the advanced Stamp **Bluetooth 5.1 module** provides a highly cost-effective, flexible and easy to-use hardware/software device to build a new generation of connected, smart devices. These smart-connected devices enable device to deliver a broad-range of services to consumers including energy-management, demand-response, home automation and remote access. This allows a user to manage comfort and convenience, also run diagnostics and receive alerts and notifications, in addition to managing and controlling the device. Developers can leverage the rich connectivity features of these new smart devices to create a new generation of innovative new applications and services

The device builds upon the success of Dialog's Bluetooth microcontroller device using the Dialog DA14691 and software. Adding new enhancements and capabilities.

The **AW-CU429** is powered by production quality, field-tested Dialog software that includes a rich set of software components that work together to support the development of Smart devices, and enable these devices to connect to mobile clients such as smart-phones, Internet-based Cloud and Smart-Grid services. The feature-rich software stack enables OEMs to focus on application-specific software functionality, thus enabling rapid development and reduced software development costs and risks.

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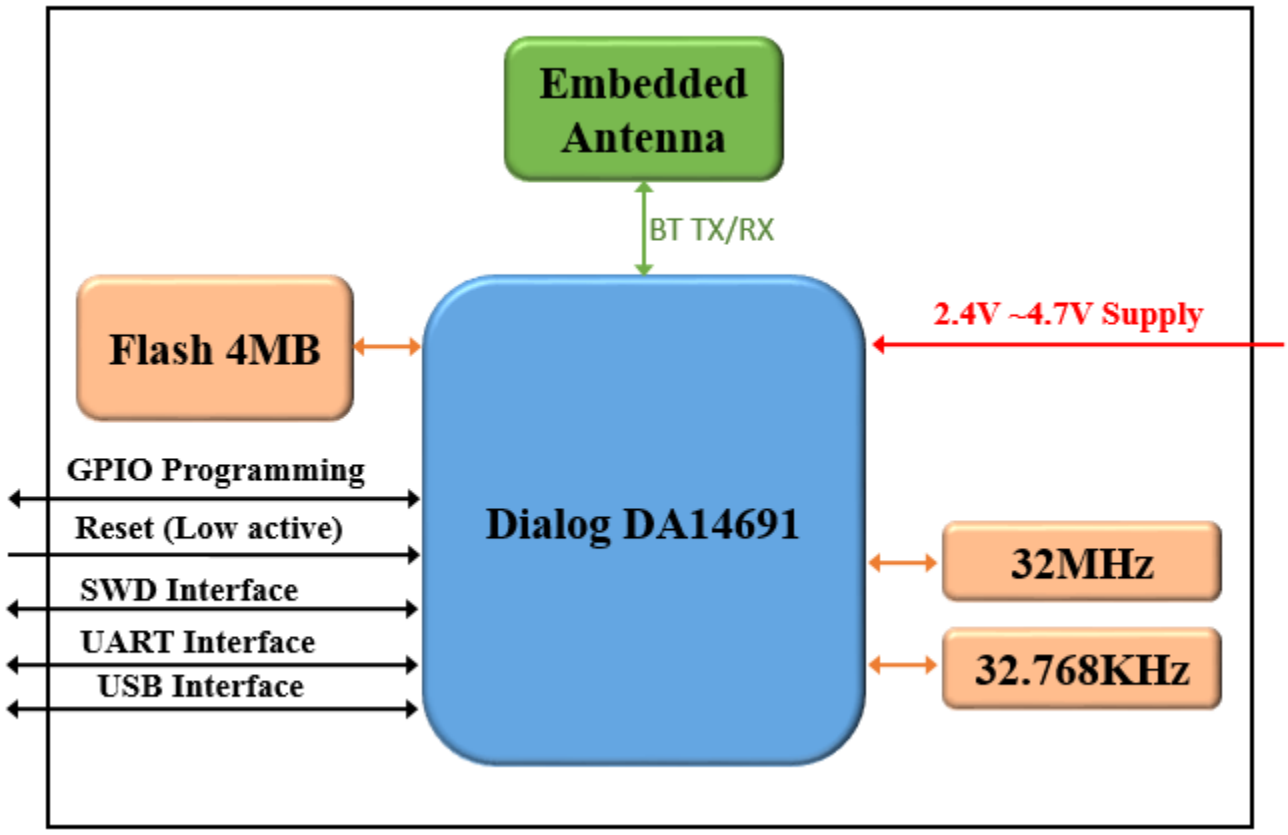
1.2 Block Diagram



Block Diagram of **AW-CU429**

FORM NO.: FR2-015_ A Responsible Department：WBU Expiry Date: Forever
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1.3 Specifications Table

1.3.1 General

Features	Description
Product Description	**AW-CU429** Bluetooth® Low Energy 5.1(LE ONLY) Stamp Module
Major Chipset	Dialog DA14691
Host Interface	UART / SPI / I2C /PCM/ GPIO / ADC /QSPI/USB 1.1
Dimension	19.6 mm x 15 mm x 2.45 mm
Package	Stamp 79-pin
Antenna	Embedded Antenna
Weight	1.1g

1.3.2 Bluetooth

Features	Description
Bluetooth Standard	Bluetooth 5.1 complaint (LE ONLY)
Frequency Rage	2402~2480MHz
Modulation	LE GFSK
Output Power (Board Level Limit)*	<table><tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr><tr><td>BLE</td><td>-4</td><td>-</td><td>2</td><td>dBm</td></tr></table>
Receiver Sensitivity	1 Mbps, PER = 30.8 %, Dirty Transmitter: off <table><tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr><tr><td>BLE</td><td></td><td>-97</td><td>-94</td><td>dBm</td></tr></table> 2 Mbps, PER = 30.8 %, Dirty Transmitter: off <table><tr><td></td><td>Min</td><td>Typ</td><td>Max</td><td>Unit</td></tr><tr><td>BLE</td><td></td><td>-94.5</td><td>-91.5</td><td>dBm</td></tr></table>
Data Rate	Bluetooth® Low Energy 5.1 2 Mbit/s
Range	TBD

* If you have any certification questions about output power please contact FAE directly.

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1.3.3 Operating Conditions

Features	Description
Operating Conditions	
Voltage	3.3V (Typical)
Operating Temperature	-40 ~ 85℃
Operating Humidity	Less than 85% R.H.
Storage Temperature	-40 ~ 85℃
Storage Humidity	Less than 60% R.H
ESD Protection	
Human Body Model	2.2KV per JEDEC EID/JESD22-A114
Changed Device Model	500V per JEDEC EIA/JESD22-C101

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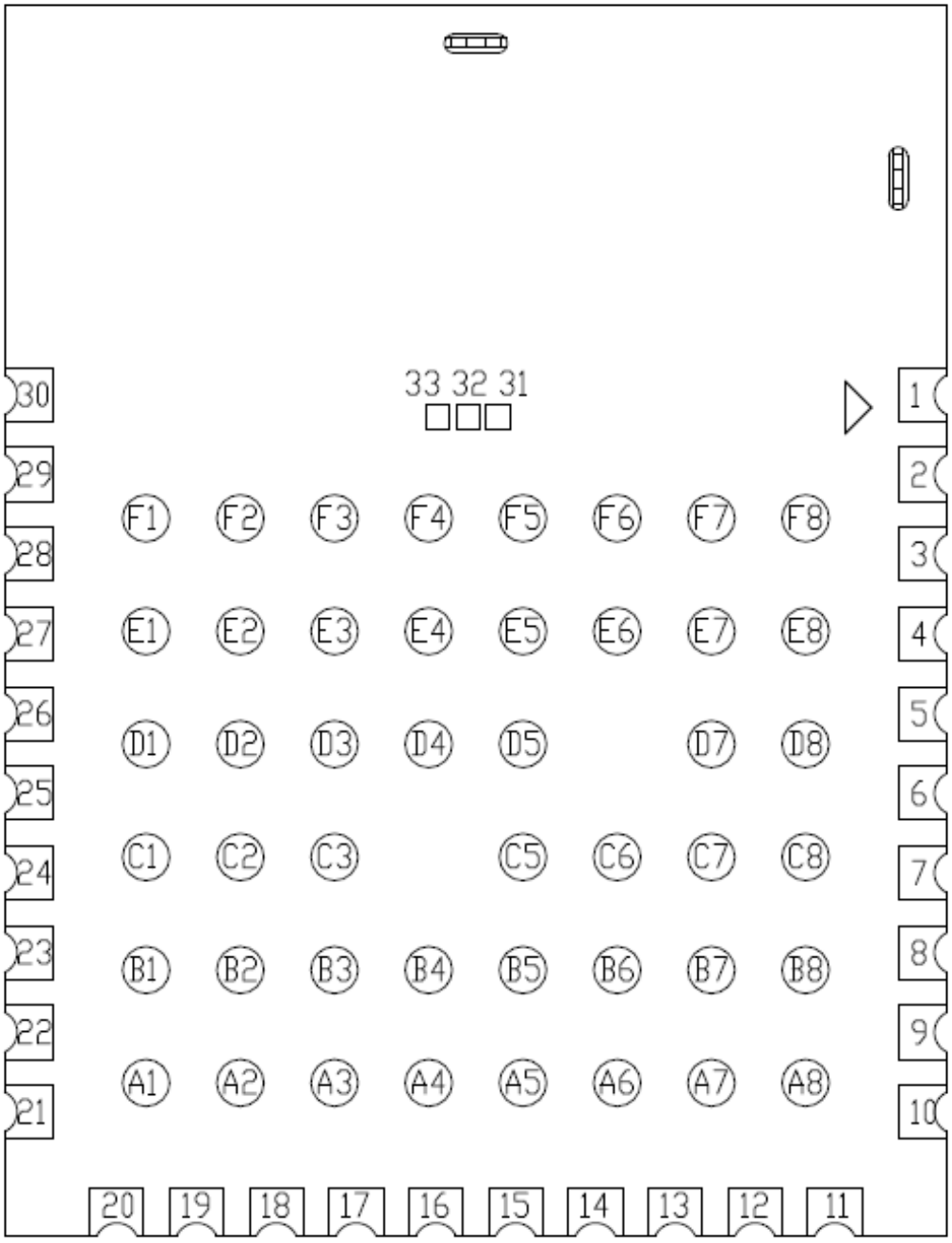
1. Pin Definition

2.1 Pin Map

Bottom View



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2.2 Pin Table

2.2.1 Power

Pin No	Definition	Basic Description	Type	Level
15	VBAT_3V3	INPUT. 3.3V Power rail	PWR	3.3V

2.2.2 Reset

Pin No	Definition	Basic Description	Type	Level
17	RSTn	INPUT. Reset signal (active LOW).	I	1.2

1.2.3 GPIO

Pin No	GPIO	SWD/USB	QSPI RAM	Analog	Clocks	PWM	LCD Controller	LEVEL
3	P0_0		QSPIR_D0					3V/1.8V
4	P0_1		QSPIR_D1					
5	P0_2		QSPIR_D2					
6	P0_3		QSPIR_D3					
7	P0_4		QSPIR_CS					
8	P0_5		QSPIR_CLK					
11	P0_6			SDADC_GND				
12	P0_7			NTC Input				
10	P0_8	UART Boot RX		GPADC_2 \ SDADC_2				
9	P0_9	UART Boot TX		GPADC_3 \ SDADC_3				
24	P0_10	M33_SWDIO						
25	P0_11	M33_SWCLK						
13	P0_12	CMAC_SWDIO			XTAL_32M			
14	P0_13	CMAC_SWCLK			RC_32M			
A2	P0_14	USBp ports.(Note 1)			XTAL_32k			
A1	P0_15	USBm ports.(Note 1)			DIVN			

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22	P0_16			SDADC_ REF	RCX			
23	P0_17				RC32k			
29	P0_19							
C2	P0_20							
E6	P0_21							
F1	P0_22				XTAL_32km			
C1	P0_23				XTAL_32kp			
D1	P0_24						LCD_TE	
B7	P0_25			GPADC_1 \ SDADC_1				
D5	P0_26						LCD_VCK	
B8	P0_28						LCD_VST PLCD_VSYNC	
E4	P0_29						LCD_HCK PLCD_CLK	
F6	P0_30						LCD_HST PLCD_HSYNC	
E8	P0_31						LCD_XRST	
E3	P1_0			NTC Supply				3V/1.8V
D3	P1_1					Timer.PWM		
19	P1_2						LCD_BLUE0	
F4	P1_3						LCD_BLUE1	
C7	P1_4						LCD_GREEN0	
C5	P1_5						LCD_GREEN1	
C3	P1_6					Timer2.PWM		
E1	P1_7						LCD_RED0	
C6	P1_8						LCD_RED1	
D2	P1_9			GPADC_0 \ SDADC_0				

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18	P1_10						LCD_VCOM / FRP / LCD_EXTCOMIN	
D4	P1_11						LCD_XFRP	

(Note 1) The P0_14, P0_15 are the USB pins and they are used also by charger for the wall-charger detection. So better leave them alone if you don't run out of GPIOs and must use the USB pads

2.2.4 Reserve Pin

Pin No	Definition	Basic Description	Type	Level
28	NC6	Please don't connect to this pin		
32	RF1	Please don't connect to this pin.		
34	NC1	Please don't connect to this pin		
35	NC0	Please don't connect to this pin		
A3	P0_14X	Please don't connect to this pin		
A4	VBUS	Please don't connect to this pin.		
A5	VBUSn	Please don't connect to this pin		
A6	VBATn	Please don't connect to this pin		
A7	NC5	Please don't connect to this pin		
A8	V12	Please don't connect to this pin		
B3	P0_15X	Please don't connect to this pin		
B4	V30	Please don't connect to this pin		
C8	V18	Please don't connect to this pin		
D7	V18P	Please don't connect to this pin		
E2	NC7	Please don't connect to this pin		
F2, F3	NC2	Please don't connect to this pin.		
F7	NC4	Please don't connect to this pin.		
F8	NC3	Please don't connect to this pin.		
F5	V14	Please don't connect to this pin		

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2.2.5 GND

Pin No	Definition	Basic Description	Type	Level
1	GND			
2				
16				
20				
21				
26				
27				
30				
31				
33				
B1				
B2				
D8				
E5				
E7				
B5				
B6				

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT_3V3	3.3V power supply			6	V

3.2 Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VBAT_3V3	3.3V power supply	2.4		4.75	V

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3.3 Reset Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIH	Input High Voltage	0.7 * 1.2			V
VIL	Input Low Voltage			0.3 * 1.2	V

3.4 Digital IO Pin DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Unit
VIH	Input High Voltage	0.7 * 1.2			V
VIL	Input Low Voltage			0.3*1.2	V
VOL_1V8	HIGH level output voltage	0.8*1.8			V
VOL_1V8	LOW level output voltage			0.2*1.8	V
VOH_3V0	HIGH level output voltage	0.8*3.0			V
VOL_3V0	LOW level output voltage			0.2*3.0	V

3.5 General Purpose ADC Characteristics

3.5.1 General Purpose ADC - Recommended Operating Condition

Symbol	Parameter		Minimum	Typical	Maximum	Unit
NBIT(ADC)	number of bits (resolution)			10		bit

3.5.2 General Purpose ADC - DC Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
EG	gain error without calibration	Trimmed bandgap	-3		3	%
EG_CALIBRATED	gain error after calibration	Trimmed bandgap & Gain Error + Offset correction applied	-0.5		0.5	%
EOFS	offset error without calibration	Trimmed bandgap	-20		20	LSB
EOFS_CALIBRATED	offset error after calibration	Trimmed bandgap & Gain Error + Offset correction applied	-2		2	LSB

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EG_ATTN3x	gain error of the 3x attenuator	Trimmed bandgap & GPADC Gain Error + Offset correction applied		-1		%
EG_VBAT	gain error of the VBAT attenuator	Trimmed bandgap & GPADC Gain Error + Offset correction applied		-1.7		%
INL	integral non-linearity		-2		2	LSB
DNL	differential non-linearity		-2		2	LSB
ENOB	Effective Number Of Bits	no averaging, no chopping, Single-Ended: VIN,PP = 1.1V		9		bit
ENOB(AVG128)	Effective Number Of Bits	128x averaging, Single- Ended: VIN,PP = 1.1V		11		bit

3.6 I2C Protocols

The I2C Controller has the following protocols:

- START and STOP Conditions
- Addressing Slave Protocol
- Transmitting and Receiving Protocol
- START BYTE Transfer Protocol

3.6.1 START and STOP Conditions

When the bus is idle, both the SCL and SDA signals are pulled high through external pull-up resistors on the bus. When the master wants to start a transmission on the bus, the master issues a START condition. This is defined to be a high-to-low transition of the SDA signal while SCL is 1. When the master wants to terminate the transmission, the master issues a STOP condition. This is defined to be a low-to-high transition of the SDA line while SCL is 1. Below figure shows the timing of the START and STOP conditions. When data is being transmitted on the bus, the SDA line must be stable when SCL is 1.

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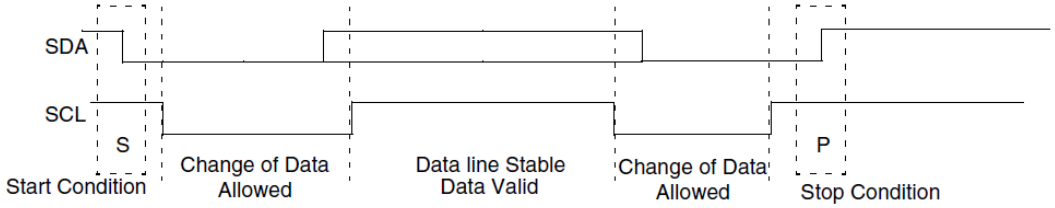

Figure. Start and Stop conditions

Note: The signal transitions for the START/STOP conditions, as depicted in above figure, reflect those observed at the output signals of the Master driving the I2C bus. Care should be taken when observing the SDA/SCL signals at the input signals of the Slave(s), because unequal line delays may result in an incorrect SDA/SCL timing relationship.

3.7. UART interface

The **AW-CU429**(DA14691) contains two identical instances of this block, i.e. UART and UART2.

The UART is compliant to the industry-standard 16550 and is used for serial communication with a peripheral. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

There is also DMA support on the UART block thus the internal FIFOs can be used. Both UARTs support hardware flow control signals (RTS, CTS). **Features**

- 16 bytes Transmit and receive FIFOs
- Hardware flow control support (CTS/RTS)
- Shadow registers to reduce software overhead and also include a software programmable reset
- Transmitter Holding Register Empty (THRE) interrupt mode
- IrDA 1.0 SIR mode supporting low power mode.
- Functionality based on the 16550 industry standard:
- Programmable character properties, such as number of data bits per character (5-8), optional
- parity bit (with odd or even select) and number of stop bits (1, 1.5 or 2)
- Line break generation and detection
- Prioritized interrupt identification
- Programmable serial data baud rate as calculated by the following: baud rate = (serial clock frequency)/(16 * divisor).

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3.8. SPI+ interface

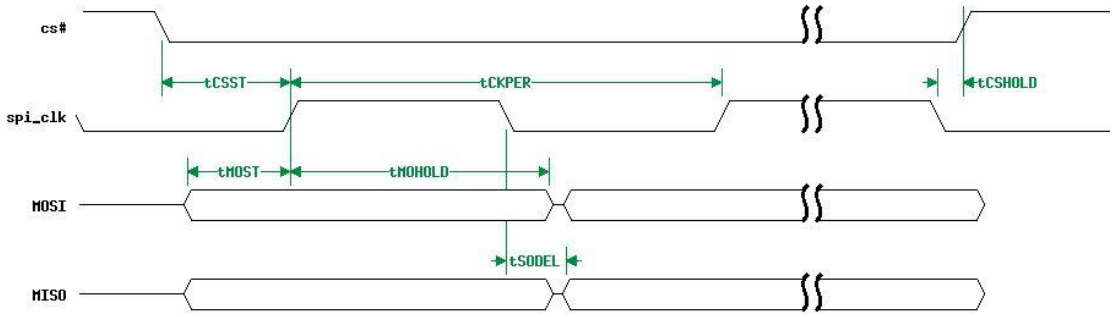
This interface supports a subset of the Serial Peripheral Interface (SPI™). The serial interface can transmit and receive 8, 16 or 32 bits in master/slave mode and transmit 9 bits in master mode. The SPI+ interface has enhanced functionality with bidirectional 2x16-bit word FIFOs. SPI is a trademark of Motorola, Inc.

Features

- Slave and Master mode
- 8 bit, 9 bit, 16 bit or 32 bit operation
- Clock speeds up to 16 MHz for the SPI controller. Programmable output frequencies of SPI source clock divided by 1, 2, 4, 8
- SPI clock line speed up to 8 MHz
- SPI mode 0, 1, 2, 3 support (clock edge and phase)
- Programmable SPI_DO idle level
- Maskable Interrupt generation
- Bus load reduction by unidirectional writes-only and reads-only modes.
- Built-in RX/TX FIFOs for continuous SPI bursts.
- DMA support

3.8.1 SPI Timing

The timing of the SPI interface when the SPI controller is in Slave mode is presented in below figure.



Symbol	Parameter	Minimum	Typical	Maximu	Unit

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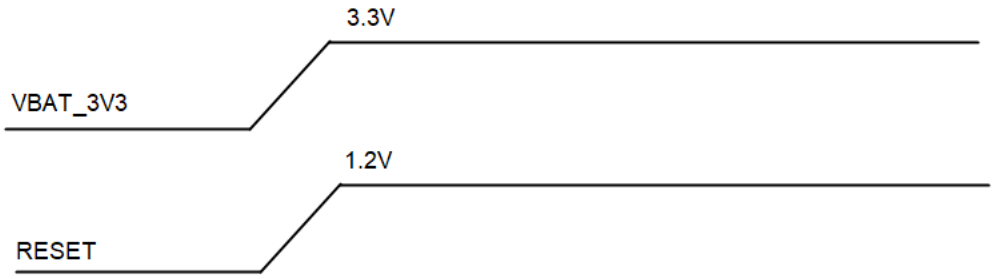
				m	
t_{CKPER}	spi_clk clock period			0.25 *	ns
t_{CSST}	CS active time before rising edge	10.6 +T_{INT}	5.2 + T_{INT}	3.1 + T_{INT}	ns
t_{CSHOLD}	CS active time after falling edge of	0	0	0	ns
t_{MOST}	Input data latching setup time	2.7	1.5	0.9	ns
t_{MOHOLD}	Input data hold time	0	0	0	ns
t_{SODEL}	Output data hold time	17.2	8.6	5.5	ns

Note TINT represents the internal SPI clock period and is equal to 1.5 * spi_clk period.

3.9 Power up Sequence/Rest Timing

3.9.1 Power up sequence



3.9.2 Power-on Reset timing

The AW-CU429 has a RSTN pad which is active low. It contains a RC filter for spikes suppression with 400 kΩ resistor and a 2.8 pF capacitor. It also includes a 25 kΩ pull-up resistor. This pad should be driven externally using a FET or a single button connected to Ground. The typical latency of the RSTN pad is about 2 µs.

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3.10 Power Consumption*

3.10.1 Bluetooth

No.	Mode	Packet Type	RF Power (dBm)	Voltage=3.3V	
				Max.	Avg.
1.	TX	LE	-1.2dBm	3.2mA	3.1mA
2.	RX	LE	n/a	3.4mA	3.4mA

Current Unit: mA

* The power consumption is based on Azurewave test environment, these data for reference only

3.11 Certifications FCC Bluetooth 2.4GHz Power Table

FCC Bluetooth 2.4GHz Power Table:

Embedded Antenna (3.78dBi)

Modulation	Channel	Meter Power (Averag.dBm)	Meter Power (Peak.dBm)
802.15.1 (BT5.1)	0(2402MHz)	TBD	TBD
	19(2440MHz)	TBD	TBD
	39(2480MHz)	TBD	TBD

Embedded Antenna Spec

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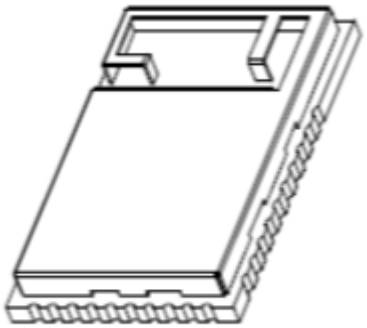
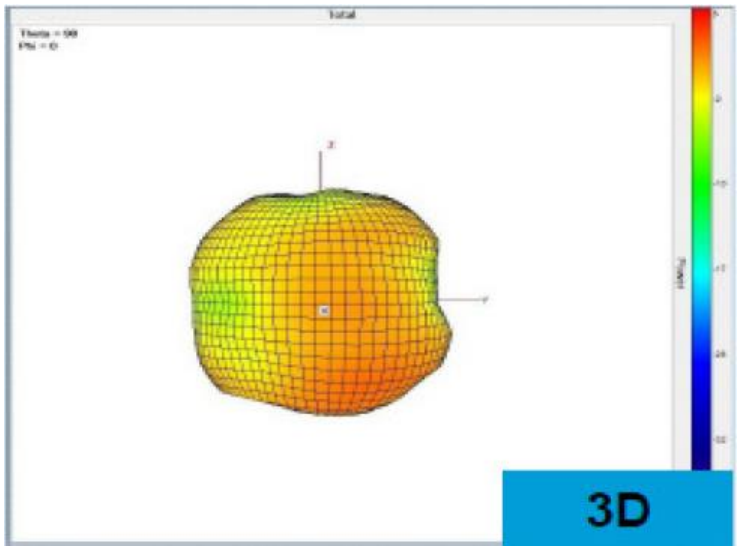


Ant.			
Frequency (MHz)	2400	2450	2500
Efficiency (dB)	-1.43	-1.36	-1.44
Peak Gain (dBi)	2.13	2.3	2.11
Efficiency (%)	71.96	73.1	71.82



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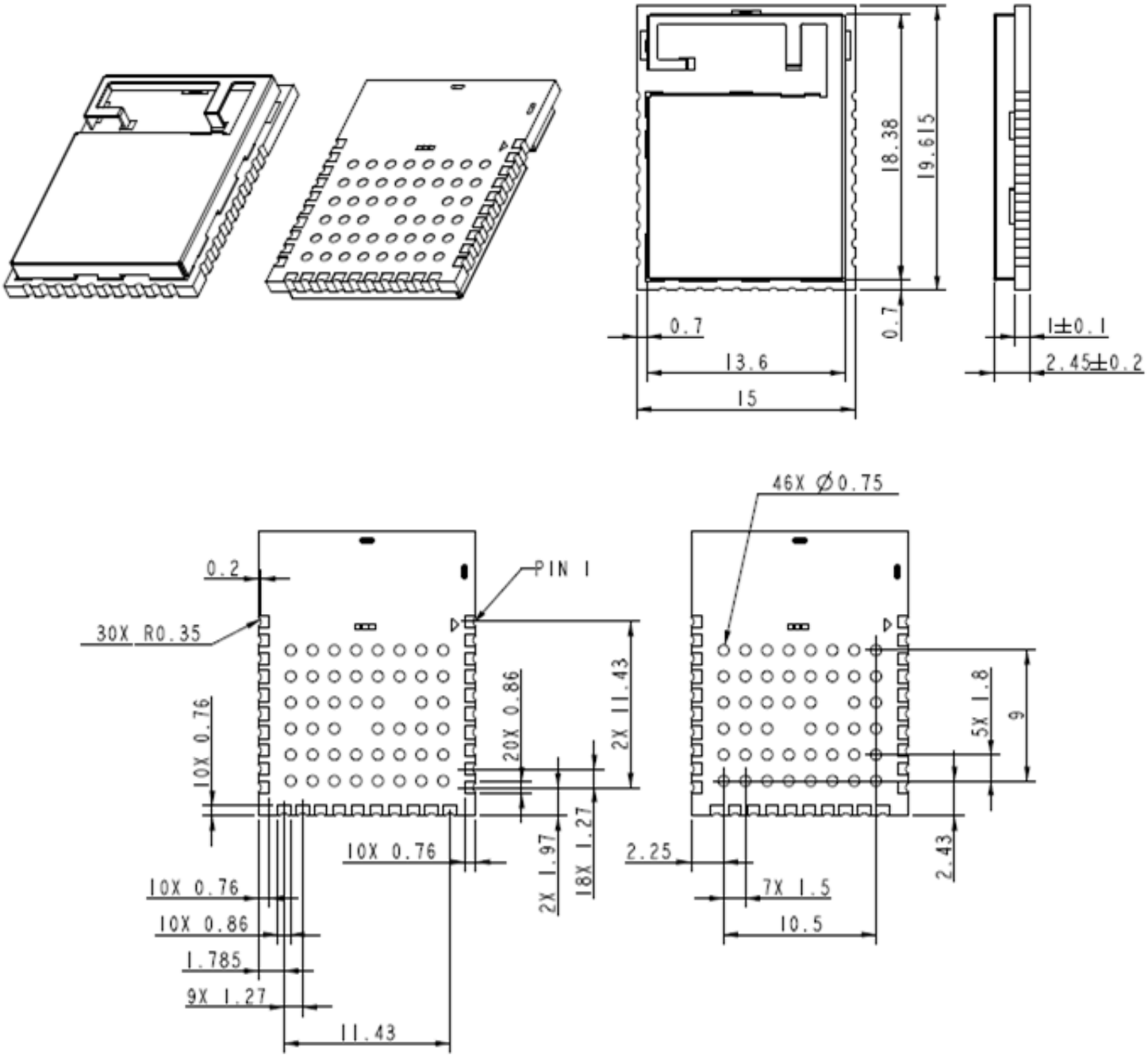
4. Mechanical Information

4.1 Mechanical Drawing



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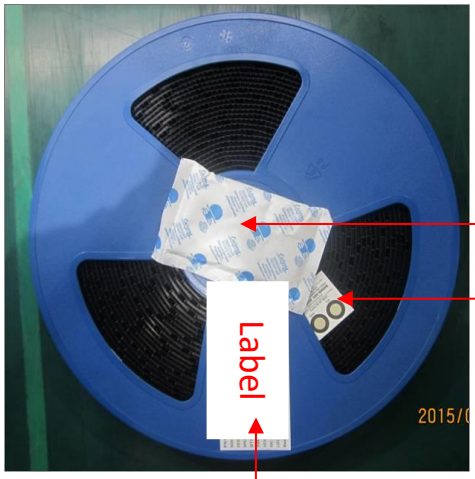
5. Packaging Information

Tape reel = 1 Box = 700 pcs

Carton = 3 Boxes = 2,100 pcs

5.1 Tape & Reel Picture

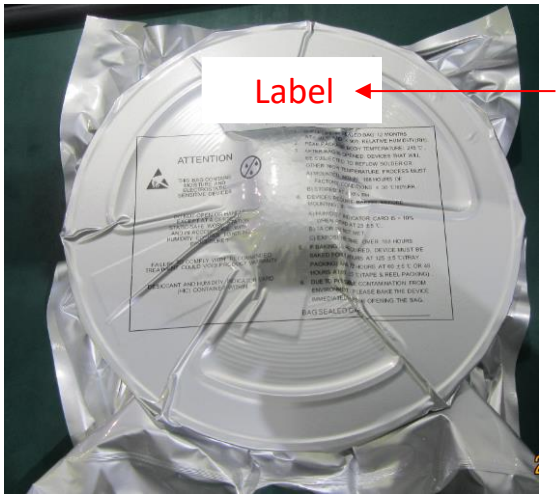


DESICCANT

HUMIDITY INDICATOR CARD

AFFIX PACKING LABEL

5.2 Packing Picture



AFFIX PACKING LABEL

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5.3 Inside of Inner Box Picture

5.4 Inner Box Picture

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5.5 Inside of Carton Picture

1 Carton = 3 Boxes

5.6 Carton and Label Picture

AFFIX SHIPPING LABEL

AFFIX PACKING LABEL

AFFIX BOX LABEL

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