AT25SL641

64-Mbit, 1.7 V Minimum SPI Serial Flash Memory with Dual I/O, Quad I/O and QPI Support

Features

- Single 1.7 V - 2.0 V Supply
- 64-Mbit Flash Memory
- Serial Peripheral Interface (SPI) and Quad Peripheral Interface (QPI) Compatible
  - Supports SPI Modes 0 and 3
  - Supports Dual Output Read and Quad I/O Program and Read
  - Supports QPI Program and Read
  - 133 MHz Maximum Operating Frequency
  - Clock-to-Output (t_{V1}) of 6 ns
  - Up to 66 MB/s Continuous Data Transfer Rate
- Full Chip Erase
- Flexible, Optimized Erase Architecture for Code and Data Storage Applications
  - 0.6 ms Typical Page Program (256 Bytes) Time
  - 60 ms Typical 4-kByte Block Erase Time
  - 200 ms Typical 32-kByte Block Erase Time
  - 350 ms Typical 64-kByte Block Erase Time
- Hardware Controlled Locking of Status Registers via $\overline{\text{WP}}$ Pin
- 4-kbit Secured One-Time Programmable Security Register
- Hardware Write Protection
- Serial Flash Discoverable Parameters (SFDP) Register
- Flexible Programming
  - Byte/Page Program (1 to 256 Bytes)
  - Dual or Quad Input Byte/Page Program (1 to 256 Bytes)
- Erase/Program Suspend and Resume
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 2 µA Deep Power-Down Current (Typical)
  - 10 µA Standby current (Typical)
  - 5 mA Active Read Current (Typical)
- Endurance: 100,000 program/erase cycles (4-kB, 32-kB or 64-kB blocks)
- Data Retention: 20 Years
- Industrial Temperature Range: -40 °C to +85 °C
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-pad DFN (6 x 5 x 0.6 mm)
  - 8-Lead 208-mil SOIC
  - 8-ball WLCSP

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1. Product Overview

The AT25SL641 is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer based applications in which program code executed in place (XiP) or shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT25SL641 is ideal for data storage as well, eliminating the need for additional data storage devices.

The erase block sizes of the AT25SL641 have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own erase regions, the wasted and unused memory space that occurs with large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

SPI clock frequencies of up to 133 MHz are supported allowing equivalent clock rates of 266 MHz for Dual Output and 532 MHz for Quad Output when using the QPI and Fast Read Dual/Quad I/O commands.The AT25SL641 array is organized into 32,768 programmable pages of 256-bytes each. Up to 256 bytes can be programmed at a time using the Page Program commands. Pages can be erased 4-kB block, 32-kB block, 64-kB block or the entire chip.

The devices operate on a single 1.7 V to 1.95 V power supply with current consumption as low as 5 mA active and 2 µA for Deep Power-Down. All devices offered in space-saving packages. The device supports JEDEC standard manufacturer and device identification with a 4-kbit Secured OTP.

The physical block size for this device is 8 Mbit.

2. Pinouts and Pin Descriptions

The following figures show the pinout of each available package type.

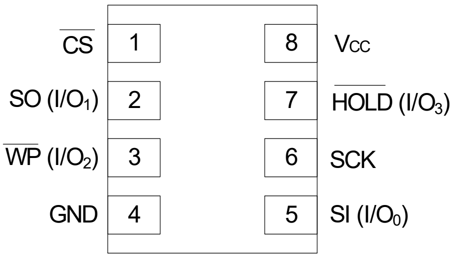


Figure 1. 8-UDFN (Top View)

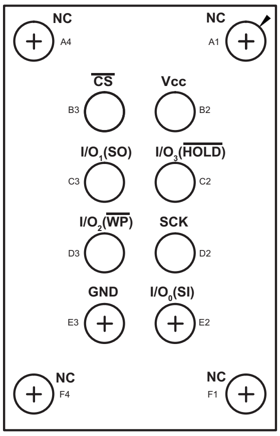


Figure 2. 8-WLCSP (Bottom View)

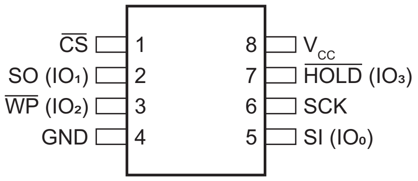


Figure 3. 8-WSOIC (Top View)

During all operations, V_{CC} must be held stable and within the specified valid range: V_{CC} (min) to V_{CC} (max).

All of the input and output signals must be held high or low (according to voltages of V_{IH}, V_{OH}, V_{IL} or V_{OL}).

Table 1. Pin Descriptions

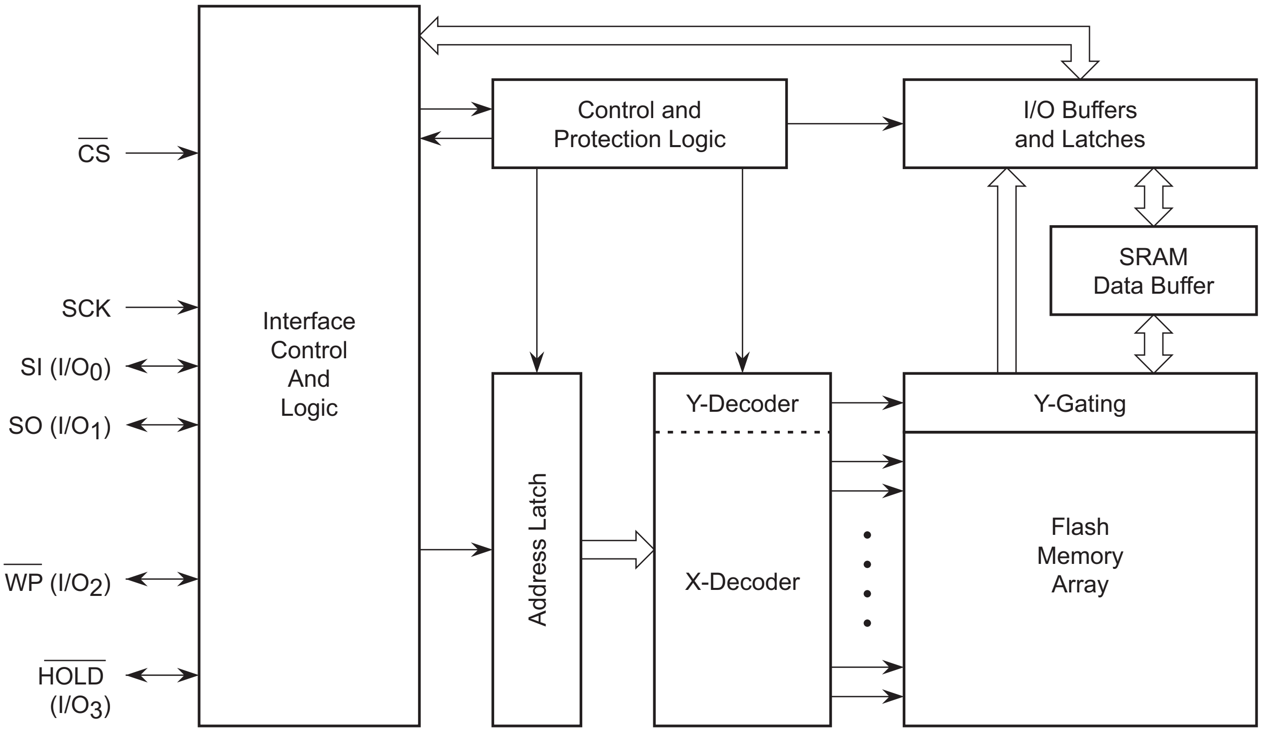
Symbol	Name and Function	Asserted State	Type
$\overline{\text{CS}}$	**CHIP SELECT** When this input signal is high, the device is deselected and serial data output pins are at high impedance. Unless an internal program, erase, or write status register cycle is in progress, the device is in the standby power mode (this is not the deep power-down mode). Driving Chip Select ($\overline{\text{CS}}$) low enables the device, placing it in the active power mode. After power-up, a falling edge on Chip Select ($\overline{\text{CS}}$) is required prior to the start of any command. To ensure correct power-up sequencing, it is recommended to add a 10k Ohm pull-up resistor from $\overline{\text{CS}}$ to VCC. This ensures $\overline{\text{CS}}$ ramps together with V_{CC} during power-up.	Low	Input
SCK	**SERIAL CLOCK** This input signal provides the timing for the serial interface. Commands, addresses, or data present at serial data input are latched on the rising edge of Serial Clock (SCK). Data are shifted out on the falling edge of the Serial Clock (SCK).	-	Input
SI (I/O_0)	**SERIAL INPUT** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched in on the rising edge of SCK. With the Dual-Output and Quad-Output Read commands, the SI Pin becomes an output pin (I/O_0) in conjunction with other pins to allow two or four bits of data on (I/O_{3-0}) to be clocked in on every falling edge of SCK To maintain consistency with the SPI nomenclature, the SI (I/O_0) pin is referenced as the SI pin unless specifically addressing the Dual-I/O and Quad-I/O modes in which case it is referenced as $I/O_{0.}$ Data present on the SI pin is ignored whenever the device is deselected ($\overline{\text{CS}}$ is deasserted).	-	Input/Output

Table 1. Pin Descriptions *(Continued)*

Symbol	Name and Function	Asserted State	Type
SO (I/O_1)	**SERIAL OUTPUT** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK. With the Dual-Output Read commands, the SO Pin remains an output pin (I/O0) in conjunction with other pins to allow two bits of data on (I/O_{1-0}) to be clocked in on every falling edge of SCK. To maintain consistency with the SPI nomenclature, the SO (I/O_1) pin is referenced as the SO pin unless specifically addressing the Dual-I/O modes in which case it is referenced as I/O_1. The SO pin is in a high-impedance state whenever the device is deselected ($\overline{\text{CS}}$ is deasserted).	-	Input/Output
$\overline{\text{WP}}$ (I/O_2)	**WRITE PROTECT** This pin is used either for write-protection, in which case it is referred to as $\overline{\text{WP}}$, or as one of the quad-SPI I/O pins, in which case it is referred to as IO_2. When the Quad Enable (QE) bit of Status Register 2 is 0, and the SRP1 and SRP0 bits are 0 and 1, respectively, the pin can be used for write-protection. It then can be asserted (driven low) to protect the Status Registers from modification. When the QE bit of Status Register 2 is 1, quad-SPI communication is enabled, and the pin is used as I/O pin IO_2 in any command that makes use of quad-SPI. In this setting, do not use the pin for write-protection. The $\overline{\text{WP}}$ pin does not have an internal pull-up; thus, it must either be driven or, if not used, pulled up with an external resistor to V_{CC}.	-	Input/Output
$\overline{\text{HOLD}}$ (I/O_3)	**HOLD** This pin is used either for pausing communication, in which case it is referred to as $\overline{\text{HOLD}}$, or as one of the quad-SPI I/O pins, in which case it is referred to as IO_3. When the Quad Enable (QE) bit of Status Register 2 is 0, this pin is used as a $\overline{\text{HOLD}}$ pin. When the QE bit of Status Register 2 is 1, quad-SPI communication is enabled, and the pin is used as I/O pin IO_3 in any command that makes use of quad-SPI. In this setting, do not use the pin for pausing communication. The $\overline{\text{HOLD}}$ pin is used to pause a SPI sequence without resetting the clocking sequence. To enable the $\overline{\text{HOLD}}$ mode, $\overline{\text{CS}}$ must be low. The HOLD mode effect is on with the falling edge of the $\overline{\text{HOLD}}$ signal with SCK being low. The HOLD mode ends on the rising edge of the $\overline{\text{HOLD}}$ signal with SCK being low. The $\overline{\text{HOLD}}$ pin does not have an internal pull-up; thus, it must either be driven or, if not used, pulled up with an external resistor to V_{CC}.	-	Input/Output
V_{CC}	**DEVICE POWER SUPPLY:** V_{CC} is the supply voltage. It is the single voltage used for all device functions including read, program, and erase. The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results; do not attempt them.	-	Power
GND	**GROUND:** V_{SS} is the reference for the V_{CC} supply voltage. The ground reference for the power supply. Connect GND to the system ground.	-	Power

3. Block Diagram

Figure 4 shows a block diagram of the AT25SL641 serial Flash.

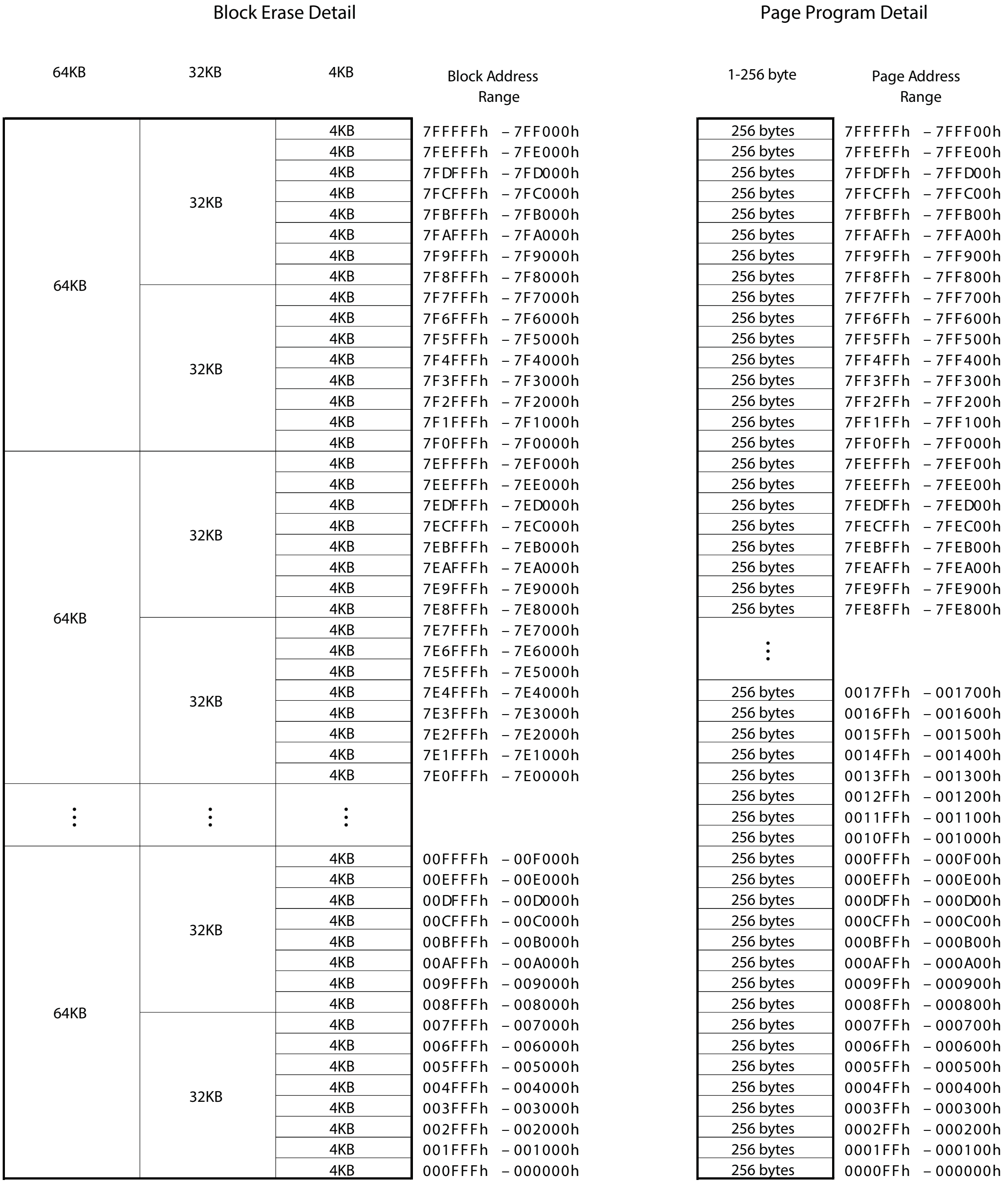


Note: I/O_{3-0} pin naming convention is used for Dual-I/O and Quad-I/O commands.

Figure 4. AT25SL641 Block Diagram

4. Memory Array

To provide the greatest flexibility, the memory array of the AT25SL641 can be erased in four levels of granularity including a full chip erase. The size of the erase blocks is optimized for both code and data storage applications, allowing both code and data segments to reside in their own erase regions. The Memory Architecture Diagram shows of each erase level.



Block Erase Detail

64KB	32KB	4KB	Block Address Range
64KB	32KB	4KB	7FFFFFh – 7FF000h
		4KB	7FEFFFh – 7FE000h
		4KB	7FDFFFh – 7FD000h
		4KB	7FCFFFh – 7FC000h
		4KB	7FBFFFh – 7FB000h
		4KB	7FAFFFh – 7FA000h
		4KB	7F9FFFh – 7F9000h
		4KB	7F8FFFh – 7F8000h
	32KB	4KB	7F7FFFh – 7F7000h
		4KB	7F6FFFh – 7F6000h
		4KB	7F5FFFh – 7F5000h
		4KB	7F4FFFh – 7F4000h
		4KB	7F3FFFh – 7F3000h
		4KB	7F2FFFh – 7F2000h
		4KB	7F1FFFh – 7F1000h
		4KB	7F0FFFh – 7F0000h
64KB	32KB	4KB	7EFFFFh – 7EF000h
		4KB	7EEFFFh – 7EE000h
		4KB	7EDFFFh – 7ED000h
		4KB	7ECFFFh – 7EC000h
		4KB	7EBFFFh – 7EB000h
		4KB	7EAFFFh – 7EA000h
		4KB	7E9FFFh – 7E9000h
		4KB	7E8FFFh – 7E8000h
	32KB	4KB	7E7FFFh – 7E7000h
		4KB	7E6FFFh – 7E6000h
		4KB	7E5FFFh – 7E5000h
		4KB	7E4FFFh – 7E4000h
		4KB	7E3FFFh – 7E3000h
		4KB	7E2FFFh – 7E2000h
		4KB	7E1FFFh – 7E1000h
		4KB	7E0FFFh – 7E0000h
⋮	⋮	⋮	
64KB	32KB	4KB	00FFFFh – 00F000h
		4KB	00EFFFh – 00E000h
		4KB	00DFFFh – 00D000h
		4KB	00CFFFh – 00C000h
		4KB	00BFFFh – 00B000h
		4KB	00AFFFh – 00A000h
		4KB	009FFFh – 009000h
		4KB	008FFFh – 008000h
	32KB	4KB	007FFFh – 007000h
		4KB	006FFFh – 006000h
		4KB	005FFFh – 005000h
		4KB	004FFFh – 004000h
		4KB	003FFFh – 003000h
		4KB	002FFFh – 002000h
		4KB	001FFFh – 001000h
		4KB	000FFFh – 000000h

Page Program Detail

1-256 byte	Page Address Range
256 bytes	7FFFFFh – 7FFF00h
256 bytes	7FFEFFh – 7FFE00h
256 bytes	7FFDFFh – 7FFD00h
256 bytes	7FFCFFh – 7FFC00h
256 bytes	7FFBFFh – 7FFB00h
256 bytes	7FFAFFh – 7FFA00h
256 bytes	7FF9FFh – 7FF900h
256 bytes	7FF8FFh – 7FF800h
256 bytes	7FF7FFh – 7FF700h
256 bytes	7FF6FFh – 7FF600h
256 bytes	7FF5FFh – 7FF500h
256 bytes	7FF4FFh – 7FF400h
256 bytes	7FF3FFh – 7FF300h
256 bytes	7FF2FFh – 7FF200h
256 bytes	7FF1FFh – 7FF100h
256 bytes	7FF0FFh – 7FF000h
256 bytes	7FEFFFh – 7FEF00h
256 bytes	7FEEFFh – 7FEE00h
256 bytes	7FEDFFh – 7FED00h
256 bytes	7FECFFh – 7FEC00h
256 bytes	7FEBFFh – 7FEB00h
256 bytes	7FEAFFh – 7FEA00h
256 bytes	7FE9FFh – 7FE900h
256 bytes	7FE8FFh – 7FE800h
⋮	
256 bytes	0017FFh – 001700h
256 bytes	0016FFh – 001600h
256 bytes	0015FFh – 001500h
256 bytes	0014FFh – 001400h
256 bytes	0013FFh – 001300h
256 bytes	0012FFh – 001200h
256 bytes	0011FFh – 001100h
256 bytes	0010FFh – 001000h
256 bytes	000FFFh – 000F00h
256 bytes	000EFFh – 000E00h
256 bytes	000DFFh – 000D00h
256 bytes	000CFFh – 000C00h
256 bytes	000BFFh – 000B00h
256 bytes	000AFFh – 000A00h
256 bytes	0009FFh – 000900h
256 bytes	0008FFh – 000800h
256 bytes	0007FFh – 000700h
256 bytes	0006FFh – 000600h
256 bytes	0005FFh – 000500h
256 bytes	0004FFh – 000400h
256 bytes	0003FFh – 000300h
256 bytes	0002FFh – 000200h
256 bytes	0001FFh – 000100h
256 bytes	0000FFh – 000000h

Figure 5. Memory Architecture Diagram

5. Device Operation

5.1 Standard SPI Operation

The AT25SL641 features a serial peripheral interface on four signals: Serial Clock (SCK). Chip Select ($\overline{\text{CS}}$), Serial Data Input (SI) and Serial Data Output (SO). Standard SPI commands use the SI input pin to serially write commands, addresses or data to the device on the rising edge of SCK. The SO output pin is used to read data or status from the device on the falling edge of SCK.

SPI bus operation Modes 0 (0, 0) and 3 (1, 1) are supported. The primary difference between Mode 0 and Mode 3 concerns the normal state of the SCK signal when the SPI bus master is in standby and data is not being transferred to the Serial Flash. For Mode 0 the SCK signal is normally low on the falling and rising edges of $\overline{\text{CS}}$. For Mode 3 the SCK signal is normally high on the falling and rising edges of $\overline{\text{CS}}$.

5.2 Dual SPI Operation

The AT25SL641 supports Dual SPI operation. This command allows data to be transferred to or from the device at two times the rate of the standard SPI. The Dual Read command is ideal for quickly downloading code to RAM upon power-up (code-shadowing) or for executing non-speed- critical code directly from the SPI bus (XiP). When using Dual SPI commands the SI and SO pins become bidirectional I/0 pins; IO$_0$ and IO$_1$.

5.3 Quad SPI Operation

The AT25SL641 supports Quad SPI operation. This command allows data to be transferred to or from the device at four times the rate of the standard SPI. The Quad Read command offers a significant improvement in continuous and random access transfer rates allowing fast code- shadowing to RAM or execution directly from the SPI bus (XiP). When using Quad SPI command the SI and SO pins become bidirectional IO$_0$ and IO$_1$, and the $\overline{\text{WP}}$ and $\overline{\text{HOLD}}$ pins become IO$_2$ and IO$_3$ respectively. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register-2 to be set.

5.4 QPI Operation

The AT25SL641 supports Quad Peripheral Interface (QPI) operation when the device is switched from Standard/Dual/ Quad SPI mode to QPI mode using the Enable QPI (38h) command. To enable QPI mode, the non-volatile Quad Enable bit (QE) in Status Register-2 is required to be set. When using QPI commands, the SI and SO pins become bidirectional IO$_0$ and IO$_1$, and the $\overline{\text{WP}}$ and $\overline{\text{HOLD}}$ pins become IO$_2$ and IO$_3$ respectively.

The typical SPI protocol requires that the byte-long command code being shifted into the device only via SI pin in eight serial clocks. The QPI mode utilizes all four I/O pins to input the command code, thus only two serial clocks are required. This can significantly reduce the SPI command overhead and improve system performance in an XiP environment. Standard/Dual/Quad SPI mode and QPI mode are exclusive. Only one mode can be active at any given time. The enable QPI (38h) and Disable QPI/ Disable QPI 2 (FFh) commands are used to switch between these two modes. Upon power-up or after software reset using the Reset (99h) command, the default state of the device is Standard/Dual/Quad SPI mode.

6. Write Protection

To protect inadvertent writes by the possible noise, several means of protection are applied to the Flash memory.

6.1 Write Protect Features

- While Power-on reset, all operations are disabled and no command is recognized.
- An internal time delay of t_{PUW} can protect the data against inadvertent changes while the power supply is outside the operating specification. This includes the Write Enable, Page program, Block Erase, Chip Erase, Write Security Register and the Write Status Register commands.
- For data changes, Write Enable command must be issued to set the Write Enable Latch (WEL) bit to “0”. Power-up, Completion of Write Disable, Write Status Register, Page program, Block Erase, and Chip Erase are subjected to this condition.
- Using setting the Status Register protect (SRP) and Block protect (SEC, TB, BP2, BP1, and BP0) bits a portion of memory can be configured as reading only called software protection.
- Write Protect ($\overline{\text{WP}}$) pin can control to change the Status Register under hardware control.
- The Deep Power-Down mode provides extra protection from unexpected data changes as all commands are ignored under this status except for Release Deep Power-Down command.

7. Status Register

The Read Status Register command can be used to provide status on the availability of the Flash memory array, if the device is write enabled or disabled the state of write protection and the Quad SPI setting. The Write Status Register command can be used to configure the devices writes protection features and Quad SPI setting. Write access to the Status Register is controlled by in some cases of the $\overline{\text{WP}}$ pin.

Table 2. Status Register-1

S7	S6	S5	S4	S3	S2	S1	S0
SRP0	**SEC**	**TB**	**BP2**	**BP1**	**BP0**	**WEL**	**BUSY**
Status Register Protect 0 (Non- Volatile)	Sector Protect (Non-Volatile)	Top/Bottom Write Protect (Non- Volatile)	Block Protect (Non- Volatile)	Block Protect (Non-Volatile)	Block Protect (Non-Volatile)	Write Enable Latch	Erase or Write in Progress

Table 3. Status Register-2

S15	S14	S13	S12	S11	S10	S9	S8
SUS	**CMP**	**(R)**	**(R)**	**(R)**	**(R)**	**QE**	**SRP1**
Suspend Status	Complement Protect (Non-Volatile)	Reserved	Reserved	Reserved	Reserved	Quad Enable (Non-Volatile)	Register Protect 1 (Non-Volatile)

7.1 Busy

BUSY is a read only bit in the status register (S0) that is set to a 1 state when the device is executing a Page Program, Erase, Write Status Register or Write Security Register command. During this time, the device ignores further commands except for the Read Status Register and Erase / Program Suspend command (see t_W, t_{PP}, t_{SE}, t_{BE1}, t_{BE2} and t_{CE} in AC Characteristics). When the Program, Erase, Write Status Register or Write Security Register command has completed, the BUSY bit is cleared to a 0 state indicating the device is ready for further commands.

7.2 Write Enable Latch (WEL)

Write Enable Latch (WEL) is a read only bit in the status register (S1) that is set to a 1 after executing a Write Enable command. The WEL status bit is cleared to a 0 when device is write disabled. A write disable state occurs upon power-up or after any of the following commands: Write Disable, Page Program, Erase and Write Status Register.

7.3 Block Protect Bits (BP2, BP1, BP0)

The Block Protect Bits (BP2, BP1, BP0) are non-volatile read/write bits in the status register (S4, S3, and S2) that provide write protection control and status. Block protect bits can be set using the Write Status Register Command (see t_W in AC characteristics). All, none or a portion of the memory array can be protected from Program and Erase commands (see Table 5 and Table 6). The factory default setting for the Block Protection Bits is 0, none of the array protected.

7.4 Top/Bottom Block protect (TB)

The Top/Bottom bit (TB) is non-volatile bits in the status register (S5) that controls if the Block Protect Bits (BP2, BP1, BP0) protect from the Top (TB = 0) or the Bottom (TB = 1) of the array, as shown in the Table 5 and Table 6. The factory default setting is TB = 0. The TB bit can be set with the Write Status Register Command depending on the state of the SRP0, SRP1 and WEL bits.

7.5 Sector/Block Protect (SEC)

The Sector protect bit (SEC) is non-volatile bits in the status register (S6) that controls if the Block Protect bits (BP2, BP1, BP0) protect 4-kB Sectors (SEC = 1) or 64-kB blocks (SEC = 0) in the Top (TB = 0) or the Bottom (TB = 1) of the array, as shown in Table 5 and Table 6. The default setting is SEC = 0.

7.6 Status Register Protect (SRP1, SRP0)

The Status Register Protect bits (SRP1 and SRP0) are non-volatile read/write bits in the status register (S8 and S7). The SRP bits control the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable (OTP) protection.

Table 4. Status Register Protection

SRP1	**SRP0**	**$\overline{\text{WP}}$**	**Status Register**	**Description**
0	0	X	Software Protected	$\overline{\text{WP}}$ pin no control. The register can be written to after a Write Enable command, WEL = 1. [Factory Default]
0	1	0	Hardware Protected	When $\overline{\text{WP}}$ pin is low the Status Register locked and can not be written to.
0	1	1	Hardware Unprotected	When $\overline{\text{WP}}$ pin is high the Status register is unlocked and can be written to after a Write Enable command, WEL = 1.
1	0	X	Power Supply Lock-Down	Status Register is protected and cannot be written to again until the next power-down, power-up cycle (Note 1).
1	1	X	One Time Program	Status Register is permanently protected and cannot be written to.

Note: 1. When SRP1, SRP0 = (1,0), a power-down, power-up cycle changes SRP1, SRP0 to the (0,0) state.

7.7 Quad Enable (QE)

The Quad Enable (QE) bit is a non-volatile read/write bit in the status register (S9) that allows Quad operation. When the QE bit is set to a 0 state (factory default) the $\overline{\text{WP}}$ pin and $\overline{\text{HOLD}}$ are enabled. When the QE pin is set to a 1 the Quad IO_2 and IO_3 pins are enabled.

WARNING: Never set the QE bit to a 1 during standard SPI or Dual SPI operation if the $\overline{\text{WP}}$ or $\overline{\text{HOLD}}$ pins are tied directly to the power supply or ground.

7.8 Complement Protect (CMP)

The Complement Protect bit (CMP) is a non-volatile read/write bit in the status register (S14). It is used in conjunction with SEC, TB, BP2, BP1 and BP0 bits to provide more flexibility for the array protection. Once CMP is set to 1, previous array protection set by SEC, TB, BP2, BP1 and BP0 are reversed. For instance, when CMP = 0, a top 4 kB sector can be protected while the rest of the array is not; when CMP = 1, the top 4 kB sector becomes unprotected while the rest of the array become read-only. See Table 5 and Table 6 for details. The default setting is CMP = 0.

7.9 Erase/Program Suspend Status (SUS)

The Suspend Status bit (SUS) is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75h) command. The SUS status bit is cleared to 0 by Erase/Program Resume (7Ah) command as well as a power-down, power-up cycle.

Table 5. Status Register Memory Protection (CMP = 0)

Status Register Bits					Memory Protection			
SEC	**TB**	**BP2**	**BP1**	**BP0**	**Sector(s)**	**Addresses**	**Density**	**Portion**
x	X	0	0	0	NONE	NONE	NONE	NONE
0	0	0	0	1	126 and 127	7E0000h - 7FFFFFh	128 kB	Upper 1/64
0	0	0	1	0	124 - 127	7C0000h - 7FFFFFh	256 kB	Upper 1/32
0	0	0	1	1	120 - 127	780000h - 7FFFFFh	512 kB	Upper 1/16
0	0	1	0	0	112 - 127	700000h - 7FFFFFh	1 MB	Upper 1/8
0	0	1	0	1	96 - 127	600000h - 7FFFFFh	2 MB	Upper 1/4
0	0	1	1	0	64 - 127	400000h - 7FFFFFh	4 MB	Upper 1/2
0	1	0	0	1	0 and 1	000000h - 01FFFFh	128 kB	Lower 1/64
0	1	0	1	0	0 - 3	000000h - 03FFFFh	256 kB	Lower 1/32
0	1	0	1	1	0 - 7	000000h - 07FFFFh	512 kB	Lower 1/16
0	1	1	0	0	0 - 15	000000h - 0FFFFFh	1 MB	Lower 1/8
0	1	1	0	1	0 - 31	000000h - 1FFFFFh	2 MB	Lower 1/4
0	1	1	1	0	0 - 63	000000h - 3FFFFFh	4 MB	Lower 1/2
X	X	1	1	1	0 - 127	000000h - 7FFFFFh	8 MB	ALL
1	0	0	0	1	127	7FF000h - 7FFFFFh	4 kB	U – 1/2048
1	0	0	1	0	127	7FE000h - 7FFFFFh	8 kB	U – 1/1024
1	0	0	1	1	127	7FC000h - 7FFFFFh	16 kB	U – 1/512
1	0	1	0	X	127	7F8000h - 7FFFFFh	32 kB	U – 1/256
1	1	0	0	1	0	000000h - 000FFFh	4 kB	L – 1/2048
1	1	0	1	0	0	000000h - 001FFFh	8 kB	L – 1/1024
1	1	0	1	1	0	000000h - 003FFFh	16 kB	L – 1/512
1	1	1	0	X	0	000000h - 007FFFh	32 kB	L – 1/256

1. X = Don’t care.
2. L = Lower; U = Upper.
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command is ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 1 in Appendix A for details.

Table 6. Status Register Memory Protection (CMP = 1)

Status Register Bits					Memory Protection			
SEC	**TB**	**BP2**	**BP1**	**BP0**	**Sector(s)**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	0 - 127	000000h - 7FFFFFh	8 MB	ALL
0	0	0	0	1	0 - 125	000000h – 7DFFFFh	8,064 kB	Lower 63/64
0	0	0	1	0	0 - 121	000000h – 7BFFFFh	7,936 kB	Lower 31/32
0	0	0	1	1	0 - 119	000000h – 77FFFFh	7,680 kB	Lower 15/16
0	0	1	0	0	0 - 111	000000h – 6FFFFFh	7,168 kB	Lower 7/8
0	0	1	0	1	0 - 95	000000h – 5FFFFFh	6 MB	Lower 3/4
0	0	1	1	0	0 - 63	000000h – 3FFFFFh	4 MB	Lower 1/2
0	1	0	0	1	2 - 127	020000h - 7FFFFFh	8,064 kB	Upper 63/64
0	1	0	1	0	4 - 127	040000h - 7FFFFFh	7,936 kB	Upper 31/32
0	1	0	1	1	8 - 127	080000h - 7FFFFFh	7,680 kB	Upper 15/16
0	1	1	0	0	16 - 127	100000h - 7FFFFFh	7,168 kB	Upper 7/8
0	1	1	0	1	32 - 127	200000h - 7FFFFFh	6 MB	Upper 3/4
0	1	1	1	0	64 - 127	400000h - 7FFFFFh	4 MB	Upper 1/2
X	X	1	1	1	NONE	NONE	NONE	NONE
1	0	0	0	1	0 - 127	000000h - 7FEFFFh	8,188 kB	L – 2047/2048
1	0	0	1	0	0 - 127	000000h - 7FDFFFh	8,184 kB	L – 1023/1024
1	0	0	1	1	0 - 127	000000h - 7FBFFFh	8,176 kB	L – 511/512
1	0	1	0	X	0 - 127	000000h - 7F7FFFh	8,160 kB	L – 255/256
1	1	0	0	1	0 - 127	001000h - 7FFFFFh	8,188 kB	U – 2047/2048 (4)
1	1	0	1	0	0 - 127	002000h - 7FFFFFh	8,184 kB	U – 1023/1024
1	1	0	1	1	0 - 127	004000h - 7FFFFFh	8,176 kB	U – 511/512
1	1	1	0	X	0 - 127	008000h - 7FFFFFh	8,160 kB	U – 255/256

1. X = don’t care.
2. L = Lower; U = Upper.
3. If any Erase or Program command specifies a memory region that contains protected data portion, this command is ignored.
4. Note 3 does not apply to this Status Register Bit setting. See Errata 2 in Appendix A for details.

8. Commands

The SPI command set of the AT25SL641 consists of thirty eight basic commands, and the QPI command set of the AT25SL641 consists of thirty one basic commands that are fully controlled through the SPI bus (see Table 8, Table 9, and Table 10). Commands are initiated with the falling edge of Chip Select ($\overline{CS}$) and are completed with the rising edge of edge $\overline{CS}$. The first byte of data clocked into the input pins (SI or $IO_{3:0}$) provides the command code. Data on the SI input is sampled on the rising edge of clock with most significant bit (MSB) first.

Clock relative timing diagrams are included for each command below. All read commands can be completed after any clocked bit. However, all commands that Write, Program or Erase must complete on a byte boundary ($\overline{CS}$ driven high after a full 8-bit have been clocked); otherwise, the command is terminated. This feature further protects the device from inadvertent writes. Also, while the memory is being programmed or erased, or when the Status Register is being written, all commands except for Read Register are ignored until the program or erase cycle has completed.

Table 7. Manufacturer and Device Identification

		ID code	Command
Manufacturer ID	Renesas Electronics	1Fh	90h, 92h, 94h, 9Fh
Device ID	AT25SL641	16h	90h, 92h, 94h, ABh
Memory Type ID	SPI / QPI	43h	9Fh
Capacity Type ID	64M	17h	9Fh

8.1 Command Set Tables

Table 8. Command Set Table 1 (SPI Commands)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
(Clock Number)	**(0 - 7)**	**(8 - 15)**	**(16 - 23)**	**(24 - 31)**	**(32 - 39)**	**(40 - 47)**
Write Enable	06h					
Write Enable For Volatile Status Register	50h					
Write Disable	04h					
Read Status Register-1	05h	(SR7-SR0)(2)				
Read Status Register-2	35h	(SR15-SR8)(2)				
Write Status Register-1	01h	(SR7-SR0)	(SR15-SR8)			
Write Status Register-2	31h	(SR15-SR8)				
Read Data	03h	A23-A16	A15-A8	A7-A0	(D7-D0)	
Fast Read Data	0Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)
Page Program	02h	A23-A16	A15-A8	A7-A0	(D7-D0)(3)	
Enable QPI	38h					
Block Erase (4 kB)	20h	A23-A16	A15-A8	A7-A0		
Block Erase (32 kB)	52h	A23-A16	A15-A8	A7-A0		
Block Erase (64 kB)	D8h	A23-A16	A15-A8	A7-A0		
Chip Erase	60h/C7h					
Erase/Program Suspend	75h					
Erase/Program Resume	7Ah					
Deep Power-Down	B9h					

Table 8. Command Set Table 1 (SPI Commands) *(Continued)*

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
(Clock Number)	**(0 - 7)**	**(8 - 15)**	**(16 - 23)**	**(24 - 31)**	**(32 - 39)**	**(40 - 47)**
Release Deep Power Down/Device ID[4]	ABh	dummy	dummy	dummy	(ID7-ID0)[2]	
Read Manufacturer/ Device ID[4]	90h	00h	00h	00h or 01h	(MID7-MID0)	(DID7-DID0)
Read JEDEC ID	9Fh	(MID7-MID0) (Manufacturer)	(D7-D0) (Memory Type)	(D7-D0) (Capacity Type)		
Reset Enable	66h					
Reset	99h					
Enter Secured OTP	B1h					
Exit Secured OTP	C1h					
Read Security Register	2Bh	(SC7-SC0) [10]				
Write Security Register	2Fh					
Read Serial Flash Discovery Parameters	5Ah	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)

Table 9. Command Set Table 2 (Dual SPI Commands)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
(Clock Number)	**(0 - 7)**	**(8 - 15)**	**(16 - 23)**	**(24 - 31)**	**(32 - 39)**	**(40 - 47)**
Fast Read Dual Output	3Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)[6]
Fast Read Dual I/O	BBh	A23-A8[5]	A7-A0, M7-M0	(D7-D0, …)[6]		
Read Dual Manufacturer/ Device ID[4]	92h	0000h	(00h, xxxx) or (01h, xxxx)	(MID7-MID0) (DID7-DID0)[6]		

Table 10. Command Set Table 3 (Quad SPI Commands)

Command Name	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5	Byte 6
(Clock Number)	**(0 - 7)**	**(8 - 15)**	**(16 - 23)**	**(24 - 31)**	**(32 - 39)**	**(40 - 47)**
Fast Read Quad Output	6Bh	A23-A16	A15-A8	A7-A0	dummy	(D7-D0) [8]
Fast Read Quad I/O	EBh	A23-A0, M7-M0[7]	(xxx, D7-D0,…)[9]	(D7-D0, …)[8]		
Quad Page Program	33h	A23-A0 (D7-D0, …)[8]				
Read Quad Manufacturer /Device ID[4]	94h	(00_0000h, xx) or (00_0001h, xx)	(xxxx,MID7-MID0) (xxxx,DID7-DID0)[9]			
Word Read Quad I/O	E7h	A23-A0, M7-M0[7]	(xx, D7-D0..)	(D7-D0)[8]		
Set Burst with Wrap	77h	xxxxxx, W6-W4[7]				

Table 11. Command Set Table 4 (QPI Commands)

Command Name		Byte 1	Byte 3	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
(Clock Number)		(0, 1)	(2, 3)	(4, 5)	(6, 7)	(8, 9)	(10, 11)	(12, 13)	(14, 15)	(16, 17)
Write Enable		06h								
Write Enable for Volatile Status Register		50h								
Write Disable		04h								
Read Status Register-1		05h	(SR7-SR0)(2)							
Read Status Register-2		35h	(SR15-SR8)(2)							
Write Status Register-1(5)		01h	(SR7-SR0)	(SR15-SR8)						
Write Status Register-2		31h	(SR15-SR8)							
Set Read Parameter		C0h	P7-P0							
Fast Read Data	>80 MHz	0Bh	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)		
	>104 MHz		A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	(D7-D0)	
	up to 133 MHz		A23:A16	A15:A8	A7:A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)
Page Program		02h	A23-A16	A15-A8	A7-A0	(D7-D0)(3)				
Block Erase (4 kB)		20h	A23-A16	A15-A8	A7-A0					
Block Erase (32 kB)		52h	A23-A16	A15-A8	A7-A0					
Block Erase (64 kB)		D8h	A23-A16	A15-A8	A7-A0					
Chip Erase		60h/C7h								
Erase/Program Suspend		75h								
Erase/Program Resume		7Ah								
Deep Power-Down		B9h								
Release Deep Power Down		ABh								
Read Manufacturer/Device ID(4)		90h	00h	00h	00h or 01h	(MID7-MID0)	(DID7-DID0)			
Read JEDEC ID(4)		9Fh	(MID7-MID0) Manufacturer	(D7-D0) Memory Type	(D7-D0) Capacity Type					
Enter Security		B1h								
Exit Security		C1h								
Read Security Register		2Bh	(SC7-SC0)(10)							
Write Security Register		2Fh								

Table 11. Command Set Table 4 (QPI Commands) ***(Continued)***

Command Name		Byte 1	Byte 3	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9
(Clock Number)		**(0, 1)**	**(2, 3)**	**(4, 5)**	**(6, 7)**	**(8, 9)**	**(10, 11)**	**(12, 13)**	**(14, 15)**	**(16, 17)**
Fast Read Quad I/O(11)	>80 MHz	EBh	A23-A16	A15-A8	A7-A0	(M7-M0)	Dummy	(D7-D0)		
	>104 MHz		A23-A16	A15-A8	A7-A0	(M7-M0)	Dummy	Dummy	(D7-D0)	
	up to 133 MHz		A23-A16	A15-A8	A7-A0	(M7-M0)	Dummy	Dummy	Dummy	(D7-D0)
Reset Enable		66h								
Reset		99h								
Disable QPI		FFh								
Burst Read with Wrap	>80 MHz	0Ch	A23-A16	A15-A8	A7-A0	Dummy	Dummy	(D7-D0)		
	>104 MHz		A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	(D7-D0)	
	up to 133 MHz		A23-A16	A15-A8	A7-A0	Dummy	Dummy	Dummy	Dummy	(D7-D0)
Quad Page Program		33h	A23-A16	A15-A8	A7-A0	(D7-D0)				

1. Data bytes are shifted with Most Significant Bit first. Byte fields with data in parenthesis "()" indicate data being read from the device on the IO pin.
2. SR = status register, The Status Register contents and Device ID repeats continuously until $\overline{CS}$ terminates the command.
3. At least one byte of data input is required for Page Program, Quad Page Program and Program Security Register, up to 256 bytes of data input. If more than 256 bytes of data are sent to the device, the addressing wraps to the beginning of the page and overwrites previously sent data.
4. See **Table 7** for Device ID information.
5. Dual Input Address
   IO0 = A22, A20, A18, A16, A14, A12, A10, A8, A6, A4, A2, A0, M6, M4, M2, M0
   IO1 = A23, A21, A19, A17, A15, A13, A11, A9, A7, A5, A3, A1, M7, M5, M3, M1
6. Dual Output data
   IO0 = (D6, D4, D2, D0)
   IO1 = (D7, D5, D3, D1)
7. Quad Input Address

Quad Input Address	Set Burst with Wrap Input
IO0 = A20, A16, A12, A8, A4, A0, M4, M0	IO0 = x, x, x, x, x, x, W4, x
IO1 = A21, A17, A13, A9, A5, A1, M5, M1	O1 = x, x, x, x, x, x, W5, x
IO2 = A22, A18, A14, A10, A6, A2, M6, M2	IO2 = x, x, x, x, x, x, W6, x
IO3 = A23, A19, A15, A11, A7, A3, M7, M3	IO3 = x, x, x, x, x, x, x x

8. Quad Input/ Output Data
   IO0 = (D4, D0…)
   IO1 = (D5, D1…)
   IO2 = (D6, D2…)
   IO3 = (D7, D3…)
9. Fast Read Quad I/O Data Output
   IO0 = (x, x, x, x, D4, D0…)
   IO1 = (x, x, x, x, D5, D1…)
   IO2 = (x, x, x, x, D6, D2…)
   IO3 = (x, x, x, x, D7, D3…)
10. SC = security register
11. The M7-M0 bits are counted as dummy clocks.

8.2 Write Enable (06h)

Write Enable command is for setting the Write Enable Latch (WEL) bit in the Status Register. The WEL bit must be set prior to every Program, Erase and Write Status Register command. To enter the Write Enable command, $\overline{\text{CS}}$ goes low prior to the command (06h) being driven onto the SI pin on the rising edge of SCK, and then driving $\overline{\text{CS}}$ high.

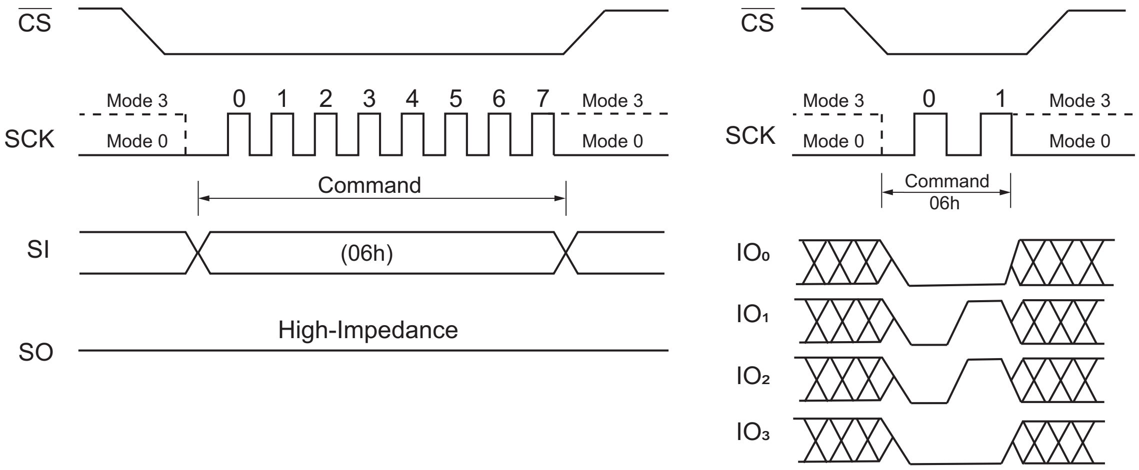


Figure 6. Write Enable Command for SPI Mode (left) and QPI Mode (right)

8.3 Write Enable for Volatile Status Register (50h)

This command gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the Status Register non-volatile bits. To write the volatile values into the Status Register bits, the Write Enable for Volatile Status Register (50h) command must be issued prior to a Write Status Register (01h) command.

The Write Enable for Volatile Status Register command (Figure 7) does not set the Write Enable Latch (WEL) bit. Once Write Enable for Volatile Status Register is set, do not issue a Write Enable command or Write Status Register command (01h or 31h). When the Write Enable for Volatile Status Register (50h) is executed in QPI Mode, the SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 must be driven to high after Write Status Register command (01h). Once the Read Status Register (05h or 31h) command is issued, the read values of the SUS bit (S15) and Reserved bits (S13, S12, S11 and S10) of the Status Register-2 are ignored.

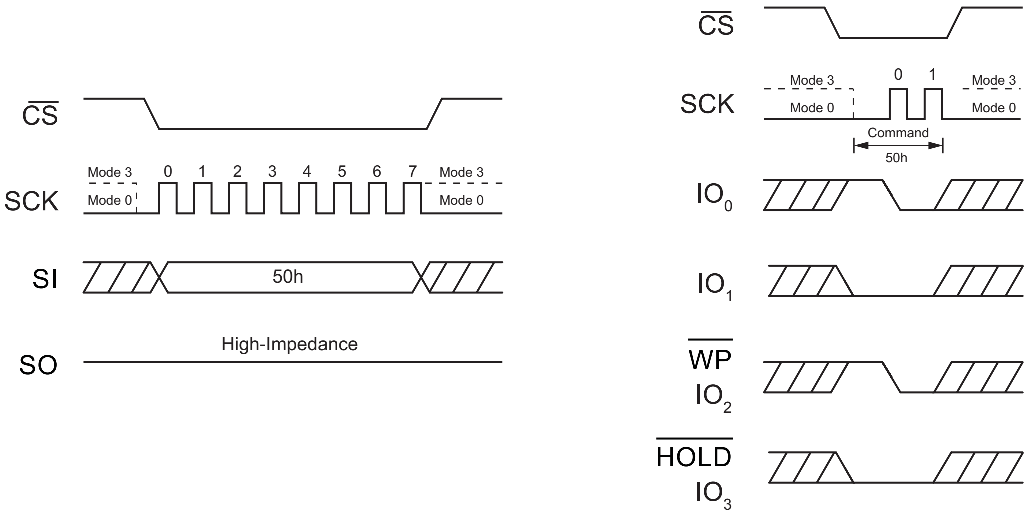


Figure 7. Write Enable for Volatile Status Register Command for SPI Mode (left) and QPI Mode (right)

8.4 Write Disable (04h)

The Write Disable command is to reset the Write Enable Latch (WEL) bit in the Status Register. To enter the Write Disable command, $\overline{CS}$ goes low prior to the command 04h being driven onto the SI pin on the rising edge of SCK, and then driving $\overline{CS}$ high. The WEL bit is automatically reset write-disable status of “0” after power-up and upon completion of the every Program, Erase and Write Status Register command.

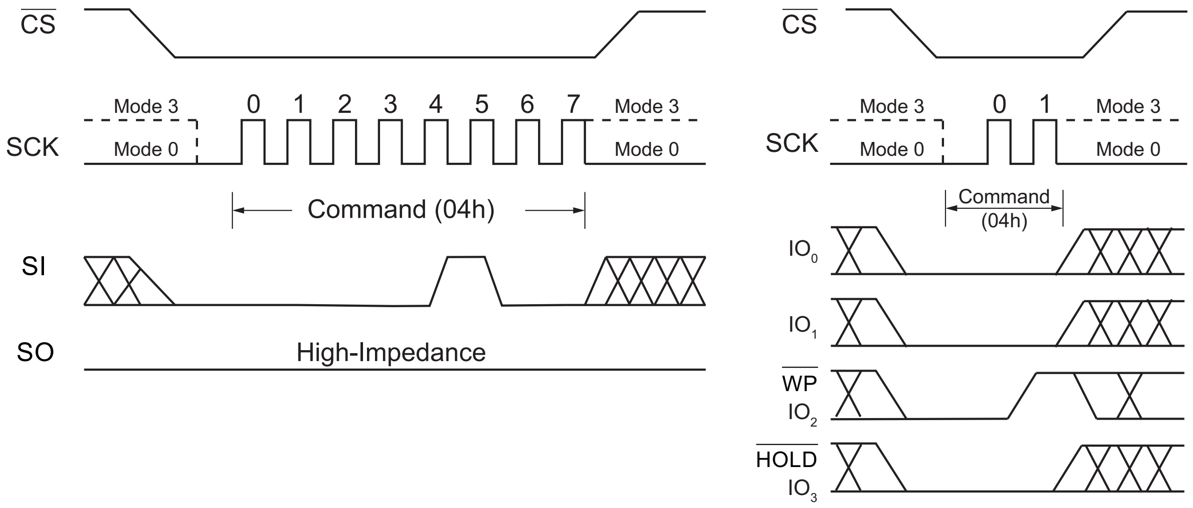


Figure 8. Write Disable Command for SPI Mode (left) and QPI Mode (right)

8.5 Read Status Register-1 (05h) and Read Status Register-2 (35h)

The Read Status Register commands 05h and 35h are used to read Status Registers 1 and 2 respectively. The Read Status Register can be read at any time (even in program/erase/write Status Register and Write Security Register condition). It is recommended to check the BUSY bit before sending a new command when a Program, Erase, Write Status Register, or Write Status Register operation is in progress.

The command is entered by driving $\overline{CS}$ low and sending the command code (05h) for Status Register-1 or (35h) for Status Register-2 onto the SI pin on the rising edge of SCK. The Status Register bits are then shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first, as shown in (Figure 9 and Figure 10). The Status Register can be read continuously. The command is completed by driving $\overline{CS}$ high.

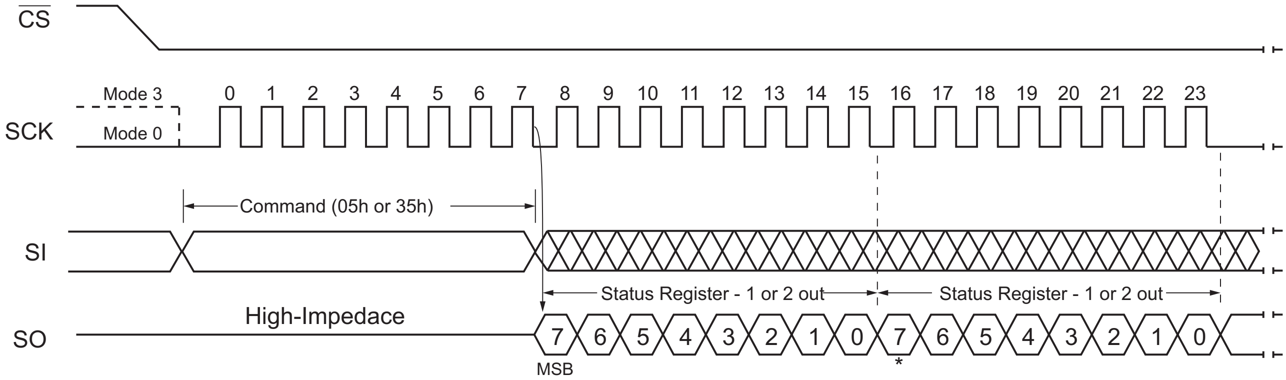


Figure 9. Read Status Register Command (SPI Mode)

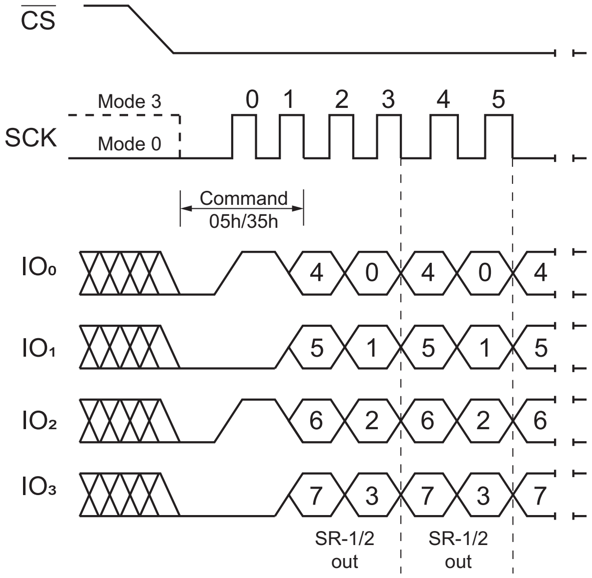


Figure 10. Read Status Register Command (QPI Mode)

8.6 Write Status Register (01h)

The Write Status Register command is used to write the non-volatile Status Register-1 bit (SRP0) and Status Register-2 bits (QE and SRP1). All other Status Register bit locations are read-only and are not affected by the Write Status Register command.

A Write Enable command must previously have been issued prior to setting Write Status Register Command (Status Register bit WEL must equal 1). Once the write is enabled, the command is entered by driving $\overline{CS}$ low, sending the command code, and then writing the status register data byte as illustrated in Figure 11 and Figure 12.

The $\overline{CS}$ pin must be driven high after either the eighth or sixteenth bit of data is clocked in. If this is not done, the Write Status Register command is not executed. If $\overline{CS}$ is driven high after the eighth clock, the CMP, QE, and SRP1 bits are cleared to 0. After $\overline{CS}$ is driven high, the self-timed Write Status Register cycle commences for a time duration of t_W (see Section 9.6, AC Electrical Characteristics).

While the Write Status Register cycle is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is driven high during the Write Status Register cycle and driven low when the cycle has finished and is ready to accept other commands. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in Status Register is cleared to 0.

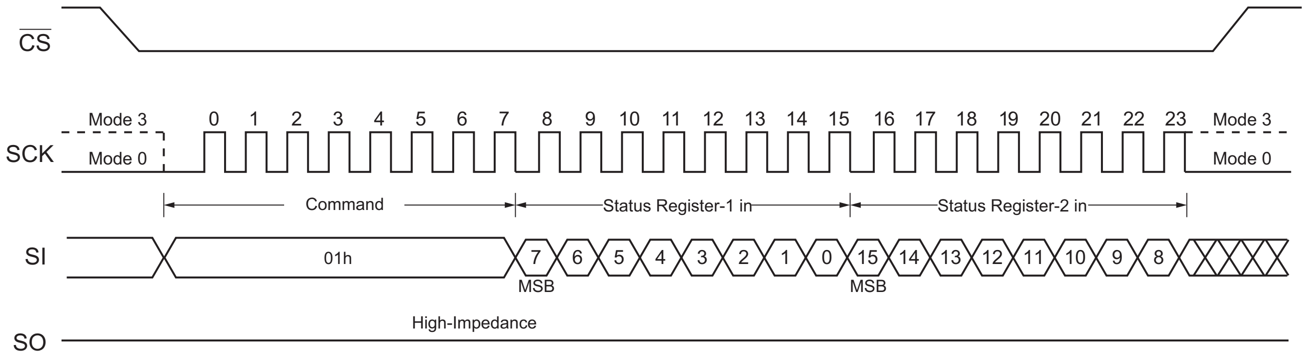


Figure 11. Write Status Register Command (SPI Mode)

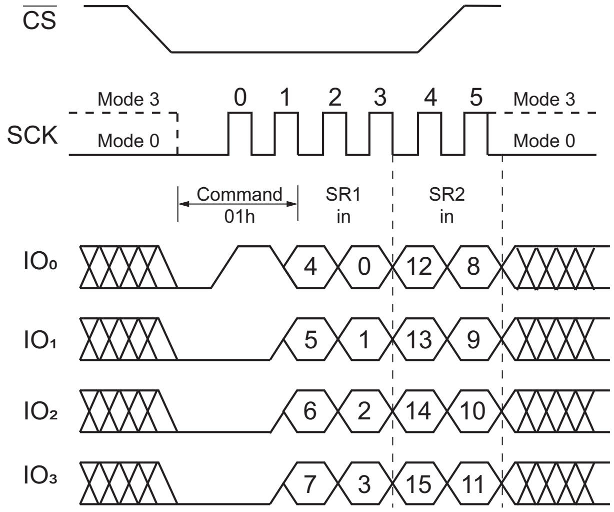


Figure 12. Write Status Register Command (QPI Mode)

8.7 Write Status Register-2 (31h)

The Write Status Register-2 command is used to write only non-volatile Status Register-2 bits (CMP, QE and SRP1).

A Write Enable command must previously have been issued prior to setting Write Status Register Command (Status Register bit WEL must equal 1). Once write is enabled, the command is entered by driving $\overline{CS}$ low, sending the command code, and then writing the Status Register data byte as illustrated in Figure 13 and Figure 14.

Using Write Status Register-2 (31h) command, software can individually access each one-byte Status Register via different commands.

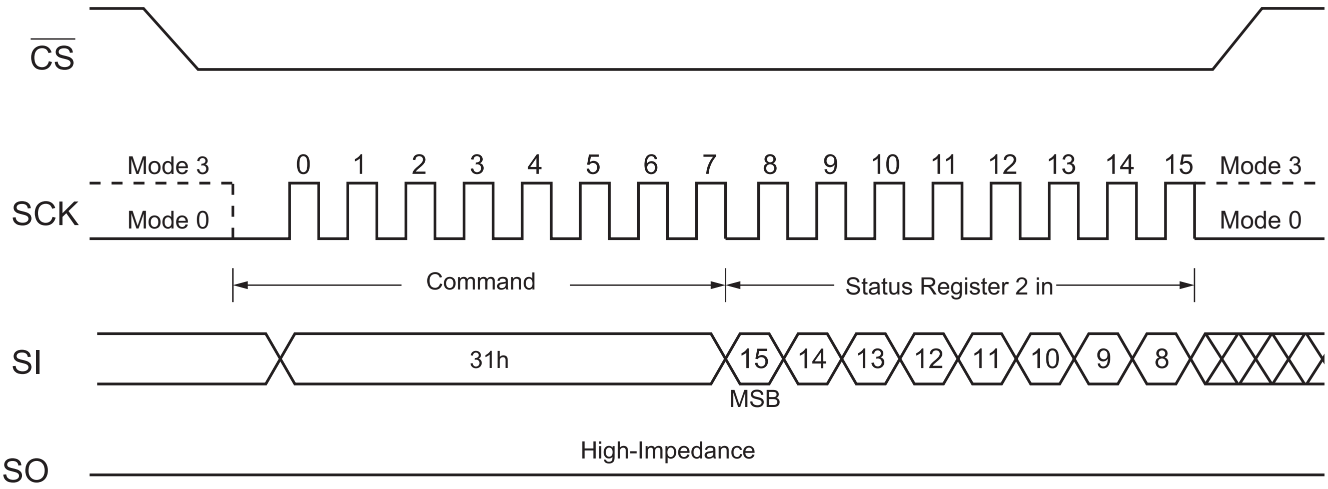


Figure 13. Write Status Register-2 Command (SPI Mode)

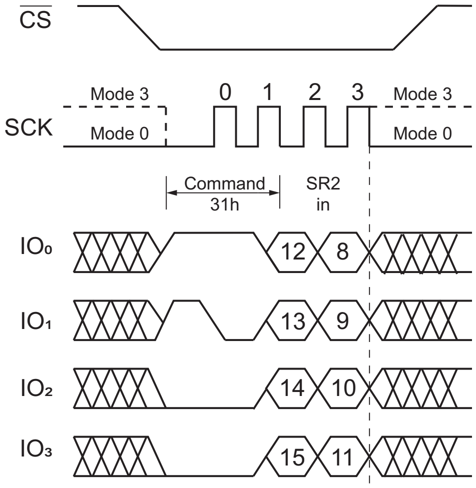


Figure 14. Write Status Register-2 Command (QPI Mode)

8.8 Set Read Parameters (C0h)

In QPI mode, to accommodate a wide range of applications with different needs for either maximum read frequency or minimum data access latency, the Set Read Parameters (C0h) command can be used to configure the number of dummy clocks for the Fast Read (0Bh), Fast Read Quad I/O (EBh), and Burst Read with Wrap (0Ch) commands, and to configure the number of bytes of wrap length for the Burst Read with Wrap (0Ch) command.

In Standard SPI mode, the Set Read Parameters (C0h) command is not accepted. The dummy clocks for various Fast Read commands in Standard/Dual/Quad SPI mode are fixed. The wrap length is set by the W6-W5 bits in the Set Burst with Wrap (77h) command. This setting remains unchanged when the device is switched from Standard SPI mode to QPI mode.

The default wrap length after a power up or a Reset command is 8 bytes, and the default number of dummy clocks is 4.

Table 12. Encoding of the P[5:4] Bits

P5, P4	Dummy Clocks	Maximum Read Frequency
00	4	80 MHz
01	4	80 MHz
10	6	104 MHz
11	8	133 MHz

Table 13. Encoding of the P[1:0] Bits

P1, P0	Wrap Length
0 0	8-byte
0 1	16-byte
1 0	32-byte
1 1	64-byte

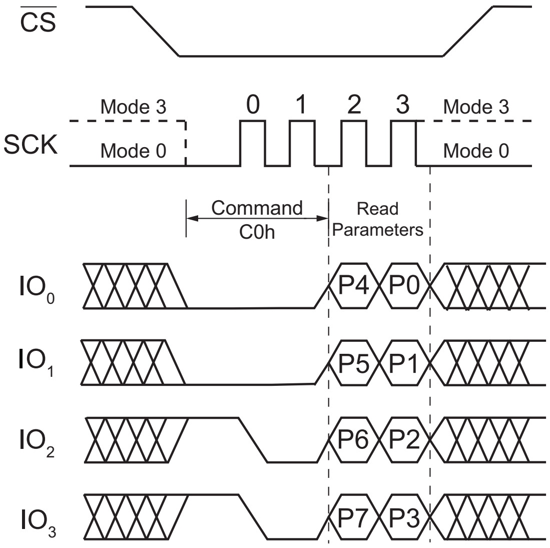


Figure 15. Set Read Parameters Command (QPI Mode)

8.9 Read Data (03h)

The Read Data command is used to read data out from the device. The command is initiated by driving the $\overline{\text{CS}}$ pin low and then sending the command code 03h, followed by a 24-bit address (A23- A0), onto the SI pin. After the address is received, the data byte of the addressed memory location is shifted out on the SO pin at the falling edge of SCK with the most significant bit (MSB) first. The address is automatically incremented to the next higher address and the next byte of data is shifted out, allowing for a continuous stream of data. This means that the entire memory can be accessed with a single command as long as the clock continues.

The command is completed by driving $\overline{\text{CS}}$ high. The Read Data command sequence is shown in Figure 16. If a Read Data command is issued while an Erase, Program, or Write Status Register cycle is in process (BUSY = 1) the command is ignored and does not effect the current cycle. The Read Data command allows clock rates from D.C to a maximum of f_R (see Section 9.6, AC Electrical Characteristics).

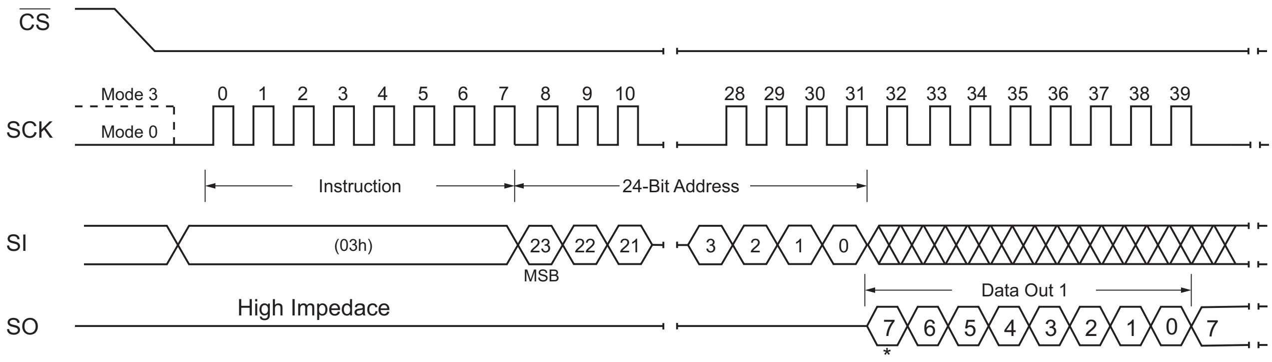


Figure 16. Read Data Command

8.10 Fast Read (0Bh)

The Fast Read command is a high speed reading mode that can operate at the highest possible frequency of FR. The address is latched on the rising edge of the SCK. After the 24-bit address, eight dummy clocks are shifted in (Figure 17). The dummy clocks allow the internal circuits the time required to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. Data of each bit shifts out on the falling edge of SCK.

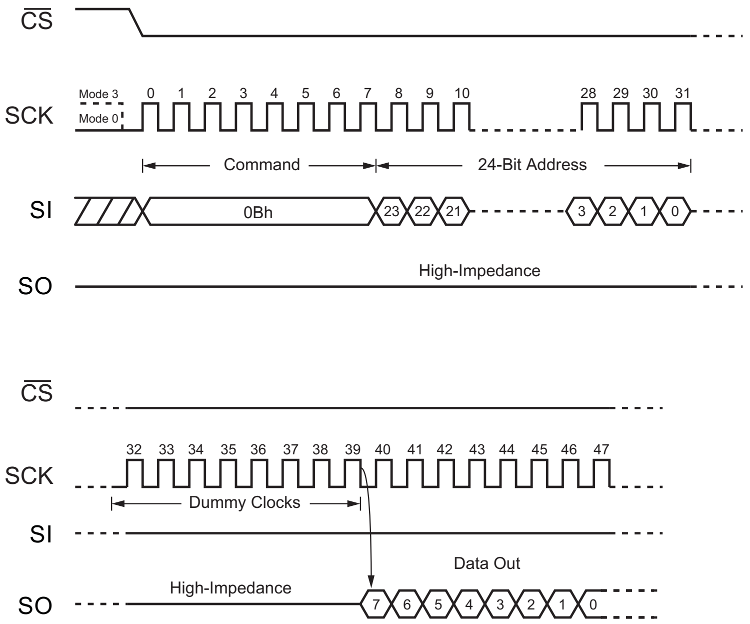
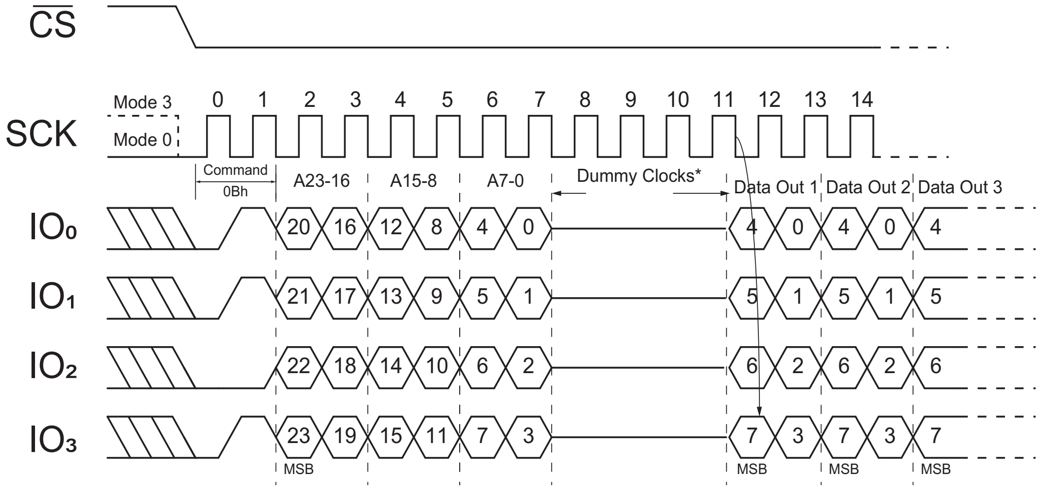


Figure 17. Fast Read Command (SPI Mode)

8.10.1 Fast Read in QPI Mode

When QPI mode is enabled, the number of dummy clock is configured by the Set Read Parameters (C0h) command to accommodate a wide range applications with different needs for either maximum Fast Read frequency or minimum data access latency. The number of dummy clock cycles can be configured as either 4, 6 or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command, as shown in Table 12. The default number of dummy clocks upon power up or after a Reset command is 4. See Figure 18.



* = “Set Read Parameters” command (C0h) can set the number of dummy clocks

Figure 18. Fast Read Command (QPI Mode)

8.11 Fast Read Dual Output (3Bh)

By using two pins (IO_0 and IO_1, instead of just IO_0), the Fast Read Dual Output command allows data to be transferred from the AT25SL641 at twice the rate of standard SPI devices. The Fast Read Dual Output command is ideal for quickly downloading code from Flash to RAM upon power-up or for application that cache code-segments to RAM for execution.

The Fast Read Dual Output command can operate at the highest possible frequency of F_R (see Section 9.6, AC Electrical Characteristics). After the 24-bit address, eight dummy clocks are driven on the SI pin, as shown in Figure 19. The dummy clocks allow the internal circuits the time required for setting up the initial address. During the dummy clocks, the data value on the SO pin is a "don't care". However, ensure the IO**0** pin is high-impedance before the falling edge of the first data out clock.

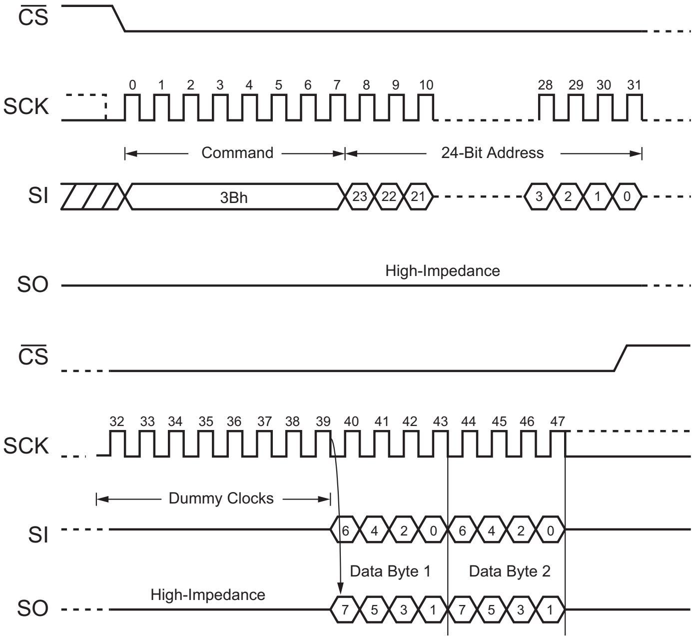


Figure 19. Fast Read Dual Output command (SPI Mode)

8.12 Fast Read Quad Output (6Bh)

By using four pins (IO_0, IO_1, IO_2, and IO_3), the Fast Read Quad Output command allows data to be transferred from the AT25SL641 at four times the rate of standard SPI devices. Prior to executing the 6Bh command, the Quad Enable (QE) bit of Status Register 2 must be set.

The Fast Read Quad Output command can operate at the highest possible frequency of F_R (see Section 9.6, AC Electrical Characteristics). This is accomplished by adding eight dummy clocks after the 24- bit address, as shown in Figure 20. The dummy clocks allow the internal circuits the time required to set up the initial address. During the dummy clocks, the data value on the SO pin is a “don’t care”. However, ensure the IO_0 pin is high-impedance before the falling edge of the first data out clock.

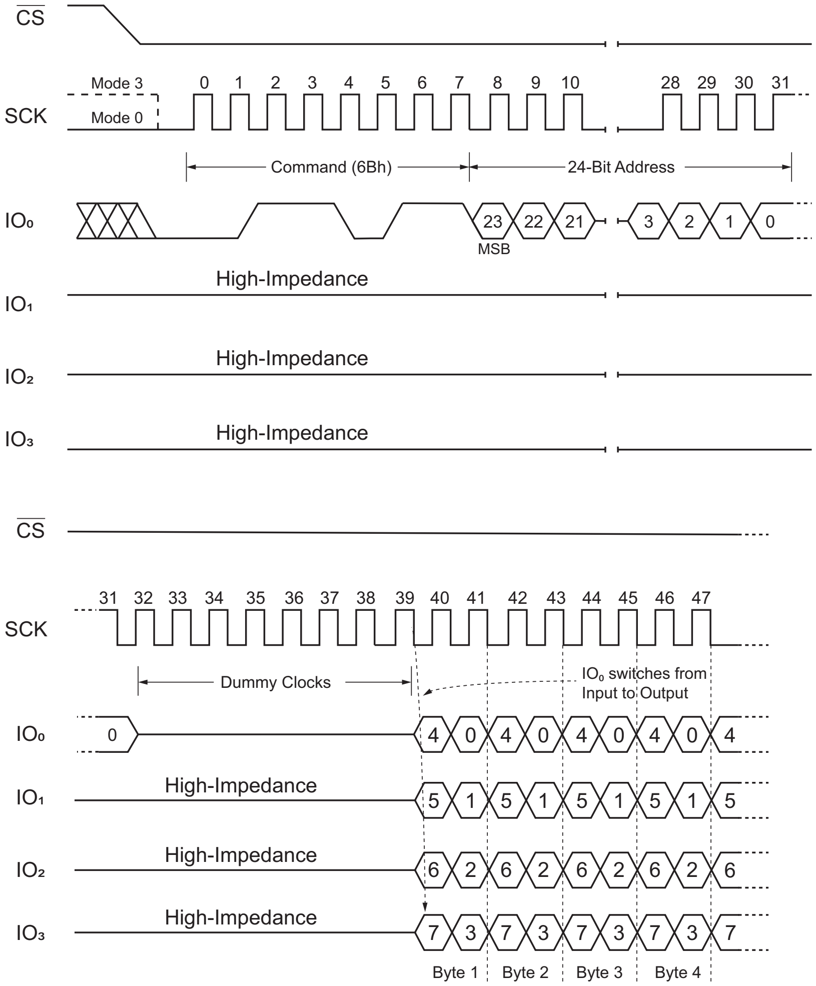


Figure 20. Fast Read Quad Output Command (SPI Mode)

8.13 Fast Read Dual I/O (BBh)

The Fast Read Dual I/O command reduces cycle overhead by using two IO pins: IO_0 and IO_1 to transfer data.

8.13.1 Continuous Read Mode

The Fast Read Dual I/O command supports a continuous read mode using the Mode bits (M7-0), which are shifted into the device after address bits (A23-0). The upper nibble of the Mode (M7-4) controls whether the command code must be driven to the device on subsequent access. If the Mode bits (M7-0) equal “Ax” hex, then the next Fast Dual I/O command (after $\overline{CS}$ is raised and then lowered) does not require the command (BBh) code, as shown in Figure 21 and Figure 22. This reduces the command sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low.

If Mode bits (M7-0) are any value other “Ax” hex, the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation. A mode bit reset can be used to reset Mode bits (M7-0) before issuing normal commands. The bits of the lower nibble (M3-0) are don’t care (“X”). However, ensure the I/O pins are high-impedance before the falling edge of the first data out clock.

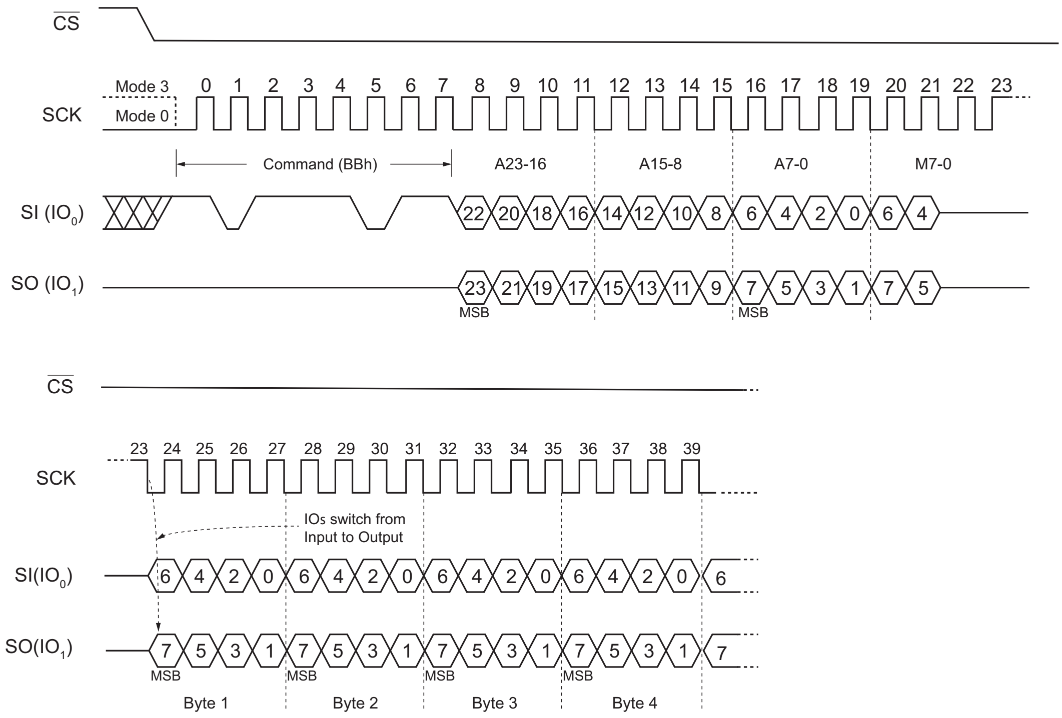


Figure 21. Fast Read Dual I/O Command (initial command or previous M7-0≠ Axh)

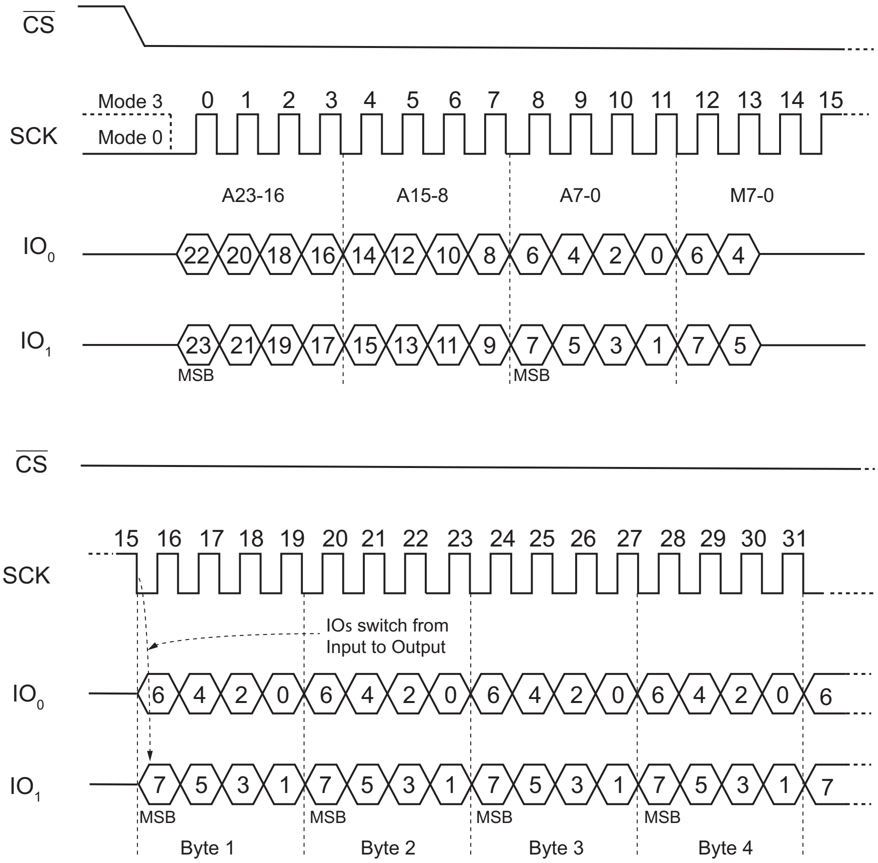


Figure 22. Fast Read Dual I/O Command (previous M7-0 = Axh)

8.14 Fast Read Quad I/O (EBh)

The Fast Read Quad I/O command reduces cycle overhead through quad access using four IO pins: IO_{0-3}. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Fast read Quad I/O Command.

8.14.1 Continuous Read Mode

The Fast Read Quad I/O command can further reduce command overhead through setting the Mode bits (M7-0) following the input Address bits (A23-0), as shown in Figure 23. The upper nibble of the Mode (M7-4) controls the length of the next Fast Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the Mode (M3-0) are don't care ("X"). However, ensure the I/O pins are high-impedance before the falling edge of the first data out clock. Note: the mode bits are counted as dummy clocks.

If the Mode bits (M7-0) equal Ax hex, then the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the EBh command code, as shown in Figure 24. This reduces the command sequence by eight clocks and allows the address to be immediately entered after $\overline{CS}$ is asserted low. If the Mode bits (M7-0) are any value other than "Ax" hex, the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus retuning normal operation. A mode bit reset can be used to reset Mode bits (M7-0) before issuing normal commands.

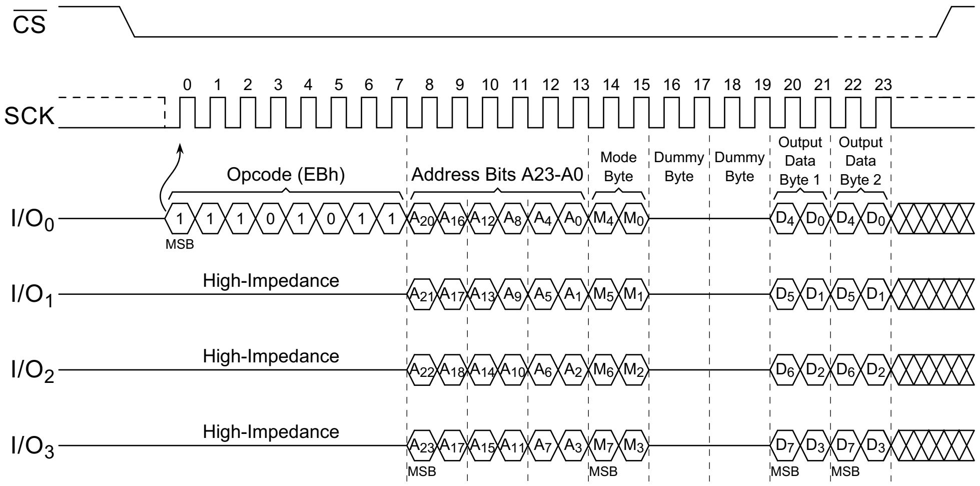


Figure 23. Fast Read Quad I/O Command (Initial command or previous M7-0 ≠ Axh, SPI mode)

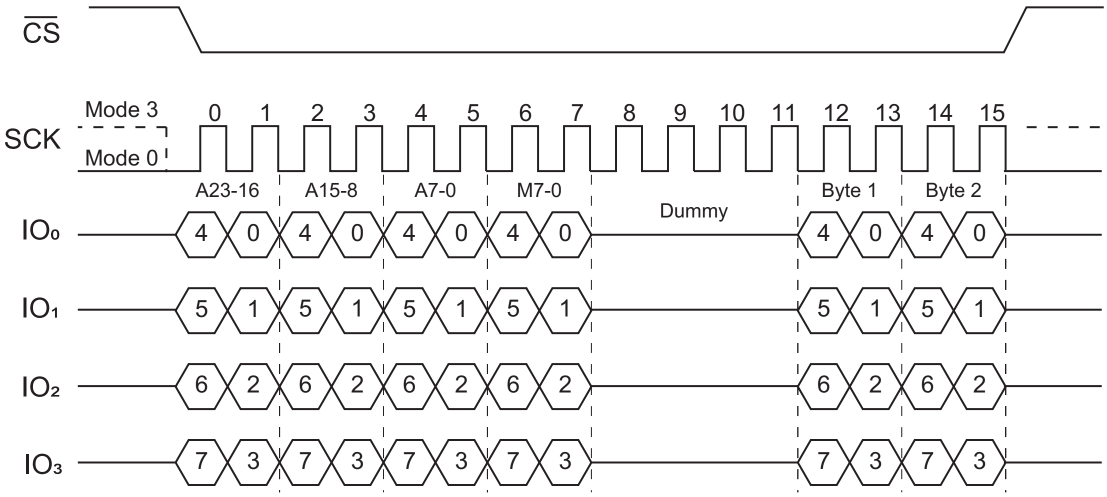


Figure 24. Fast Read Quad I/O Command (previous M7-0 = Axh, SPI mode)

8.14.2 Wrap Around in SPI mode

The Fast Read Quad I/O command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command prior to issuing the Fast Read Quad I/O (EBh) command. The Set Burst with Wrap (77h) command can either enable or disable the Wrap Around feature for the following Fast Read Quad I/O command.

When Wrap Around is enabled, the data being accessed can be limited to an 8/16/32/64-byte section of a 256-byte page. The output data starts at the initial address specified in the command. Once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing multiple read commands. (See Section 8.32, Set Burst with Wrap (77h)).

8.14.3 Fast Read Quad I/O in QPI Mode

When QPI mode in enabled, the number of dummy clocks is configured by the Set Read Parameters (C0h) command to accommodate a wide range applications with different needs for either maximum fast read frequency or minimum data access latency. The number of dummy clock cycles can be configured as either 4, 6, or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command, as shown in Table 12. The default number of dummy clocks upon power up or after a Reset (99h) command is four.

The Continuous Read Mode feature is also available in QPI mode for Fast Read Quad I/O command. In QPI mode, the Continuous Read Mode bits M7-M0 are also considered as dummy clocks.

The Wrap Around feature is not available in QPI mode for Fast Read Quad I/O command. To perform a read operation with fixed data length wrap around in QPI mode, a Burst Read with Wrap (0Ch) command must be used. See Section 8.33, Burst Read with Wrap (0Ch).

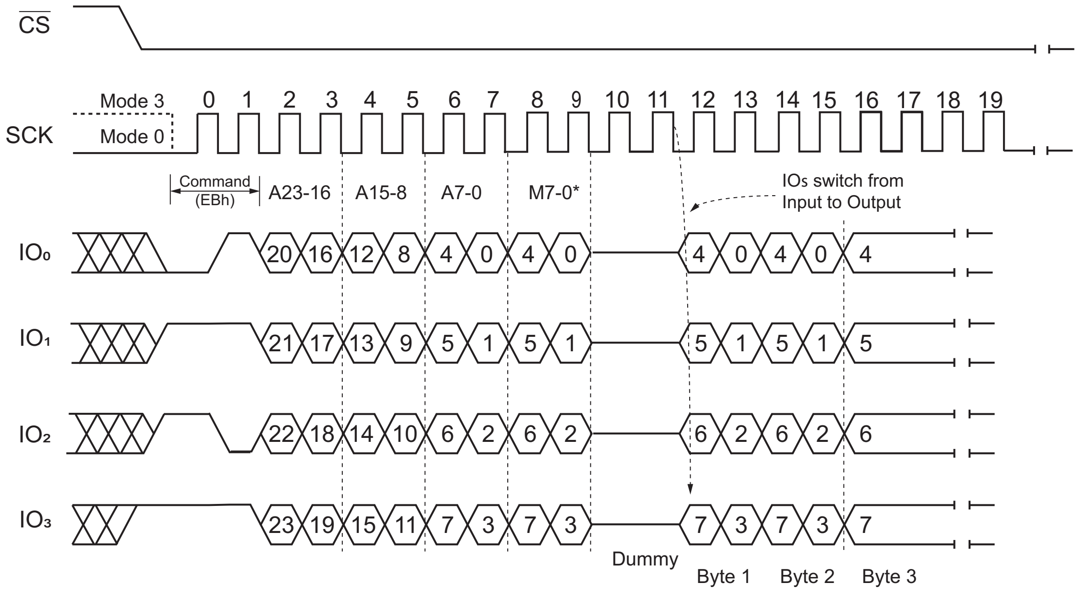


Figure 25. Fast Read Quad I/O Command (Initial command or previous M7-0 ≠ Axh, QPI mode)

8.15 Page Program (02h)

The Page Program command is used for programming the memory to “0”. A Write Enable command (06h) must be issued before the device accept the Page Program Command (Status Register bit WEL = 1). After the Write Enable (WREN) command has been decoded, the device sets the Write Enable Latch (WEL) bit in the Status Register. The command is entered by driving the $\overline{\text{CS}}$ pin low and then sending the command code 02h followed by a 24-bits address (A23-A0) and at least one data byte on the SI pin. The $\overline{\text{CS}}$ pin must be driven low for the entire time of the command while data is being sent to the device. The $\overline{\text{CS}}$ pin must be driven low for the entire time of the command while data is being sent to the device. See Figure 26 and Figure 27.

If an entire 256 byte page is to be programmed, set the last address byte (the 8 least significant address bits) to 0. If the last address byte is not zero, and the number of clocks exceeds the remaining page length, the addressing wraps to the beginning of the page. In some cases, less than 256 bytes (a partial page) can be programmed without having any effect on other bytes within the same page. One condition to perform a partial page program is that the number of clocks cannot exceed the remaining page length. If more than 256 bytes are sent to the device the addressing wraps to the beginning of the page and overwrite previously sent data.

The $\overline{\text{CS}}$ pin must be driven high after the eighth bit of the last byte has been latched. If this is not done the Page Program command is not executed. After $\overline{\text{CS}}$ is driven high, the self-timed Page Program command commences for a time duration of t_{PP} (see Section 9.6, AC Electrical Characteristics). While the Page Program cycle is in progress, the Read Status Register command may still be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Page Program cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

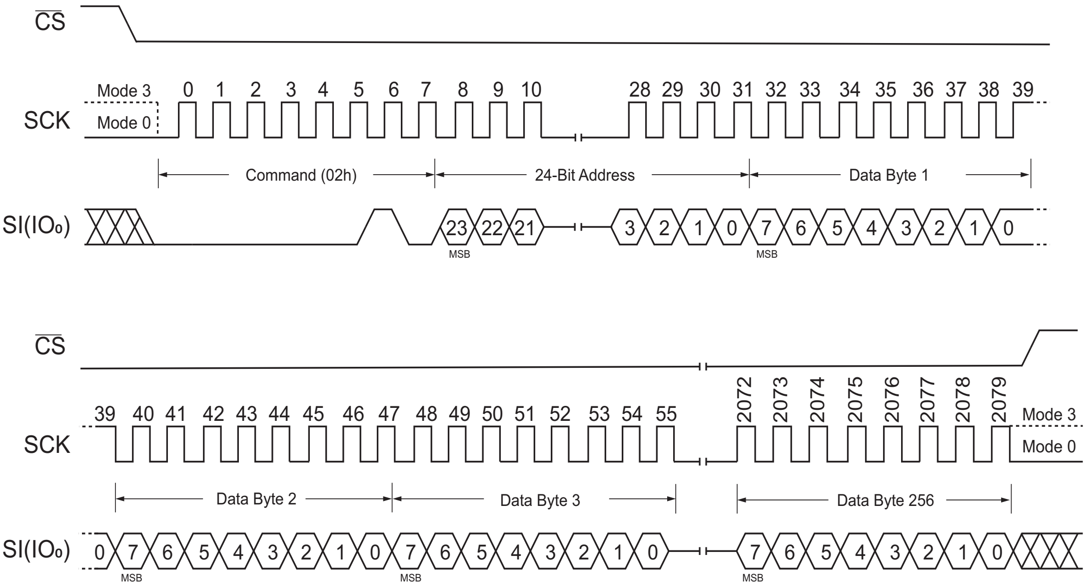


Figure 26. Page Program Command (SPI Mode)

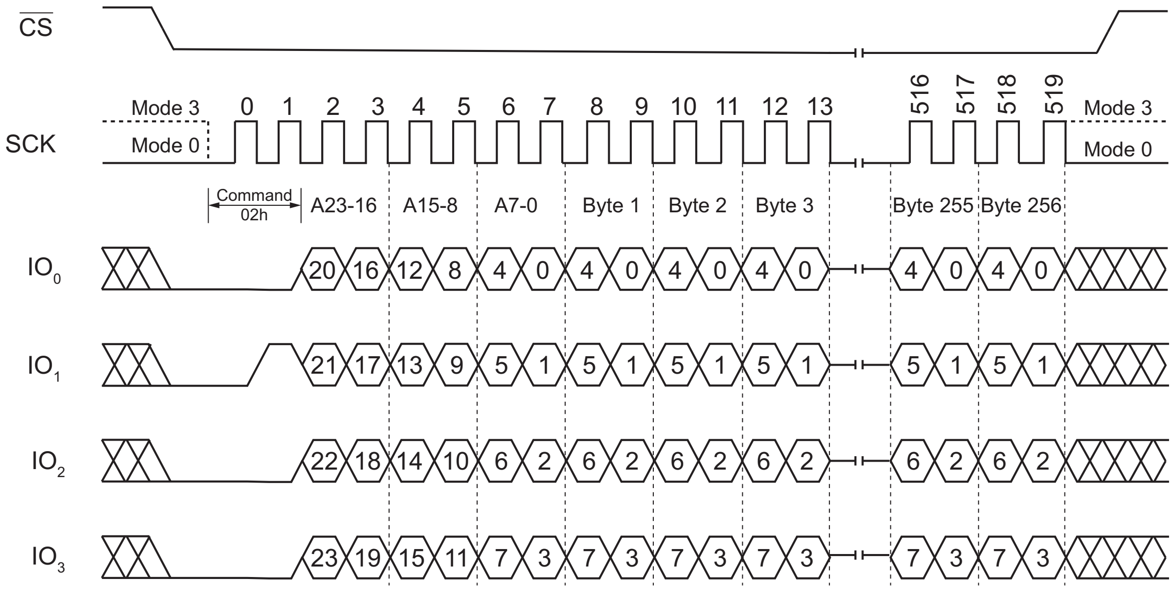


Figure 27. Page Program Command (QPI Mode)

8.16 Quad Page Program (33h)

The Quad Page Program command is used to program the memory to “0” at previously erased memory areas. The Quad Page Program uses four pins to transfer address and data: IO_0, IO_1, IO_2, and IO_3**.** This improves performance and data throughput of lower clock frequencies of less than 5 MHz. Systems using a faster clock speed do not get more benefit for the Quad Page Program as the required internal page program time is far more than the time required to clock data in.

To use Quad Page Program, the Quad Enable bit must be set, A Write Enable (06h) command must be executed before the device can accept the Quad Page Program command (Status Register-1, WEL = 1). The command is initiated by driving the $\overline{\text{CS}}$ pin low, then sending the command code 33h followed by a 24-bit address (A23 - A0) and at least one data, into the I/O pins. The $\overline{\text{CS}}$ pin must be held low for the entire length of the command while data is being sent to the device. All other functions of Quad Page Program are the same as the standard Page Program. See Figure 28 and Figure 29.

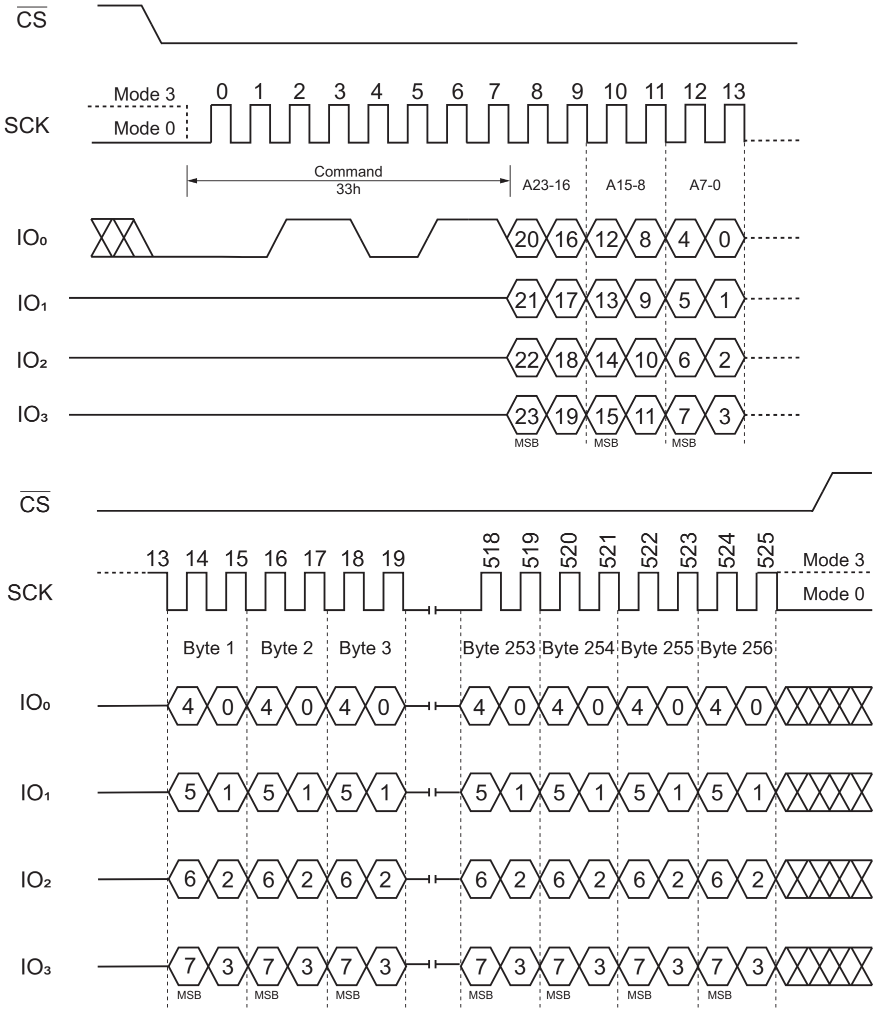


Figure 28. Quad Page Program Command (SPI mode)

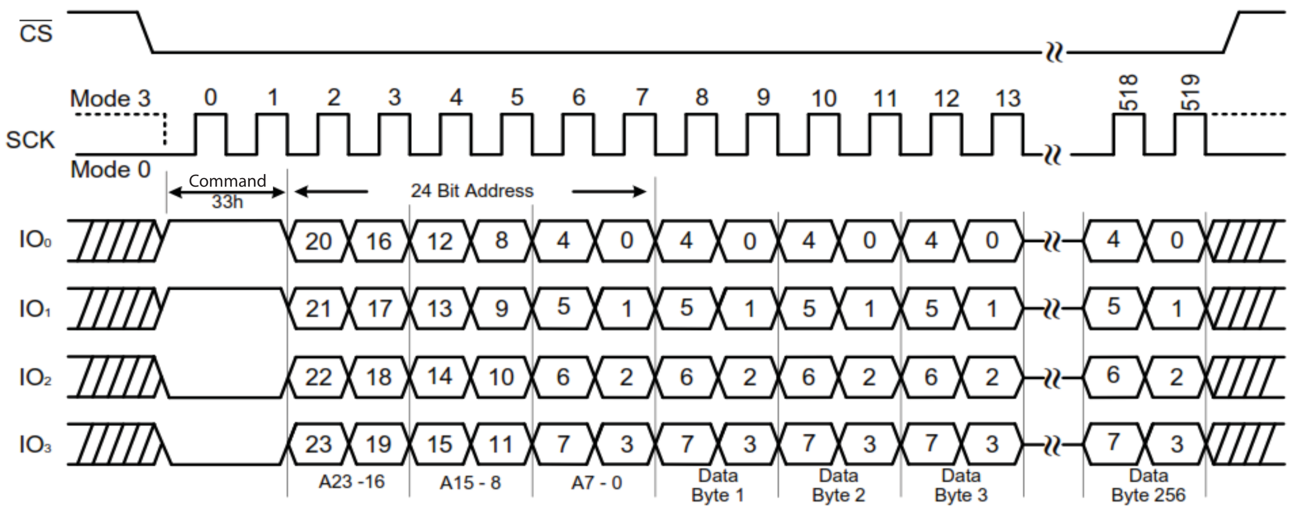


Figure 29. Quad Page Program Command (QPI mode)

8.17 4-kByte Block Erase (20h)

The Block Erase command is used to erase the data of the selected block by setting the memory locations to "1". The command is used to erase a 4-kB block. Prior to the Block Erase Command, the Write Enable command must be issued. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 20h followed by a 24-bit block address (A23 - A0). (See Figure 30 and Figure 31.)

The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in; otherwise, the Block Erase command is not executed. After $\overline{CS}$ goes high, the self-timed Block Erase command commences for a time duration of t_{SE} (see Section 9.6, AC Electrical Characteristics).

While the Block Erase cycle is in progress, the Read Status Register command can be accessed for checking the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

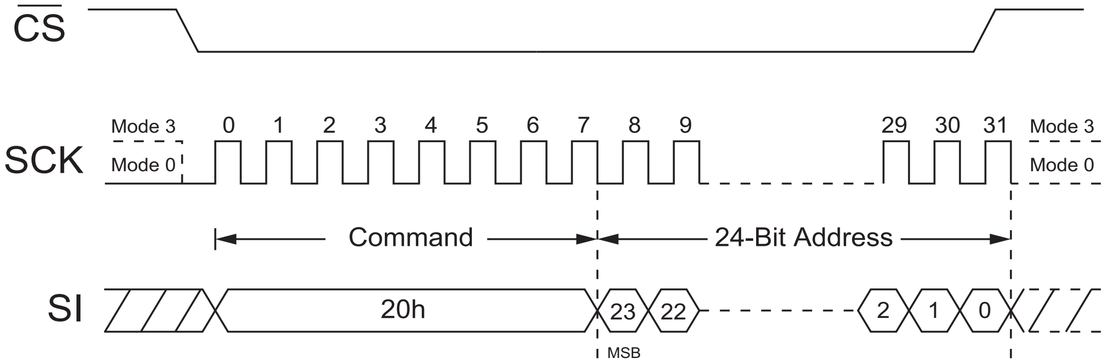


Figure 30. 4-kByte Block Erase Command (SPI Mode)

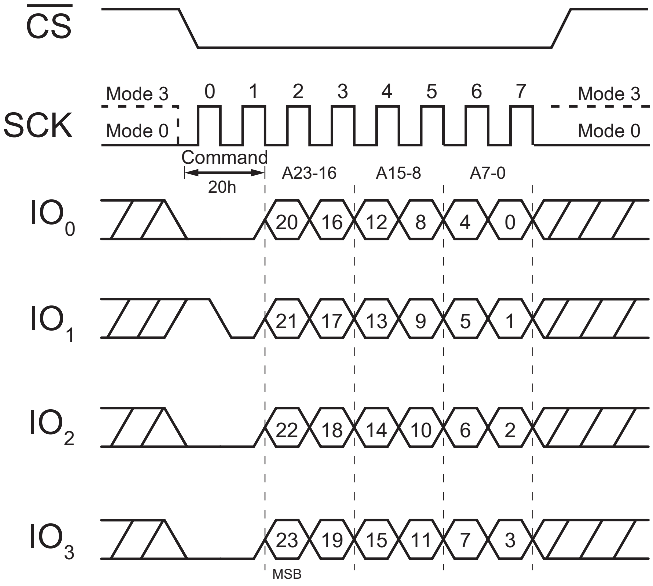


Figure 31. 4-kByte Block Erase Command (QPI Mode)

8.18 32-kByte Block Erase (52h)

The Block Erase command is used to erase the data of the selected block by setting the memory locations to “1”. The command is used for a 32-kB block erase operation. Prior to the Block Erase Command, a Write Enable command must be issued. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 52h followed by a 24-bit block address (A23 - A0). See Figure 32 and Figure 33.

The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in; otherwise, the Block Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Block Erase command commences for a time duration of t_{BE1}. See Section 9.6, AC Electrical Characteristics.

While the Block Erase cycle is in progress, the Read Status Register command may still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

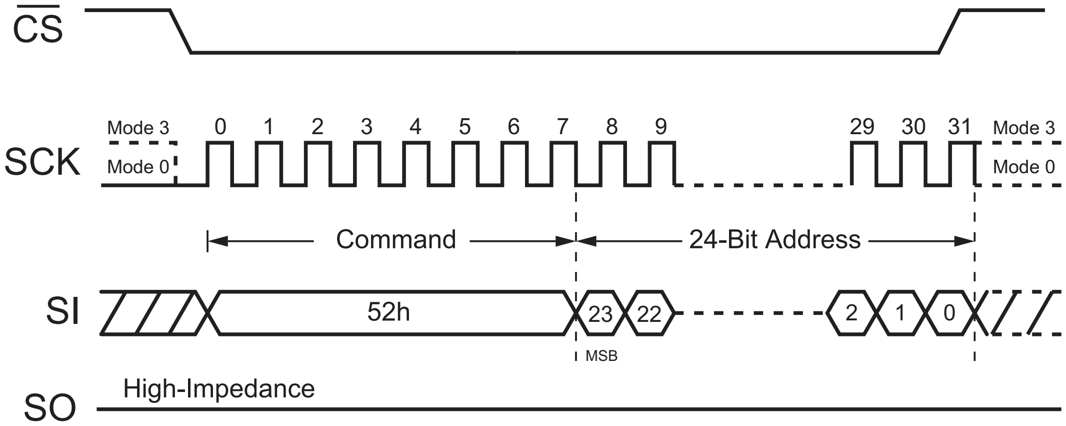


Figure 32. 32-kByte Block Erase Command (SPI Mode)

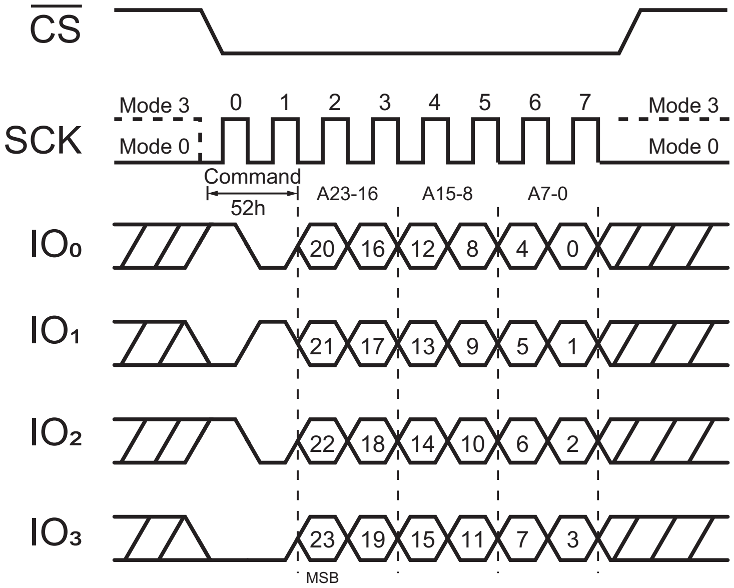


Figure 33. 32-kByte Block Erase Command (QPI Mode)

8.19 64-kByte Block Erase (D8h)

The Block Erase command is used to erase the data of a selected block by setting the memory locations of that block to “1”. The command is used for 64-kB block erase operation. Prior to the Block Erase Command, a Write Enable command must be issued. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code D8h followed by a 24-bit block address (A23 - A0). See Figure 34 and Figure 35.

The $\overline{CS}$ pin must go high after the eighth bit of the last byte has been latched in; otherwise, the Block Erase command is not executed. After $\overline{CS}$ is driven high, the self-timed Block Erase command commences for a time duration of t_{BE2}. See Section 9.6, AC Electrical Characteristics.

While the Block Erase cycle is in progress, the Read Status Register command may still be read the status of the BUSY bit. The BUSY bit is a 1 during the Block Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

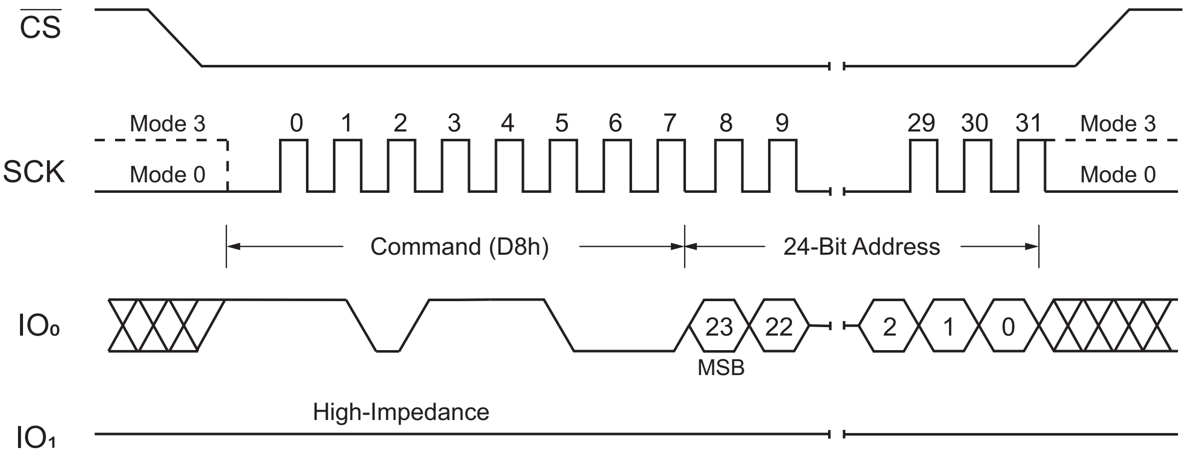


Figure 34. 64-kByte Block Erase Command (SPI Mode)

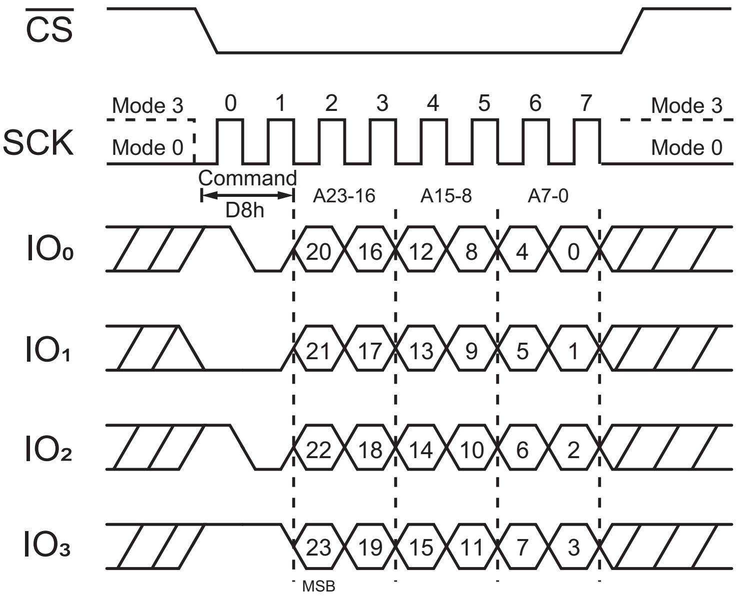


Figure 35. 64-kByte Block Erase Command (QPI Mode)

8.20 Chip Erase (C7h / 60h)

The Chip Erase command clears all bits in the device to FFh (all 1s). Prior to the Chip Erase Command, a Write Enable command must be issued. The command is initiated by driving the $\overline{\text{CS}}$ pin low and shifting the command code C7h or 60h. See Figure 36.

The $\overline{\text{CS}}$ pin must go high after the eighth bit of the last byte has been latched in; otherwise, the Chip Erase command is not executed. After $\overline{\text{CS}}$ is driven high, the self-timed Chip Erase command commences for a duration of t_{CE}. See Section 9.6, AC Electrical Characteristics.

While the Chip Erase cycle is in progress, the Read Status Register command may still be accessed to check the status of the BUSY bit. The BUSY bit is a 1 during the Chip Erase cycle and becomes a 0 when the cycle is finished and the device is ready to accept other commands. When the BUSY bit is asserted, the Write Enable Latch (WEL) bit in the Status Register is cleared to 0.

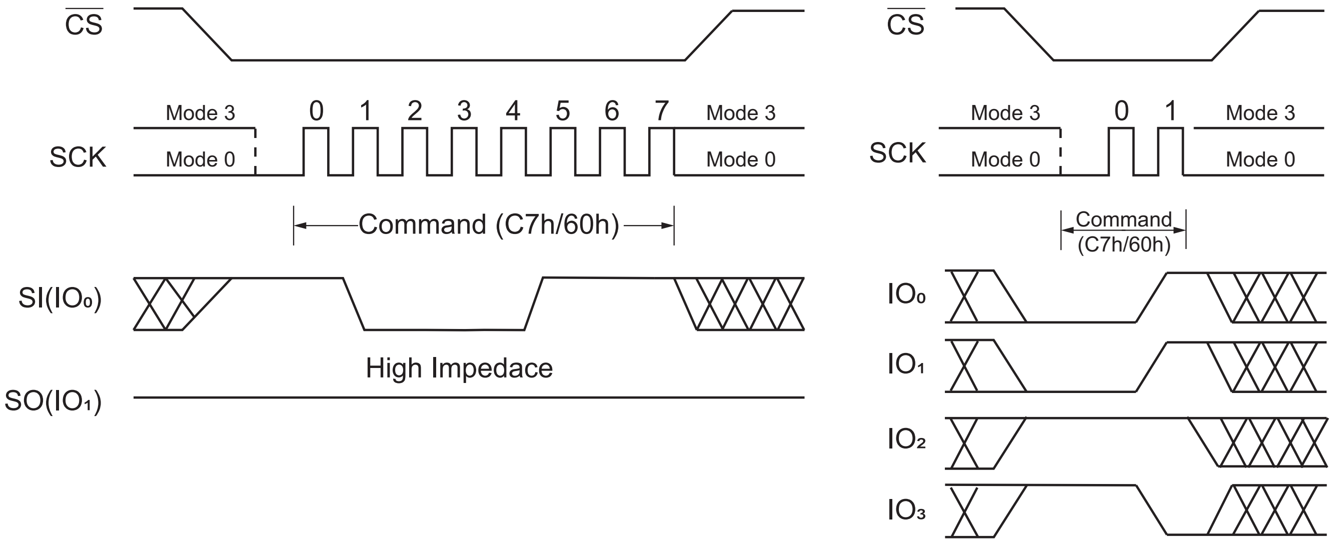


Figure 36. Chip Erase Command for SPI Mode (left) and QPI Mode (right)

8.21 Erase / Program Suspend (75h)

The Erase/Program Suspend command allows the system to interrupt a Block Erase, Block Erase operation, or a Page Program, Quad Data Input Page Program, Quad Page Program operation.

Erase Suspend is valid only during a Block Erase operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) command and Erase commands (20h, 52h, D8h, C7h, 60h) are not allowed during an Erase Suspend. During the Chip Erase operation, the Erase Suspend command is ignored.

Program Suspend is valid only during the Page Program, Quad Data Input Page Program, or Quad Page Program operation. The Write Status Register-1 (01h), Write Status Register-2 (31h) command, Program commands (02h and 33h) and Erase Commands (20h, 52h, D8h, C7h, 60h) are not allowed during Program Suspend.

The Erase/Program Suspend command 75h is accepted by the device only if the SUS bit in the Status Register equals to 0 and the BUSY bit equals to 1 while a Block Erase or a Page Program operation is on-going. If the SUS bit equals 1 or the BUSY bit equals 0, the Suspend command is ignored by the device. A maximum of time of t_{SUS} (see Section 9.6, AC Electrical Characteristics) is required to suspend the erase or program operation.

After executing the Erase/Program Suspend, the SUS bit in the Status Register is toggled from 0 to 1 immediately. The BUSY bit in the Status Register is cleared from 1 to 0 within t_{SUS}. For a previously resumed Erase/Program operation, it is also required that the Suspend command 75h is not issued earlier than a minimum of time of t_{SUS} following the preceding Resume command 7Ah.

Unexpected power-off during the Erase/Program suspend state resets the device and releases the suspend state. The SUS bit in the Status Register is also reset to 0. The data within the page or block that was being suspended can become corrupted. It is recommended to implement system design techniques to guard against the accidental power interruption and preserve data integrity during the erase/program suspend state. (See Figure 37 and Figure 38).

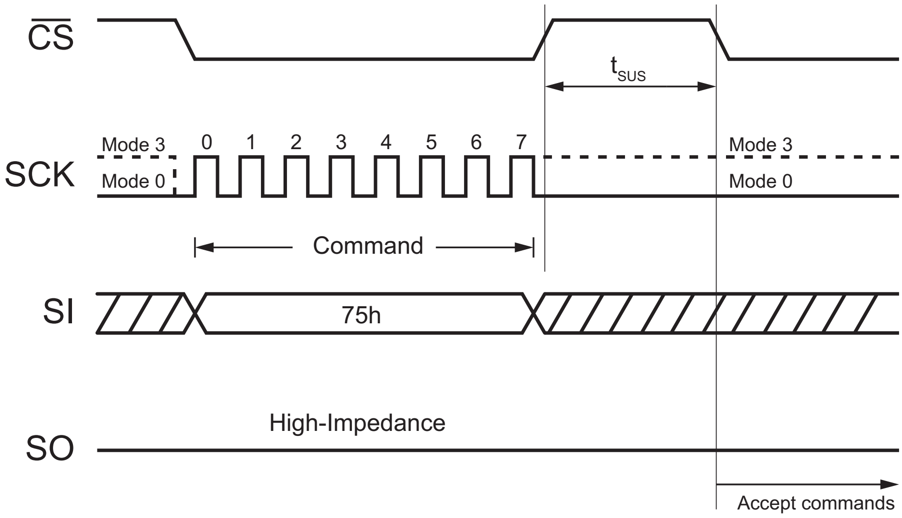


Figure 37. Erase Suspend Command (SPI Mode)

Note:

A read operation from a physical block that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.

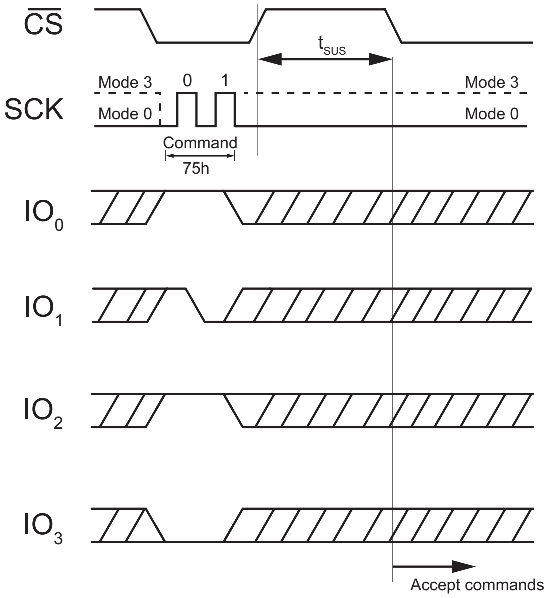


Figure 38. Erase Suspend Command (QPI Mode)

Note:

A read operation from an 8-Mbit area (referred to as a physical block) that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.

8.22 Erase / Program Resume (7Ah)

The Erase/Program Resume command 7Ah is used to restart the Block Erase operation or the Page Program operation after an Erase/Program Suspend (75h). The Resume command 7Ah is accepted by the device only if the SUS bit in the Status Register is set and the BUSY bit is cleared. After the 7Ah command is issued, hardware clears the SUS bit immediately and sets the BUSY bit within 200ns. The block completes the erase operation or the page completes the program operation. If either the SUS bit is cleared or the BUSY bit is set, the Resume command 7Ah is ignored by the device.

The Resume command cannot be accepted if the previous Erase/Program Suspend operation was interrupted by unexpected power-off. It is also required that a subsequent Erase/Program Suspend command not to be issued within a minimum of time of t_{SUS} following a previous Resume command. (See Figure 39 and Figure 40).

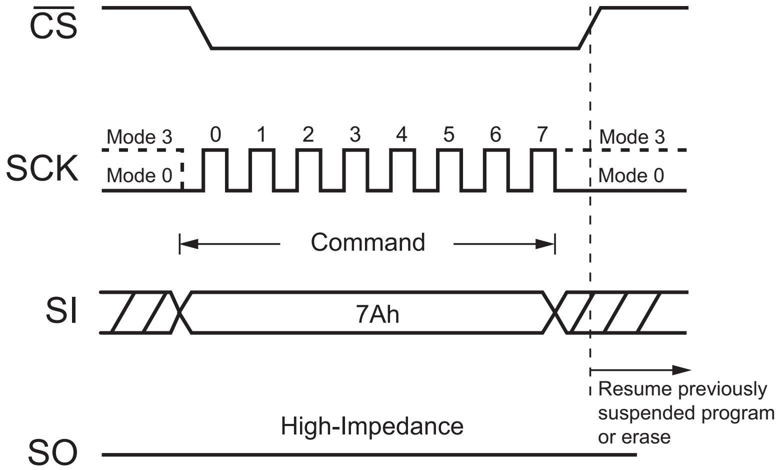


Figure 39. Erase / Program Resume Command (SPI Mode)

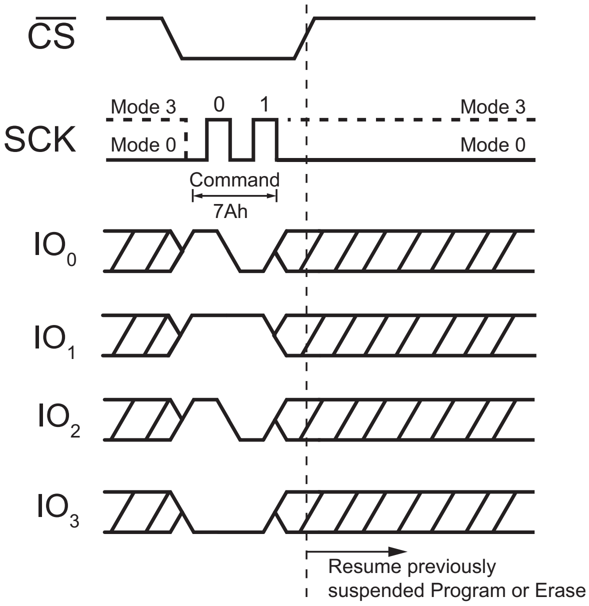


Figure 40. Erase / Program Resume Command (QPI Mode)

Note:

A read operation from an 8-Mbit area (referred to as a physical block) that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.

8.23 Deep Power-Down (B9h)

Executing the Deep Power-Down command is the best way to put the device in the lowest power consumption. The Deep Power-Down command reduces the standby current (from I_{CC1} to I_{CC2} as specified in AC characteristics). The command is entered by driving the $\overline{CS}$ pin low following execution of the B9h command. (See Figure 41 and Figure 42).

The $\overline{CS}$ pin must go high exactly at the byte boundary (the latest eighth bit of command code been latched-in); otherwise, the Deep Power-Down command is not executed. After $\overline{CS}$ goes high, it requires a delay of t_{DP} and the Deep Power-Down mode is entered. While in the Deep Power-Down mode, the Release Deep Power-Down / Device ID command is used to restore the device to normal operation. All other commands are ignored, including the Read Status Register command, which is always available during normal operation.

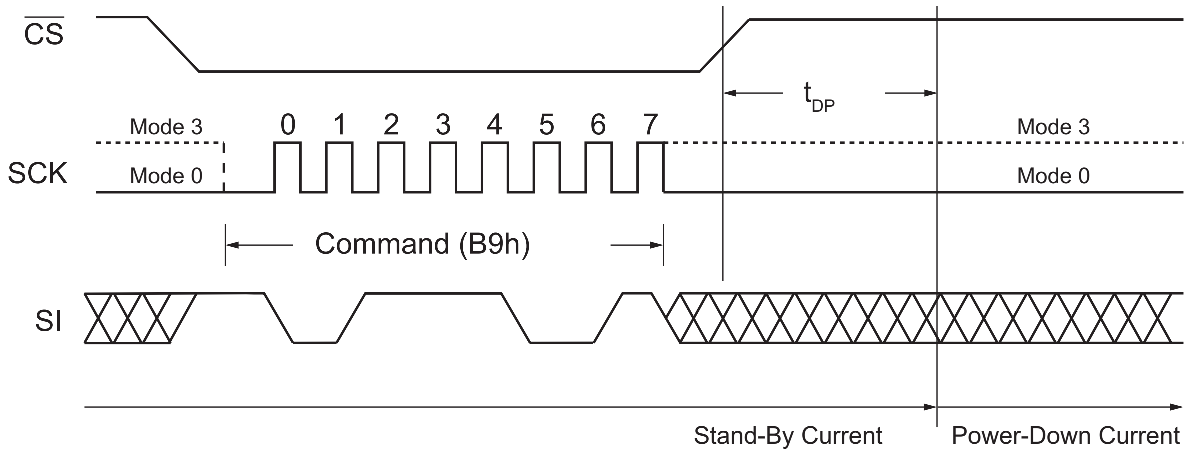


Figure 41. Deep Power-Down Command (SPI Mode)

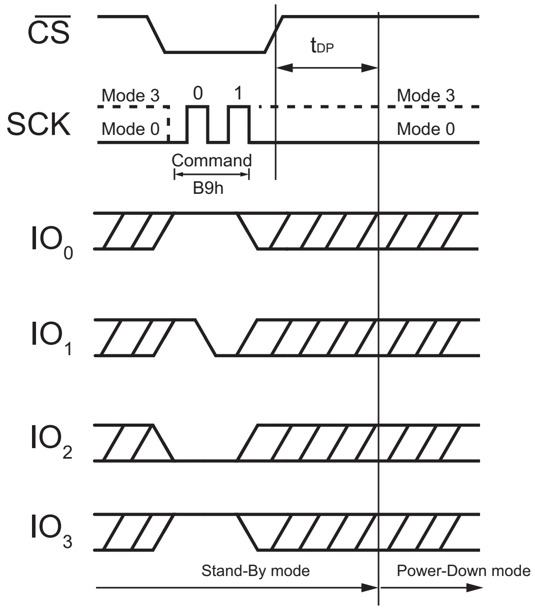


Figure 42. Deep Power-Down Command (QPI Mode)

8.24 Release Deep Power-Down / Device ID (ABh)

The Release Deep Power-Down / Device ID command is a multi-purpose command. It can be used to release the device from the Deep Power-Down state or obtain the device identification (ID).

The command is issued by driving the $\overline{\text{CS}}$ pin low and driving a value of ABh onto the bus, then driving $\overline{\text{CS}}$ high, as shown in Figure 43 and Figure 44. The Release from Deep Power-Down command requires the time duration of t_{RES1} (see Section 9.6, AC Electrical Characteristics) before accepting other commands. The $\overline{\text{CS}}$ pin must keep high during the t_{RES1} time duration.

The Device ID can be read during SPI mode only. In other words, the Device ID feature is not available in QPI mode for the Release Deep Power-Down/Device ID command. To obtain the Device ID in SPI mode, the command is initiated by driving the $\overline{\text{CS}}$ pin low and sending the command code ABh followed by 3-dummy bytes. The Device ID bits are then shifted on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 45. After $\overline{\text{CS}}$ is driven high it must keep high for a time duration of t_{RES2} (see Section 9.6, AC Electrical Characteristics). The Device ID can be read continuously. The command is completed by driving $\overline{\text{CS}}$ high.

If the Release from Deep Power-Down /Device ID command is issued while an Erase, Program, or Write cycle is in process (when BUSY equals 1), the command is ignored and does not have any effect on the current cycle.

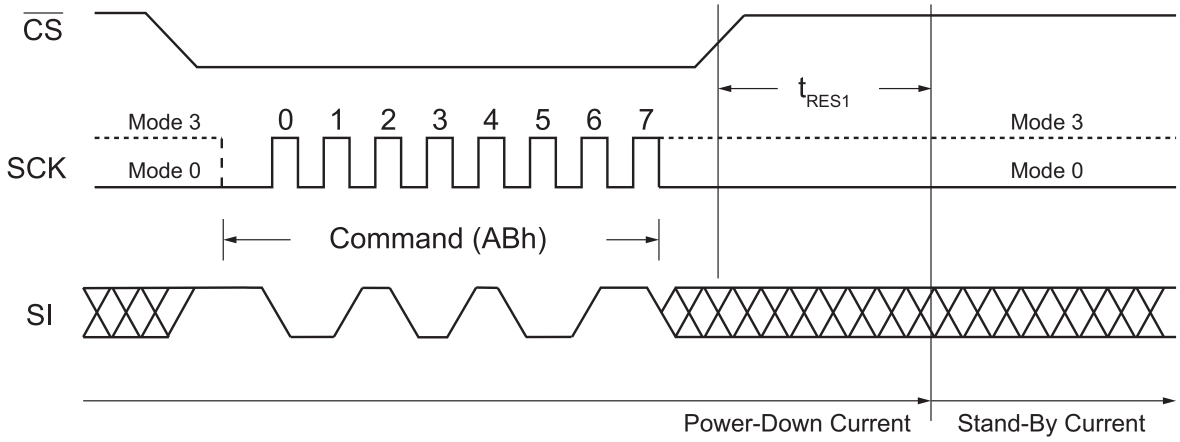


Figure 43. Release Power-Down Command (SPI Mode)

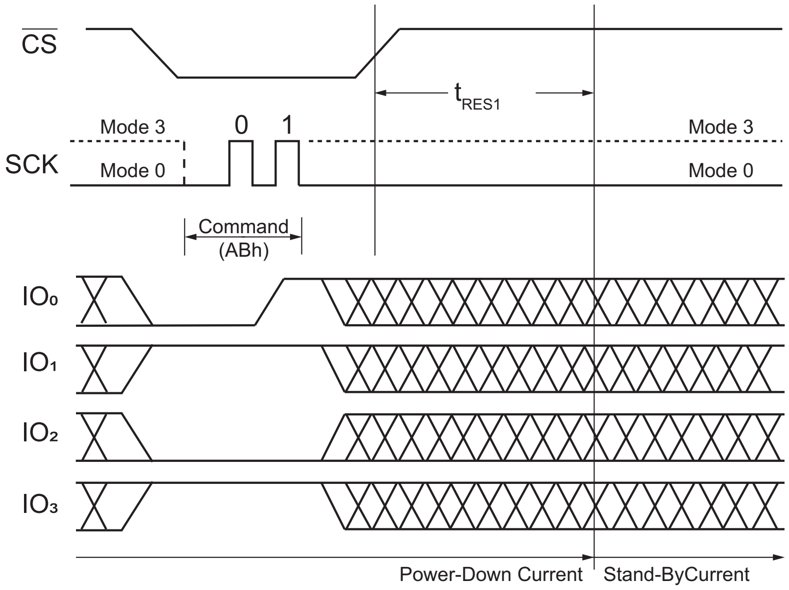


Figure 44. Release Power-Down Command (QPI Mode)

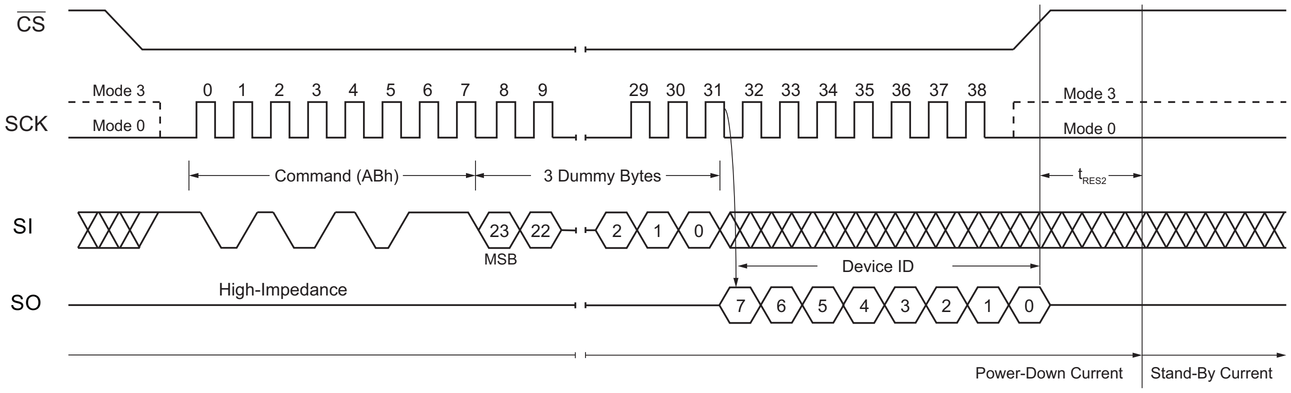


Figure 45. Release Power-Down / Device ID Command (SPI Mode)

8.25 Read Manufacturer / Device ID (90h)

The Read Manufacturer/ Device ID command provides both the JEDEC assigned manufacturer ID and the specific device ID. This command can be issued in both SPI mode and QPI mode. In SPI mode, the 90h command is called a 1-1-1 transfer, where the command, address, and data are all driven on a single pin (SI for command and address, and SO for data). In QPI mode, the 90h command is called a 4-4-4 transfer, where the command, address, and data are driven on the bidirectional IO_0 - IO_3 pins.

Note that in QPI mode, the following events must occur in the order shown.

1. Set the QE bit in Status Register-2
2. Execute the QPI Enable (38h) command
3. Execute the 90h command

In SPI mode, the operation is initiated by driving the $\overline{CS}$ pin low and then driving the command code 90h onto the SI pin, followed by a 24-bit address (A23-A0) of 000000h. The 90h command requires 8 clocks to transfer, and the 24-bit address requires 24 clocks to transfer. The Manufacturer ID for Renesas Electronics (1Fh) and the Device ID (17h) are shifted out on the SO pin on the falling edge of SCK with most significant bit (MSB) first. A minimum of 16 clocks are required to transfer the manufacturer and device ID information. If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

In QPI mode, the SI, SO, $\overline{WP}$, and $\overline{HOLD}$ pins are configured as bidirectional pins IO_0, IO_1, IO_2, and IO_3 respectively. The 90h operation the operation is initiated by driving the $\overline{CS}$ pin low and then driving the command code 90h onto the IO_0 - IO_3 pins, followed by a 24-bit address (A23-A0) of 000000h. The 90h command requires 2 clocks to transfer, and the 24-bit address requires 6 clocks to transfer. The Manufacturer ID for Renesas Electronics (1Fh) and the Device ID (17h) are shifted out on the bidirectional IO_0 - IO_3 pins on the falling edge of SCK, with most significant bit (MSB) first. A minimum or 4 clocks are required to transfer the manufacturer and device ID information. If the 24-bit address is initially set to 000001h the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

Figure 46 shows the 90h command as executed in SPI mode. In this mode the command and address are driven on the SI pin.

Figure 47 shows the 90h command as executed in QPI mode. In this mode the command and address are driven on all four I/O pins.

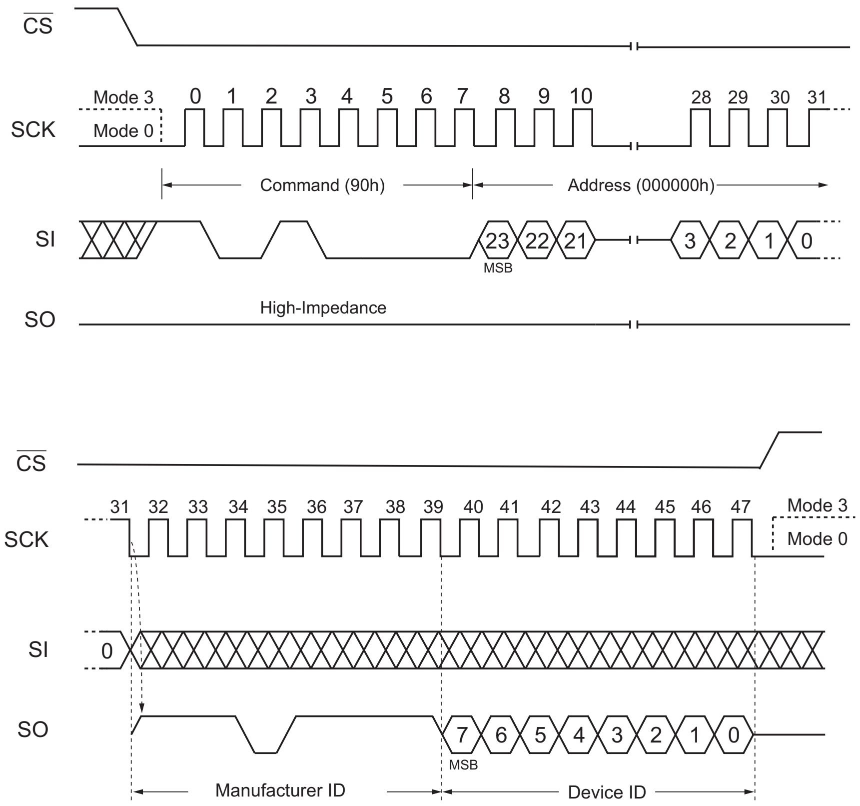


Figure 46. Read Manufacturer/ Device ID Command (SPI Mode)

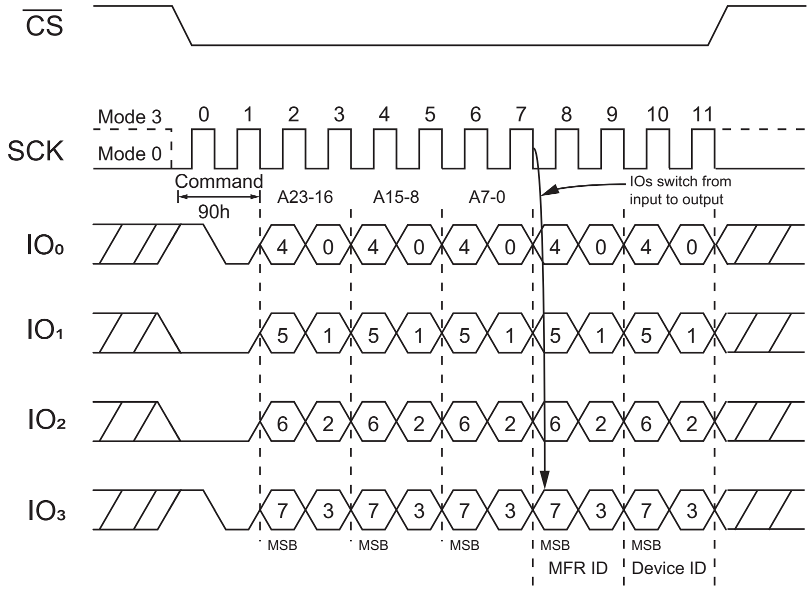


Figure 47. Read Manufacturer/ Device ID Command (QPI Mode)

8.26 Read Manufacturer / Device ID Dual I/O (92h)

The Read Manufacturer/ Device ID Dual I/O command provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID command is very similar to the Fast Read Dual I/O command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 92h followed by a 24-bit address (A23-A0) of 000000h. The Manufacturer ID for Renesas Electronics (1Fh) and the Device ID(17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 48. If the 24-bit address is initially set to 000001h, the Device ID is read first and then followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

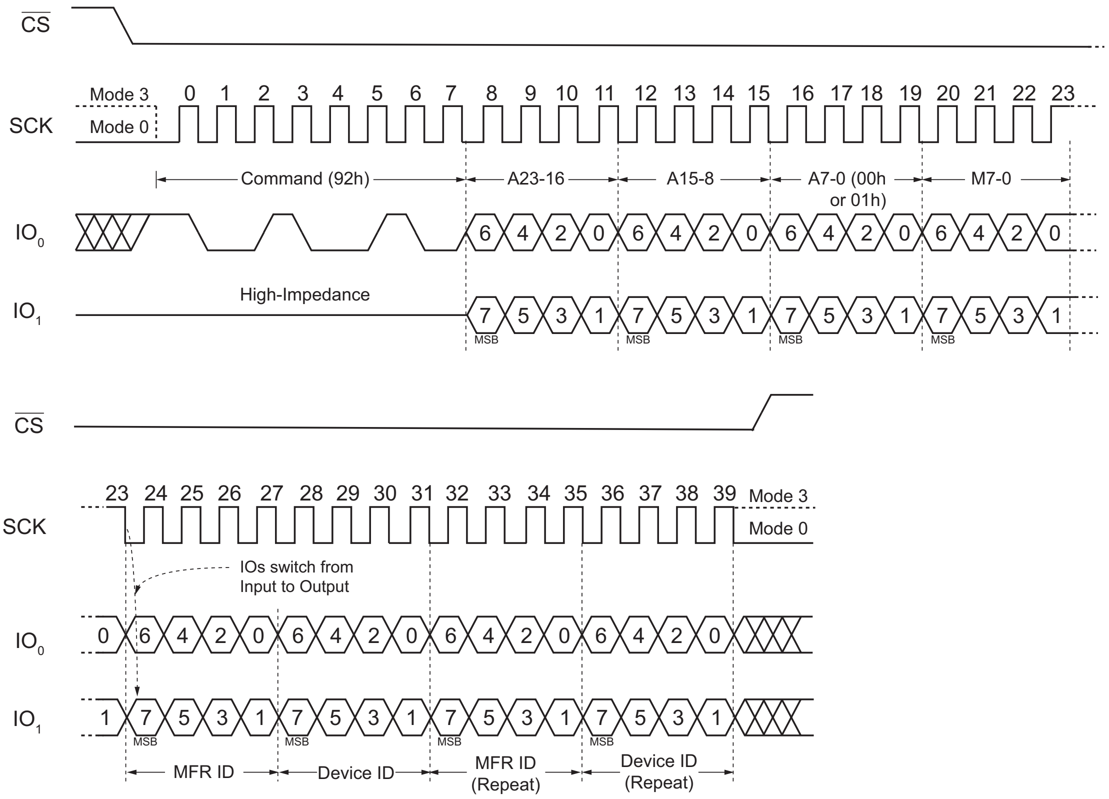


Figure 48. Read Dual Manufacturer/ Device ID Dual I/O Command (SPI Mode)

8.27 Read Manufacturer / Device ID Quad I/O (94h)

The Read Manufacturer/ Device ID Quad I/O command provides both the JEDEC assigned manufacturer ID and the specific device ID.

The Read Manufacturer/ Device ID Quad I/O command is very similar to the Fast Read Quad I/O command. The command is initiated by driving the $\overline{CS}$ pin low and shifting the command code 94h followed by a 24-bit address (A23-A0) of 000000h. The Manufacturer ID for Renesas Electronics (1Fh) and the Device ID (17h) are shifted out on the falling edge of SCK with most significant bit (MSB) first, as shown in Figure 49. If the 24-bit address is initially set to 000001h the Device ID is read first, followed by the Manufacturer ID. The Manufacturer and Device ID can be read continuously, alternating from one to the other. The command is completed by driving $\overline{CS}$ high.

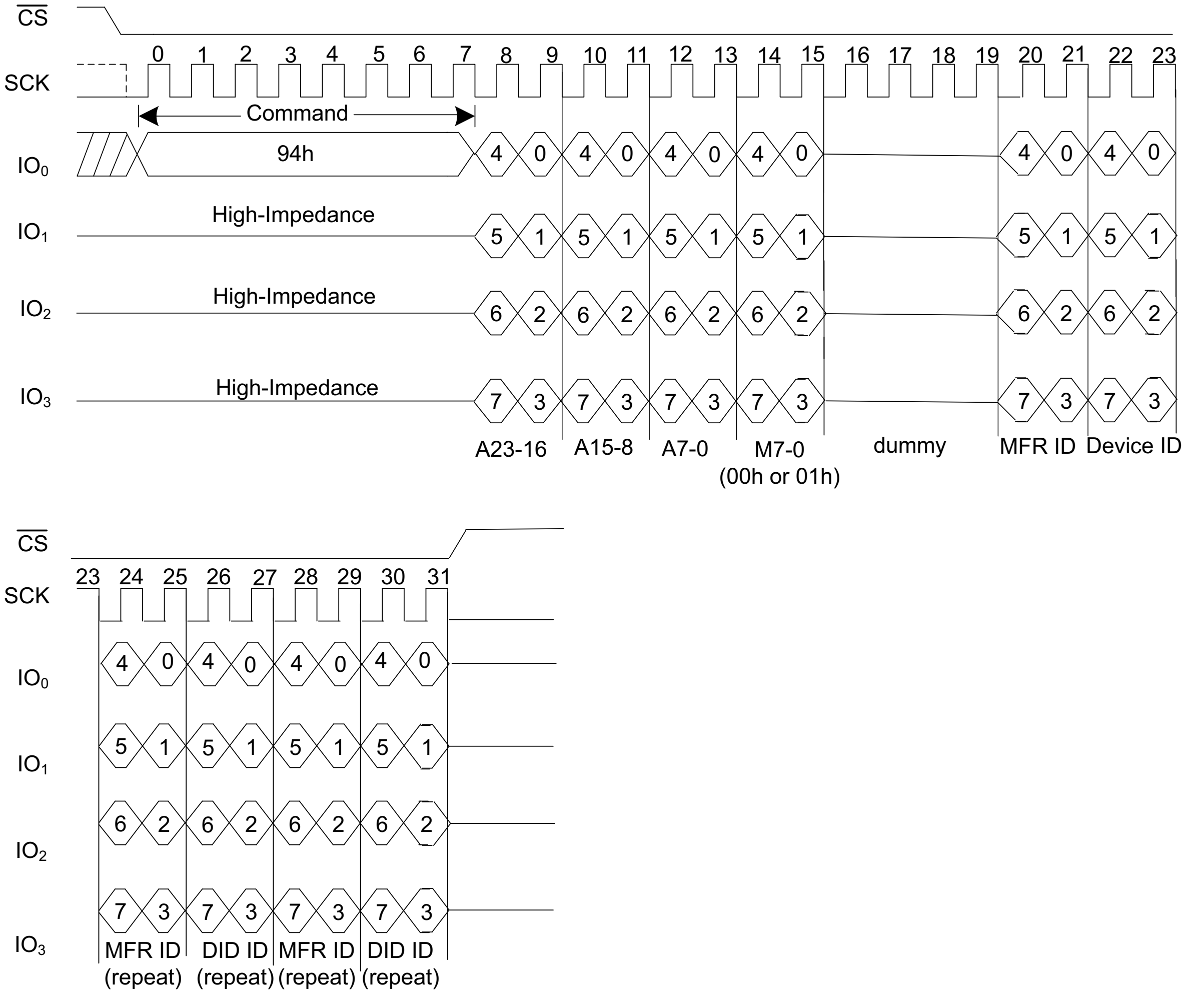


Figure 49. Read Quad Manufacturer/ Device ID Quad I/O Command (SPI Mode)

8.28 JEDEC ID (9Fh)

For compatibility, the AT25SL641 provides several commands to determine the identity of the device. The Read JEDEC ID command complies with the JEDEC standard for SPI compatible serial flash memories, which was adopted in 2003.

The command is entered by driving the $\overline{CS}$ pin low following the opcode 9Fh. The JEDEC-assigned Manufacturer ID byte for Renesas Electronics (1Fh) and two Device ID bytes, Memory Type (ID15-ID8) and Capacity (ID7-ID0), are then shifted out on the falling edge of SCK, with the most significant bit (MSB) first, as shown in Figure 50 and Figure 51. For memory type and capacity values, see Table 7. The JEDEC ID can be read continuously. The command is terminated by driving $\overline{CS}$ high.

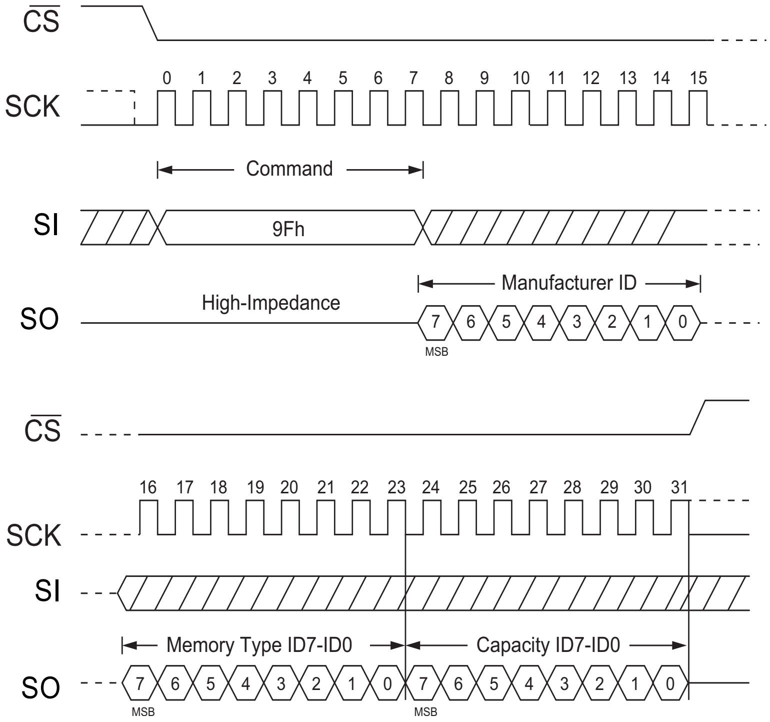


Figure 50. Read JEDEC ID Command (SPI Mode)

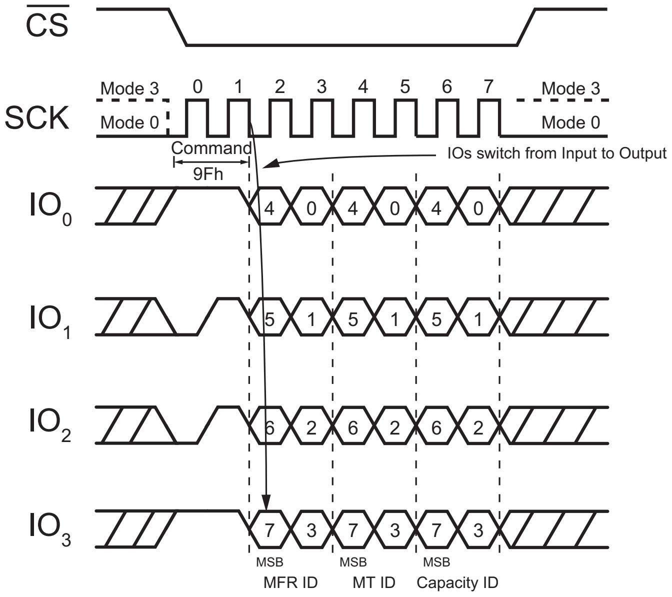


Figure 51. Read JEDEC ID Command (QPI Mode)

8.29 Enable QPI (38h)

The AT25SL641 supports both the Standard/Dual/Quad Serial Peripheral interface (SPI) and Quad Peripheral Interface (QPI). However, SPI mode and QPI mode cannot be used at the same time. The Enable QPI command is used to switch the device from SPI mode to QPI mode.

To switch the device to QPI mode, the Quad Enable (QE) bit in Status Register 2 must be set, followed by an Enable QPI command. If the Quad Enable (QE) bit is 0, the Enable QPI command is ignored and the device remains in SPI mode.

After power-up, the default state of the device is SPI mode. See the command Set Table 8 for all the commands supported in SPI mode and the command Set Table 11 for all the commands supported in QPI mode.

When the device is switched from SPI mode to QPI mode, the existing Write Enable and Program/Erase Suspend status, and the Wrap Length setting remains unchanged.

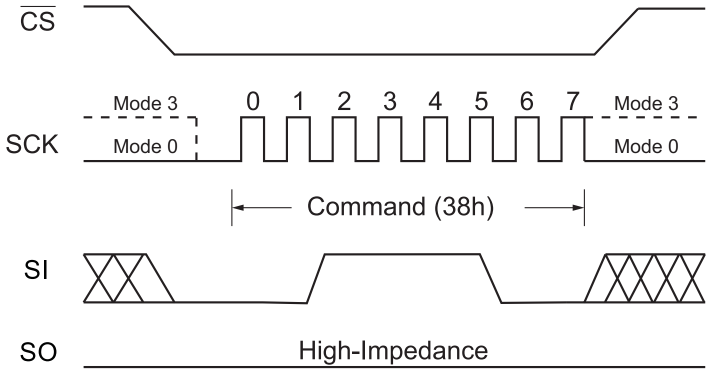


Figure 52. Enable QPI Command (SPI Mode only)

8.30 Disable QPI (FFh)

By issuing a Disable QPI (FFh) command, the device is reset back to SPI mode. When the device is switched from QPI mode to SPI mode, the existing Write Enable Latch (WEL) and Program/Erase Suspend status, and the Wrap Length settings remains unchanged.

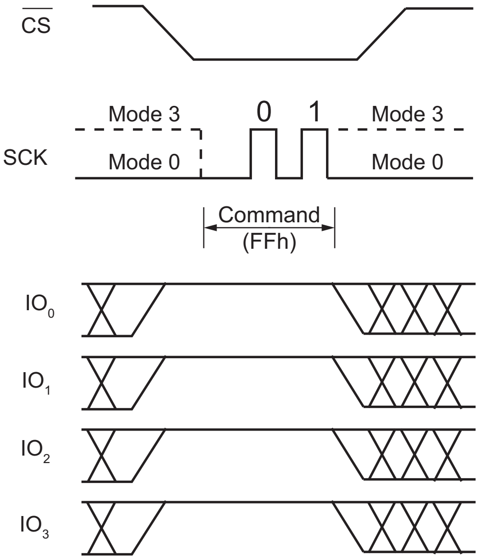


Figure 53. Disable QPI Command for QPI Mode

8.31 Word Read Quad I/O (E7h)

The Quad I/O significantly reduces command overhead, allowing faster random access for code execution (XiP) directly from the Quad SPI. The Quad Enable bit (QE) of Status Register-2 must be set to enable the Word Read Quad I/O command. The lowest Address bit (A0) must equal 0 and only two dummy clocks are required prior to the data output.

8.31.1 Continuous Read Mode

The Word Read Quad I/O command can further reduce command overhead through setting the Continuous Read Mode bits (M7-0) after the input Address bits (A23-0), as shown in Figure 54. The upper nibble of the (M7-4) controls the length of the next Word Read Quad I/O command through the inclusion or exclusion of the first byte command code. The lower nibble bits of the (M[3:0]) are don't care ("X"). However, ensure the I/O pins are high-impedance before the falling edge of the first data out clock.

If the "Continuous Read Mode" bits M[7-4] = Ah, then the next Fast Read Quad I/O command (after $\overline{CS}$ is raised and then lowered) does not require the E7h command code, as shown in Figure 55. This reduces the command sequence by eight clocks and allows the Read address to be immediately entered after $\overline{CS}$ is asserted low. If the Continuous Read Mode bits M[7:4] do not equal to Ah (1,0,1,0) the next command (after $\overline{CS}$ is raised and then lowered) requires the first byte command code, thus returning to normal operation.

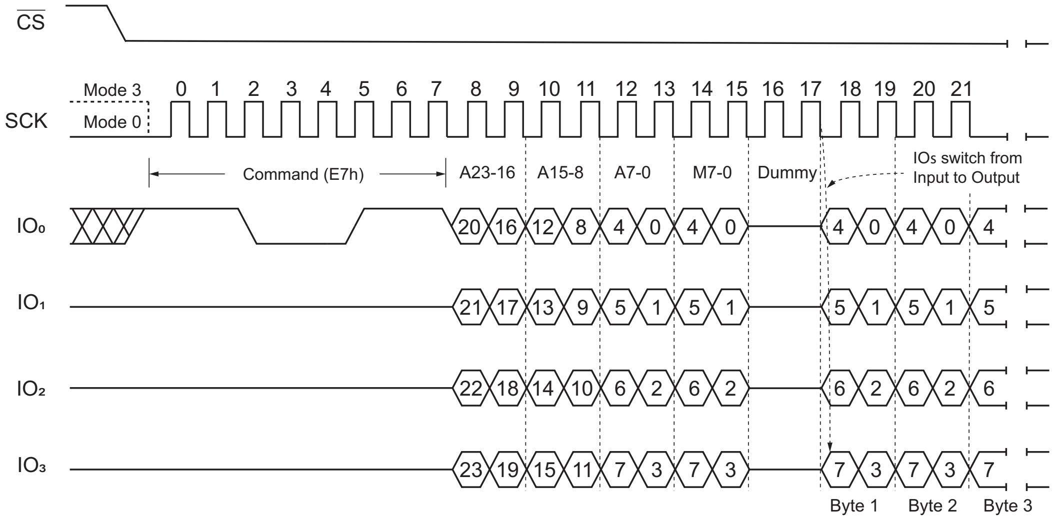


Figure 54. Word Read Quad I/O Command (Initial command or previous set M7-0 ≠ Axh, SPI Mode)

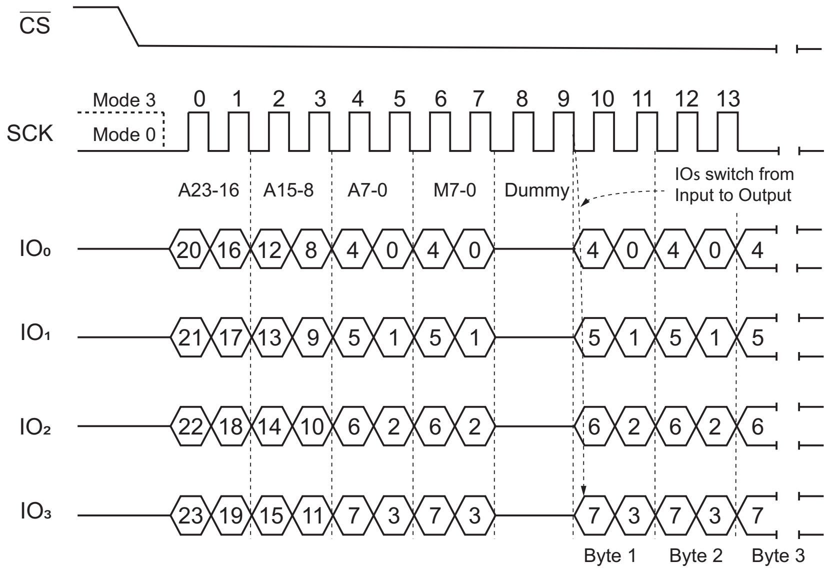


Figure 55. Word Read Quad I/O Command (Previous command set M7-0 = Axh, SPI Mode)

8.31.2 Wrap Around in SPI mode

The Word Read Quad I/O command can also be used to access a specific portion within a page by issuing a Set Burst with Wrap (77h) command prior to E7h. The Set Burst with Wrap command can either enable or disable the Wrap Around feature for the following E7h commands. When Wrap Around is enabled, the output data starts at the initial address specified in the command, once it reaches the ending boundary of the 8/16/32/64-byte section, the output wraps around to the beginning boundary automatically until $\overline{CS}$ is pulled high to terminate the command.

The Burst with Wrap feature allows applications that use cache to quickly fetch a critical address and then fill the cache afterwards within a fixed length (8/16/32/64-byte) of data without issuing read commands.

The Set Burst with Wrap command allows three wrap bits, W6-4, to be set. The W4 bit is used to enable or disable the Wrap Around operation, while W6-5 is used to specify the length of the wrap around section within a page.

8.32 Set Burst with Wrap (77h)

The Set Burst with Wrap (77h) command is used in conjunction with Fast Read Quad I/O and Word Read Quad I/O commands to access a fixed length of 8/16/32/64-byte section within a 256-byte page. Certain applications can benefit from this feature and improve the overall system code execution performance. Before the device accepts the Set Burst with Wrap command, a Quad enable of Status Register-2 must be executed (Status Register bit QE must equal 1).

The Set Burst with Wrap command is initiated by driving the $\overline{CS}$ pin low and then shifting the command code 77h followed by 24 dummy bits and 8 wrap bits, W7 - W0. The command sequence is shown in Set Burst with Wrap Command Sequence. Wrap bit W7 and W3-0 are not used.

Table 14. Encoding of W6 - W4 Wrap Bits

W6, W5	W4 = 0		W4 = 1(Default)	
	Wrap Around	Wrap Length	Wrap Around	Wrap Length
0 0	Yes	8-byte	No	N/A
0 1	Yes	16-byte	No	N/A
1 0	Yes	32-byte	No	N/A
1 1	Yes	64-byte	No	N/A

Once W6-4 is set by a Set Burst with Wrap command, all the following Fast Read Quad I/O and Word Read Quad I/O commands use the W6-4 setting to access the 8/16/32/64-byte section within any page. To exit the Wrap Around function and return to normal read operation, issue another Set Burst with Wrap command to set W4 = 1. The default value of W4 upon power on is 1. In the case of a system Reset while W4 = 0, it is recommended that the controller issues a Set Burst with Wrap command or Reset (99h) command to reset W4 = 1 prior to any normal Read commands since the AT25SL641 does not have a hardware reset pin.

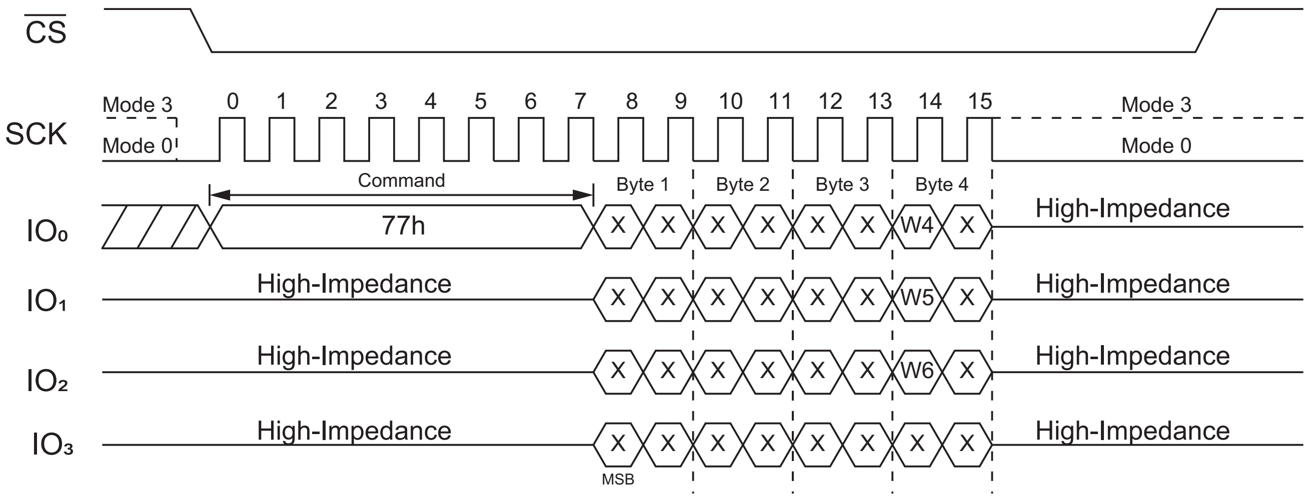


Figure 56. Set Burst with Wrap Command Sequence

8.33 Burst Read with Wrap (0Ch)

The Burst Read with Wrap (0Ch) command provides an alternative way to perform the read operation with Wrap Around in QPI mode. The command is similar to the Fast Read (0Bh) command in QPI mode, except the addressing of the read operation wraps around to the beginning boundary of the wrap length once the ending boundary is reached.

The number of dummy clock cycles can be configured as either 4, 6, or 8 by setting bits P[5:4] in the 8-bit parameter of the Set Read Parameters (C0h) command, as shown in Table 12.

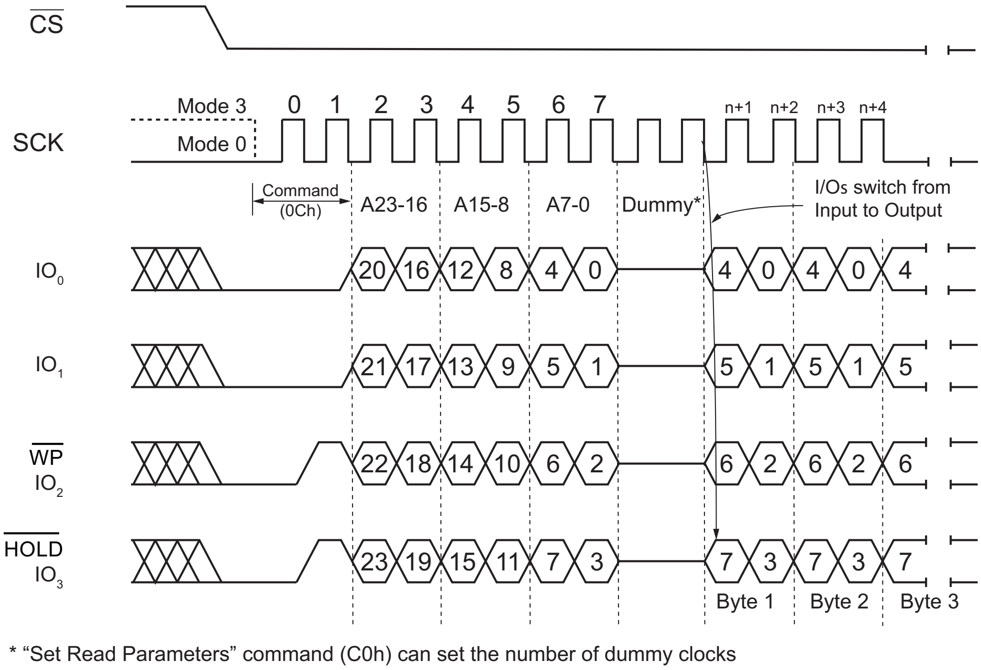


Figure 57. Burst Read with Wrap Command (QPI Mode)

8.34 Enable Reset (66h) and Reset (99h)

For eight-pin packages, the AT25SL641 provide a software Reset command (99h) instead of a dedicated RESET pin.

Once the Reset command is accepted, any on-going internal operations are terminated and the device returns to its default power-on state and loses all current volatile settings, such as Volatile Status Register bits, Write Enable Latch (WEL) status, Program/Erase Suspend status, Continuous Read Mode bit setting, Read parameter setting and Wrap bit setting.

The Enable Reset (66h) and Reset (99h) commands can be issued in either SPI mode or QPI mode. To avoid accidental reset, both commands must be issued in sequence. The execution of any command other than Reset (99h) after the Reset Enable (66h) command is executed disables the reset enable state. A new sequence of Enable Reset (66h) and Reset (99h) would then be required to reset the device. Once the Reset command is accepted by the device, it takes approximately $t_{RST} = 30\ \mu s$ to reset. During this period, no command is accepted.

Data corruption may happen if there is an on-going or suspended internal Erase or Program operation when Reset command sequence is accepted by device. It is recommended to check the BUSY bit and the SUS bit in Status Register before issuing the Reset command sequence.

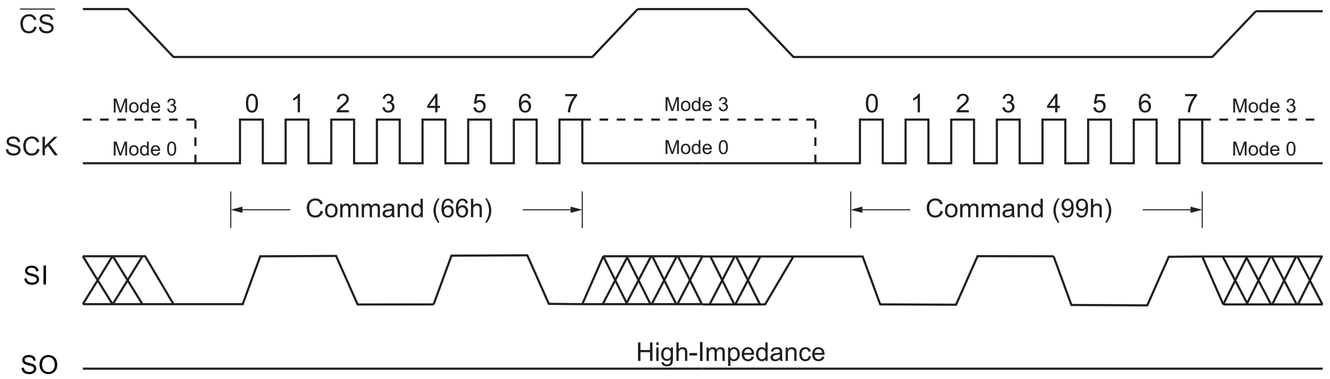


Figure 58. Enable Reset and Reset Command (SPI Mode)

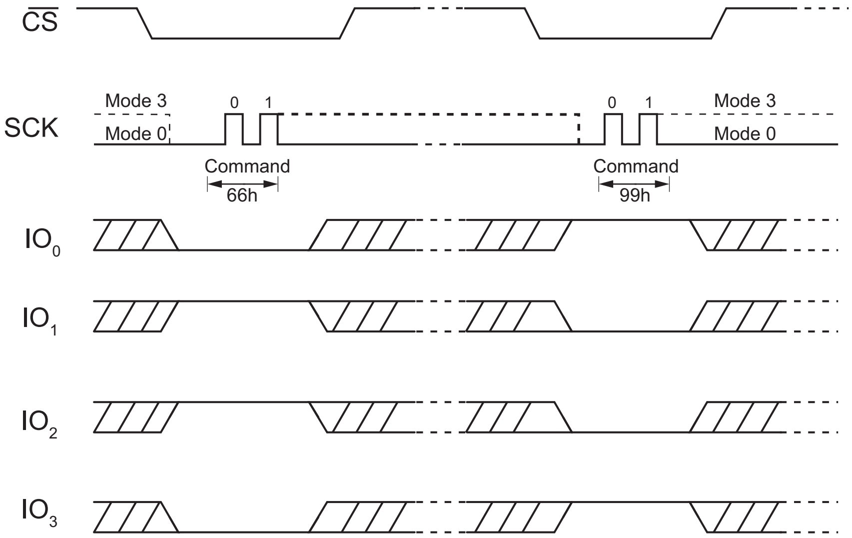


Figure 59. Enable Reset and Reset Command (QPI Mode)

8.35 Read Serial Flash Discovery Parameter (5Ah)

The Read Serial Flash Discovery Parameter (SFDP) command allows reading the Serial Flash Discovery Parameter area (SFDP). This SFDP area is composed of 2048 read-only bytes containing operating characteristics and vendor specific information. The SFDP area is factory programmed. If the SFDP area is blank, the device is shipped with all the SFDP bytes at FFh. If only a portion of the SFDP area is written to, the portion not used is shipped with bytes in erased state (FFh).

The command sequence for the read SFDP has the same structure as that of a Fast Read command. First, the device is selected by driving Chip Select ($\overline{\text{CS}}$) low. Next, the 8-bit command code (5Ah) and the 24-bit address are shifted in, followed by 8 dummy clock cycles. The bytes of SFDP content are shifted out on the Serial Data Output (SO) starting from the specified address. Each bit is shifted out during the falling edge of Serial Clock (SCK). The command sequence is shown here. The Read SFDP command is terminated by driving Chip Select ($\overline{\text{CS}}$) High at any time during data output.

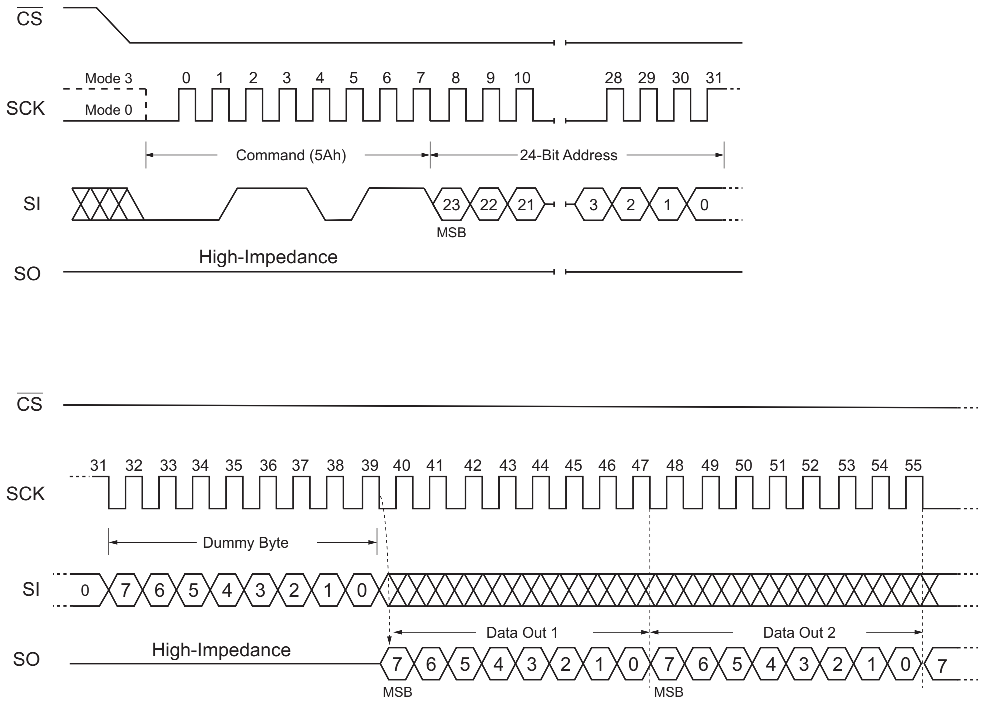


Figure 60. Read SFDP Register Command

Table 15. SFDP Signature and Headers

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
SFDP Signature		00h	07:00	0101 0011	53h
		01h	15:08	0100 0110	46h
		02h	23:16	0100 0100	44h
		03h	31:24	0101 0110	50h
SFDP Minor Revision	Start from 00h	04h	07:00	0000 0110	06h
SFDP Major Revision	Start from 01h	05h	15:08	0000 0001	01h
Number of Parameters Headers	Start from 00h	06h	23:16	0000 0001	01h
Reserved	FFh	07h	31:24	1111 1111	FFh
JEDEC Parameter ID (LSB)	JEDEC Parameter ID (LSB) = 00h	08h	07:00	0000 0000	00h
Parameter Table Minor Revision	Start from 00h	09h	15:08	0000 0110	06h
Parameter Table Major Revision	Start from 01h	0Ah	23:16	0000 0001	01h
Parameter Table Length (double words)	How many DWORDs in the parameter table	0Bh	31:24	0001 0000	10h
Parameter Table Pointer	Address of Renesas Electronics Parameter Table	0Ch	07:00	0011 0000	30h
		0Dh	15:08	0000 0000	00h
		0Eh	23:16	0000 0000	00h
JEDEC Parameter ID (MSB)	JEDEC Parameter ID (MSB):FFh	0Fh	31:24	1111 1111	FFh
JEDEC Parameter ID (LSB)	Renesas Electronics Manufacturer ID	10h	07:00	0001 1111	1Fh
Parameter Table Minor Revision	Start from 00h	11h	15:08	0000 0000	00h
Parameter Table Major Revision	Start from 01h	12h	23:16	0000 0001	01h
Parameter Table Length (double words)	How many DWORDs in the parameter table	13h	31:24	0000 0010	02h
Parameter Table Pointer (PTP)	Address of Renesas Electronics Parameter Table	14h	07:00	1000 0000	80h
		15h	15:08	0000 0000	00h
		16h	23:16	0000 0000	00h
Reserved	FFh	17h	31:24	0000 0001	01h

Table 16. SFDP Parameters Table 1

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Erase Granularity	01: 4 kB available 11: 4 kB not available	30h	01:00	01	E5h
Write Granularity	0: 1 Byte 1: 64 bytes or larger		02	1	
Volatile Status Register Block Protect Bits	0: Nonvolatile status bit 1: Volatile status bit		03	0	
Volatile Status Register Write Enable Opcode	0: 50h Opcode to enable, if bit 3 = 1		04	0	
Reserved			07:05	111	
4 kB Erase Opccde	Opcode or FFh	31h	15:08	0010 0000	20h
Fast Dual Read Output (1 -1 -2)	0: Not supported, 1: Supported	32h	16	1	F1h
Number of Address Bytes	00: 3 Byte only 01: 3 or 4 Byte 10: 4 Byte only 11: Reserved		18:17	00	
Double Transfer Rate (DTR) Clocking	0: Not supported, 1: Supported		19	0	
Fast Dual I/O Read (1-2- 2)	0: Not supported, 1: Supported		20	1	
Fast Quad I/O Read (1-4-4)	0: Not supported, 1: Supported		21	1	
Fast Quad Output Read (1-1-4)	0: Not supported, 1: Supported		22	1	
Reserved	FFh		23	1	
Reserved	FFh	33h	31:24	1111 1111	FFh
Flash Memory Density		34h	07:00	1111 1111	FFh
		35h	15:08	1111 1111	FFh
		36h	23:16	1111 1111	FFh
		37h	31:24	0000 0011	03h
Fast Quad I/O (1-4-4) Number of dummy clocks	Number of dummy clocks	38h	04:00	00100	44h
Fast Quad I/O (1-4-4) Number of mode bits	Number of mode bits		07:05	010	
Fast Quad I/O (1-4-4) Read Opcode	Opcode or FFh	39h	15:08	1110 1011	EBh
Fast Quad Output (1-1-4) Number of dummy clocks	Number of dummy clocks	3Ah	20:16	01000	08h
Fast Quad Output (1-1-4) Number of mode bits	Number of mode bits		23:21	000	
Fast Quad Output (1-1-4) Read Opcode	Opcode or FFh	3Bh	31:24	0110 1011	6Bh
Fast Dual Output (1-1-2) Number of dummy clocks	Number of dummy clocks	3Ch	04:00	01000	08h
Fast Dual Output (1-1-2) Number of mode bits	Number of mode bits		07:05	000	
Fast Dual Output (1-1-2) Read Opcode	Opcode or FFh	3Dh	15:08	0011 1011	3Bh

Table 16. SFDP Parameters Table 1 *(Continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Fast Dual I/O (1-2-2) Number of dummy clocks	Number of dummy clocks	3Eh	20:16	00000	80h
Fast Dual I/O (1-2-2) Number of mode bits	Number of mode bits		23:21	100	
Fast Dual I/O (1-2-2) Read Opcode	Opcode or FFh	3Fh	31:24	1011 1011	BBh
Fast Dual DPI (2-2-2)	0: Not supported, 1: Supported	40h	0	0	FEh
Reserved	FFh		03:01	111	
Fast Quad QPI (4-4-4)	0: Not supported, 1: Supported		04	1	
Reserved	FFh		07:05	111	
Reserved	FFh	41h	15:08	1111 1111	FFh
Reserved	FFh	42h	23:16	1111 1111	FFh
Reserved	FFh	43h	31:24	1111 1111	FFh
Reserved	FFh	44h	07:00	1111 1111	FFh
Reserved	FFh	45h	15:08	1111 1111	FFh
Fast Dual DPI (2-2-2) Number of dummy clocks	Number of dummy clocks	46h	20:16	0 0000	00h
Fast Dual DPI (2-2-2) Number of mode bits	Number of mode bits		23:21	000	
Fast Dual DPI(2-2-2) Read Opcode	Opcode or FFh	47h	31:24	1111 1111	FFh
Reserved	FFh	48h	07:00	1111 1111	FFh
Reserved	FFh	49h	15:08	1111 1111	FFh
Fast Quad QPI (4-4-4) Number of dummy clocks	Number of dummy clocks	4Ah	20:16	00010	42h
Fast Quadl QPI (4-4-4) Number of mode bits	Number of mode bits		23:21	010	
Fast Quad QPI(4-4-4) Read Opcode	Opcode or FFh	4Bh	31:24	1110 1011	EBh
Erase type-1 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	4Ch	07:00	0000 1100	0Ch
Erase type-1 Opcode	Opcode or FFh	4Dh	15:08	0010 0000	20h
Erase type-2 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	4Eh	23:16	0000 1111	0Fh
Erase type-2 Opcode	Opcode or FFh	4Fh	31:24	0101 0010	52h
Erase Type-3 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	50h	07:00	0001 0000	10h
Erase Type-3 Opcode	Opcode or FFh	51h	15:08	1101 1000	D8h
Erase Type-4 Size	4 kB = 2^0Ch, 32 kB = 2^0Fh, 64 kB = 2^10h; (2^Nbyte)	52h	23:16	0000 0000	00h
Erase Type-4 Opcode	Opcode or FFh	53h	31:24	1111 1111	FFh

Table 16. SFDP Parameters Table 1 *(Continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Erase Maximum/Typical Ratio	Maximum = 2 * (COUNT + 1) * Typical	54h 55h 56h 57h	03:00	0011	33h 62h D5h 00h
Erase type-1 Typical time	Count or 00h		08:04	0 0011	
Erase type-1 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		10:09	01	
Erase type-2 Typical time	Count or 00h		15:11	0110 0	
Erase type-2 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		17:16	01	
Erase type-3 Typical time	Count or 00h		22:18	101 01	
Erase type-3 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		24:23	01	
Erase type-4 Typical time	Count or 00h		29:25	00 000	
Erase type-4 Typical units	00b: 1ms 01b: 16ms 10b: 128ms 11b: 1s		31:30	00	
Program Maximum/Typical Ratio	Maximum = 2 * (COUNT + 1) * Typical	58h	03:00	0100	84h
Page Size	2^N bytes		07:04	1000	
Program Page Typical time	Count or 00h	59h 5Ah 5Bh	12:08	0 1001	29h 01h C7h
Program Page Typical units	0: 8µs, 1: 64µs		13	1	
Program Byte Typical time, 1st byte	Count or 00h		17:14	01 00	
Program Byte Typical units, 1st byte	0: 1µs, 1: 8µs		18	0	
Program Additional Byte Typical time	Count or 00h		22:19	000 0	
Program Additional Byte Typical units	0: 1µs, 1: 8µs		23	0	
Erase Chip Typical time	Count or 00h		28:24	0 0111	
Erase Chip Typical units	00b: 16ms 01b: 256ms 10b: 4s 11b: 64s		30:29	10	
Reserved	1h		31	1	
Prohibited Op during Program Suspend	see datasheet	5Ch	03:00	11010	ECh
Prohibited Op during Erase Suspend	see datasheet		07:04	1110	

Table 16. SFDP Parameters Table 1 *(Continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Reserved	1h	5Dh 5Eh 5Fh	08	1	A1h 07h 3Dh
Program Resume to Suspend time	Count of 64µs		12:09	0 000	
Program Suspend Maximum time	Count or 00h		17:13	11 101	
Program Suspend Maximum units	00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs		19:18	01	
Erase Resume to Suspend time	Count of 64µs		23:20	0000	
Erase Suspend Maximum time	Count or 00h		28:24	1 1101	
Erase Suspend Maximum units	00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs		30:29	01	
Suspend / Resume supported	0: Program and Erase suspend supported 1: not supported		31	0	
Program Resume Opcode	Opcode or FFh	60h	7:0	0111 1010	7Ah
Program Suspend Opcode	Opcode or FFh	61h	15:8	0111 0101	75h
Resume Opcode	Opcode or FFh	62h	23:16	0111 1010	7Ah
Suspend Opcode	Opcode or FFh	63h	31:24	0111 0101	75h
Reserved	11b	64h	01:00	11	F7h
Status Register Busy Polling	xxxxx1b: Opcode = 05h, bit 0 = 1 Busy, xxxx1xb: Opcode = 70h, bit 7 = 0 Busy, Others: reserved		07:02	1111 01	
Exit Deep Power-down time	Count or 00h	65h 66h 67h	12:08	0 0010	A2h D5h 5Ch
Exit Deep Power-down units	00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs		14:13	01	
Exit Deep Power-down Opcode	Opcode or FFh		22:15	101 0101 1	
Enter Deep Power-down Opcode	Opcode or FFh		30:23	101 1100 1	
Deep Power-down Supported	0: Deep Power-down supported, 1: not supported		31	0	

Table 16. SFDP Parameters Table 1 *(Continued)*

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
Disable 4-4-4 Read Mode		68h 69h 6Ah	03:00	1001	19h F6h 1Ch
Enable 4-4-4 Read Mode			08:04	0 0001	
Fast Quad I/O Continuous (0-4-4) supported	0: not supported, 1: Quad I/O 0-4-4 supported		09	1	
Fast Quad I/O Continuous (0-4-4) Exit			15:10	1111 01	
Fast Quad I/O Continuous (0-4-4) Enter			19:16	1100	
Quad Enable Requirements (QER)			22:20	001	
HOLD or RESET Disable	0: not supported, 1: use Configuration register bit 4		23	0	
Reserved	FFh	6Bh	31;24	1111 1111	FFh
Status Register Opcode		6Ch	06:00	110 1000	E8h
Reserved	1h		07	1	
Soft Reset Opcodes		6Dh	13:08	01 0000	10h C0h
4-Byte Address Exit		6Eh	23:14	1100 0000 00	
4-Byte Address Enter		6Fh	31:24	1000 0000	80h

Table 17. SFDP Parameters Table 2

Description	Comment	Address (h) Byte	Address (Bit)	Data (b) (Bit)	Data (h) (Byte)
V_{CC} Minimum Voltage	1650h: 1.65V, 1700h: 1.70V, 2300h: 2.30V, 2500h: 2.50V, 2700h: 2.70V	80h 81h	15:0	0000 0000 0001 0111	00h 17h
V_{CC} Maximum Voltage	1950h: 1.95V, 3600h: 3.60V, 4000h: 4.00V, 4400h: 4.40V	82h/83h	31:16	0000 0000 0010 0000	00h 20h
Array Protection Method	10b: Use non-volatile Status register	84h 85h	01:00	00	00h 00h
Power up Protection default	0: power up unprotected 1: power up protected		02	0	
Protection Disable Opcodes	011b: Use status register		05:03	000	
Protection Enable Opcodes	011b: Use status register		08:06	0 00	
Protection Read Opcodes	011b: Use status register		11:09	000	
Protection Register Erase Opcode	00b: Not supported, 01b: Opcodes 3Dh, 2Ah, 7Fh, CFh,		13:12	00	
Protection Register Program Opcode	00b: Not supported 01b: Opcodes 3Dh, 2Ah, 7Fh, FCh		15:14	00	
Reserved	FFh	86h	23:16	1111 1111	FFh
Reserved	FFh	87h	31:24	1111 1111	FFh
Reserved	FFh	88h - FFh			Reserved

8.36 Enter Secured OTP (B1h)

The Enter Secured OTP command is used for entering the additional 4-kbit secured OTP mode. The OTP array is independent from main array, which may be used to store unique serial number for system identifier. After entering the Secured OTP mode, and then follow standard read or program, procedure to read out the data or update data. The Secured OTP data cannot be updated again once it is locked down.

Note that the Write Status Register-1, Write Status Register-2 and Write Security Register commands are not acceptable during the access to the secure OTP region. Once security OTP is locked down, only commands related with read are valid. The Enter Secured OTP command sequence is shown in Figure 61.

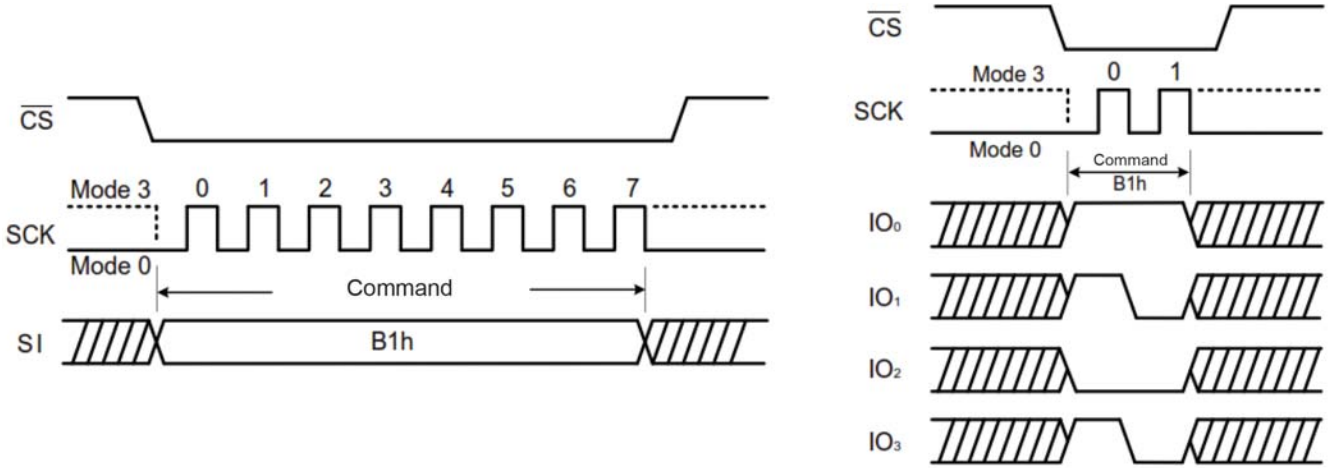


Figure 61. Enter Secured OTP Command for SPI Mode (left) and QPI Mode (right)

8.37 Exit Secured OTP (C1h)

The Exit Secured OTP command is for exiting the additional 4-kbit secured OTP mode (see Figure 62).

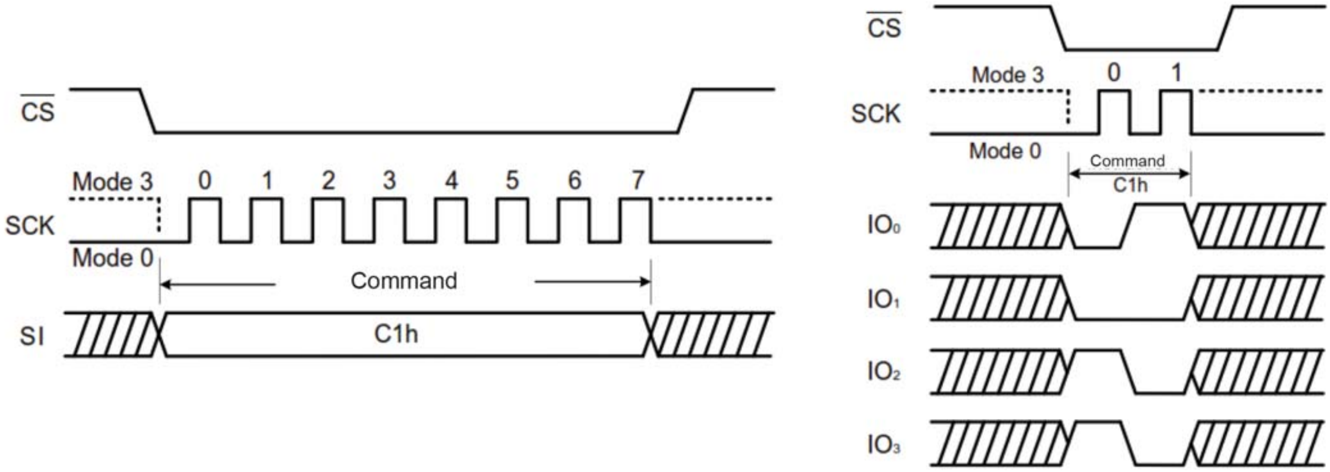


Figure 62. Exit Secured OTP command for SPI Mode (left) and QPI Mode (right)

8.38 Read Security Register (2Bh)

The Read Security Register read the value of Security Register bits at any time (even in program/erase/write status register-1 and write status register-2 condition) and continuously.

Secured OTP Indicator bit. The Secured OTP indicator bit shows whether the chip is factory-locked or non-factory-locked. When the bit is "0", it indicates a non-factory lock, a "1" indicates a factory-lock.

Lock-down Secured OTP (LDSO) bit. By writing Write Security Register command, the LDSO bit can be set to "1" for customer lock-down purpose. However, once the bit it set to "1" (lock-down), the LDSO bit and the 4-kbit Secured OTP area cannot be updated any more. While it is in 4-kbit Secured OTP mode, array access is not allowed to write.

Table 18. Security Register Definition

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
x	x	x	x	x	x	LDSO (indicate if lock-down)	Secured OTP indicator bit
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0: no lock down 1: lock- down (cannot program/ erase OTP)	0: non factory lock 1: factory lock
Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Volatile bit	Non Volatile bit	Non-Volatile bit

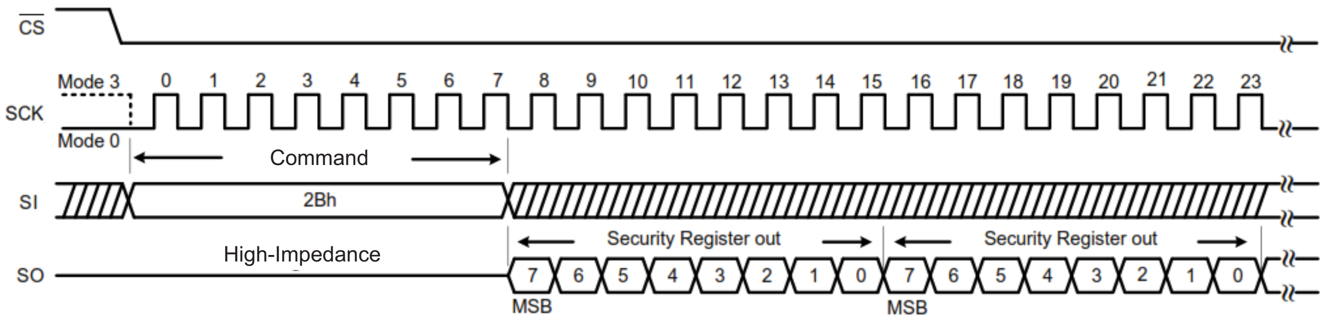


Figure 63. Read Security Register Command (SPI Mode)

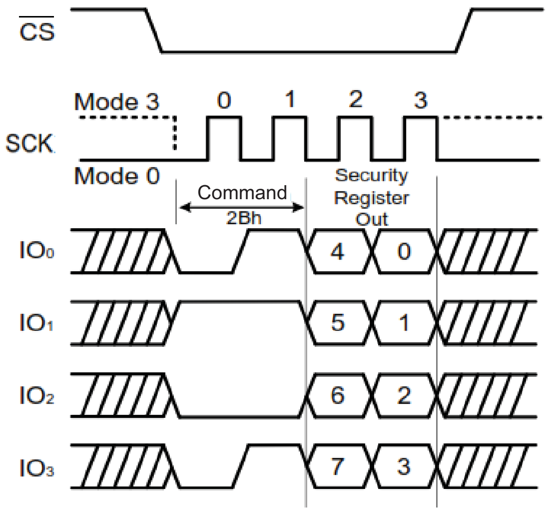


Figure 64. Read Security Register Command (QPI Mode)

8.39 Write Security Register (2Fh)

The Write Security Register command is for changing the values of Security Register bits. Unlike the Write Status Register, the Write Enable command is not required before executing the Write Security Register command. The Write Security Register command can be used to change the value of bit 1 (LDSO) to lock-down the 4-kbit Secured OTP area. Once the LDSO bit is set, the Secured OTP area can no longer be updated.

The $\overline{\text{CS}}$ must go high exactly at the boundary; otherwise, the command is not executed.

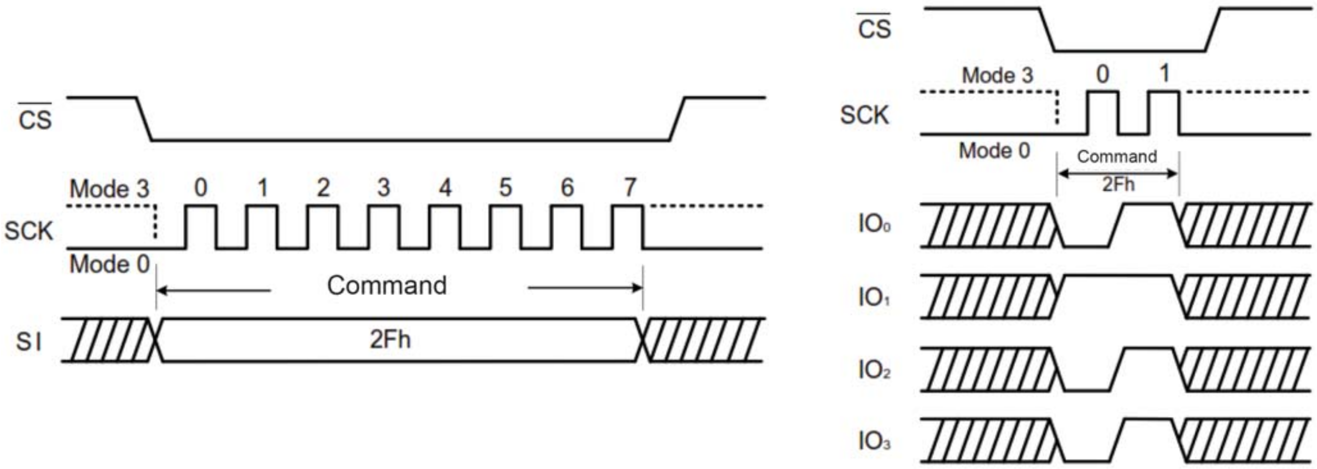


Figure 65. Write Security Register Command for SPI Mode (left) and QPI Mode (right)

8.40 4-kbit Secured OTP

This value provides a 4-kbit one-time-program area for setting the device unique serial number which can be set by the factory or the customer.

- Security register bit 0 indicates whether the chip is locked by factory.
- To program the 4-kbit secured OTP, enter the 4-kbit secured OTP mode (with ENSO command) and go through the normal program procedure; then, exit the 4K-bit secured OTP mode by writing the EXSO command.
- The customer can lock-down bit 1 as “1”.

Note. Once the value is locked down by either the factory the or customer, it can no longer be changed. While in 4-kbit secured OTP mode, array access is not allowed to write.

Table 19. Encoding of 4K bit Secured OTP Address

Address Range	Size	Standard	Customer Lock
000000 ~ 00000F	128 bits	ESN (Electrical Serial Number)	Determined by customer
000010 ~ 0001FF	3,968 bits	N/A	

9. Electrical Characteristics

Table 20. Absolute Maximum Ratings [1]

Parameter	Symbol	Conditions	Range	Unit
Supply Voltage	V_{CC}		-0.6 to V_{CC}+0.4	V
Voltage Applied to Any Pin	V_{IO}	Relative to Ground	-0.6 to V_{CC} +0.4	V
Transient Voltage on any Pin	V_{IOT}	<20 ns Transient Relative to Ground	-1.0 V to V_{CC} +1.0 V	V
Storage Temperature	T_{STG}		-65 to +150	˚C
Lead Temperature	T_{LEAD}		See Note 2	˚C
Electrostatic Discharge Voltage	V_{ESD}	Human Body Model [3]	-2000 to +2000	V

1. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. The “Absolute Maximum Ratings” are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Voltage extremes referenced in the “Absolute Maximum Ratings” are intended to accommodate short duration undershoot/overshoot conditions and does not imply or guarantee functional device operation at these levels for any extended period of time.
2. Compliant with JEDEC Standard J-STD-20C for small body Sn-Pb or Pb-free (Green) assembly and the European directive on restrictions on hazardous substances (RoHS) 2002/95/EU.
3. JEDEC Std JESD22-A114A (C1=100pF, R1=1500 ohms, R2=500 ohms).

9.1 Operating Ranges

Table 21. Device Operating Rate

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{CC}	f_R = 133 MHz (Single/Dual/Quad SPI) f_R = 50 MHz (Read Data 03h)	1.7	2.0	V
Ambient Operating Temperature	T_A	Industrial	-40	+85	˚C

9.2 Endurance and Data Retention

Table 22. Endurance and Data Retention

Parameter	Condition	Min	Max	Unit
Erase/Program Cycles	4-kB block, 32-/64-kB block or full chip	100,000		Cycles
Data Retention	Full temperature range		20	Years

9.3 Power-Up Timing and Write Inhibit Threshold

Table 23. Power-up Timing and Write Inhibit Threshold Parameters

Parameter	Symbol	Min	Max	Unit
V_{CC} (min) to $\overline{CS}$ Low	t_{VSL}(1)	15		µs
Time Delay Before Write Command	t_{PUW}(1)	1	10	ms
Write Inhibit Threshold Voltage	V_{WI}(1)	1.0	1.4	V

1. These parameters are characterized at -10C & +85C only

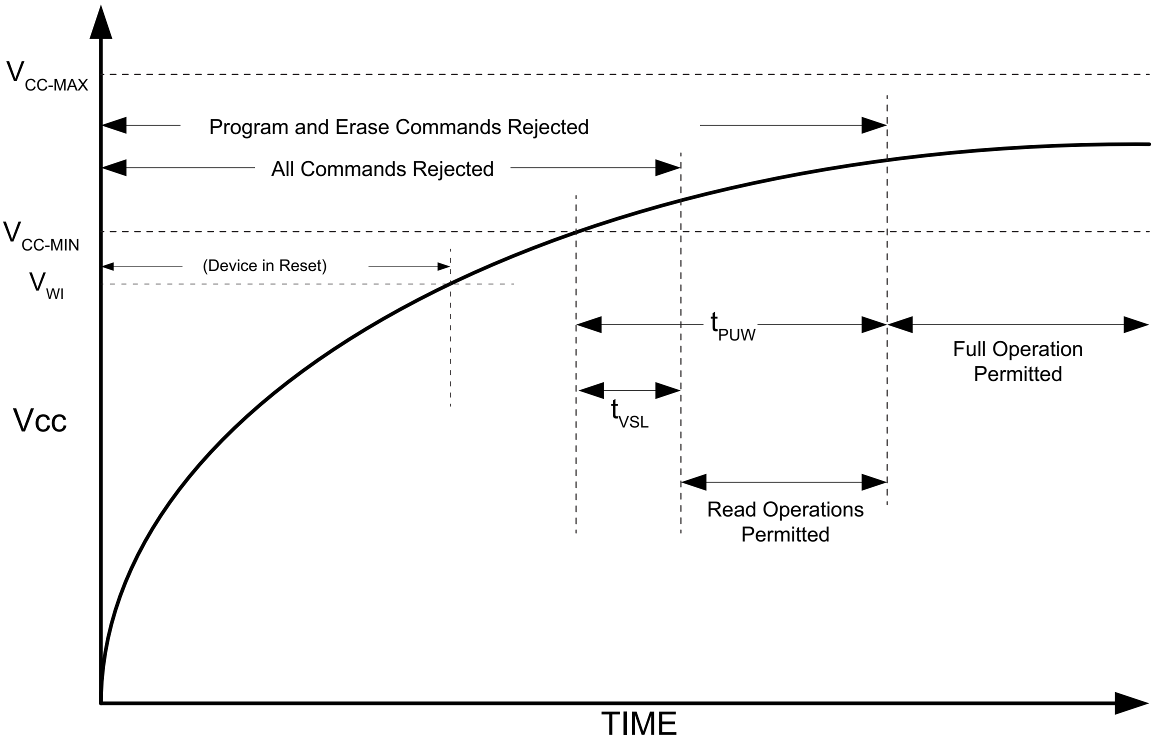


Figure 66. Power-up Timing and Voltage Levels

9.4 DC Electrical Characteristics

Table 24. DC Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Capacitance	CIN(1)	V_{IN} = 0 V(2)			6	pF
Output Capacitance	COUT(1)	V_{OUT} = 0 V(2)			8	pF
Input Leakage	I_{LI}				±2	µA
I/O Leakage	I_{LO}				±2	µA
Standby Current	I_{CC1}	$\overline{CS}$ = V_{CC}, VIN = GND or V_{CC}		10	50	µA
Power-Down Current	I_{CC2}	$\overline{CS}$ = VCC, VIN = GND or V_{CC}		2	20	µA
Current Read Data/ Dual/Quad 50 MHz(2)	I_{CC3}	C = 0.1 V_{CC} / 0.9 V_{CC} IO = Open		8	15	mA
Current Read Data/ Dual/Quad 80 MHz(2)	I_{CC3}	C = 0.1 V_{CC} / 0.9 V_{CC} IO = Open		13	18	mA
Current Read Data/ Dual/Quad 104 MHz(2)	I_{CC3}	C = 0.1 V_{CC} / 0.9 V_{CC} IO = Open		13	20	mA
Current Read Data/ Dual/Quad 133 MHz(2)	I_{CC3}	C = 0.1 V_{CC} / 0.9 V_{CC} IO = Open		15	27	mA
Current Write Status Register	I_{CC4}	$\overline{CS}$ = V_{CC}		10	20	mA
Current Page Program	I_{CC5}	$\overline{CS}$ = V_{CC}		15	25	mA
Current Block Erase	I_{CC6}	$\overline{CS}$ = V_{CC}		15	25	mA
Current Chip Erase	I_{CC7}	$\overline{CS}$ = V_{CC}		15	25	mA
Input Low Voltage	V_{IL}		-0.5		V_{CC} x 0.2	V
Input High Voltage	V_{IH}		V_{CC} x 0.8		V_{CC} + 0.4	V
Output Low Voltage	V_{OL}	I_{OL} = 100 µA			0.2	V
Output High Voltage	V_{OH}	I_{OH} = -100 µA	V_{CC} - 0.2			V

1. Tested on sample basis and specified through design and characterization data, TA = 25˚C, V_{CC} = 1.8V.
2. Checkerboard pattern.

9.5 AC Measurement Conditions

Table 25. AC Measurement Conditions

Parameter	Symbol	Min	Max	Unit
Load Capacitance	C_L		30	pF
Input Rise and Fall Times	T_R, T_F		5	ns
Input Pulse Voltages	V_{IN}	0.2 V_{CC} to 0.8 V_{CC}		V
Input Timing Reference Voltages	IN	0.3 V_{CC} to 0.7 V_{CC}		V
Output Timing Reference Voltages	OUT	0.5 V_{CC} to 0.5 V_{CC}		V

1. Output Hi-Z is defined as the point where data out is no longer driven

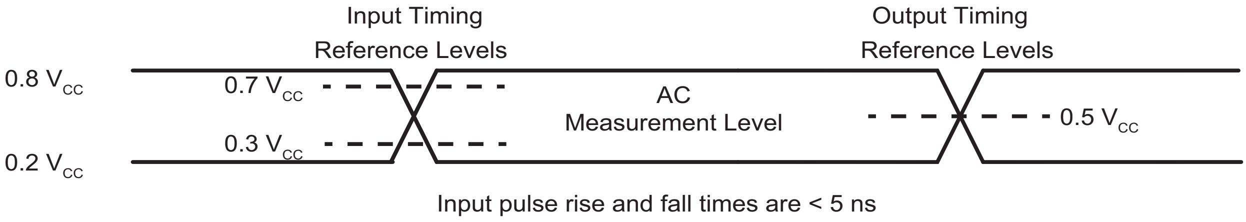


Figure 67. AC Measurement I/O Waveform

9.6 AC Electrical Characteristics

Table 26. AC Electrical Characteristics

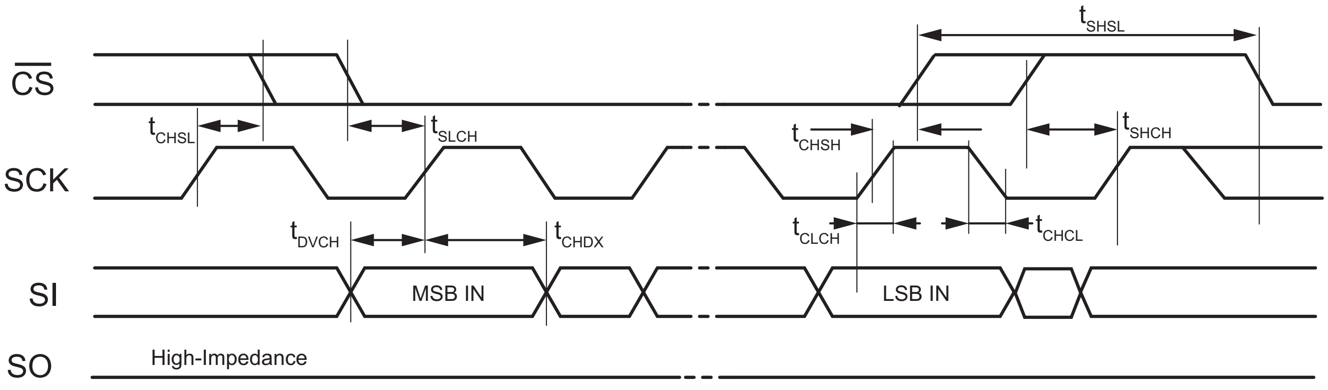
Parameter [5]	Symbol	Alt	Min	Typ	Max	Unit
Clock frequency for all commands, except Read Data and Fast Read Data in SPI mode (03h, 0Bh) 1.7 V - 2.0 V V_{CC} and industrial temperature	F_R	f_C	D.C.		133	MHz
Clock freq. Fast Read Data command in SPI mode (0Bh)	f_R		D.C.		104	MHz
Clock freq. Read Data command in SPI mode (03h)	f_R		D.C.		50	MHz
Clock High, Low Time except Read Data (03h)	t_{CLH}, t_{CLL} [1]		3.5			ns
Clock High, Low Time for Read Data (03h) commands	t_{CRLH},		8			ns
Clock Rise Time peak to peak	t_{CLCH} [2]		0.1			V/ns
Clock Fall Time peak to peak	t_{CHCL} [2]		0.1			V/ns
$\overline{CS}$ Active Setup Time relative to Clock	t_{SLCH}	t_{CSS}	5			ns
$\overline{CS}$ Not Active Hold Time relative to Clock	t_{CHSL}		5			ns
Data In Setup Time	t_{DVCH}	t_{DSU}	2			ns
Data In Hold Time	t_{CHDX}	t_{DH}	3			ns
$\overline{CS}$ Active Hold Time relative to Clock	t_{CHSH}		5			ns
$\overline{CS}$ Not Active Setup Time relative to Clock	t_{CHSH}		5			ns
$\overline{CS}$ Deselect Time (for Read commands/Write, Erase and Program commands)	t_{SHSL}	t_{CSH}	100			ns
Output Disable Time	t_{SHQZ} [2]	t_{DIS}			7	ns
Clock Low to Output Valid	t_{CLQV}	t_{V1}			6	ns
Clock Low to Output Valid (Except Main Read) [3]	t_{CLQV}	t_{V2}			7	ns
Output Hold Time	t_{CLQX}	t_{HO}	1.5			ns
$\overline{HOLD}$ Active Setup Time relative to Clock	t_{HLCH}		5			ns
$\overline{HOLD}$ Active Hold Time relative to Clock	t_{CHHH}		5			ns
$\overline{HOLD}$ Not Active Setup Time relative to Clock	t_{HHCH}		5			ns
$\overline{HOLD}$ Not Active Hold Time relative to Clock	t_{CHHL}		5			ns
$\overline{HOLD}$ to Output Low-Z	t_{HHQX} [2]	t_{LZ}			7	ns
$\overline{HOLD}$ to Output High-Z	t_{HLQZ} [2]	t_{HZ}			12	ns
Write Protect Setup Time Before $\overline{CS}$ Low	t_{WHSL} [4]		20			ns
Write Protect Setup Time After $\overline{CS}$ High	t_{SHWL} [4]		100			ns
$\overline{CS}$ High to Power-Down Mode	t_{DP} [2]				3	µs
$\overline{CS}$ High to Standby Mode without Electronic Signature Read	t_{RES1} [2]				3	µs
$\overline{CS}$ High to Standby Mode with Electronic Signature Read	t_{RES2} [2]				1.8	µs
$\overline{CS}$ High to next Command after Suspend	t_{SUS} [2]				30	µs
$\overline{CS}$ High to next Command after Reset	t_{RST} [2]				30	µs
Write Status Register Time	t_W			5	15	ms

Table 26. AC Electrical Characteristics *(Continued)*

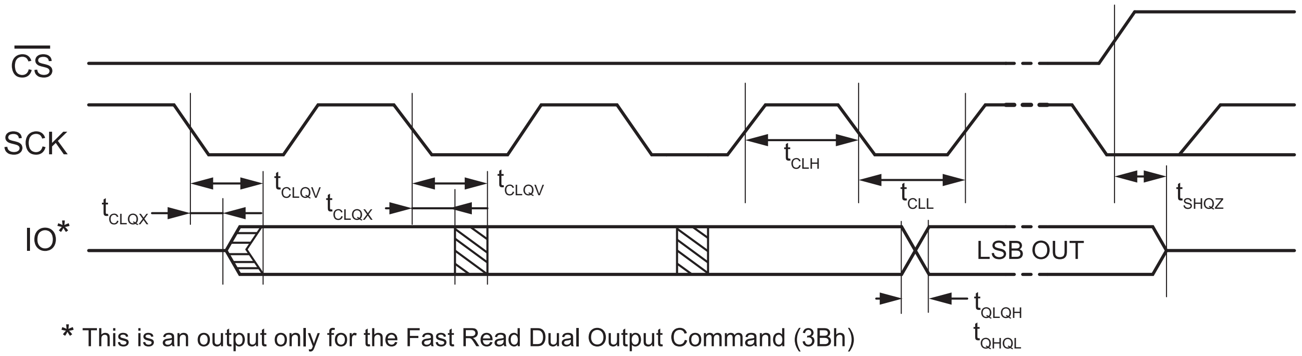
Parameter [5]	Symbol	Alt	Min	Typ	Max	Unit
Byte Program Time	t_{BP}			5	150	µs
Page Program Time	t_{PP}			0.6	5	ms
Block Erase Time (4 kB)	t_{SE}			0.06	0.4	s
Block Erase Time (32 kB)	t_{BE1}			0.2	1.5	s
Block Erase Time (64 kB)	t_{BE2}			0.35	2	s
Chip Erase Time	t_{CE}			60	150	s

1. Clock high + Clock low must be less than or equal to 1/fc.
2. Value guaranteed by design and/or characterization, not 100% tested in production.
3. Contains: Read Status Register-1,2/ Read Manufacturer/Device ID, Dual, Quad/ Read JEDEC ID/ Read Security Register/ Read Serial Flash Discovery Parameter.
4. Only applicable as a constraint for a Write Status Register command when Sector Protect Bit is set to 1.
5. Commercial temperature only applies to Fast Read (FR). Industrial temperature applies to all other parameters.

9.7 Input Timing

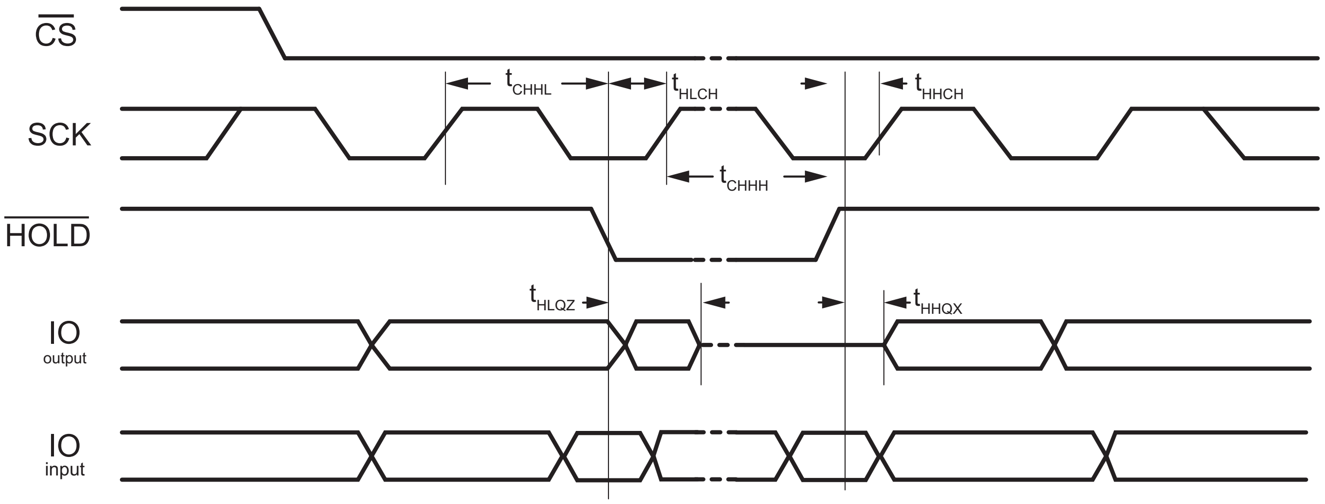


9.8 Output Timing

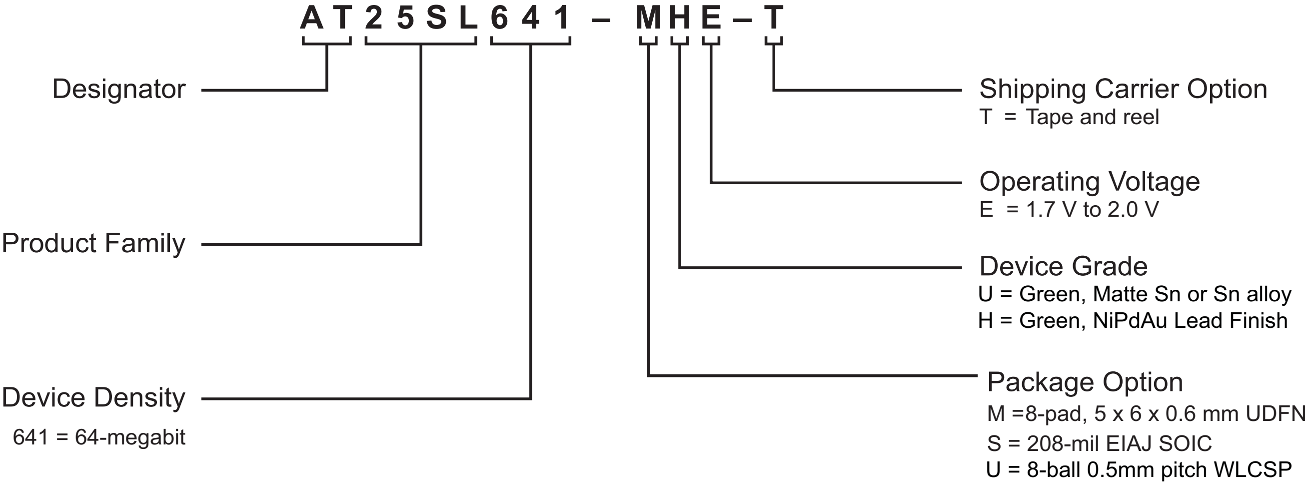


* This is an output only for the Fast Read Dual Output Command (3Bh)

9.9 $\overline{\text{Hold}}$ Timing



10. Ordering Information

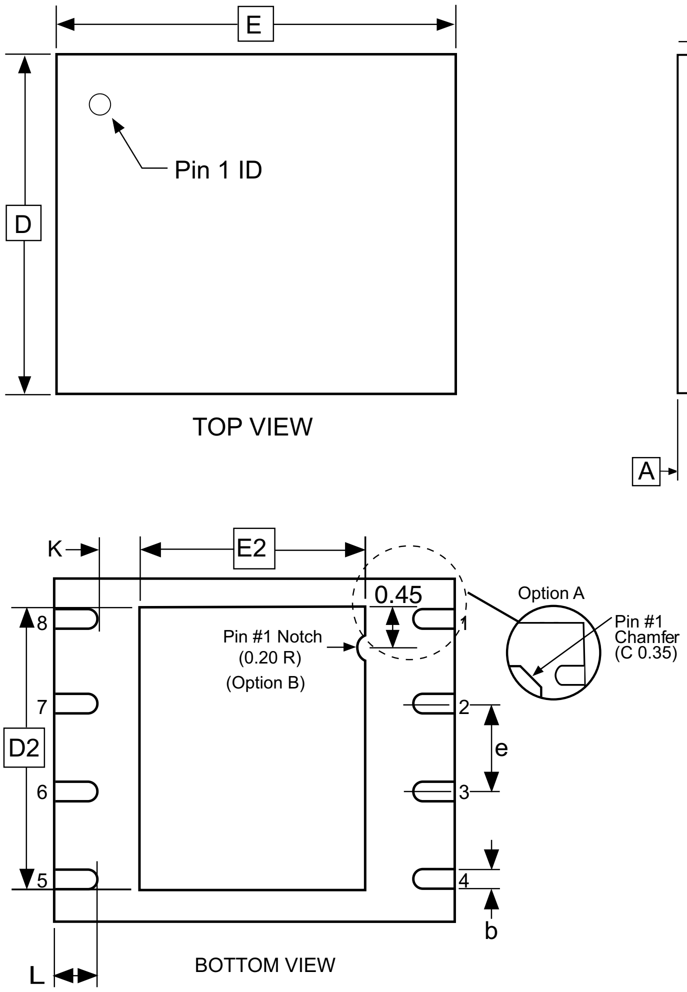


Ordering Code[1]	Package	Lead Finish	Operating Voltage	Max. Freq.	Operation Range
AT25SL641-MHE-T	8-pad (5 x 6 x 0.6 mm body), Thermally Enhanced Plastic Ultra-Thin Dual Flat No-lead (UDFN)	NiPdAu	1.7V - 2.0V	133 MHz	-40 ˚C to 85 ˚C (Industrial Temperature Range)
AT25SL641-SHE-T	8-lead, 208-mil Wide Plastic Gull Wing Small Outline Package EIAJ SOIC				
AT25SL641-UUE-T	8-ball, 0.5mm pitch WLCSP	SnAgCu			

1. The shipping carrier option code is not marked on the devices.

11. Packaging Information

11.1 UDFN



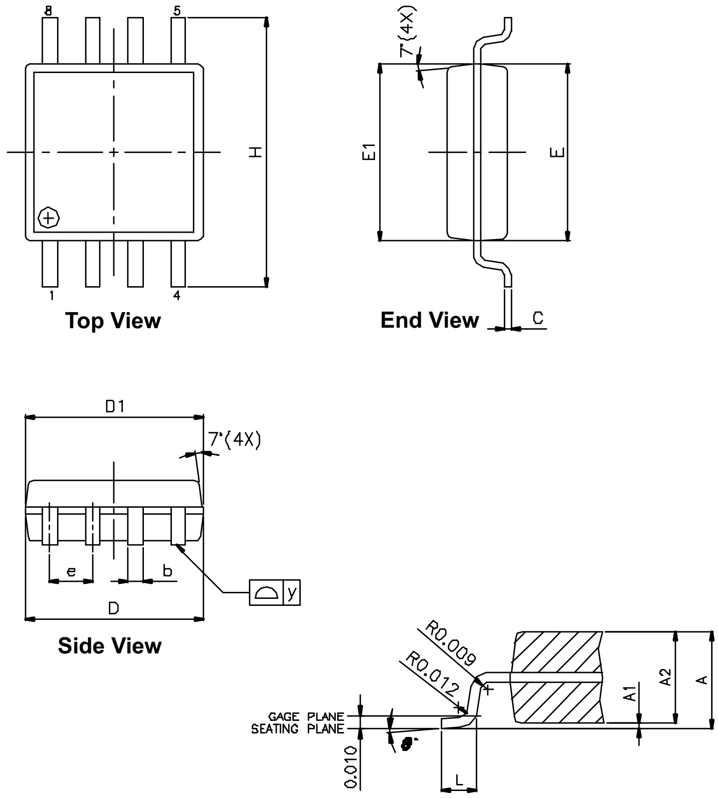
COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.45	0.55	0.60	
A1	0.00	0.02	0.05	
b	0.35	0.40	0.48	
C		0.152 REF		
D	4.90	5.00	5.10	
D2	3.80	4.00	4.20	
E	5.90	6.00	6.10	
E2	3.20	3.40	3.60	
e		1.27		
L	0.50	0.60	0.75	
y	0.00	–	0.08	
K	0.20	–	–	

Notes: 1. This package conforms to JEDEC reference MO-229, Saw Singulation.
2. The terminal #1 ID is a Laser-marked Feature.

	TITLE	GPC	REV.
	8-pad (5 x 6 x 0.6 mm Body), Thermally Enhanced Plastic Ultra Thin Dual Flat No Lead Package (UDFN)	YFG	D

11.2 8-Lead, 208-mil EIAJ SOIC

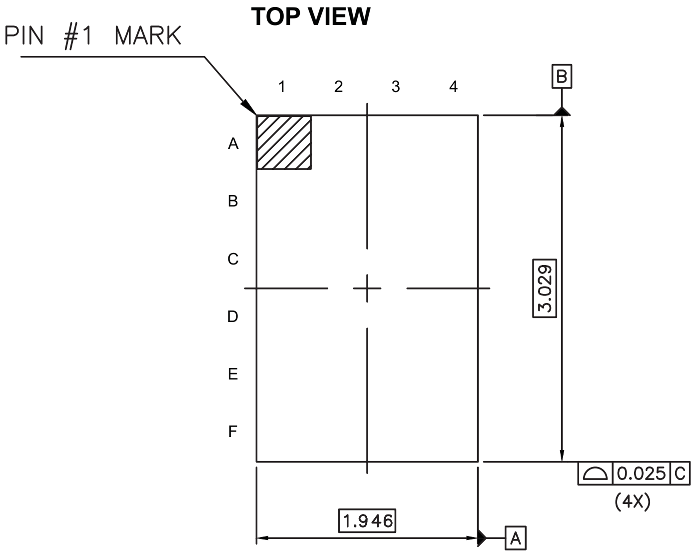


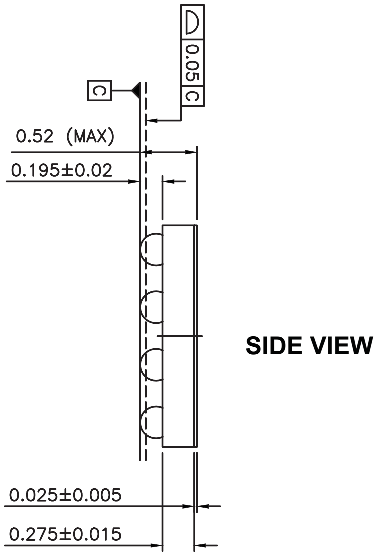
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.75	1.95	2.16	0.069	0.077	0.085
A1	0.05	0.15	0.25	0.002	0.006	0.010
A2	1.70	1.80	1.91	0.067	0.071	0.075
b	0.35	0.42	0.48	0.014	0.017	0.019
C	0.19	0.20	0.25	0.007	0.008	0.010
D	5.18	5.28	5.38	0.204	0.208	0.212
D1	5.13	5.23	5.33	0.202	0.206	0.210
E	5.18	5.28	5.38	0.204	0.208	0.212
E1	5.13	5.23	5.33	0.202	0.206	0.210
e	—	1.27	—	—	0.050	—
H	7.70	7.90	8.10	0.303	0.311	0.319
L	0.50	0.65	0.80	0.020	0.026	0.031
y	—	—	0.10	—	—	0.004
θ	0°	—	8°	0°	—	8°

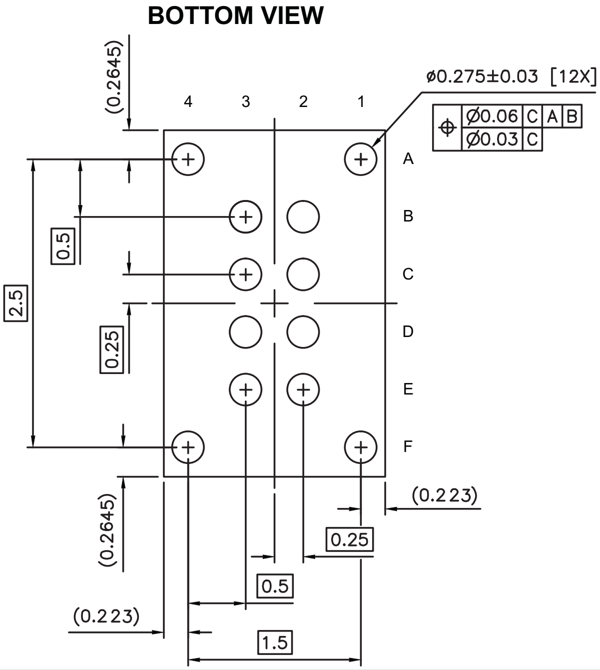
NOTES :

1. CONTROLLING DIMENSION : INCH
2. LEAD FRAME MATERIAL : COPPER 194.
3. DIMENSION "D","D1" DOES NOT INCLUDE MOLD FLASH, MOLD FLASH SHALL NOT EXCEED 0.006"[0.15mm] PER END. DIMENSION "E","E1" DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010"[0.25mm] PER SIDE.
4. DIMENSION "b" DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.003"[0.08mm].

11.3 8-Ball WLCSP







COMMON DIMENSIONS
(Unit of Measure = mm)

Pin Assignment Matrix

	A	**B**	**C**	**D**	**E**	**F**
1	NC					NC
2		V_{CC}	I/O_3 ($\overline{HOLD}$)	SCK	I/O_0 (SI)	
3		$\overline{CS}$	I/O_1 (SO)	I/O_2 ($\overline{WP}$)	GND	
4	NC					NC

	TITLE	**GPC**	**DRAWING NO.**	**REV.**
RENESAS	**8-WLCSP,** 8-ball (2 x 4 Array), Wafer Level Chip Scale Package (WLCSP)	YFG	8W-8A	A

12. Revision History

Revision Level	Date	Change History
A	6/2016	Initial release.
B	8/2016	Added 8-WLCSP package. Added 18-WLCSP package. Updated voltage range. Removed Sector and Block Protect descriptions. Removed Status Register Memory Protection tables. Updated t_{CSH} specification.
C	11/2016	Updated UDFN and 8-WLCSP package drawing and dimensions. Updated SFDP tables (to version 1.6). Added description to Write Status Register in QPI mode.
D	2/2017	Updated Note 1 on Table 8.1.
E	11/2017	Updated Table 1-1 ($\overline{\text{WP}}$ pin description). Updated 5.1 (Write Protect Features). Updated Tables 6-1 and 6-2. Restored Sector and Block Protect descriptions. Restored Status Register Memory Protection tables (Tables 6-3 and 6-4). Updated document status from Advanced to Complete. Added Errata 11.1. Removed references to 133 MHz option. Removed RESET option. Removed 18-WLCSP and 24-ball BGA package options. Removed references to ACC feature.
F	12/2018	Updated maximum frequency to 133 MHz on first page. Updated maximum frequencies in Section 1, Introduction. Added 133 MHz entry to the EBh command (Fast Read Quad I/O) in Table 7-5, QPI commands. Added 133 MHz entry to the 0Ch command (Burst Read with Wrap) in Table 7-5, QPI commands. Updated maximum frequency to 133 MHz in Figure 7-13, Fast Read command (0Bh). Updated maximum frequency to 133 MHz in Figure 7-21, Fast Read Quad I/O command (EBh). Replaced Figure 7-50, Word Read Quad I/O (E7h). Updated maximum frequency to 133 MHz in Figure 7-54, Burst Read with Wrap command (0Ch). Section 7.33, Set Parameters (C0h) renamed to Section 7.8, Set Parameters (C0h). Added title and number to the first table (now Table 7-6) and added P5:P4 = 11 encode row. Added title and number to the second table (now Table 7-7) and added P1:P0 = 11 encode row. Updated maximum frequency to 133 MHz in Section 8.2, Operating Ranges. Added 133 MHz ICC3 entry to Table 8.5, DC Characteristics. Reworked first four rows of Section 8.7, AC Characteristics to include 133 MHz and differentiate between the 03h and 0Bh commands. Updated maximum frequency to 133 MHz in Section 9.1, Ordering Codes. Standardization of all tables in document. Reformat as necessary. Updated package type text at the bottom of the 8S4 package drawing. Modified text for the 90h command in Section 7.25 to clarity QPI operation.
G	09/2022	Applied new corporate template to document. Added physical block size information to Section 1 Introduction. Removed the 208-mil SOIC package option in Section 10 and Section 11. Added the following note to the description of the 75h command: “A read operation from an 8-Mbit area (referred to as a physical block) that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.” Changed “AT25SL641-SUE-T” to “AT25SL641-MHE-T” in Section 10. Removed the “S” from Package Options in Section 10. Removed “AT25SL641-SUE-T” from Ordering Code in Section 11. Removed “8S4” from Package Type in Section 10. Added the following note to the end of the description of the 75h opcode: “Note: A read operation from a physical block that includes a suspended area might provide unreliable data. For the definition of the physical block and for the techniques to ensure high data integrity, see application note AN-500.” Changed parameter t_{VCSL} to t_{VSL} in Figure 65. In Table 2, added sentence to the end of the description of $\overline{\text{CS}}$ and changed the description of $\overline{\text{WP}}/\text{IO}_2$ and $\overline{\text{HOLD}}/\text{IO}_3$. Added typical values for ICC3 in Table 24.
H	03/2023	Added the 208-mil SOIC package option. Updated the WLCSP POD.
I	05/2024	Deleted erroneous reference to ACC in Table 26. Added pinout for 8-WSOIC.

12.1 Errata

1. If Status Register-2 CMP bit is 0, and Status Register-1 bits {SEC,TB,BP2,BP1,BP} are {1,0,0,0,1}, addresses 7FF000h-7FFFFFh *are protected* from any Program or Erase commands. However, this setting does *not* protect the rest of Sector 127 or the rest of Block 255 from 64-kbit or 32-kbit Block Erase commands. If a 64-kbit Block Erase Command is issued to Sector 127, addresses 7F0000h-7FEFFFh *are* erased. If a 32-kbit Block Erase Command is issued to Block 255, addresses 7F8000h-7FEFFFh *are* erased.

Workaround: If this protection bit combination is used and the behavior described in Note 3 is required, avoid using 64-kbit or 32-kbit Block Erase commands for this specific memory region.

2. If Status Register-2 CMP bit is 1, and Status Register-1 bits {SEC,TB,BP2,BP1,BP} are {1,1,0,0,1}, addresses 001000h-7FFFFFh *are protected* from any Program or Erase commands. However, this setting does *not* protect the rest of Sector 0 or the rest of Block 0 from 64-kbit or 32-kbit Block Erase commands. If a 64-kbit Block Erase Command is issued to Sector 0, addresses 000000h-000FFFh *are* erased. If a 32-kbit Block Erase Command is issued to Block 0, addresses 000000h-000FFFh *are* erased.

Workaround: If this protection bit combination is used and the behavior described in Note 3 is required, avoid using 64-kbit or 32-kbit Block Erase commands for this specific memory region.

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