ASI4U-V5

ASi-5 Transceiver

R19DS0107ED0102
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Outline

Description

The ASI4U-V5 ASSP is a silicon solution that implements an Actuator-Sensor-Interface version 5 (ASi-5) fieldbus transceiver. It reduces the integration effort of an ASi-5 interface to a minimum. The implementation of the complex transmission process is optimally distributed between hardware and firmware components. Both slave options outlined in the ASi-5 specification are easily implemented. In simple slave mode, the chip is only supplied with process data via digital I/O pins. For complex slave implementations, process data and acyclic communication are handled via a serial interface. The compact, power-saving design enables the development into small form factors.

Features

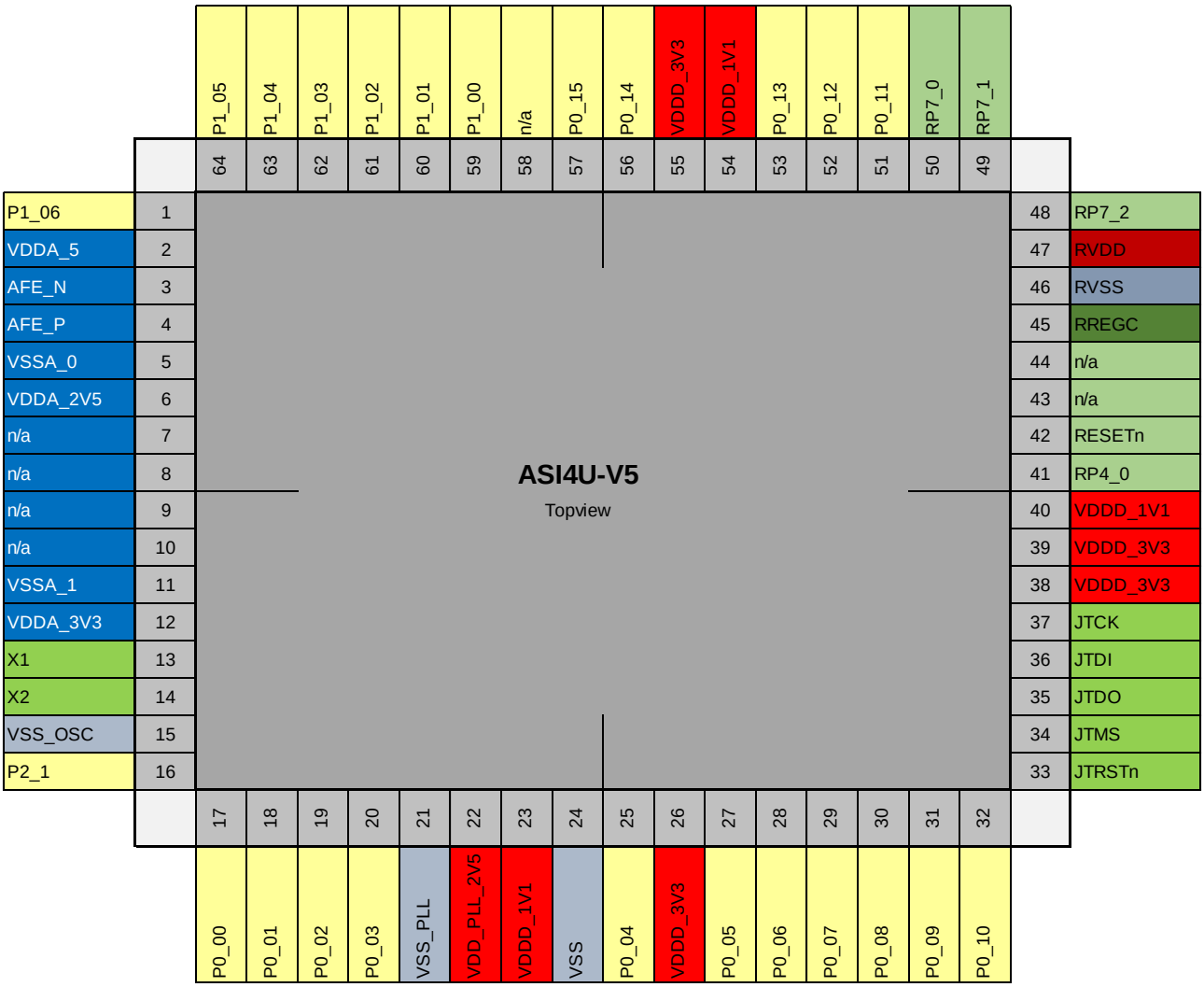
The ASI4U-V5 ASSP offers the following features.

- Silicon solution implementing an ASi-5 transceiver
- ASi-5 supports the integration of up to 96 devices, operation down to 1.27 ms cycle time and up to 200 meter cable length.
- Up to 32 bytes of cyclic data per device.
- Diagnostics and event handling for industry 4.0 applications
- Backwards compatibility with ASi-3 devices
- Exceptional robustness against electromagnetic disturbers
- Supports simple slave and complex slave applications
- Operating Temperature: -40°C to +85°C
- Supply voltages: 5V & 3.3V
- Package: 64-pin Quad Flat No-lead (QFN), 9 x 9 mm, 0.5 mm pitch

Ordering Information

Part No.	Application	Package
R9J06G039UGNP	ASi-5 Transceiver	64-pin Quad Flat No-lead (QFN) (9 x 9 mm, 0.5 mm pitch)

Pin Arrangement



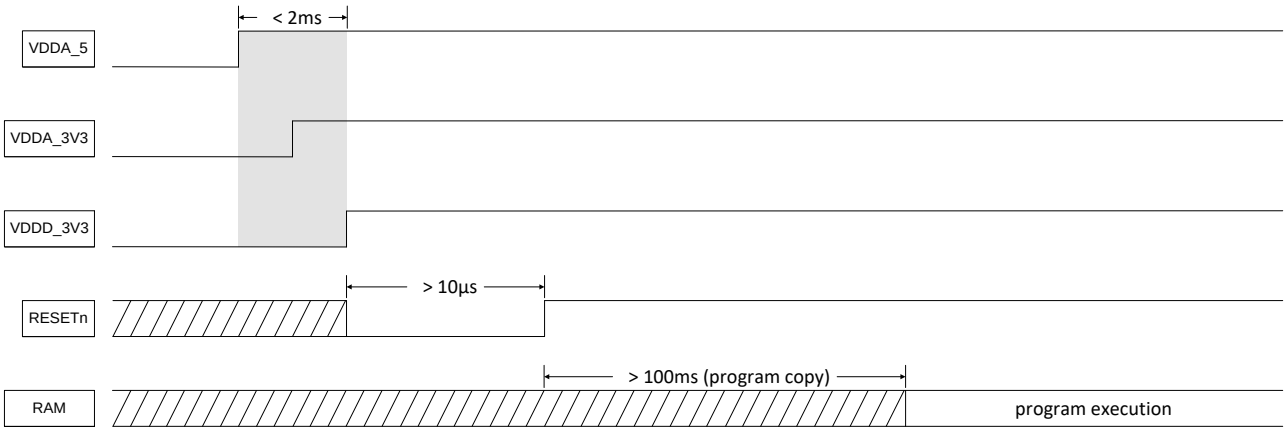
Pin Description

Pin No.	Pin Name	Function
1	P1_06	General purpose digital I/O signal
2	VDDA_5	external 5V AFE supply input
3	AFE_N	APOS PHY interface I/O
4	AFE_P	APOS PHY interface I/O
5	VSSA_0	External AFE GND input
6	VDDA_2V5	2.5V AFE regulator output (only used for smoothing capacitor)
7	n/a	Not connected (leave open)
8	n/a	Not connected (leave open)
9	n/a	Not connected (leave open)
10	n/a	Not connected (leave open)
11	VSSA_1	External AFE GND input
12	VDDA_3V3	External 3.3V AFE supply input
13	X1	Connection external oscillator 30 MHz input
14	X2	Connection external oscillator 30 MHz output
15	VSS_OSC	Kelvin GND for oscillator
16	P2_1	General purpose digital I/O signal Alternate Function: Input: INTP0
17	P0_00	General purpose digital I/O signal
18	P0_01	General purpose digital I/O signal
19	P0_02	General purpose digital I/O signal
20	P0_03	General purpose digital I/O signal
21	VSS_PLL	GND for PLL
22	VDD_PLL_2V5	2.5V PLL regulator output (only used for smoothing capacitor)
23	VDDD_1V1	1.1V power supply output (from internal regulator)
24	VSS	External digital GND input
25	P0_04	General purpose digital I/O signal
26	VDDD_3V3	External 3.3V digital supply input
27	P0_05	General purpose digital I/O signal Alternate Function: Output: EXCLK
28	P0_06	General purpose digital I/O signal
29	P0_07	General purpose digital I/O signal
30	P0_08	General purpose digital I/O signal
31	P0_09	General purpose digital I/O signal
32	P0_10	General purpose digital I/O signal
33	JTRSTn	Test Reset Input, JTAG Reset. Input: Reset signal of the target port. External pull-down (4.7KΩ to VSS).
34	JTMS	Test Mode Select Input, JTAG interface is activated from the debug unit. pull-up (4.7KΩ to VDDD_3V3).
35	JTDO	Test Data Output (can be left open)
36	JTDI	Test Data Input, External pull-up (4.7KΩ to VDDD_3V3)
37	JTCK	Test Clock Input, JTAG clock signal to the ASI4U-V5 device. It is recommended that this pin is set to a defined state on the target board. External pull-up (4.7KΩ to VDDD_3V3).
38	VDDD_3V3	External 3.3V digital supply input
39	VDDD_3V3	External 3.3V digital supply input
40	VDDD_1V1	1.1V power supply output (from internal regulator)
41	RP4_0	LED output & Flash programming, SPI communication LED
42	RESETn	Global reset input (active low)
43	n/a	Not connected (leave open)
44	n/a	Not connected (leave open)

Pin No.	Pin Name	Function
45	RREGC	External digital GND input (RL78) (use capacitor of 0.47 to 1 µF)
46	RVSS	External digital GND input (RL78)
47	RVDD	External 3.3V digital supply input (RL78)
48	RP7_2	LED output, SPI communication LED
49	RP7_1	LED output, SPI communication LED
50	RP7_0	LED output, SPI communication LED
51	P0_11	General purpose digital I/O signal
52	P0_12	General purpose digital I/O signal
53	P0_13	General purpose digital I/O signal
54	VDDD_1V1	1.1V power supply output (from internal regulator)
55	VDDD_3V3	External 3.3V digital supply input
56	P0_14	General purpose digital I/O signal Alternate Function: Output: UART1_TXD
57	P0_15	General purpose digital I/O signal Alternate Function: Input: UART1_ RXD
58	n/a	Connect to pull-down resistor (10KΩ to VSS)
59	P1_00	General purpose digital I/O signal
60	P1_01	General purpose digital I/O signal Alternate Function: Input: USPI_CLKI / Output: USPI_CLKO
61	P1_02	General purpose digital I/O signal Alternate Function: Input: USPI_MOSI / Output: USPI_MOSI
62	P1_03	General purpose digital I/O signal Alternate Function: Input: USPI_MISO / Output: USPI_MISO
63	P1_04	General purpose digital I/O signal Alternate Function: Input: USPI_CSI / Output: USPI_CSO
64	P1_05	General purpose digital I/O signal Alternate Function: Input: UART0_RXD / Output: UART0_TXD

Start-Up Procedure

The start-up procedure including AFE and oscillator control is defined in the picture below.



Following signals are relevant for the start-up procedure:

- **RESETn:** external reset, input a low level for 10µs or more to the RESETn pin.
- **VDDA_5, VDDA_3V3, VDDD_3V3**: external supplies.
- **VDD_PLL_2V5, VDDD_1V1**: these supplies are generated by internal LDOs in the ASI4U-V5 device. They start ramping up after the IDDQ release of the digital power block.

Supply voltages (VDDA_5, VDDA_3V3, VDDD_3V3) shall be stable within less than 2ms.

To perform an external reset during power on, input a low level to the RESETn pin for at least 10µs after the operating voltage range is stable.

After RESETn pin is released, the ASI4U-V5 application program will be copied from RL78 Flash to ASI4U-V5 device RAM. This takes at least 100ms, before the application program is ready to execute.

Electrical Characteristics

RL78 Related Pins

The following package pins are directly connected to the RL78 MCU:

ASI4U-V5 package pin	RL78 related pin
RVDD	VDD, EVDD0
RVSS	VSS, EVSS0
RREGC	REGC
RESETn	RESETn
RP4_0	P40
RP7_2	P72
RP7_1	P71
RP7_0	P70

Note: Please also refer to document “r01ds0053ej0331-rl78g14.pdf” (or later current issue) in terms of the electrical characteristics of these RL78 pins.

Please note that the pin RP4_0 must be at high level during reset release. Otherwise, the RL78 enters external flash programming mode.

General Requirements of Chip Related Pins

Caution Note: In order to prevent undesired cross currents in the IO buffers of the chip which could reduce the lifetime of the device, it is required to connect external pull-up resistors to all input pins of the chip.

Definition of Device Pin Groups

Based on the device's pinout, the following pin groups are defined:

[DG0]	Digital Pin Group 0: P2_1, P0_[05:00],
[DG1]	Digital Pin Group 1: JTCK, JTDI, JTDO, JTMS, JTRSTn, P0_[08:06]
[DG2]	Digital Pin Group 2: P0_[15:09], P1_[06:00]
[DG3]	Digital Pin Group 3: RESETn, RP4_0, RP7_[2:0] (RL78 pins)

Depending on the (standard or high) drive strength characteristics of the above IO pins, the following sub-pin groups are defined:

[DG0]	Sub-Pin Group 0 (standard drive strength):	P2_1, P0_[05:00],
[DG1a]	Sub-Pin Group 1a (high drive strength):	JTDO, JTMS
[DG1b]	Sub-Pin Group 1b (standard drive strength):	JTCK, JTDI, JTRSTn, P0_[08:06]
[DG2a]	Sub-Pin Group 2a (high drive strength):	P1_[03:01]
[DG2b]	Sub-Pin Group 2b (standard drive strength):	P0_[15:09], P1_[06:04;00]
[DG3]	Sub-Pin Group 3 (standard drive strength):	RESETn, RP4_0, RP7_[2:0]

Notes: (1) The pins JTCK, JTDI, JTMS, and JTRSTn are input only pins.

(2) The pin JTDO is an output only pin.

Absolute Maximum Ratings

Caution Notes: (1) The device's function is not guaranteed outside of the ratings given in this chapter.

(2) Stresses beyond these ratings may cause permanent damage to the device.

(3) These are stress ratings only and functional operation of the device at these or other conditions beyond those indicated in the operational conditions within this specification is not implied.

(4) Exposure to these ratings for extended periods may affect device reliability.

Temperature Ratings

In this chapter the absolute maximum ratings of junction and storage temperature are specified.

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
M1	**Temperature ratings**						
M1.1	Junction temperature	TJ,abs	Cond.: –40°C < Ta < 85°C	–40		125	°C
M1.2	Storage temperature	TST		–55		125	°C
Table Notes: None.							

Voltage Ratings

In this chapter the absolute maximum ratings of supply voltages, ground and input voltages are specified.

Note: Reference ground potential: VSSA = VSS_OSC = 0V, with VSSA = external AFE ground supply pin and VSS_OSC = external oscillator ground supply pin. VSSA and VSS_OSC are the analog ground system.

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
M2	**Analog supply (ASUPPLY) voltage ratings**						
M2.1	External 5V AFE supply voltage	VDDA_5		–0.3		5.5	V
M2.2	External 3.3V AFE supply voltage	VDDA_3V3		–0.3		4.2	V
M3	**Digital supply (DSUPPLY) voltage ratings**						
M3.1	External 3.3V digital supply	VDDD_3V3		–0.3		4.2	V
M3.2	External 3.3V digital supply (RL78)	RVDD		-0.3		6.5	V
M4	**Ground ratings**						
M4.1	External digital ground supply / External PLL ground supply (Kelvin ground)	VSS / VSS_PLL	Cmt.: Digital ground system	–0.3		0.3	V
M5	**Regulator input voltage ratings**						
M5.1	Regulator capacitance pin	RREGC		–0.3		2.8 and RVDD + 0.3 Note 1	V
M6	**Input voltage ratings**						
M6.1	DMT IO pins: AFE_P, AFE_N	VI_AFE		–0.3		MIN(5.5; VDDA_5v0 + 0.3)	V
M6.2	External oscillator pins: X1, X2	VI_OSC		–0.3		2.8	V
M6.3	Digital pin group 0: P2_1, P0_[15:00]	VI_DG0		–0.3		MIN(5.5; VDDD_3v3 + 3.6)	V
M6.4	Digital pin group 1: P1_[06:00]	VI_DG1		–0.3		MIN(5.5; VDDD_3v3 + 3.6)	V
M6.5	Digital pin group 2 (JTAG): JTDI, JTDO, JTCK, JTMS, JTRSTn	VI_DG2		–0.3		MIN(5.5; VDDD_3v3 + 3.6)	V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
M6.6	Digital pin group 3 (RL78): RESETn, RP4_0, RP7_[2:0]	VI_DG3		-0.3		RVDD + 0.3 Note 2	V

Table Notes:

Note 1: Connect the REGC pin to RVSS via a capacitor (0.47 to 1uF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2: Must be 6.5 V or lower.

Current Ratings

In this chapter the absolute maximum ratings of supply currents and output peak currents are specified.

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
M7	**Analog supply (ASUPPLY) current ratings**						
M7.1	Max. input current 5V AFE voltage regulator	IIVDDA_5				50	mA
M7.2	Max. input current 3.3V AFE voltage regulator	IIVDDA_3V3			16	25	mA
M7.3	Max. output current of 2.5V AFE voltage regulator	IOVDDA_2V5	Cmt.: Connected to external smoothing capacitor			0	mA
M8	**Digital supply (DSUPPLY) current ratings**						
M8.1	Max. input current 3.3V digital voltage regulator	IIVDDD_3V3	Cmt.: 1 supply pin		90	150	mA
M8.2	Max. output current 2.5V PLL voltage regulator	IIVDD_PLL_ 2V5	Cmt.: Connected to external smoothing capacitor			0	mA
M8.3	Max. output current of 1.1V core voltage regulator	IOVDDD_1V1	Cmt.: Connected to external smoothing capacitor			0	mA
Table Notes: None.							

General Characteristics

External Supply Voltage Characteristics

Item	Symbol	Min	Typ	Max	Unit
VDDA_5V0 supply voltage	VDDA_5	4,5	5	5,5	V
VDDA_3V3 supply voltage	VDDA_3V3	3,0	3,3	3,6	V
VDDD_3V3 supply voltage	VDDD_3V3	3,0	3,3	3,6	V
RVDD supply voltage	RVDD	3.0	3.3	3.6	V

Regulator Output Supply Voltage Characteristics

Item	Symbol	Min	Typ	Max	Unit
VDDD_1V1 Output voltage	VDDD_1V1	1,1	1,1	1,2	V
VDD_PLL_2V5 Output voltage	VDD_PLL_2V5	Only used for smoothing capacitor of min. 100 nF ceramic capacitor min. 22 µF electrolyte capacitor (don’t connect otherwise)			
VDDA_2V5 Output voltage	VDDA_2V5	Only used for smoothing capacitor of min. 1 µF (don’t connect otherwise)			

Oscillator Characteristics

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating voltage: VDDA_3V3 = 3.0 ~ 3.6V
- VSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
G1	**Oscillator characteristics**						
G1.1	Oscillator frequency						
G1.1.1	Oscillator frequency for digital core	fOSCD	Cmt.: Used as PLL input clock		30		MHz
G1.1.2	Oscillator frequency for analog core	fOSCA	Cmt.: Used as AFE reference clock (AFECLK)		30		MHz
G1.2	Oscillator stabilization time	tOST			10		ms

Table Notes:

None.

The ASI4U-V5 device has been evaluated with the Daishinku Quartz oscillator type “DSX321G 30MHz”. For Quartz parameters please refer to the corresponding data sheet.

PLL Characteristics

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating voltage: VDD_PLL_2V5 = 2.3V ~ 2.7V
- VSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
G2	**PLL characteristics, Note (a)**						
G2.1	PLL jitter						
G2.1.1	PLL output period jitter	tPJ			330		ps
G2.1.2	PLL output long term jitter	tLTJ			0.33		ns
G2.2	PLL lock-up time	tLKP			2	50	µs

Table Notes:

Note (a) Input clock: oscillator, clock for digital core (see par. G1.1.1)

Operating Conditions

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: VDDD_3V3 = 3.0 ~ 3.6V
- Operating analog IO supply voltage: VDDA_5 = 4.5 ~ 5.5V
- VSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
G3	**Operating IO output currents**						
G3.1	**Continuous output of analog pins**						
G3.1.1	AFE_P, AFE_N	IOAFE		-50		50	mA
G3.2	**Continuous output current of digital pins, Note (a)**						
G3.2.1	Digital pin group 0 (DG0)	IODG0		-2		2	mA
G3.2.2	Digital pin group 1a (DG1a)	IODG1a		-4		4	mA
G3.2.3	Digital pin group 1b (DG1b)	IODG1b		-2		2	mA
G3.2.4	Digital pin group 2a (DG1a)	IODG2a		-4		4	mA
G3.2.5	Digital pin group 2b (DG2b)	IODG2b		-2		2	mA
G3.2.6	Total pin current		All pins	-40		40	mA
G4	**Operating frequencies**						
G4.1	Digital core system clock operating frequency	fSYSCLK	Cmt.: CPU and peripheral		120		MHz
G4.2	Trace clock operating frequency	fATCLK			120		MHz
G4.3	Debug system clock operating frequency	fDSYSCLK			120		MHz
G4.4	Sampling clock operating frequency	fSMPCLK			30		MHz

Table Notes:

Note (a) Explanation of specification values given: [min.] = output high current; [max.] = output low current.

IO Capacitances

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
G5	**IO capacitances**						
G5.1	Input capacitance of P2_1, P0_[15:00], P1_[06:00] and all JTAG pins	CID	Cond.: fC = 1MHz, 0V at unmeasured pins			10	pF
G5.2	Input capacitance of oscillator pin X1	CIX1				10	pF
Table Notes: None.							

Electrical Characteristics

Leakage Current Characteristics

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: VDDD_3V3 = RVDD = 3.0 ~ 3.6V
- Operating analog IO supply voltage: VDDA_5 = 4.5 ~ 5.5V
- VSS = RVSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E1.1	**Leakage current characteristics**						
E1.1.1	Leakage Current of Analog pins: AFE_P, AFE_N	ILAFE		-300		350	µA
E1.2	**Leakage current of digital pins w/ high drive strength:** sub-pin group DG1a and DG2a, Note (a)						
E1.2.1	Input level high	ILIH1	Cond.: Pull-up resistor disabled; VI = 3.3V			10	µA
E1.2.2	Input level low	ILIL1	Cond.: Pull-up resistor disabled; VI = 0V	–10			µA
E1.3	**Leakage current of digital pins w/ standard drive strength:** sub-pin groups DG0, DG1b, DG2b						
E1.3.1	Input level high	ILIH2	Cond.: Pull-up resistor disabled; VI = 3.3V			10	µA
E1.3.2	Input level low	ILIL2	Cond.: Pull-up resistor disabled; VI = 0V	–10			µA
E1.4	**Leakage current of digital pins w/ standard drive strength:** sub-pin groups JTAG						
E1.4.1	Input level high	ILIH3				10	µA
E1.4.2	Input level low	ILIL3		-10			µA

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E1.5	**Leakage current of digital pins w/standard drive strength:** sub-pin group DG3						
E1.5.1	Input level high	ILIH4	VI = RVDD			1	µA
E1.5.2	Input level low	ILIL4	VI = RVSS	-1			µA

Table Notes:

Note (a) Exclude JTDO pin since it is output only.

Note (b) Excluding JTDI, JTMS, JTCK and JTRSTn pins, which are input only.

DC Characteristics

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: VDDD_3V3 = RVDD = 3.0 ~ 3.6V
- Operating analog IO supply voltage: VDDA_5 = 4.5 ~ 5.5V
- VSS = RVSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E2	**DC characteristics**						
E2.1	**Input levels of analog pins:**						
E2.1.1	Input common mode voltage range (for small signal amplitude; signal amplitude will reduce common mode range due to ESD clamp)	AFE_P, AFE_N		0.0		5.0	V
E2.2	**Input voltage high level (VIH) of digital IO pins (DGn, n = 0..2, DGSiP), Note (c)**						
E2.2.1	Schmitt	VIH	Cnd.: VDDD_3v3=3.0~3.6V Schmitt input	2.0		5.5	V
E2.3	**Input voltage low level (VIL) of digital IO pins (DGn, n = 0..2, DGSiP), Note (c)**						
E2.3.1	Schmitt	VIL	Cnd.: VDDD_3v3=3.0~3.6V Schmitt input	0		0.8	V
E2.4	**Input voltage high level (VIH) of digital IO pins (DG3)**						
E2.4.1		VIH		0.8 RVDD		RVDD	V
E2.5	**Input voltage low level (VIL) of digital IO pins (DG3)**						
E2.5.1		VIL		0		0.2 RVDD	V
E2.6	**Output levels of analog pins:**						
E2.6.1	Output common mode voltage range	AFE_P, AFE_N		0.0		5.0	V
E2.7	**Output high voltage level (VOH) of digital IO pins, Note (d)**						

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E2.7.1	**Digital pins w/ high drive strength:** sub-pin groups DG1a and DG2a	VOH1	Cond.: Iload=-4mA	2.4			V
E2.7.2	**Digital pins w/ standard drive strength:** sub-pin groups DG0, DG1b, DG2b and DGSiP	VOH2	Cond.: Iload=-2mA	2.4			V
E2.8	**Output high current (IOH) of digital IO pins (test condition), Note (d)**						
E2.8.1	**Digital pins w/ high drive strength:** sub-pin groups DG1a and DG2a	IOH1	Cond.: @VOH,min			-4.0	mA
E2.8.2	**Digital pins w/ standard drive strength:** sub-pin groups DG0, DG1b, DG2b and DGSiP	IOH2	Cond.: @VOH,min			-2.0	mA
E2.9	**Output low voltage level (VOL) of digital IO pins, Note (d)**						
E2.9.1	**Digital pins w/ high drive strength:** sub-pin groups DG1a and DG2a	VOL1	Cond.: Iload=4mA			0.4	V
E2.9.2	**Digital pins w/ standard drive strength:** sub-pin groups DG0, DG1b, DG2b and DGSiP	VOL2	Cond.: Iload=2mA			0.4	V
E2.10	**Output current level (IOL) of digital IO pins (test condition), Note (d)**						
E2.10.1	**Digital pins w/ high drive strength:** sub-pin groups DG1a and DG2a	IOL1	Cond.: @VOL,max	4.0			mA
E2.10.2	**Digital pins w/ standard drive strength:** sub-pin groups DG0, DG1b, DG2b and DGSiP	IOL2	Cond.: @VOL,max	2.0			mA

Table Notes:

Note (c) Excluding JTDO pin, which is output only.

Note (d) Excluding JTDI, JTMS, JTCK and JTRSTn pins, which are input only.

AC Characteristics

AC Test Conditions

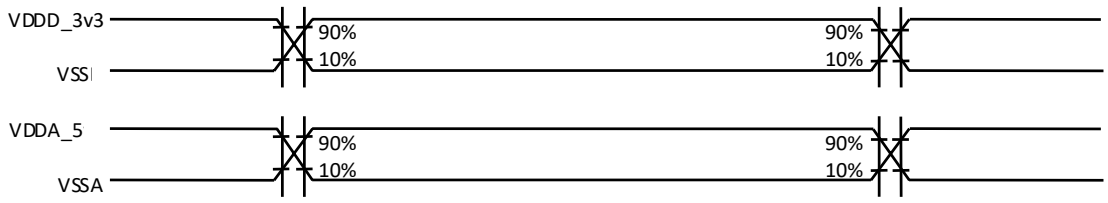
(1) General Conditions

Below conditions are valid for all subsequent AC timing specifications - if not noted otherwise:

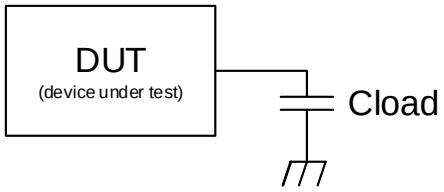
- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: VDDD_3V3 = 3.0 ~ 3.6V
- Operating core supply voltage: VDDD_1V1 = 1.1 ~ 1.2V
- Operating analog IO supply voltage: VDDA_5 = 4.5 ~ 5.5V
- VSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSS = VSS_PLL = 0V.
- Output buffer drive strength of digital IOs: standard.
- Capacitive load connected to output pins is Cload = 20pF, see also definition below (AC Load Definition)

(2) Input and Output Measurement Points

If not stated otherwise, the below given AC timing specification is based on the measurements points as follows:



(3) AC Load Definition

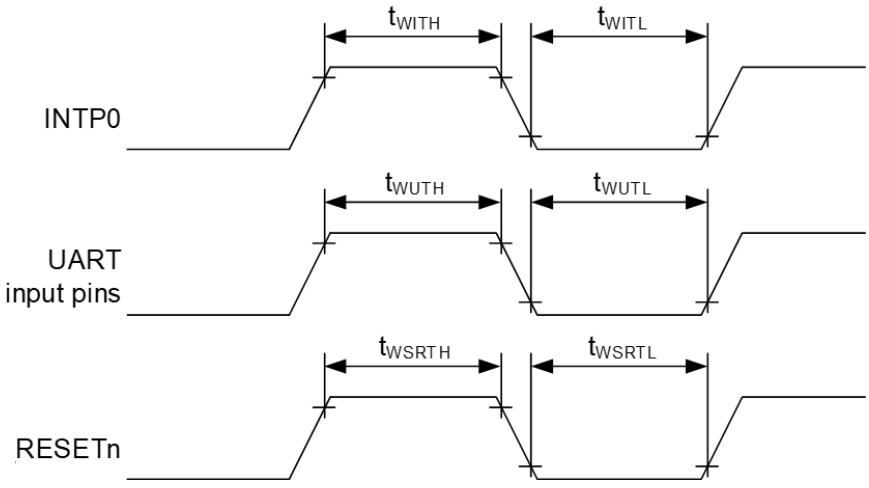


Note: If not otherwise stated in the conditions preceding to below AC timing specifications the following capacitive load condition is valid: Cload = 20pF.

Noise Filter Timing

Note: Conditions for below table: see (1) General Conditions.

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E3	**Interrupt input noise filter timing, pin INTP0 (pin P2_1)**						
E3.1	INTP0 input high level width	tWITH			67		ns
E3.2	INTP0 input low level width	tWITL			67		ns
E3.3	INTP0 pulse rejection width	tWITR			66		ns
E4	**UART input noise filter timing, pins P0_15, P1_06**						
E4.1	P0_15, P1_06 input high level width	tWUTH			500		ns
E4.2	P0_15, P1_06 input low level width	tWUTL			500		ns
E4.3	P0_15, P1_06 pulse rejection width	tWUTR			467		ns
E5	**Reset input noise filter timing, pin RESETn**						
E5.1	RESETn input high level width	tWSRTH			67		ns
E5.2	RESETn input low level width	tWSRTL			67		ns
E5.3	RESETn pulse rejection width	tWSRTR			66		ns
Table Notes: None.							



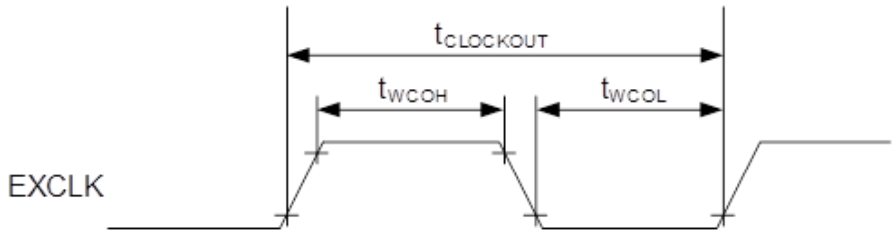
EXCLK Timing

Notes: (1) Following device pin can be used as external clock output (available as alternate pin function):

P0_05: EXCLK

(2) Conditions for below table: see (1) General Conditions

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E6	**EXCLK timing, pin P0_05**						
E6.1	EXCLK period time	tCLKOUT		1			µs
E6.2	EXCLK high-level width	tWCOH			tCLKOUT/2		ns
E6.3	EXCLK low-level width	tWCOL			tCLKOUT/2		ns
Table Notes: None.							



UARTn Timing

Notes: (1) Following device pins can be used as UARTn, n = 0..1 interface (available as alternate pin function):

P1_05: UART0_TXD

P1_05: UART0_RXD

P0_14: UART1_TXD

P0_15: UART1_RXD

(2) Conditions for below table: see (1) General Conditions

The below table applies to the following conditions:

- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: VDDD_3V3 = 3.0 ~ 3.6V
- VSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V.

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E7	**UARTn Timing**						
E7.1	Transfer rate	RRLurt		0.028		625	Kbit/s
Table Notes: None.							

USPI Timing

(1) Master Mode

Notes: (1) Following device pins can be used as USPI interface in master mode (available as alternate pin function):

P1_01: USPI_CLKO

P1_02: USPI_MOSI

P1_03: USPI_MISO

P1_04: USPI_CSO

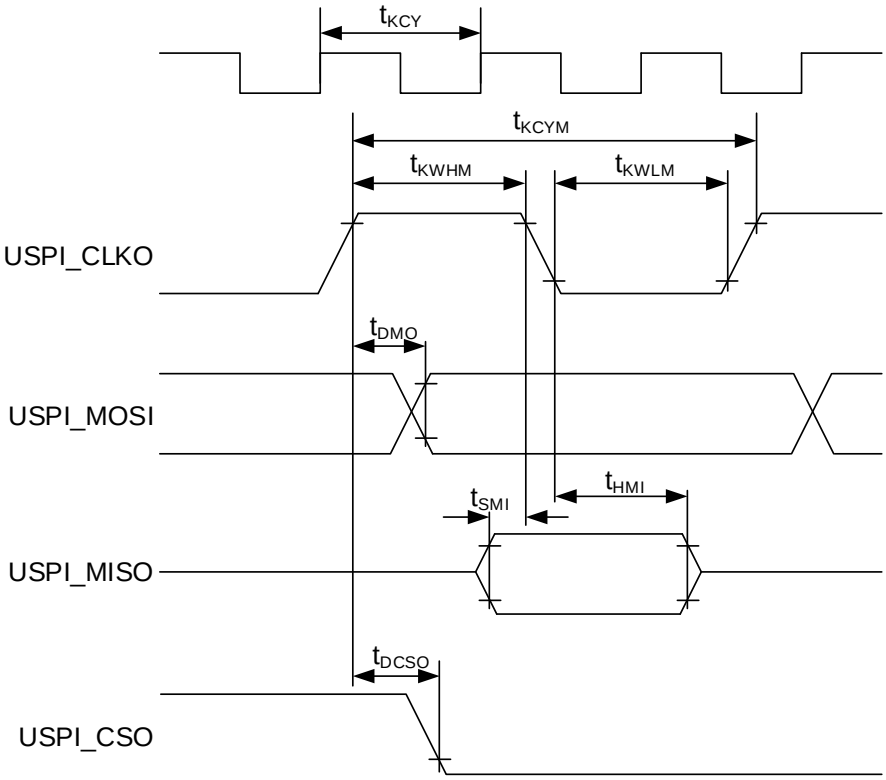
(2) Basic conditions for below tables: see (1) General Conditions. However, in the below given tables some of these conditions are overruled!

The below table applies to the following conditions:

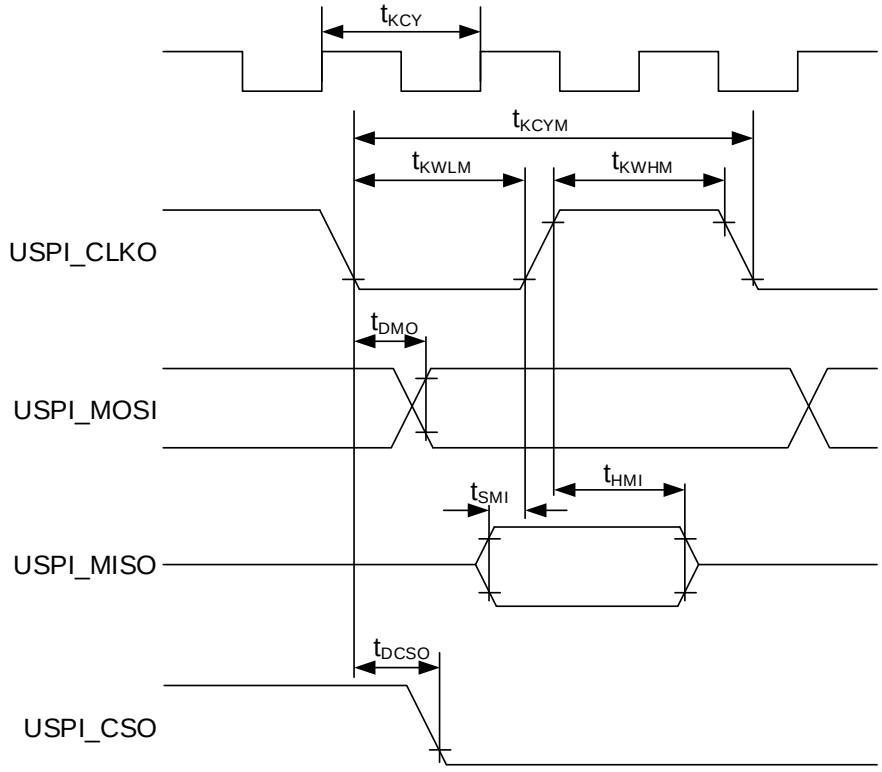
- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: VDDD_3V3 = 3.0 ~ 3.6V
- VSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E8	**USPI Master Mode Timing**						
E8.1	SPI macro cycle time	tKCY	Cond.: Note (e)	8.33			ns
E8.2	USPI_CLKO cycle time	tKCYM	Cond.: Note (e)	50			ns
E8.3	USPI_CLKO high level width	tKWHM	Cond.: Note (e)	5			ns
E8.4	USPI_CLKO low level width	tKWLM	Cond.: Note (e)	5			ns
E8.5	USPI_MISO setup time vs. USPI_CLKO	tSMI	Cond.: Note (e), based on 40%-60% signal levels	17			ns
E8.6	USPI_MISO hold time vs. USPI_CLKO	tHMI	Cond.: Note (e), based on 40%-60% signal levels	0			ns
E8.7	USPI_MOSI output delay time	tDMO	Cond.: Note (e), based on 50%-50% signal levels			10	ns
E8.8	USPI_CSO output delay time	tDCSO	Cond.: Note (e), based on 50%-50% signal levels			10	ns
Table Notes: Note (e) Maximum external load capacitance at output pins: CL = 40pF.							

USPI Master Mode Timing:



USPI Master Mode Timing (Inverted Clock):



(2) Slave Mode (25Mbit/s)

Notes: (1) Following device pins can be used as USPI interface in slave mode (available as alternate pin function):

P1_01: USPI_CLKI

P1_02: USPI_MOSI

P1_03: USPI_MISO

P1_04: USPI_CSI

(2) Basic conditions for below tables: see (1) General Conditions. However, in the below given tables some of these conditions are overruled!

The below table applies to the following conditions:

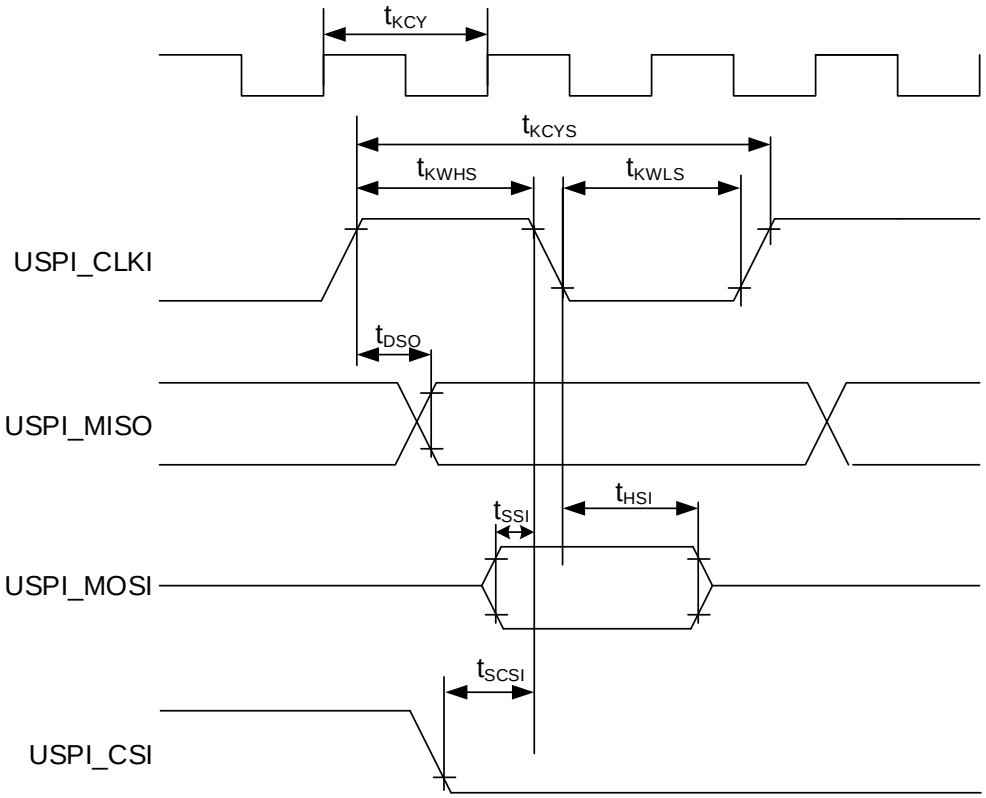
- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: VDDD_3V3 = 3.0 ~ 3.6V
- VSS = VSS_PLL = VSS_OSC = VSSA
- Reference ground potential: VSSA = VSS_OSC = 0V

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E9	**USPI Slave Mode Timing**						
E9.1	SPI macro cycle time	tKCY	Cond.: Note (e)	8.33			ns
E9.2	USPI_CLKI cycle time	tKCYS	Cond.: Note (e)	40			ns
E9.3	USPI_CLKI high level width	tKWHS	Cond.: Note (e)	16			ns
E9.4	USPI_CLKI low level width	tKWLS	Cond.: Note (e)	16			ns
E9.5	USPI_MOSI setup time vs. USPI_CLKI	tSSI	Cond.: Note (e), based on 40%-60% signal levels	1			ns
E9.6	USPI_MOSI hold time vs. USPI_CLKI	tHSI	Cond.: Note (e), based on 40%-60% signal levels	7			ns
E9.7	USPI_MISO output delay time	tDSO	Cond.: Note (e), based on 50%-50% signal levels			8	ns
E9.8	USPI_CSI setup time vs. USPI_CLKI	tSCSI	Cond.: Note (e), based on 50%-50% signal levels	1			ns

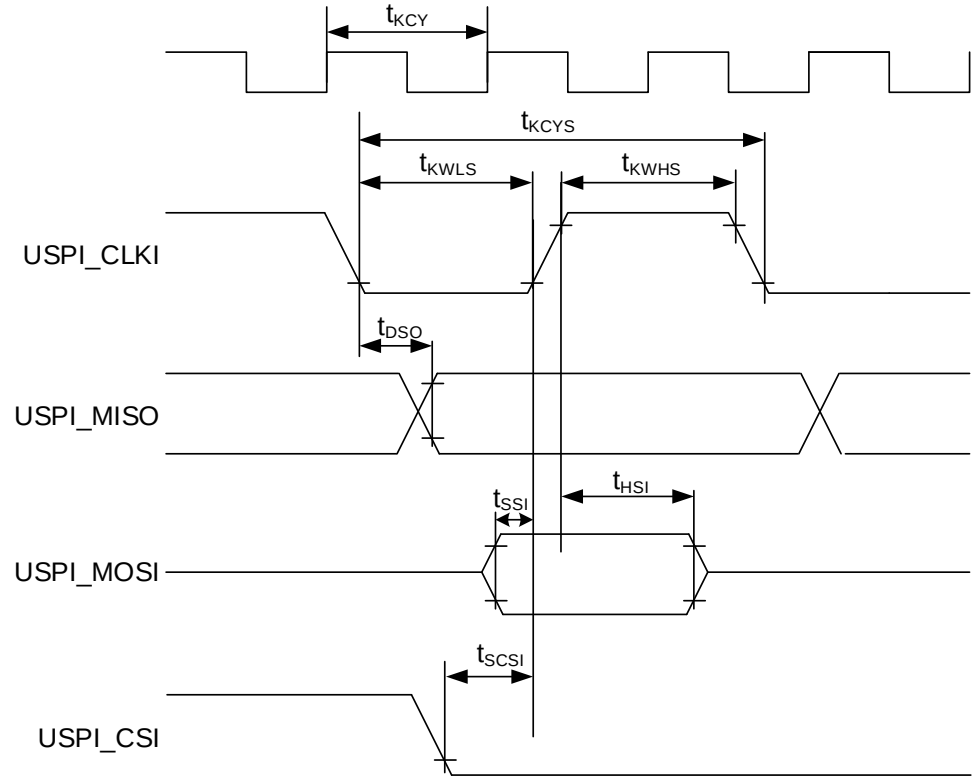
Table Notes:

Note (a) Maximum external load capacitance at output pins: CL = 40pF.

USPI Slave Mode Timing:



USPI Slave Mode Timing (Inverted Clock):



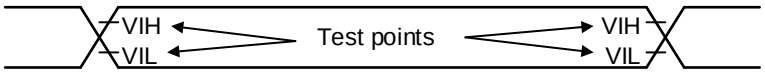
RESET Timing

The below table applies to the following conditions:

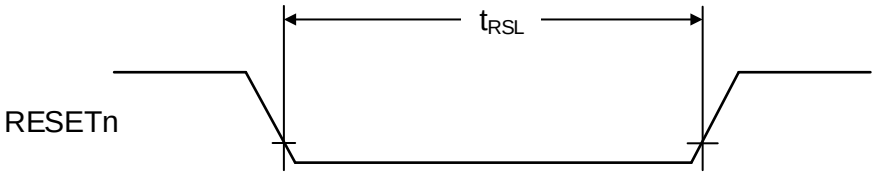
- Ambient temperature range: Ta = –40 ~ 85°C.
- Junction temperature range: see parameter M1.1.
- Operating digital IO supply voltage: RVDD = 3.0 ~ 3.6V
- VSS = RVSS = VSS_PLL = VSS_OSC = VSSA

ID	Parameter	Symbol	Conditions (Cond.) / Comments (Cmt.)	MIN.	TYP.	MAX.	Unit
E10	**RESET timing, pin RESETn**						
E10.1	RESETn low-level width	tRSL		10			µs
Table Notes: None.							

AC Timing Test Points



RESETn Input Timing



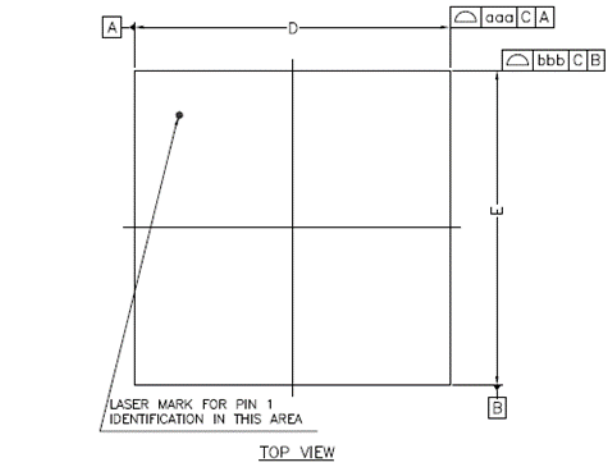
RL78 Programming

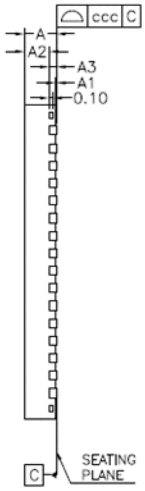
For RL78 flash memory programming the E1 emulator in conjunction with the Renesas Flash Programmer V3 shall be used. Please follow the instructions in the appropriate manuals as listed below.

- **Renesas E1 emulator:** Please download document “E1/E20/E2 Emulator, E2 Emulator Lite” (Doc Number R20UT2937EJ0300) from the Renesas internet.
- **Renesas Flash Programmer:** Please download document “Renesas Flash Programmer V3.05” (Doc Number R20UT4307EJ0200) from the Renesas internet.

Package Dimensions

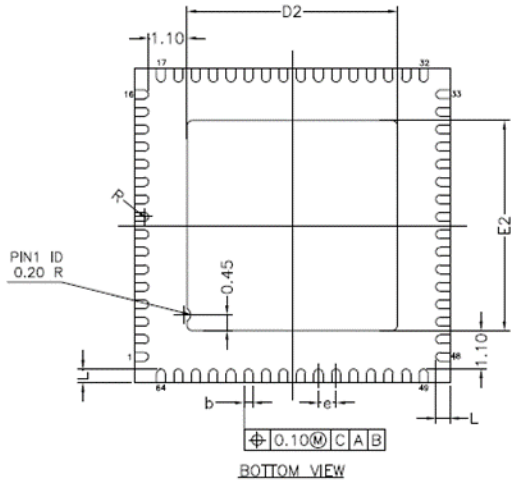
The ASI4U-V5 device features a 64-pin Quad Flat No-lead (QFN) package.
The ball pitch is 0.5 mm. The housing outside dimensions is to 9 X 9 mm.





* CONTROLLING DIMENSION : MM

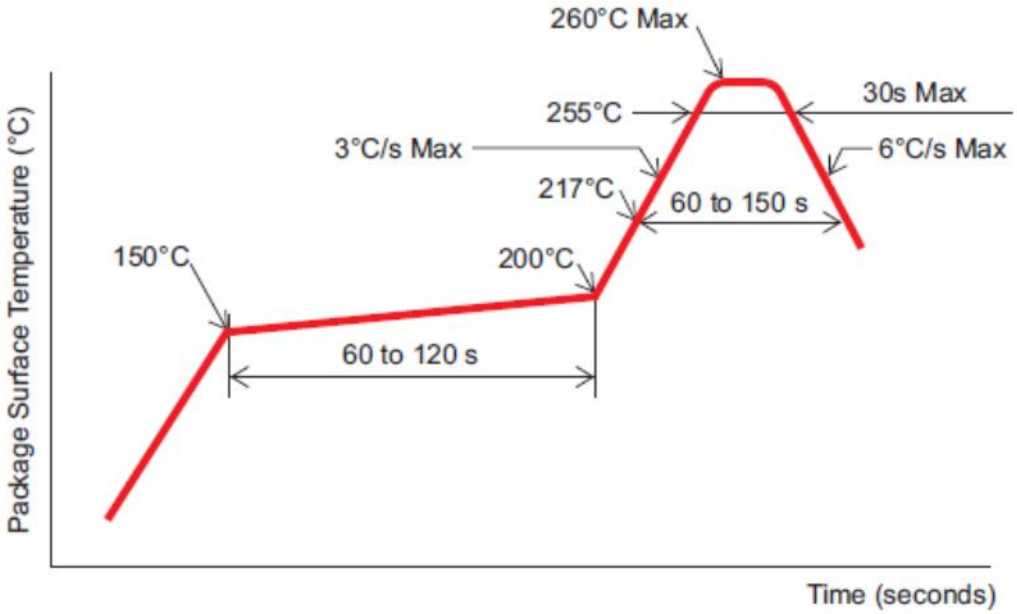
SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	---	---	0.90	---	---	0.035
A1	---	---	0.05	---	---	0.002
A2	---	0.65	0.70	---	0.026	0.028
A3	0.200 REF.			0.008 REF.		
b	0.18	0.25	0.30	0.007	0.010	0.012
D	9.00 bsc			0.354 bsc		
D2	5.90	6.00	6.10	0.232	0.236	0.240
E	9.00 bsc			0.354 bsc		
E2	5.90	6.00	6.10	0.232	0.236	0.240
L	0.35	0.40	0.45	0.014	0.016	0.018
e	0.50 bsc			0.020 bsc		
R	0.09	---	---	0.004	---	---
TOLERANCES OF FORM AND POSITION						
aaa	0.10			0.004		
bbb	0.10			0.004		
ccc	0.05			0.002		



NOTES :
1.ALL DIMENSIONS ARE IN MILLIMETERS.
2.DIE THICKNESS ALLOWABLE IS 0.305 mm MAXIMUM(.012 INCHES MAXIMUM)
3.DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. -1994.
4.THE PIN #1 IDENTIFIER MUST BE PLACED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
5.EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
6.PACKAGE WARPAGE MAX 0.08 mm.
7.APPLIED FOR EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDING PART OF EXPOSED PAD FROM MEASURING.
8.APPLIED ONLY TO TERMINALS.

Recommended Soldering Conditions

Although QFN package products have a thermal resistance of 260°C (maximum) to support lead-free solders as stipulated in JEDEC J-STD 020D, individual products may have a different thermal resistance temperature. Contact your Renesas sales representative for details on individual products.



Revision History

Rev.	Date	Description	
		Page	Summary
0.01	Dec. 18, 2019	-	First Edition issued
0.02	Jan. 23, 2020	2	Pin Arrangement revised
		3 to 4	Pin Description revised
1.00	Dec. 03, 2020	5	Picture in Start-Up Procedure revised
		5	Description of power on behaviour revised
		6	RL78 relationship added in table
		6	RL78 Related Pins Note revised
		7	Added a DG3 sub-pin group 3 definition
		9	Added voltage ratings for RVDD (M3.2)
		9	Added voltage ratings for RREGC (M5.1)
		10	Added voltage ratings for VI_DG3 (M6.6)
		12	Added supply voltage RVDD
		17 to 18	Modified Leakage Current Characteristics (Add leakage current for DF3)
		19	Modified DC Characteristics (add VIH and VIL for DG3)
		29	Added RESET timing

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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