

FEATURES:

- Advanced Memory Buffer for Fully buffered DIMMs
- 3.2 and 4 Gbit/s serial speeds (DDR2-533 and 667 DRAM)
- Support for up to eight DIMMs per channel
- Repeater Mode for extending FB-DIMM links
- Northbound and Southbound single lane fail over and channel error detection
- Voltage and Timing margin high-speed I/O test capability
- Fully Supports the FB-DIMM configuration register set
- Test features supported include:
 - Integrated thermal sensor and status indicator
 - Supports MEMBIST, IBIST and Virtual Host mode
 - Transparent mode and direct access mode for DRAM testing
- Complies with JEDEC Architecture and Protocol Specification
- Available in 655 ball FCBGA package

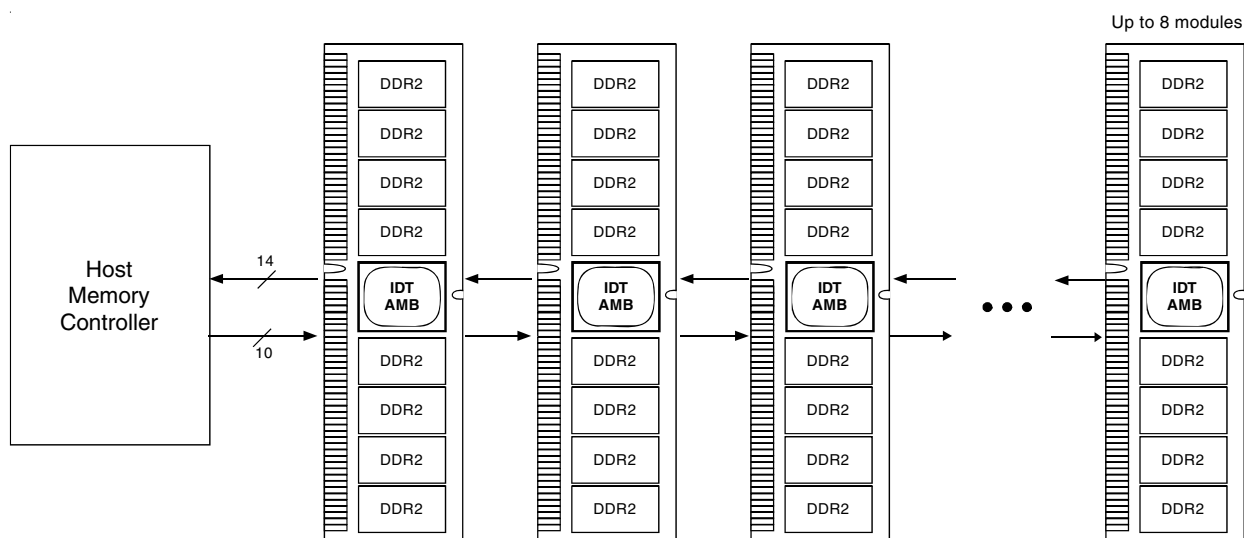
EXPANDED FEATURES:

- Wide range DDR Timing Control
- Superfine adjustment for DDR timing
- Wide range of DDR slew rate control
- Slew rate controllable independent of output impedance
- High speed SMBus in test mode
- IBIST IDT PRBS Generator

DESCRIPTION:

The fully buffered dual in-line memory module (FB-DIMM) is the next generation memory architecture to meet the growing memory requirement of servers and workstations. The IDT Advanced Memory Buffer (AMB) chip is the essential building block located on each FB-DIMM. The IDT AMB receives commands and data from the host controller to control and write/read data to/from the DRAMs on the DIMM. Commands and write data are sent southbound from the host controller to AMBs in a daisy chain fashion and interpreted by the target AMB. Status and read data are sent northbound from AMBs to the host controller also in a daisy chain fashion, passing through non-target AMBs. This unique channel structure alleviates buffer loading issues common in registered DIMM technology, enabling designers to use a large number of DIMMs within a single system.

IDTAMB0480 complies with the latest JEDEC defined FB-DIMM Architecture and Protocol Specification and supports DDR2-533 and DDR2-667 DRAM. It also enables serial data transfer at 3.2 and 4.0Gbps. The IDTAMB0480 supports servers, workstations, storage devices and communication applications that support the next generation FB-DIMM architecture.

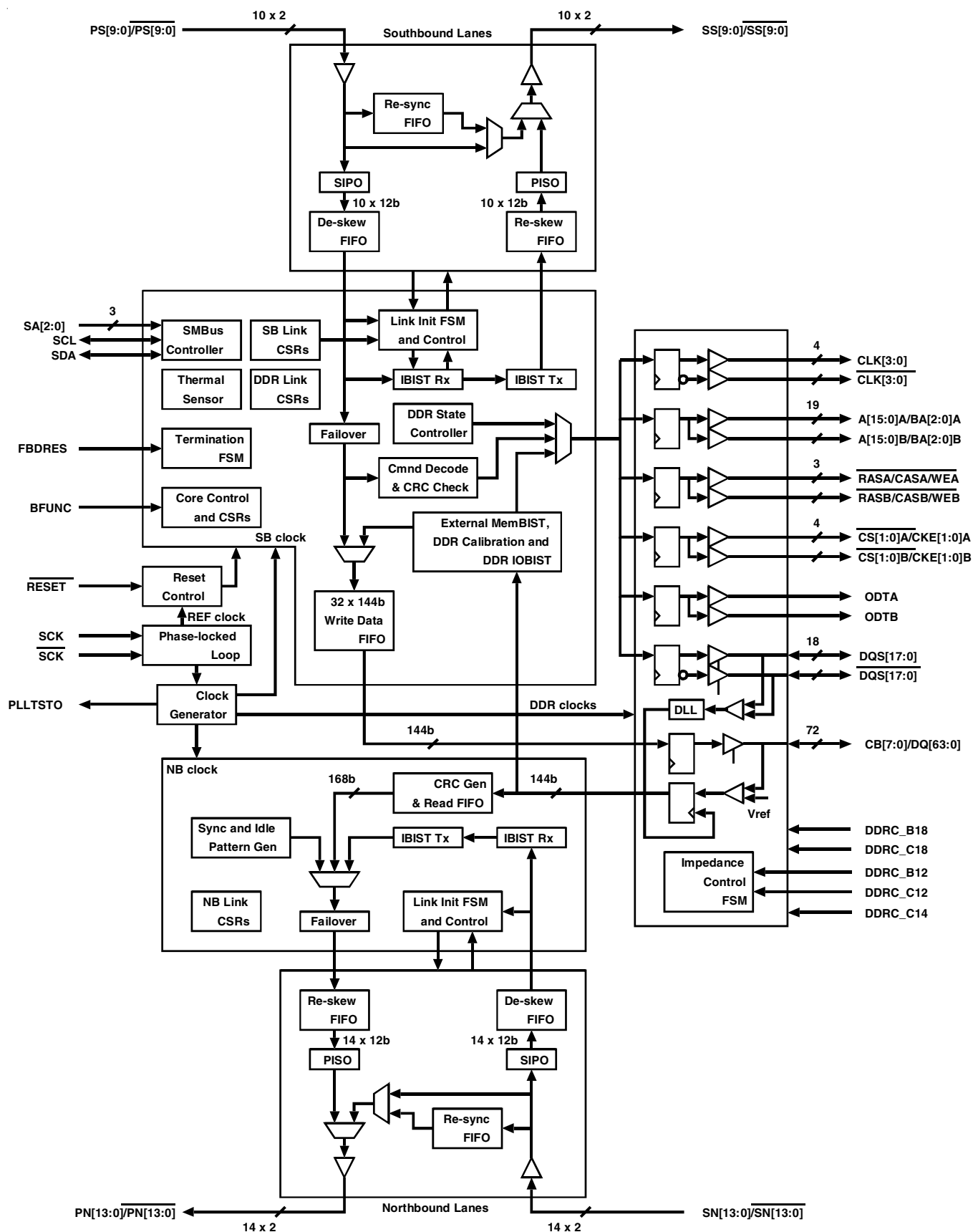
FDB MEMORY CHANNEL


The IDT logo is a registered trademark of Integrated Device Technology, Inc.

COMMERCIAL TEMPERATURE RANGE

APRIL 2006

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
A			VSS	DQ26	DQ12	VDD	DQS ₁₀	DQ13	VDD	DQS ₁	DQ10	VDD	TEST LO	VDD	VDD
B		VDD	DQS3	DQS3	VSS	DQ14	DQS ₁₀	VSS	DQ11	DQS1	VSS	DDRC_B12	TEST LO	VDD	VSS
C	VSS	DQS2	DQ18	VSS	DQ4	DQS9	VSS	DQ15	DQ9	VSS	DQ8	DDRC_C12	VSS	DDRC_C14	DQS ₁₇
D	DQ19	DQS2	VSS	DQ16	DQ24	VSS	DQS9	DQ7	VSS	DQ3	DQS0	VSS	DQS8	DQS8	VDD
E	DQ21	VSS	DQ17	DQ29	VSS	DQ25	DQ6	VSS	DQ5	DQ1	VSS	DQ0	CB1	VSS	CB2
F	VSS	DQ20	DQ23	VSS	DQ31	DQ27	VSS	TEST LO	TEST	VSS	DQS0	DQ2	VDD	CB0	CB3
G	DQS ₁₁	DQS ₁₁	NC	NC	NC	VSS	DQS ₁₂	DQS ₁₂	NC	NC	NC	BFUNC	RFU	RFU	RFU
H	DQ22	VSS	NC	NC	NC	DQ28	DQ30	VSS	NC	NC	NC	VSS	VDD	VSS	VDD
J	VSS	CLK2	NC	NC	NC	BA1A	VSS	CKE _{1A}	NC	NC	NC	VDD	VSS	VDD	VSS
K	CLK2	CLK0	NC	NC	NC	VSS	WEA	RASA	NC	NC	NC	VSS	VCC	VSS	VCC
L	CLK0	VSS	NC	NC	NC	A0A	CKE _{0A}	VSS	NC	NC	NC	VCC	VSS	VCC	VSS
M	ODT _{0A}	RFU	NC	NC	NC	CASA	VSS	BA2A	NC	NC	NC	VSS	VCC	VSS	VCC
N	CS1A	CS0A	NC	NC	NC	VSS	BA0A	A10A	NC	NC	NC	VCC	VSS	VCC	VSS
P	A6A	VSS	NC	NC	NC	A2A	A1A	A3A	NC	NC	NC	VSS	VCC	VSS	VCC
R	VSS	A8A	NC	NC	NC	A11A	VSS	A5A	NC	NC	NC	VCC	VSS	VCC	VSS
T	A4A	A13A	NC	NC	NC	VSS	A9A	A7A	NC	NC	NC	VSS	VCC	VSS	VCC
U	PN0	PN0	NC	NC	NC	A15A	A14A	A12A	NC	NC	NC	RFU	VCC FBD	VSS	VSS
V	PN1	PN1	VSS	SN0	SN0	VCC FBD	VSS	VCC FBD	VSS	RFU ⁽¹⁾	RFU ⁽¹⁾	VCC FBD	VSS	VSS	VSS
W	PN2	PN2	VSS	SN1	SN1	SN3	SN4	SN5	SN13	SN12	SN6	SN7	SN8	SN9	SN10
Y	PN3	PN3	VSS	SN2	SN2	SN3	SN4	SN5	SN13	SN12	SN6	SN7	SN8	SN9	SN10
AA	VSS	PN4	PN4	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS
AB		VSS	RESET	PN5	PN13	RFU ⁽¹⁾	PN12	PN6	PN7	PN8	PN9	VSS APPL	VCC APPL	PN10	PN11
AC			VSS	PN5	PN13	RFU ⁽¹⁾	PN12	PN6	PN7	PN8	PN9	FBD RES	PLL TSTO	PN10	PN11

FCBGA
TOP VIEW, LEFT SIDE

NOTE:

1. These pin positions are reserved for forward clocks to be used in future implementations.

	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A	VDD	TEST	VDD	DQ52	DQS15	VDD	DQ49	$\overline{\text{DQS6}}$	VDD	DQ48	DQ38	VDD		
B	VDD	TEST LO	DDRC _B18	VSS	$\overline{\text{DQS15}}$	DQ53	VSS	DQS6	DQ50	VSS	$\overline{\text{DQS13}}$	DQS13	VSS	
C	$\overline{\text{DQS17}}$	VSS	DDRC _C18	DQ54	VSS	DQ55	DQ51	VSS	DQS7	DQ56	VSS	DQ46	$\overline{\text{DQS14}}$	VDD
D	CB6	CB7	VSS	DQS16	DQ63	VSS	DQ59	$\overline{\text{DQS7}}$	VSS	DQ36	DQ44	VSS	DQS14	DQ47
E	VSS	CB5	$\overline{\text{DQS16}}$	VSS	DQ61	DQ57	VSS	DQ58	DQ39	VSS	DQ33	DQ45	VSS	DQ41
F	CB4	VDD	DQ62	DQ60	VSS	TEST	TEST	VSS	DQ37	DQ35	VSS	$\overline{\text{DQS5}}$	DQ43	VSS
G	TEST LO	RFU	RFU	NC	NC	NC	DQS4	$\overline{\text{DQS4}}$	VSS	NC	NC	NC	DQS5	DQ40
H	VSS	VDD	VSS	NC	NC	NC	VSS	DQ34	DQ32	NC	NC	NC	VSS	DQ42
J	VDD	VSS	VDD	NC	NC	NC	$\overline{\text{RASB}}$	VSS	RFU	NC	NC	NC	$\overline{\text{CLK3}}$	VSS
K	VSS	VCC	VSS	NC	NC	NC	ODT 0B	$\overline{\text{CS1B}}$	VSS	NC	NC	NC	$\overline{\text{CLK1}}$	CLK3
L	VCC	VSS	VCC	NC	NC	NC	VSS	$\overline{\text{CASB}}$	$\overline{\text{WEB}}$	NC	NC	NC	VSS	CLK1
M	VSS	VCC	VSS	NC	NC	NC	$\overline{\text{CS0B}}$	VSS	BA1B	NC	NC	NC	CKE0B	VSS
N	VCC	VSS	VCC	NC	NC	NC	A0B	A2B	VSS	NC	NC	NC	BA0B	BA2B
P	VSS	VCC	VSS	NC	NC	NC	VSS	A4B	A1B	NC	NC	NC	VSS	CKE1B
R	VCC	VSS	VCC	NC	NC	NC	A6B	VSS	A10B	NC	NC	NC	A3B	VSS
T	VSS	VCC	VSS	NC	NC	NC	A11B	A9B	VSS	NC	NC	NC	A7B	A5B
U	VSS	VCC FBD	RFU	NC	NC	NC	A8B	A15B	A14B	SA0	SCL	SDA	$\overline{\text{PS8}}$	PS8
V	VCC FBD	VSS	VCC FBD	VSS	VCC FBD	RFU ⁽¹⁾	RFU ⁽¹⁾	VSS	A13B	A12B	SA2	SA1	$\overline{\text{PS7}}$	PS7
W	VSS	$\overline{\text{SS0}}$	$\overline{\text{SS1}}$	$\overline{\text{SS2}}$	$\overline{\text{SS3}}$	$\overline{\text{SS4}}$	$\overline{\text{SS9}}$	$\overline{\text{SS5}}$	$\overline{\text{SS6}}$	$\overline{\text{SS7}}$	$\overline{\text{SS8}}$	VSS	$\overline{\text{PS6}}$	PS6
Y	VSS	SS0	SS1	SS2	SS3	SS4	SS9	SS5	SS6	SS7	SS8	VSS	$\overline{\text{PS5}}$	PS5
AA	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	$\overline{\text{PS9}}$	PS9	VSS
AB	VSS	$\overline{\text{SN11}}$	VSS	SCK	TESTLO _AB20	$\overline{\text{PS0}}$	$\overline{\text{PS1}}$	$\overline{\text{PS2}}$	$\overline{\text{PS3}}$	$\overline{\text{PS4}}$	RFU ⁽¹⁾	VDD SPD	VSS	
AC	RFU	SN11	VSS	$\overline{\text{SCK}}$	TESTLO _AC20	PS0	PS1	PS2	PS3	PS4	RFU ⁽¹⁾	VSS		

FCBGA
TOP VIEW, RIGHT SIDE

NOTE:

1. These pin positions are reserved for forward clocks to be used in future implementations.

655 BALL BGA PACKAGE ATTRIBUTES

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
A		○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
B	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
C	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
D	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
E	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
F	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
G	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
H	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
J	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
K	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
L	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
M	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
N	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
P	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
R	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
T	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
U	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
V	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
W	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
Y	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AA	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AB		○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○
AC			○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○	○

ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER

Ball No.	Signal
A3	V _{SS}
A4	DQ26
A5	DQ12
A6	V _{DD}
A7	DQS10
A8	DQ13
A9	V _{DD}
A10	$\overline{\text{DQS}}1$
A11	DQ10
A12	V _{DD}
A13	TESTLO
A14	V _{DD}
A15	V _{DD}
A16	V _{DD}
A17	TEST
A18	V _{DD}
A19	DQ52
A20	DQS15
A21	V _{DD}
A22	DQ49
A23	$\overline{\text{DQS}}6$
A24	V _{DD}
A25	DQ48
A26	DQ38
A27	V _{DD}
B2	V _{DD}
B3	DQS3
B4	$\overline{\text{DQS}}3$
B5	V _{SS}
B6	DQ14
B7	$\overline{\text{DQS}}10$
B8	V _{SS}
B9	DQ11
B10	DQS1
B11	V _{SS}
B12	DDRC_B12
B13	TESTLO
B14	V _{DD}
B15	V _{SS}
B16	V _{DD}
B17	TESTLO
B18	DDRC_B18
B19	V _{SS}
B20	$\overline{\text{DQS}}15$
B21	DQ53
B22	V _{SS}
B23	DQS6
B24	DQ50
B25	V _{SS}

Ball No.	Signal
B26	$\overline{\text{DQS}}13$
B27	DQS13
B28	V _{SS}
C1	V _{SS}
C2	DQS2
C3	DQ18
C4	V _{SS}
C5	DQ4
C6	$\overline{\text{DQS}}9$
C7	V _{SS}
C8	DQ15
C9	DQ9
C10	V _{SS}
C11	DQ8
C12	DDRC_C12
C13	V _{SS}
C14	DDRC_C14
C15	DQS17
C16	$\overline{\text{DQS}}17$
C17	V _{SS}
C18	DDRC_C18
C19	DQ54
C20	V _{SS}
C21	DQ55
C22	DQ51
C23	V _{SS}
C24	DQS7
C25	DQ56
C26	V _{SS}
C27	DQ46
C28	$\overline{\text{DQS}}14$
C29	V _{DD}
D1	DQ19
D2	$\overline{\text{DQS}}2$
D3	V _{SS}
D4	DQ16
D5	DQ24
D6	V _{SS}
D7	DQS9
D8	DQ7
D9	V _{SS}
D10	DQ3
D11	DQS0
D12	V _{SS}
D13	$\overline{\text{DQS}}8$
D14	DQS8
D15	V _{DD}
D16	CB6
D17	CB7

Ball No.	Signal
D18	V _{SS}
D19	DQS16
D20	DQ63
D21	V _{SS}
D22	DQ59
D23	$\overline{\text{DQS}}7$
D24	V _{SS}
D25	DQ36
D26	DQ44
D27	V _{SS}
D28	DQS14
D29	DQ47
E1	DQ21
E2	V _{SS}
E3	DQ17
E4	DQ29
E5	V _{SS}
E6	DQ25
E7	DQ6
E8	V _{SS}
E9	DQ5
E10	DQ1
E11	V _{SS}
E12	DQ0
E13	CB1
E14	V _{SS}
E15	CB2
E16	V _{SS}
E17	CB5
E18	$\overline{\text{DQS}}16$
E19	V _{SS}
E20	DQ61
E21	DQ57
E22	V _{SS}
E23	DQ58
E24	DQ39
E25	V _{SS}
E26	DQ33
E27	DQ45
E28	V _{SS}
E29	DQ41
F1	V _{SS}
F2	DQ20
F3	DQ23
F4	V _{SS}
F5	DQ31
F6	DQ27
F7	V _{SS}
F8	TESTLO

Ball No.	Signal
F9	TEST
F10	V _{SS}
F11	$\overline{\text{DQS}}0$
F12	DQ2
F13	V _{DD}
F14	CB0
F15	CB3
F16	CB4
F17	V _{DD}
F18	DQ62
F19	DQ60
F20	V _{SS}
F21	TEST
F22	TEST
F23	V _{SS}
F24	DQ37
F25	DQ35
F26	V _{SS}
F27	$\overline{\text{DQS}}5$
F28	DQ43
F29	V _{SS}
G1	$\overline{\text{DQS}}11$
G2	DQS11
G3	NC
G4	NC
G5	NC
G6	V _{SS}
G7	DQS12
G8	$\overline{\text{DQS}}12$
G9	NC
G10	NC
G11	NC
G12	BFUNC
G13	RFU
G14	RFU
G15	RFU
G16	TESTLO
G17	RFU
G18	RFU
G19	NC
G20	NC
G21	NC
G22	DQS4
G23	$\overline{\text{DQS}}4$
G24	V _{SS}
G25	NC
G26	NC
G27	NC
G28	DQS5

ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER (CONT.)

Ball No.	Signal	Ball No.	Signal	Ball No.	Signal	Ball No.	Signal
G29	DQ40	J20	NC	L11	NC	N2	CS0A
H1	DQ22	J21	NC	L12	Vcc	N3	NC
H2	Vss	J22	RASB	L13	Vss	N4	NC
H3	NC	J23	Vss	L14	Vcc	N5	NC
H4	NC	J24	RFU	L15	Vss	N6	Vss
H5	NC	J25	NC	L16	Vcc	N7	BA0A
H6	DQ28	J26	NC	L17	Vss	N8	A10A
H7	DQ30	J27	NC	L18	Vcc	N9	NC
H8	Vss	J28	CLK3	L19	NC	N10	NC
H9	NC	J29	Vss	L20	NC	N11	NC
H10	NC	K1	CLK2	L21	NC	N12	Vcc
H11	NC	K2	CLK0	L22	Vss	N13	Vss
H12	Vss	K3	NC	L23	CASB	N14	Vcc
H13	VDD	K4	NC	L24	WEB	N15	Vss
H14	Vss	K5	NC	L25	NC	N16	Vcc
H15	VDD	K6	Vss	L26	NC	N17	Vss
H16	Vss	K7	WEA	L27	NC	N18	Vcc
H17	VDD	K8	RASA	L28	Vss	N19	NC
H18	Vss	K9	NC	L29	CLK1	N20	NC
H19	NC	K10	NC	M1	ODT0A	N21	NC
H20	NC	K11	NC	M2	RFU	N22	A0B
H21	NC	K12	Vss	M3	NC	N23	A2B
H22	Vss	K13	Vcc	M4	NC	N24	Vss
H23	DQ34	K14	Vss	M5	NC	N25	NC
H24	DQ32	K15	Vcc	M6	CASA	N26	NC
H25	NC	K16	Vss	M7	Vss	N27	NC
H26	NC	K17	Vcc	M8	BA2A	N28	BA0B
H27	NC	K18	Vss	M9	NC	N29	BA2B
H28	Vss	K19	NC	M10	NC	P1	A6A
H29	DQ42	K20	NC	M11	NC	P2	Vss
J1	Vss	K21	NC	M12	Vss	P3	NC
J2	CLK2	K22	ODT0B	M13	Vcc	P4	NC
J3	NC	K23	CS1B	M14	Vss	P5	NC
J4	NC	K24	Vss	M15	Vcc	P6	A2A
J5	NC	K25	NC	M16	Vss	P7	A1A
J6	BA1A	K26	NC	M17	Vcc	P8	A3A
J7	Vss	K27	NC	M18	Vss	P9	NC
J8	CKE1A	K28	CLK1	M19	NC	P10	NC
J9	NC	K29	CLK3	M20	NC	P11	NC
J10	NC	L1	CLK0	M21	NC	P12	Vss
J11	NC	L2	Vss	M22	CS0B	P13	Vcc
J12	VDD	L3	NC	M23	Vss	P14	Vss
J13	Vss	L4	NC	M24	BA1B	P15	Vcc
J14	VDD	L5	NC	M25	NC	P16	Vss
J15	Vss	L6	A0A	M26	NC	P17	Vcc
J16	VDD	L7	CKE0A	M27	NC	P18	Vss
J17	Vss	L8	Vss	M28	CKE0B	P19	NC
J18	VDD	L9	NC	M29	Vss	P20	NC
J19	NC	L10	NC	N1	CS1A	P21	NC

ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER (CONT.)

Ball No.	Signal
P22	Vss
P23	A4B
P24	A1B
P25	NC
P26	NC
P27	NC
P28	Vss
P29	CKE1B
R1	Vss
R2	A8A
R3	NC
R4	NC
R5	NC
R6	A11A
R7	Vss
R8	A5A
R9	NC
R10	NC
R11	NC
R12	Vcc
R13	Vss
R14	Vcc
R15	Vss
R16	Vcc
R17	Vss
R18	Vcc
R19	NC
R20	NC
R21	NC
R22	A6B
R23	Vss
R24	A10B
R25	NC
R26	NC
R27	NC
R28	A3B
R29	Vss
T1	A4A
T2	A13A
T3	NC
T4	NC
T5	NC
T6	Vss
T7	A9A
T8	A7A
T9	NC
T10	NC
T11	NC

Ball No.	Signal
T12	Vss
T13	Vcc
T14	Vss
T15	Vcc
T16	Vss
T17	Vcc
T18	Vss
T19	NC
T20	NC
T21	NC
T22	A11B
T23	A9B
T24	Vss
T25	NC
T26	NC
T27	NC
T28	A7B
T29	A5B
U1	PN0
U2	PN0
U3	NC
U4	NC
U5	NC
U6	A15A
U7	A14A
U8	A12A
U9	NC
U10	NC
U11	NC
U12	RFU
U13	VccFBD
U14	Vss
U15	Vss
U16	Vss
U17	VccFBD
U18	RFU
U19	NC
U20	NC
U21	NC
U22	A8B
U23	A15B
U24	A14B
U25	SA0
U26	SCL
U27	SDA
U28	PS8
U29	PS8
V1	PN1

Ball No.	Signal
V2	PN1
V3	Vss
V4	SN0
V5	SN0
V6	VccFBD
V7	Vss
V8	VccFBD
V9	Vss
V10	RFU ⁽¹⁾
V11	RFU ⁽¹⁾
V12	VccFBD
V13	Vss
V14	Vss
V15	Vss
V16	VccFBD
V17	Vss
V18	VccFBD
V19	Vss
V20	VccFBD
V21	RFU ⁽¹⁾
V22	RFU ⁽¹⁾
V23	Vss
V24	A13B
V25	A12B
V26	SA2
V27	SA1
V28	PS7
V29	PS7
W1	PN2
W2	PS2
W3	Vss
W4	SN1
W5	SN1
W6	SN3
W7	SN4
W8	SN5
W9	SN13
W10	SN12
W11	SN6
W12	SN7
W13	SN8
W14	SN9
W15	SN10
W16	Vss
W17	SS0
W18	SS1
W19	SS2
W20	SS3

Ball No.	Signal
W21	SS4
W22	SS9
W23	SS5
W24	SS6
W25	SS7
W26	SS8
W27	Vss
W28	PS6
W29	PS6
Y1	PN3
Y2	PN3
Y3	Vss
Y4	SN2
Y5	SN2
Y6	SN3
Y7	SN4
Y8	SN5
Y9	SN13
Y10	SN12
Y11	SN6
Y12	SN7
Y13	SN8
Y14	SN9
Y15	SN10
Y16	Vss
Y17	SS0
Y18	SS1
Y19	SS2
Y20	SS3
Y21	SS4
Y22	SS9
Y23	SS5
Y24	SS6
Y25	SS7
Y26	SS8
Y27	Vss
Y28	PS5
Y29	PS5
AA1	Vss
AA2	PN4
AA3	PN4
AA4	Vss
AA5	Vss
AA6	Vss
AA7	Vss
AA8	Vss
AA9	Vss
AA10	Vss

NOTE:

1. These pin positions are reserved for forward clocks to be used in future implementations.

ADVANCED MEMORY BUFFER SIGNALS BY BALL NUMBER (CONT.)

Ball No.	Signal
AA11	V _{SS}
AA12	V _{SS}
AA13	V _{SS}
AA14	V _{SS}
AA15	V _{SS}
AA16	V _{SS}
AA17	V _{SS}
AA18	V _{SS}
AA19	V _{SS}
AA20	V _{SS}
AA21	V _{SS}
AA22	V _{SS}
AA23	V _{SS}
AA24	V _{SS}
AA25	V _{SS}
AA26	V _{SS}
AA27	$\overline{\text{PS}}_9$
AA28	PS ₉
AA29	V _{SS}
AB2	V _{SS}
AB3	$\overline{\text{RESET}}$
AB4	$\overline{\text{PN}}_5$
AB5	$\overline{\text{PN}}_{13}$
AB6	RFU ⁽¹⁾
AB7	$\overline{\text{PN}}_{12}$
AB8	$\overline{\text{PN}}_6$
AB9	$\overline{\text{PN}}_7$
AB10	$\overline{\text{PN}}_8$
AB11	$\overline{\text{PN}}_9$
AB12	V _{SSA} PLL
AB13	V _{CCA} PLL
AB14	$\overline{\text{PN}}_{10}$
AB15	$\overline{\text{PN}}_{11}$
AB16	V _{SS}
AB17	$\overline{\text{PN}}_{11}$
AB18	V _{SS}
AB19	SCK
AB20	TESTLO_AB20
AB21	$\overline{\text{PS}}_0$
AB22	$\overline{\text{PS}}_1$
AB23	$\overline{\text{PS}}_2$
AB24	$\overline{\text{PS}}_3$
AB25	PS ₄
AB26	RFU ⁽¹⁾
AB27	V _{DD} SPD
AB28	V _{SS}
AC3	V _{SS}
AC4	PN ₅

Ball No.	Signal
AC5	PN ₁₃
AC6	RFU ⁽¹⁾
AC7	PN ₁₂
AC8	PN ₆
AC9	PN ₇
AC10	PN ₈
AC11	PN ₉
AC12	FBDRES
AC13	PLLTSTO
AC14	PN ₁₀
AC15	PN ₁₁
AC16	RFU
AC17	SN ₁₁
AC18	V _{SS}
AC19	$\overline{\text{SCK}}$
AC20	TESTLO_AC20
AC21	PS ₀
AC22	PS ₁
AC23	PS ₂
AC24	PS ₃
AC25	PS ₄
AC26	RFU ⁽¹⁾
AC27	V _{SS}

NOTE:

1. These pin positions are reserved for forward clocks to be used in future implementations.

PIN DESCRIPTION

Signal	Type	Description
Channel Interface		
PN[13:0]	O	Northbound Output Data: High speed serial signal. Read path from AMB toward host on primary side of the DIMM connector.
$\overline{\text{PN}}[13:0]$	O	Northbound Output Data Complement
SN[13:0]	I	Northbound Input Data: High speed serial signal. Read path from the previous AMB toward this AMB on secondary side of the DIMM connector.
$\overline{\text{SN}}[13:0]$	I	Northbound Input Data Complement
PS[9:0]	I	Southbound Input Data: High speed serial signal. Write path from host toward AMB on primary side of the DIMM connector.
$\overline{\text{PS}}[9:0]$	I	Southbound Input Data Complement
SS[9:0]	O	Southbound Output Data: High speed serial signal. Write path from this AMB toward next AMB on secondary side of the DIMM connector. These output buffers are disabled for the last AMB on the channel.
$\overline{\text{SS}}[9:0]$	O	Southbound Output Data Complement
FBDRES	A	External 100 Ω precision resistor connected to Vcc. On-die termination calibrated against this resistor.
DRAM Interface		
CB[7:0]	I/O	Check bits
DQ[63:0]	I/O	Data
DQS[17:0]	I/O	Data Strobe: DDR2 data and check-bit strobe.
$\overline{\text{DQS}}[17:0]$	I/O	Data Strobe Complement: DDR2 data and check-bit strobe complements.
A0A-A15A, A0B-A15B	O	Address: Used for providing multiplexed row and column address to SDRAM.
BA0A-BA2A, BA0B-BA2B	O	Bank Active: Used to select the bank within a rank.
$\overline{\text{RASA}}$, $\overline{\text{RASB}}$	O	Row Address Strobe: Used with $\overline{\text{CS}}$, $\overline{\text{CAS}}$, and $\overline{\text{WE}}$ to specify the SDRAM command.
$\overline{\text{CASA}}$, $\overline{\text{CASB}}$	O	Column Address Strobe: Used with $\overline{\text{CS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ to specify the SDRAM command.
$\overline{\text{WEA}}$, $\overline{\text{WEB}}$	O	Write Enable: Used with $\overline{\text{CS}}$, $\overline{\text{CAS}}$, and $\overline{\text{RAS}}$ to specify the SDRAM command.
$\overline{\text{CS0A}}\text{-}\overline{\text{CS1A}}$, $\overline{\text{CS0B}}\text{-}\overline{\text{CS1B}}$	O	Chip Select: Used with $\overline{\text{CAS}}$, $\overline{\text{RAS}}$, and $\overline{\text{WE}}$ to specify the SDRAM command. These signals are used for selecting one of two SDRAM ranks. CS0 is used to select the first rank and CS1 is used to select the second rank.
CKE0A-CKE1A, CKE0B-CKE1B	O	Clock Enable: DIMM command register enable.
ODT0A, ODT0B	O	DIMM On-Die Termination: Dynamic ODT enables for each DIMM on the channel.
CLK[3:0]	O	Clock: Clocks to DRAMs. CLK0 and CLK1 are always used. CLK2 and CLK3 are used when the AMB is configured for dual rank DIMMs.
$\overline{\text{CLK}}[3:0]$	O	Clock Complement: Clocks to DRAMs.
DDR Compensation		
DDRC_C14	A	DDR Compensation Common: Common return (ground) pin for DDRC_B18 and DDRC_C18
DDRC_B18	A	DDR Compensation Ball Resistor (825 Ω) connected to Compensation Common above
DDRC_C18	A	DDR Compensation Ball Resistor (121 Ω) connected to Compensation Common above
DDRC_B12	A	DDR Compensation Ball Resistor (82 Ω) connected to Vss
DDRC_C12	A	DDR Compensation Ball Resistor (82 Ω) connected to VDD

PIN DESCRIPTION (CONT.)

Signal	Type	Description
Clocking		
SCK	I	AMB Clock: This is one of the two differential reference clock inputs to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
$\overline{\text{SCK}}$	I	AMB Clock Complement: This is the other differential reference clock input to the Phase Locked Loop in the AMB core. Phase Locked Loops in the AMB will shift this to all frequencies required by the core, DDR channels, and FBD Channel.
PLLTSTO	O	PLL Clock Observability Output: This pin can be used to observe VCO, reference clock, core clock, etc. For system debug and design characterization.
VccA PLL	A	Vcc: PLL Analog Voltage for the core PLL
VssA PLL	A	Vss: PLL Analog Voltage for the core PLL
System Management		
SCL	I/O	SMBus Clock
SDA	I/O	SMBus Address/Data
SA[2:0]		DIMM Select ID
Reset		
RESET		Power Good Reset
Miscellaneous Test		
TEST (4 pins)	N C	Pin for debug and test. Must be floated on DIMM.
TESTLO (5 pins)	A	Pin for debug and test. Must be tied to Ground on DIMM
TESTLO_AB20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VccFBD, the other resistor is connected to Vss.
TESTLO_AC20	A	Pin for debug and test. Connected to two resistors. One resistor is connected to VccFBD, the other resistor is connected to Vss.
Power Supplies		
Vcc (24 pins)	A	1.5V nominal supply for core I/O
VccFBD (8 pins)	A	1.5V nominal supply for FBD high speed I/O
VDD (24 pins)	A	1.8V nominal supply for DDR I/O
Vss (156 pins)	A	Ground
VDDSPD	A	3.3V nominal supply for SMB receivers and ESD diodes
Other Pins		
BFUNC	I	Buffer Function Bit: When BFUNC = 0, AMB is used as a regular buffer on FBDIMM. When BFUNC = 1, AMB is used as either a repeater or a buffer for LAI function. On FB-DIMM, BFUNC is tied to Ground
RFU (18 pins)	N C	Reserved for Future Use. Must be floated on DIMM. RFU pins denoted by "a" are reserved for forwarded clocks in future AMB implementations.
Other No Connect Pins		
NC (129 pins)	N C	No Connect pins

ELECTRICAL, POWER, AND THERMAL

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Min	Max	Unit
V _{DD}	Supply voltage DRAM Interface	-0.5	+2.3	V
V _{IN} (DDR2), V _{OUT} (DDR2)	Voltage on any DDR2 interface pin relative to V _{SS} ⁽²⁾	0.5	+2.3	V
I _{INK}	Input Clamp Current (V _{IN} < 0 or V _{IN} > V _{DD})		+30	mA
I _{OUTK}	Output Clamp Current (V _{OUT} < 0 or V _{OUT} > V _{DD})		+30	mA
I _{OUT}	Continuous Output Current (V _{OUT} = 0 to V _{DD})		+30	mA
N/A	Continuous current through each V _{DD} or GND		+100	mA
V _{CC}	Supply voltage for Core and High Speed Interface	-0.3	+1.75	V
T _J	Junction Temperature		+125	°C
T _{STG}	Storage Temperature Range	-55	+100	°C

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed. This value is limited to 2.3V maximum.

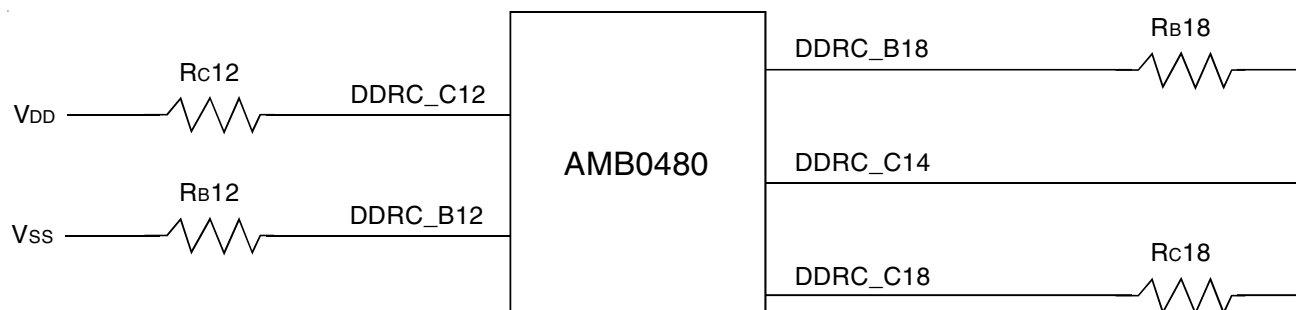
ADVANCED MEMORY BUFFER NORMAL MODE DC ELECTRICAL PARAMETERS

Parameter	Min	Typ	Max	Unit
V _{CC} link / core ^(1,2,3,4)	1.425	1.5	1.59	V
V _{DD}	1.7	1.8	1.9	V
V _{DDSPD}	3.0	3.3	3.6	V

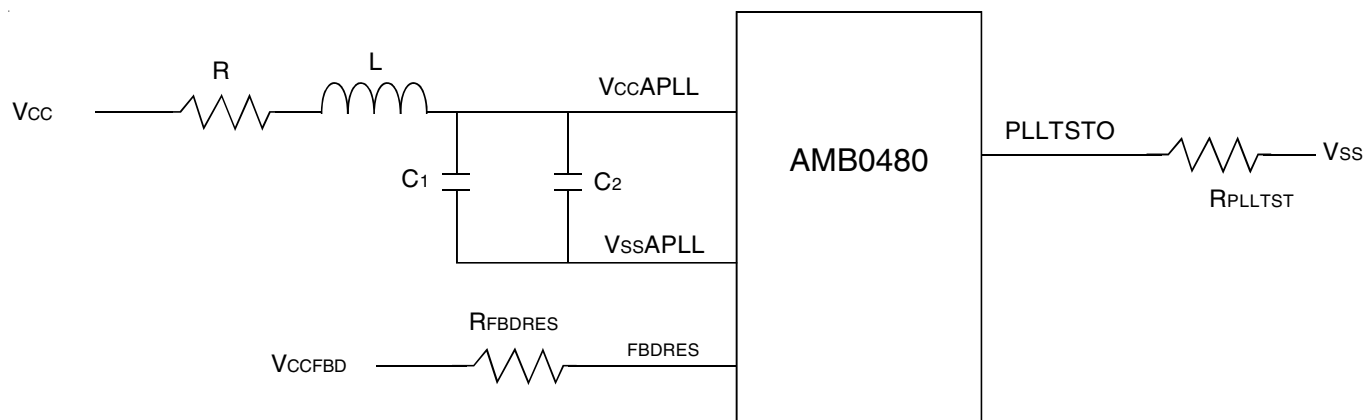
NOTES:

- AMB 1.5V voltage regulation as measured at the package Balls.
- DC defined as 0 KHz to 30 KHz.
- DC + AC specified as 1.5V +6%, -5% 30KHz to 1 MHz.
- There is also a +7%, -5% tolerance allowed for current load steps associated with initialization/error-recovery state transitions, such as into and out of EI, IBIST, and MEMBIST. For these transitions, a temporary voltage overshoot is expected and acceptable as long as it is within +7% (step transition for 20μs and maximum duty cycle of 10⁻⁶ %). Transitions between Active and Idle states are not included in this +7%, -5% tolerance.

DDR BIAS



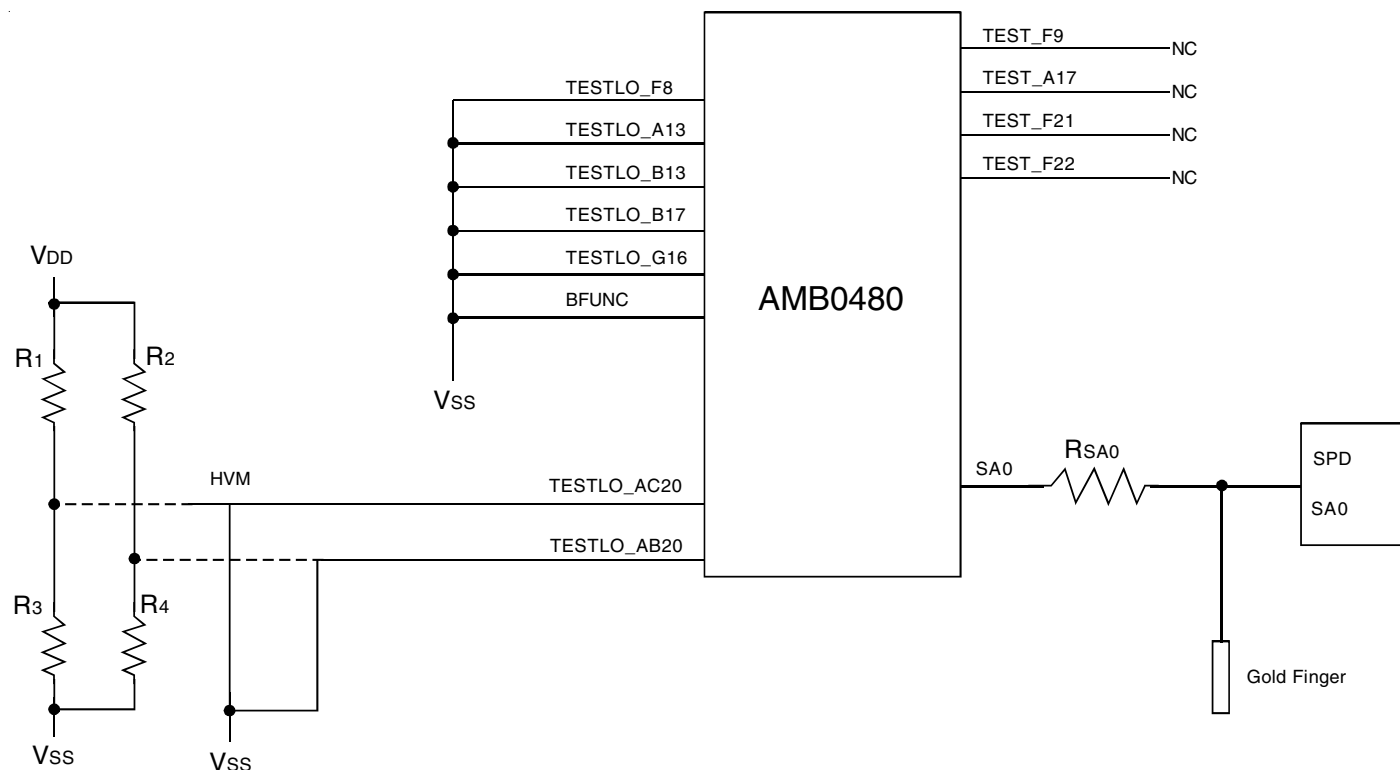
PLL AND CHANNEL BIAS



NOTES:

1. Refer to JEDEC PC2-4200/5300/6400 DDR2 FULLY BUFFERED DIMM DESIGN SPECIFICATIONS, rev 2.0.
2. The resistor R must be 0Ω and the inductor L needs to be replaced with a 0Ω resistor. The resistor RFBDRS = 100Ω and Resistor RPLLST = 51Ω.
3. It is not recommended to use a serpentine copper trace in place of the resistor R. This resistor value needs to be AMB manufacturer defined and not set to a single fixed value. Some raw cards have implemented the resistor with a serpentine copper trace on the DIMM PCB, while others use a discrete resistor. The limitation of using the copper trace has been discussed in JEDEC, highlighting that the resistor implemented as a serpentine copper trace is not a generic solution. The raw card artwork now allows the option of bypassing any serpentine trace with a 0Ω resistor to Vcc.

MISCELLANEOUS BIAS



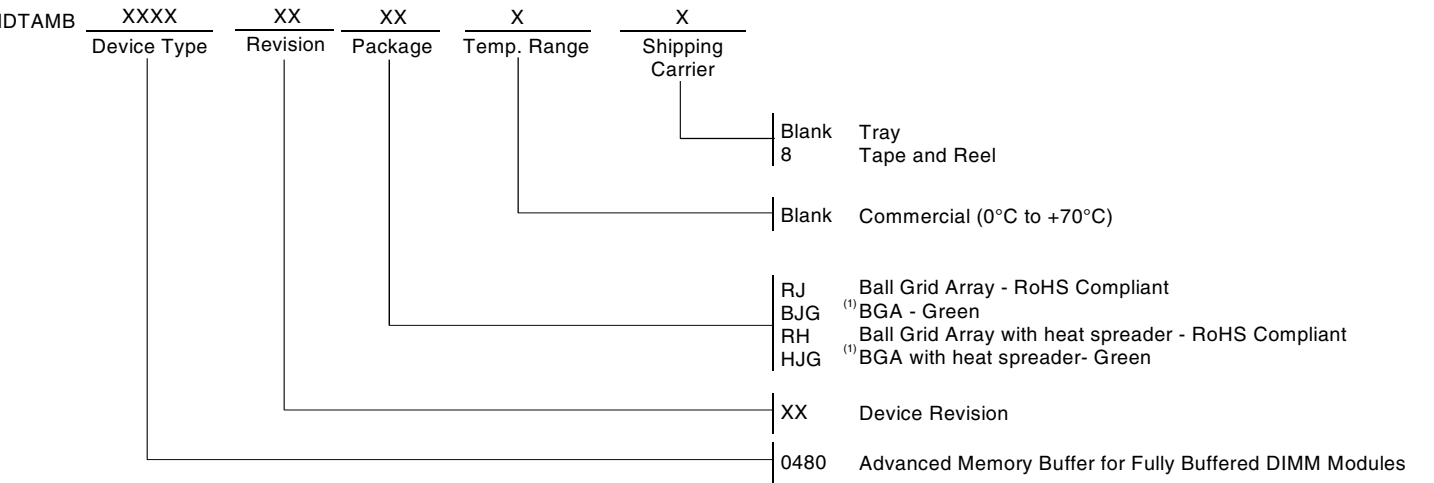
NOTES:

1. Refer to JEDEC PC2-4200/5300/6400 DDR2 FULLY BUFFERED DIMM DESIGN SPECIFICATIONS, rev 2.0.
2. Component values for the AMB0480 are summarized in the BIAS COMPONENT table.

BIAS COMPONENTS - RECOMMENDED VALUES AMB0480

Schematic Diagram	Reference	Value	Description
DDR Bias	RC12	82Ω	The impedance of the pull up (PRU) and pull down (PRD) on the AMB DDR Outputs is related to RB12 & RC12 as follows: $RC12 = RB12 = 5.3125 * \text{Desired Output Impedance}$ A resistor value of 82Ω results in an impedance at a JEDEC nominal value of 15Ω. The user can adjust these value to optimize the DDR output impedance for a DIMM raw card configuration.
	RB12	82Ω	
	RB18	825Ω	
	RC18	121Ω	
PLL and Channel	R	0Ω	Resistor R must be 0Ω
	L	0Ω	Inductor L needs to be replaced with a 0Ω resistor
	C1	10μF	
	C2	10μF	
	RPLLSTO	51Ω	
	RFBDRS	100Ω	
Miscellaneous	R1	Not loaded	
	R2	Not loaded	
	R3	0Ω	
	R4	0Ω	
	RSA0	825Ω	

ORDERING INFORMATION



NOTE:
1. Contact factory for availability.

Device Revision	Status
A5	Active

Other Ordering Information	
AMB0480xxRJ8	AMB in bare die packaged in tape/reel
AMB0480xxRJ	AMB in bare die packaged in tray
AMB0480xxRH8	AMB with heatspreader packaged in tape/reel
AMB0480xxRH	AMB with heatspreader packaged in tray

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