

ADC1453D250

Dual 14-bit ADC; up to 246 Msps; JESD204B serial outputs

Rev. 3.2 — 6 June 2014

Preliminary data sheet

1. General description

The ADC1453D is a dual channel 14-bit Analog-to-Digital Converter (ADC) with JESD204B interface (which is backward compatible with the JESD204A interface) optimized for high dynamic performance and low power consumption at sample rates up to 246 Msps. Pipelined architecture and output error correction guarantee zero missing codes over the entire operating range.

The ADC1453D has JESD204B serial outputs over a configurable number of lanes (1 or 2). Multiple Device Synchronization (MDS) allows sample-accurate synchronization of the data outputs of multiple ADC devices. It guarantees a maximum skew of one clock period between as many as 16 output lanes from up to eight ADC1453D devices.

An integrated Serial Peripheral Interface (SPI) allows easy configuration of the ADC. The device also includes a programmable full-scale to allow a flexible input voltage range of 1 V (p-p) to 2 V (p-p).

The ADC1453D is available in an VFQFPN56 package (8 mm × 8 mm outline). It is supported with customer demo boards.

2. Features and benefits

- Dual channel 14-bit resolution ADC
- Sampling rate up to 246 Msps
- JESD204B Device Subclass 0, 1 and 2 with harmonic clocking and deterministic latency support
- ADC Multiple Device Synchronization (MDS)
- Offset binary, two's complement and Gray output data
- Two JESD204B serial output lanes, up to 5 Gbps
- Flexible input voltage range from 1 V (p-p) to 2 V (p-p) by 1 dB steps
- Clock input divider from 1 to 8 supports harmonic clocking
- Duty Cycle Stabilizer (DCS)
- SNR = 70.1 dBFS; $f_s = 246$ Msps; $f_i = 190$ MHz
- SFDR = 80 dBc; $f_s = 246$ Msps; $f_i = 190$ MHz
- IMD3 = 86 dBc; $f_s = 246$ Msps; $f_{i1} = 188.5$ MHz; $f_{i2} = 191.5$ MHz
- Analog input bandwidth of 1 GHz (typical)
- Pin to pin compatible with ADC1413D and ADC1443D series
- Typical power dissipation = 1.4 W; $f_s = 246$ Msps
- Industrial temperature range from -40 °C to $+85$ °C
- Serial Peripheral Interface (SPI) for configuration control and status monitoring
- VFQFPN56 package; 8 × 8 mm



3. Applications

- Wireless infrastructure: LTE, TD-LTE, WiMAX, MC-GSM, CDMA, WCDMA, TD-SCDMA
- Software defined radio
- Medical non-invasive scanners
- Scientific particle detectors
- Microwave backhaul transceivers
- Aerospace and defense communications and radar systems
- Industrial signal analysis instruments
- General-purpose high-speed applications

4. Ordering information

Table 1. Ordering information

| Type number | f _s (Msps) | Package | | Version |
|----------------|-----------------------|---------|---|----------|
| | | Name | Description | |
| ADC1453D250NGG | 246 | VFQFPN | plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 × 8 × 1.35 mm | PSC-4449 |

5. Block diagram

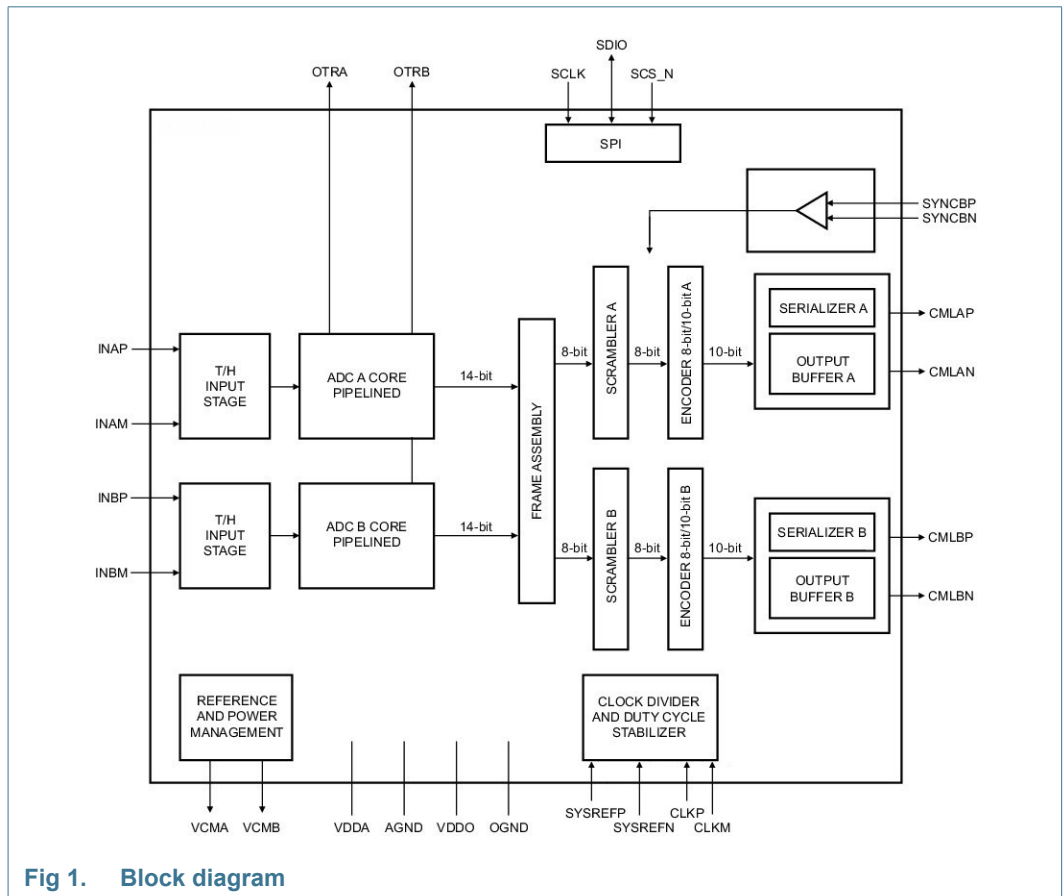
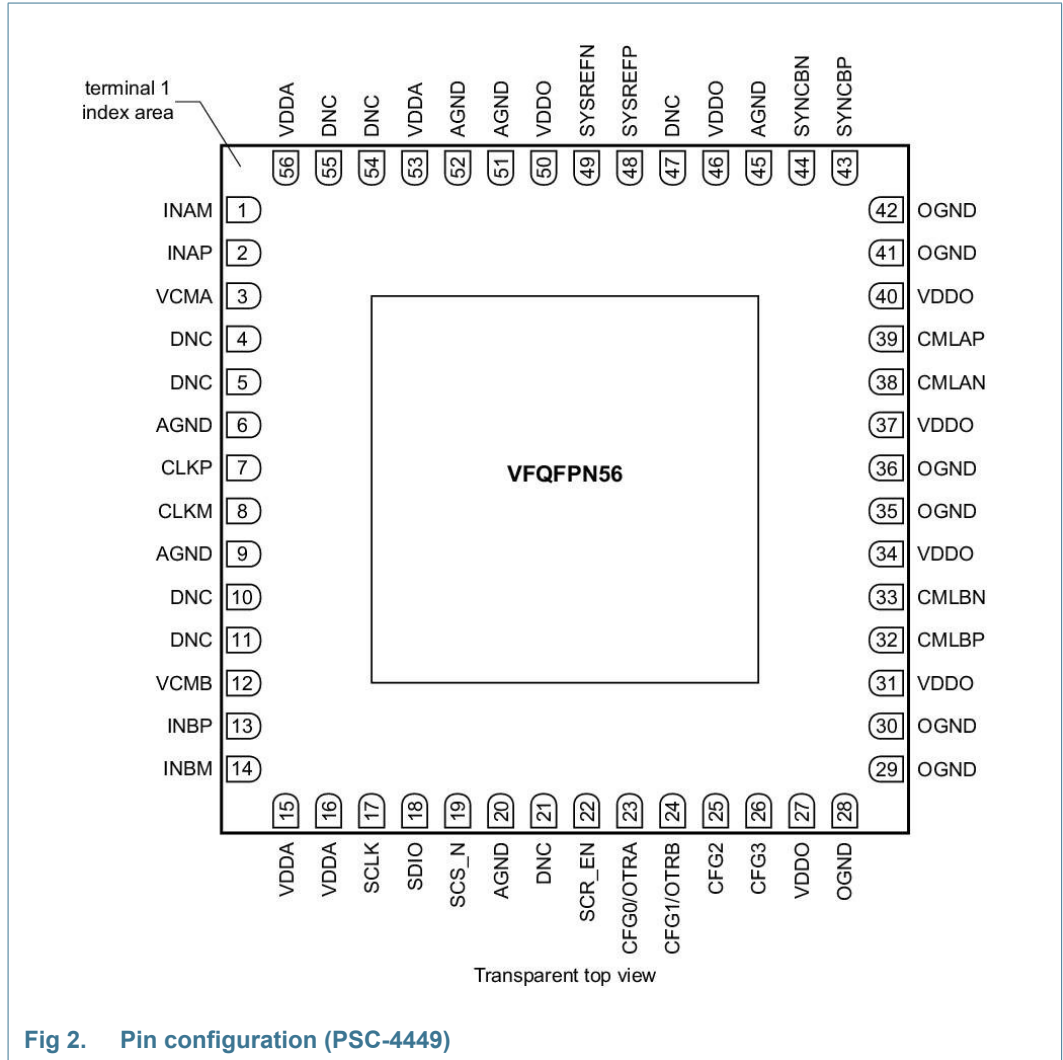


Fig 1. Block diagram

6. Pinning information

6.1 Pinning



6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type ^[1] | Description |
|-----------|-----|---------------------|--|
| INAM | 1 | I | channel A complementary analog input |
| INAP | 2 | I | channel A analog input |
| VCMA | 3 | O | channel A output common voltage |
| DNC | 4 | - | do not connect |
| DNC | 5 | - | do not connect |
| AGND | 6 | G | analog ground |
| CLKP | 7 | I | clock input |
| CLKN | 8 | I | complementary clock input |
| AGND | 9 | G | analog ground |
| DNC | 10 | - | do not connect |
| DNC | 11 | - | do not connect |
| VCMB | 12 | O | channel B output common voltage |
| INBP | 13 | I | channel B analog input |
| INBM | 14 | I | channel B complementary analog input |
| VDDA | 15 | P | analog power supply |
| VDDA | 16 | P | analog power supply |
| SCLK | 17 | I | SPI clock (50 k Ω internal pull-down) |
| SDIO | 18 | I/O | SPI data IO (50 k Ω internal pull-down) |
| SCS_N | 19 | I | SPI chip select (50 k Ω internal pull-up) |
| AGND | 20 | G | analog ground |
| DNC | 21 | - | do not connect |
| SCR_EN | 22 | I | scrambler enable (50 k Ω internal pull-up) |
| CFG0/OTRA | 23 | I/O | configuration pin 0/OuT of Range A (OTRA) (50 k Ω internal pull-down) |
| CFG1/OTRB | 24 | I/O | configuration pin 1/OuT of Range B (OTRB) (50 k Ω internal pull-down) |
| CFG2 | 25 | I/O | configuration pin 2 (50 k Ω internal pull-down) |
| CFG3 | 26 | I/O | configuration pin 3 (50 k Ω internal pull-down) |
| VDDO | 27 | P | digital output power supply |
| AGND | 28 | G | analog ground |
| OGND | 29 | G | digital output ground |
| OGND | 30 | G | digital output ground |
| VDDO | 31 | P | digital output power supply |
| CMLBP | 32 | O | channel B output |
| CMLBN | 33 | O | channel B complementary output |
| VDDO | 34 | P | digital output power supply |
| OGND | 35 | G | digital output ground |
| OGND | 36 | G | digital output ground |
| VDDO | 37 | P | digital output power supply |
| CMLAN | 38 | O | channel A complementary output |

Table 2. Pin description ...continued

| Symbol | Pin | Type ^[1] | Description |
|---------|-----|---------------------|--|
| CMLAP | 39 | O | channel A output |
| VDDO | 40 | P | digital output power supply |
| OGND | 41 | G | digital output ground |
| OGND | 42 | G | digital output ground |
| SYNCBP | 43 | I | JESD204B SYNC synchronization signal from receiver |
| SYNCBN | 44 | I | complementary SYNC from receiver |
| AGND | 45 | G | analog ground |
| VDDO | 46 | P | digital output power supply |
| DNC | 47 | - | do not connect |
| SYSREFP | 48 | I | positive clock synchronization |
| SYSREFN | 49 | I | negative clock synchronization |
| VDDO | 50 | P | digital output power supply |
| AGND | 51 | G | analog ground |
| AGND | 52 | G | analog ground |
| VDDA | 53 | P | analog power supply |
| DNC | 54 | - | do not connect |
| DNC | 55 | - | do not connect |
| VDDA | 56 | P | analog power supply |
| AGND | EXP | G | Expose PAD |

[1] P: power supply; G: ground; I: input; O: output; I/O: input/output.

6.2.1 Start-up Configuration

Because the maximum sampling clock of the ADC1453D is 246 Msps, care should be taken in case of harmonic clocking. If the input clock frequency is higher than 246 MHz, the clock divider must be set before providing the clock.

In order to avoid any issue, it is recommended to start the device in power-down mode by setting the configuration pins to logic level '1' (see [Table 19](#)). This can be done by adding for example a 1 k Ω pull-up resistor on CFG0, CFG1, CFG2 and CFG3.

When the power supplies are set, the divider can be programmed by the use of the SPI registers. Then the device is powered on and the JESD204B configuration is set by the use of the SPI registers (bits CFG_SETUP[3:0] in [Table 43](#)).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------|---------------------------|--|------|-----------------|------|
| V_{DDA} | analog supply voltage | | -0.3 | +2.1 | V |
| V_{DDO} | output supply voltage | | -0.3 | +2.1 | V |
| ΔV_{DD} | supply voltage difference | $V_{DDA} - V_{DDO}$ | -0.8 | +0.8 | V |
| V_I | input voltage | pins INP, INM, CLKP and CLKM; referenced to AGND | -0.3 | $V_{DDA} + 0.3$ | V |
| | | pins OTR, SCS_N, SDIO, SCLK, CFG, SCR_EN, SYSREFP, SYSREFN, SYNCBP, and SYNCBN; referenced to AGND | -0.3 | $V_{DDO} + 0.3$ | V |
| V_O | output voltage | pin VCM; referenced to AGND | -0.3 | $V_{DDA} + 0.3$ | V |
| | | pins CMLP, and CMLN; referenced to OGND | -0.3 | $V_{DDO} + 0.3$ | V |
| T_{stg} | storage temperature | | -55 | +125 | °C |
| T_{amb} | ambient temperature | | -40 | +85 | °C |
| T_j | junction temperature | | - | 125 | °C |

8. Thermal characteristics

Table 4. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|---------------|---|------------|----------|------|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | 66 vias | [1] 22.7 | K/W |
| $R_{th(j-c)}$ | thermal resistance from junction to case | 66 vias | [1] 9.3 | K/W |

[1] In compliance with JEDEC test board, in free air.

9. Static characteristics

Table 5. Static characteristics^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-----------------------|-----------------------------------|-----|------|--------|------|
| Supplies | | | | | | |
| V_{DDA} | analog supply voltage | | 1.7 | 1.8 | 1.9 | V |
| V_{DDO} | output supply voltage | serial link up to 4 Gbps | 1.7 | 1.8 | 1.9 | V |
| | | serial link from 4 to 5 Gbps | 1.8 | 1.85 | 1.9 | V |
| I_{DDA} | analog supply current | $f_s = 246$ Msps; $f_i = 190$ MHz | - | 407 | <tbid> | mA |
| I_{DDO} | output supply current | $f_s = 246$ Msps; $f_i = 190$ MHz | - | 345 | <tbid> | mA |

Table 5. Static characteristics^[1] ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-----------------------------|--|-----------------------|-------|---------------------|------|
| P _{tot} | total power dissipation | f _i = 190 MHz | | | | |
| | | f _s = 246 Msps | - | 1.4 | <td> | W |
| | | Power-down mode | - | 10 | - | mW |
| | | Sleep mode | - | 115 | - | mW |
| Clock inputs: pins CLKP and CLKM (AC-coupled; peak-to-peak) | | | | | | |
| V _{i(clk)} | clock input voltage | LVPECL | - | ±0.8 | - | V |
| | | LVDS | - | ±0.35 | - | V |
| | | SINE differential | ±0.5 | ±1.25 | - | V |
| | | LVCOS single | - | ±0.6 | - | V |
| C _i | input capacitance | | - | 1.2 | - | pF |
| Logic inputs | | | | | | |
| I _{IL} | LOW-level input current | absolute value | - | 30 | - | μA |
| I _{IH} | HIGH-level input current | absolute value | - | 70 | - | μA |
| C _i | input capacitance | | - | 1.2 | - | pF |
| pins SYSREFF, SYSREFN, SYNCBP, and SYNCBN (differential pins) | | | | | | |
| V _{i(cm)} | common-mode input voltage | | 0.925 | 1.2 | 1.475 | V |
| V _{i(dif)} | differential input voltage | | 0.2 | 0.7 | - | V |
| pins SCS_N, SDIO, SCLK, SCR_EN, CFG, SYNCBP and SYSREFF (Single Ended) | | | | | | |
| V _{IL} | LOW-level input voltage | | 0 | - | 0.3V _{DDO} | V |
| V _{IH} | HIGH-level input voltage | | 0.7V _{DDO} | - | V _{DDO} | V |
| Logic output: pins OTRA, OTRB and SDIO | | | | | | |
| V _{OL} | LOW-level output voltage | | 0 | - | 0.2 | V |
| V _{OH} | HIGH-level output voltage | | V _{DDO} -0.2 | - | V _{DDO} | V |
| Digital outputs: pins CMLAP, CMLAN, CMLBP, and CMLBN | | | | | | |
| V _{O(cm)} | common-mode output voltage | default current | - | 1.4 | - | V |
| V _{O(dif)} | differential output voltage | default current; peak-to-peak | - | 800 | - | mV |
| Analog inputs: pins INP and INM | | | | | | |
| I _I | input current | | - | ±5 | - | μA |
| R _I | input resistance | f _i = 190 MHz | - | 400 | - | Ω |
| C _i | input capacitance | f _i = 190 MHz | - | 5 | - | pF |
| V _{I(cm)} | common-mode input voltage | V _{INP} = V _{INM} ; T _{amb} = 25 °C | 0.8 | 0.9 | 1.0 | V |
| B _i | input bandwidth | | - | 1 | - | GHz |
| V _{I(dif)} | differential input voltage | peak-to-peak; full-scale | 1 | - | 2 | V |
| Common-mode output voltage: pins VCMA and VCMB | | | | | | |
| V _{O(cm)} | common-mode output voltage | I _{O(cm)} = 1mA | - | 0.9 | - | V |
| I _{O(cm)} | common-mode output current | T _{amb} = 25 °C | - | - | 1 | mA |
| Accuracy | | | | | | |
| INL | integral non-linearity | f _s = 246 Msps; f _i = 4.43 MHz | - | ±2.1 | ±6.62 | LSB |

Table 5. Static characteristics^[1] ...continued

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|----------------------------------|--|-------|-------|-------|------|
| DNL | differential non-linearity | $f_s = 246 \text{ Msps}$; $f_i = 4.43 \text{ MHz}$; guaranteed no missing codes | | | | |
| | | negative DNL | -0.88 | -0.71 | - | LSB |
| | | positive DNL | - | +0.87 | +1.22 | LSB |
| E_{offset} | offset error | | -20 | - | +20 | mV |
| E_G | gain error | full-scale | - | 4.1 | - | % |
| $M_{G(\text{CTC})}$ | channel-to-channel gain matching | | - | 2.5 | - | % |
| OS | Offset Spur | measured at $f_s/2$ with $f_s = 246 \text{ Msps}$ | | -80 | | dBc |
| Supply | | | | | | |
| PSRR | power supply rejection ratio | 100 mV (p-p) on V_{DDA} , 0.5 to 2MHz | - | -35 | - | dB |

[1] Typical values measured at $V_{\text{DDA}} = 1.8 \text{ V}$; $V_{\text{DDO}} = 1.85 \text{ V}$; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$. Minimum and maximum values are across the full temperature range $T_{\text{amb}} = -40 \text{ }^\circ\text{C}$ to $+85 \text{ }^\circ\text{C}$ at $V_{\text{DDA}} = 1.8 \text{ V}$; $V_{\text{DDO}} = 1.85 \text{ V}$; $V_{\text{I(dif)}} = 2 \text{ V}$; $V_{\text{INP}} - V_{\text{INM}} = -1.5 \text{ dBFS}$; unless otherwise specified.

10. Dynamic characteristics

10.1 Dynamic characteristics

Table 6. Dynamic characteristics^[1]

| Symbol | Parameter | Conditions | $f_s = 246\text{Msps}$ | | | Unit |
|---------------|--|--|------------------------|------|-----|------|
| | | | Min | Typ | Max | |
| α_{2H} | second harmonic level | $f_i = 70\text{ MHz}$ | - | -89 | - | dBc |
| | | $f_i = 140\text{ MHz}$ | - | -83 | - | dBc |
| | | $f_i = 190\text{ MHz}$ | - | -85 | - | dBc |
| | | $f_i = 230\text{ MHz}$ | - | -82 | - | dBc |
| | | $f_i = 310\text{ MHz}$ | - | -79 | - | dBc |
| α_{3H} | third harmonic level | $f_i = 70\text{ MHz}$ | - | -81 | - | dBc |
| | | $f_i = 140\text{ MHz}$ | - | -86 | - | dBc |
| | | $f_i = 190\text{ MHz}$ | - | -80 | - | dBc |
| | | $f_i = 230\text{ MHz}$ | - | -87 | - | dBc |
| | | $f_i = 310\text{ MHz}$ | - | -80 | - | dBc |
| SFDR | spurious-free dynamic range | $f_i = 70\text{ MHz}$ | - | 81 | - | dBc |
| | | $f_i = 140\text{ MHz}$ | - | 82 | - | dBc |
| | | $f_i = 190\text{ MHz}$ | - | 80 | - | dBc |
| | | $f_i = 230\text{ MHz}$ | - | 81 | - | dBc |
| | | $f_i = 310\text{ MHz}$ | - | 79 | - | dBc |
| THD | total harmonic distortion | $f_i = 70\text{ MHz}$ | - | -79 | - | dBc |
| | | $f_i = 140\text{ MHz}$ | - | -80 | - | dBc |
| | | $f_i = 190\text{ MHz}$ | - | -78 | - | dBc |
| | | $f_i = 230\text{ MHz}$ | - | -79 | - | dBc |
| | | $f_i = 310\text{ MHz}$ | - | -76 | - | dBc |
| IMD3 | third-order intermodulation distortion | $f_{i1} = 68.5\text{ MHz}; f_{i2} = 71.5\text{ MHz}$ | - | 90 | - | dBc |
| | | $f_{i1} = 138.5\text{ MHz}; f_{i2} = 141.5\text{ MHz}$ | - | 88 | - | dBc |
| | | $f_{i1} = 188.5\text{ MHz}; f_{i2} = 191.5\text{ MHz}$ | - | 90 | - | dBc |
| | | $f_{i1} = 228.5\text{ MHz}; f_{i2} = 231.5\text{ MHz}$ | - | 86 | - | dBc |
| | | $f_{i1} = 308.5\text{ MHz}; f_{i2} = 311.5\text{ MHz}$ | - | 88 | - | dBc |
| SNR | signal-to-noise ratio | $f_i = 70\text{ MHz}$ | - | 70.6 | - | dBFS |
| | | $f_i = 140\text{ MHz}$ | - | 70.5 | - | dBFS |
| | | $f_i = 190\text{ MHz}$ | - | 70.1 | - | dBFS |
| | | $f_i = 230\text{ MHz}$ | - | 69.8 | - | dBFS |
| | | $f_i = 310\text{ MHz}$ | - | 69.3 | - | dBFS |

Table 6. Dynamic characteristics^[1] ...continued

| Symbol | Parameter | Conditions | $f_s = 246\text{Msps}$ | | | Unit |
|--------------------------|--------------------------|------------------------|------------------------|------|-----|------|
| | | | Min | Typ | Max | |
| ENOB | effective number of bits | $f_i = 70\text{ MHz}$ | - | 11.1 | - | bit |
| | | $f_i = 140\text{ MHz}$ | - | 11.1 | - | bit |
| | | $f_i = 190\text{ MHz}$ | - | 11 | - | bit |
| | | $f_i = 230\text{ MHz}$ | - | 11 | - | bit |
| | | $f_i = 310\text{ MHz}$ | - | 10.9 | - | bit |
| $\alpha_{\text{ct(ch)}}$ | channel crosstalk | $f_i = 140\text{ MHz}$ | - | 83 | - | dBc |
| | | $f_i = 230\text{ MHz}$ | - | 82 | - | dBc |

[1] Typical values measured at $V_{\text{DDA}} = 1.8\text{ V}$; $V_{\text{DDO}} = 1.85\text{ V}$; $T_{\text{amb}} = 25\text{ }^\circ\text{C}$. Minimum and maximum values are across the full temperature range $T_{\text{amb}} = -40\text{ }^\circ\text{C}$ to $+85\text{ }^\circ\text{C}$ at $V_{\text{DDA}} = 1.8\text{ V}$; $V_{\text{DDO}} = 1.85\text{ V}$; $V_{\text{I(dif)}} = 2\text{ V}$; $V_{\text{INP}} - V_{\text{INM}} = -1.5\text{ dBFS}$; unless otherwise specified.

10.2 Timing

10.2.1 Clock timing

Table 7. Clock and digital output timing characteristics^[1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------|----------------------|------|-----|-------|--------------|
| $t_{lat(data)}$ | data latency time | F = 1 | 54 | - | 55 | clock cycles |
| | | F = 2 | 45.5 | - | 46 | clock cycles |
| | | F = 4 | 41 | - | 41.25 | clock cycles |
| t_{wake} | wake-up time | from Power-down mode | - | 60 | - | μ s |
| | | from Sleep mode | - | 54 | - | μ s |
| Clock timing | | | | | | |
| f_s | sampling rate | | 180 | - | 246 | MHz |
| f_{clk} | clock frequency | | 60 | - | 1000 | MHz |
| δ_{clk} | clock duty cycle | | 40 | - | 60 | % |

[1] Typical values measured at $V_{DDA} = 1.8$ V; $V_{DDO} = 1.85$ V; $T_{amb} = 25$ °C. Minimum and maximum values are across the full temperature range $T_{amb} = -40$ °C to 85 °C at $V_{DDA} = 1.8$ V; $V_{DDO} = 1.85$ V; $V_{I(dif)} = 2$ V; $V_{INP} - V_{INM} = -1.5$ dBFS; unless otherwise specified.

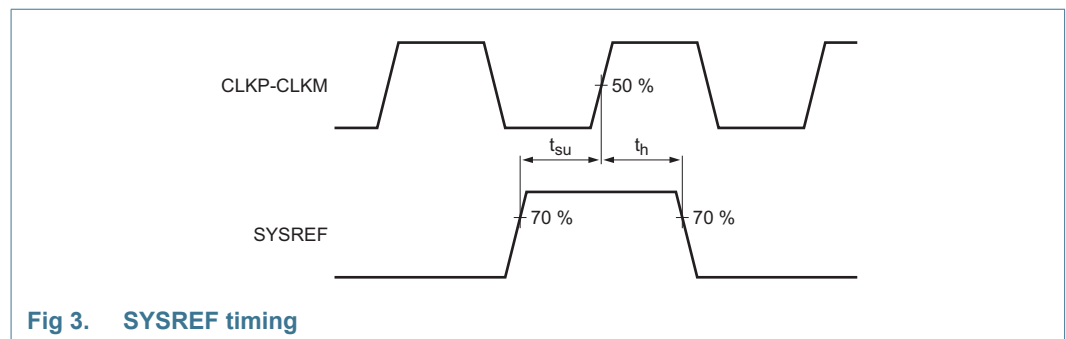
10.2.2 SYSREFP/N and SYNCBP/N timings

Table 8. SYSREF timing

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-------------|------------|-------------------------|-----|-----|------|
| t_{su} | set-up time | | 0.5 | - | - | ns |
| t_h | hold time | | ($t_{clk}/2$) -0.5 | - | - | ns |

Table 9. SYNCB timing

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|-------------|------------|--------------------------|-----|-----|------|
| t_{su} | set-up time | | 0.75 | - | - | ns |
| t_h | hold time | | ($t_{clk}/2$) -0.25 | - | - | ns |

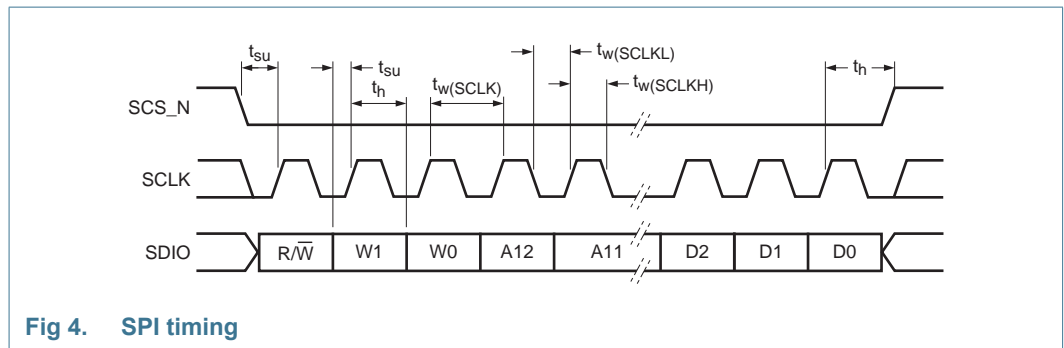


10.2.3 SPI timing

Table 10. SPI timing characteristics [1]

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|-----------------------|--------------------|-----|-----|-----|------|
| $t_{w(SCLK)}$ | SCLK pulse width | | 40 | - | - | ns |
| $t_{w(SCLKH)}$ | SCLK HIGH pulse width | | 16 | - | - | ns |
| $t_{w(SCLKL)}$ | SCLK LOW pulse width | | 16 | - | - | ns |
| t_{su} | set-up time | SDIO to SCLK HIGH | 5 | - | - | ns |
| | | SCS_N to SCLK HIGH | 5 | - | - | ns |
| t_h | hold time | SDIO to SCLK HIGH | 2 | - | - | ns |
| | | SCS_N to SCLK HIGH | 2 | - | - | ns |
| f_{clk} | clock frequency | | - | - | 25 | MHz |

[1] Typical values measured at $V_{DDA} = 1.8\text{ V}$; $V_{DDO} = 1.85\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$. Minimum and maximum values are across the full temperature range $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ at $V_{DDA} = 1.8\text{ V}$; $V_{DDO} = 1.85\text{ V}$



10.3 Typical dynamic performances¹

10.3.1 Typical FFT at 246 Msps

| | |
|--|---|
| TBD | TBD |
| <p>Fig 5. 1-tone FFT: -1.5 dBFS; $f_i = 65$ MHz; $f_s = 246$ Msps</p> | <p>Fig 6. 1-tone FFT: -1.5 dBFS; $f_i = 190$ MHz; $f_s = 246$ Msps</p> |
| TBD | TBD |
| <p>Fig 7. 1-tone FFT: -14 dBFS; $f_i = 190$ MHz; $f_s = 246$ Msps</p> | <p>Fig 8. 2-tone FFT: -7.5 dBFS; $f_{i1} = 188.5$ MHz; $f_{i2} = 191.5$ MHz; $f_s = 246$ Msps</p> |

1. Typical values measured at $V_{DDA} = 1.8$ V; $V_{DDO} = 1.85$ V; $T_{amb} = 25$ °C

10.3.2 Typical performances

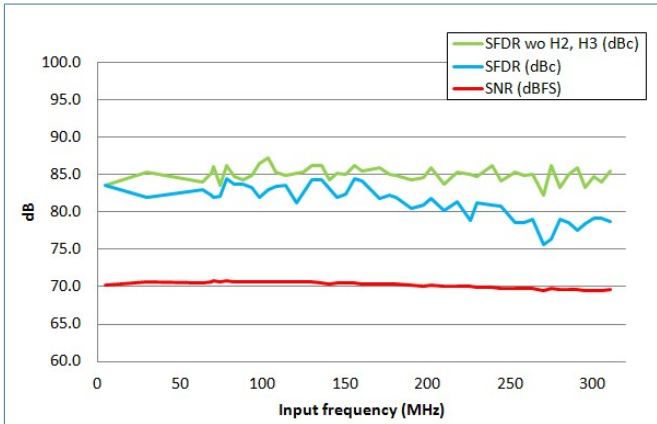


Fig 9. SNR and SFDR as a function of input frequency; -1.5 dBFS

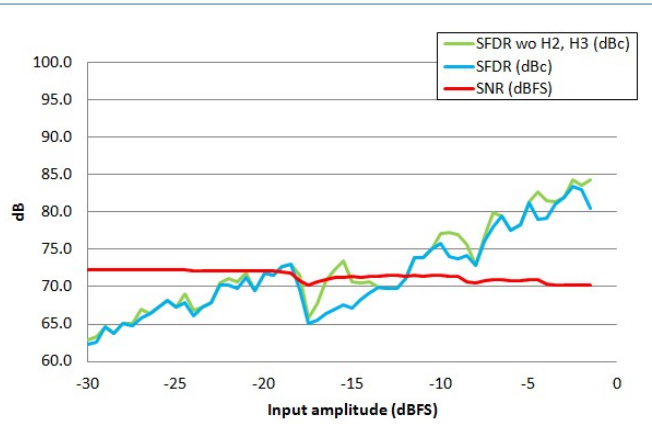


Fig 10. SNR and SFDR as a function of input amplitude; $V_{I(dif)} = 2$ V

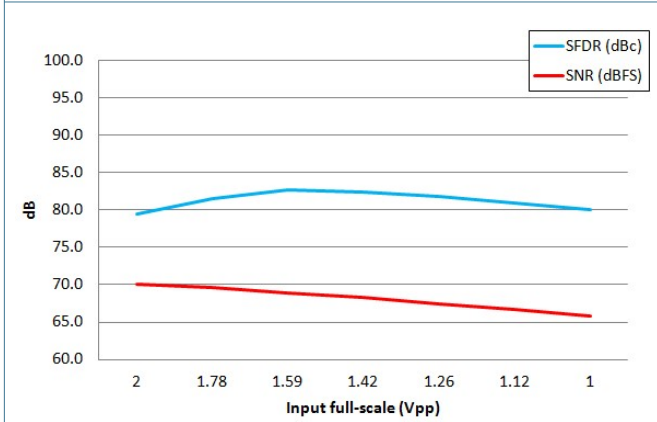


Fig 11. SNR and SFDR as a function of full-scale amplitude; -1.5 dBFS

TBD

Fig 12. tbd

11. Application information

11.1 Analog inputs

11.1.1 Input stage

The analog input of the ADC1453D supports a differential or a single-ended input drive. Optimal performance is achieved using differential inputs with respect to the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM.

The equivalent circuit of the sample and hold input stage, including ElectroStatic Discharge (ESD) protection circuit and package parasitics, is shown in [Figure 13](#).

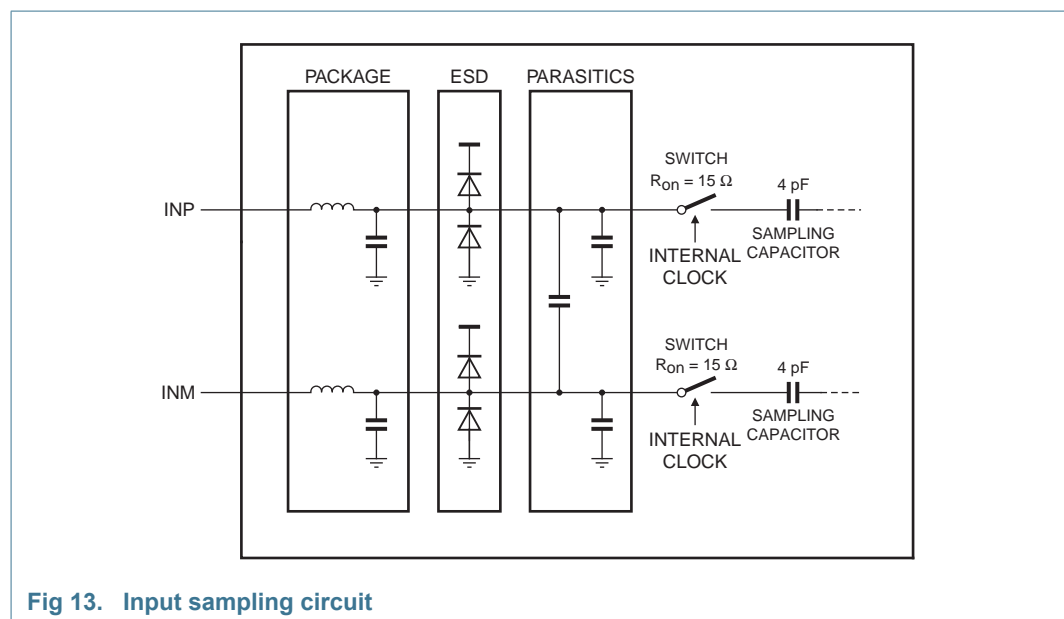


Fig 13. Input sampling circuit

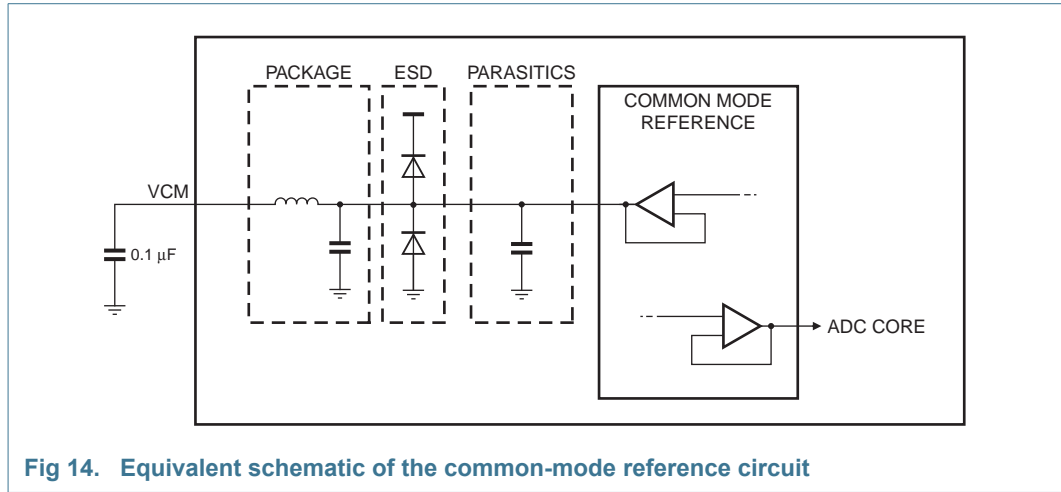
The sample phase occurs when the internal sampling clock (derived from the clock signal on pin CLKP/CLKM) is HIGH. The voltage is then held on the sampling capacitors. When the sampling clock signal becomes LOW, the device enters the hold phase and the voltage information is transmitted to the ADC core.

11.1.2 Common-mode input voltage ($V_{I(cm)}$)

Set the common-mode input voltage ($V_{I(cm)}$) on pins INP and INM externally to 0.9 V for optimal performance.

11.1.3 Pin VCM

When the input stage is AC-coupled, pin VCM can be used to set the common-mode reference for the analog inputs, for instance, via a transformer middle point. Connect a 0.1 μF filter capacitor between pin VCM and ground to ensure a low-noise common-mode output voltage.



11.1.4 Programmable full-scale

The full-scale analog input voltage range is configurable between 1 V (p-p) and 2 V (p-p) by programming internal reference gain between 0 dB and -6 dB in 1 dB steps. The full-scale range can be set independently via bits INTREF[2:0] of the SPI local registers (see Table 11 and Table 30).

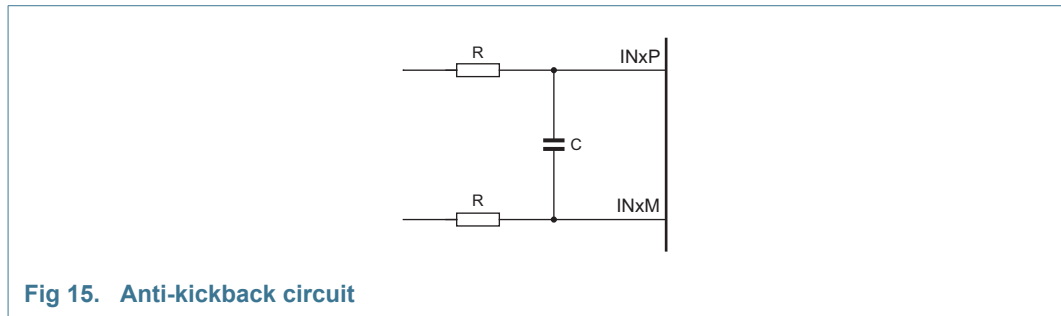
Table 11. Reference gain control
Default values are shown highlighted.

| INTREF[2:0] | Level (dB) | Full-scale (V (p-p)) |
|-------------|------------|----------------------|
| 000 | 0 | 2 |
| 001 | -1 | 1.78 |
| 010 | -2 | 1.59 |
| 011 | -3 | 1.42 |
| 100 | -4 | 1.26 |
| 101 | -5 | 1.12 |
| 110 | -6 | 1 |
| 111 | reserved | x |

11.1.5 Anti-kickback circuitry

An anti-kickback circuitry (RC-filter in Figure 15) is required to counteract the effects of the charge injection generated by the sampling capacitance.

The RC-filter is also used to filter noise from the signal before it reaches the sampling stage. It is recommended that the capacitor has a value that maximizes noise attenuation without degrading the settling time excessively.



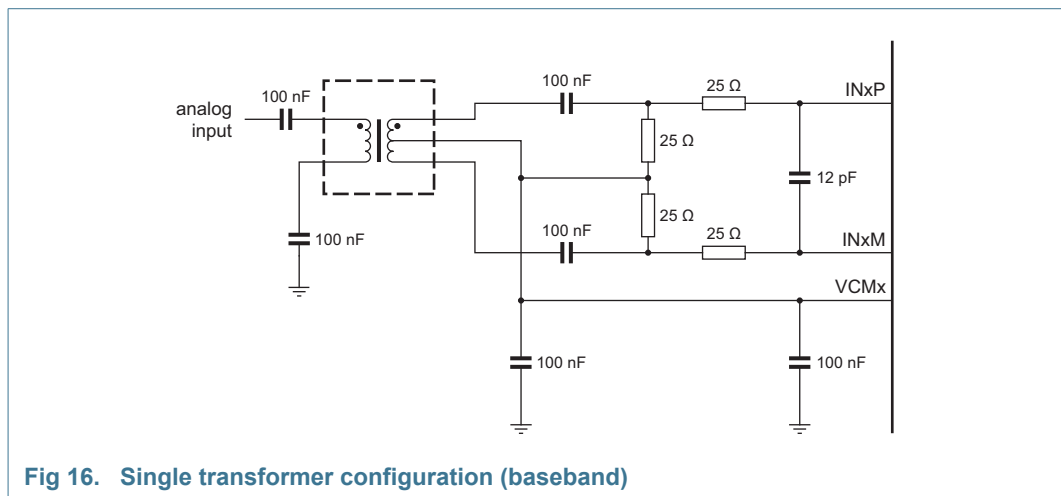
The input frequency determines the component values. Select values that do not affect the input bandwidth. The values given in the following table are advised for 50Ω impedance system.

Table 12. RC coupling versus input frequency; typical values

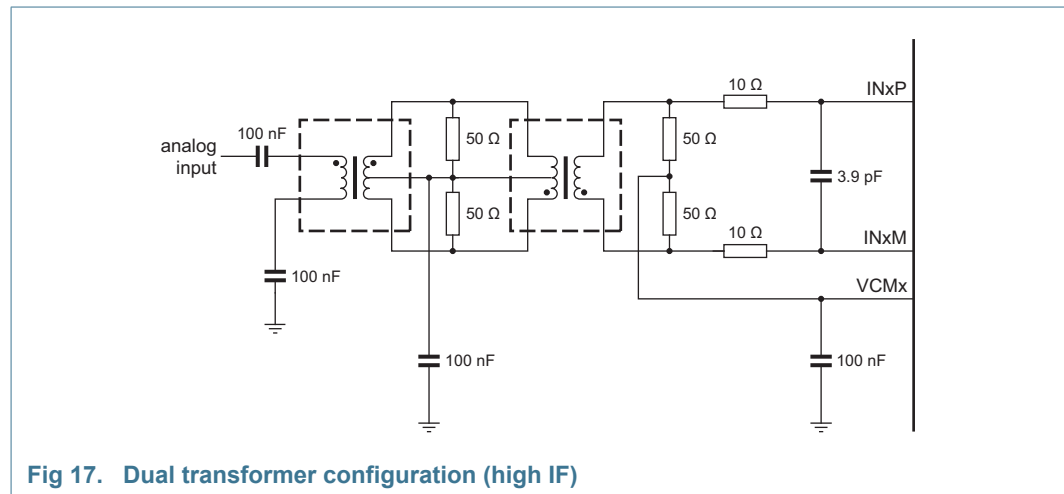
| Input frequency range (MHz) | R (Ω) | C (pF) |
|-----------------------------|-------|--------|
| 0 to 50 | 25 | 12 |
| 50 to 200 | 10 | 3.9 |
| 200 to 300 | 5 | 0.5 |

11.1.6 Transformer

The input frequency determines the configuration of the transformer circuit. The configuration shown in [Figure 16](#) is suitable for a baseband application.



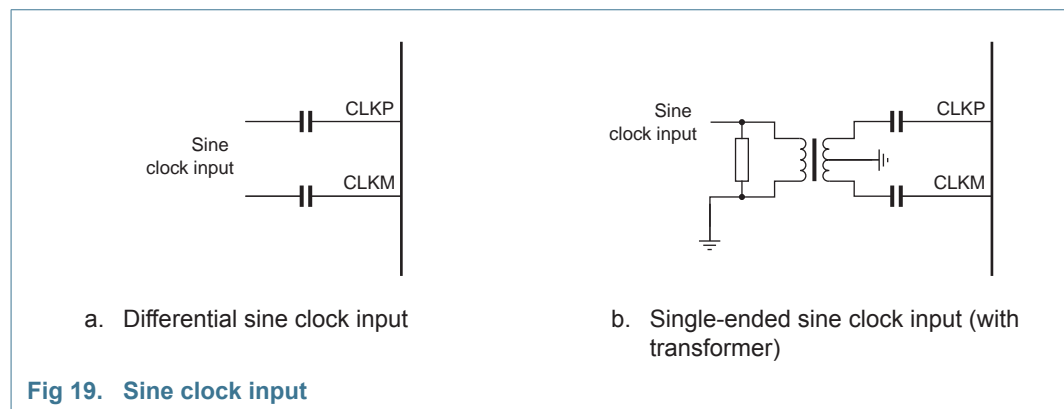
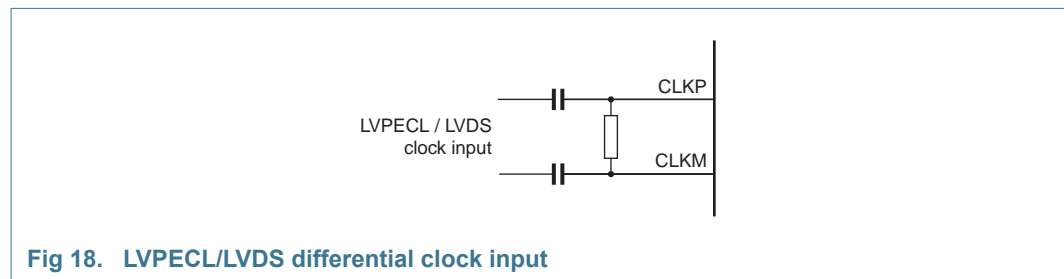
The configuration shown in [Figure 17](#) is recommended for high-frequency applications. In both cases, the choice of transformer is a compromise between cost and performance.

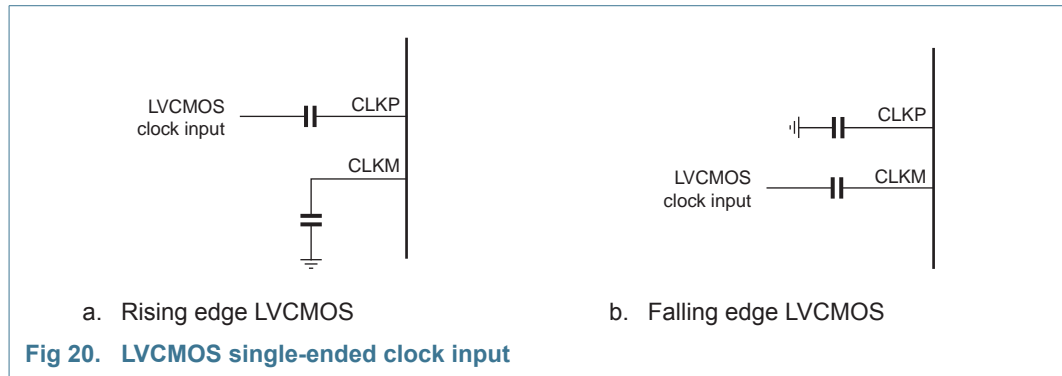


11.2 Clock input

11.2.1 Drive modes

The ADC1453D series can be driven differentially (LVPECL, LVDS or SINE). A single-ended LVCMOS signal connected to either pin CLKP or pin CLKM can also drive the device (connect the complementary pin to ground using a capacitor). The LVPECL is recommended for an optimal performance.

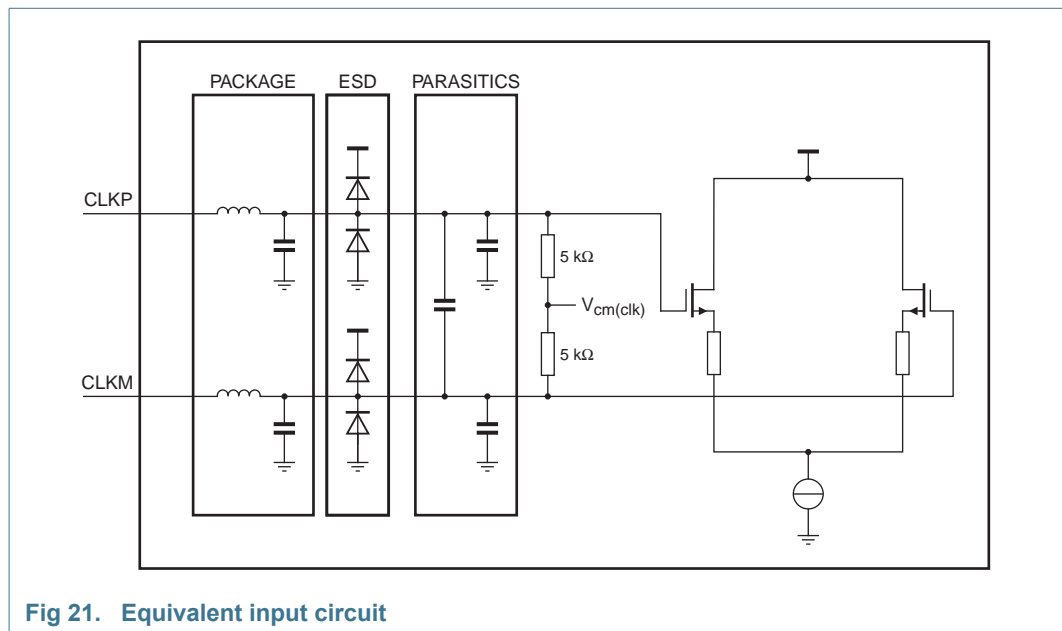




Single-ended or differential clock inputs can be selected via bit DIFF_SE of SPI. If single-ended is enabled, the input pin (pin CLKM or pin CLKP) is selected using control bit SE_SEL (see [Table 29](#)).

11.2.2 Equivalent input circuit

[Figure 21](#) shows the equivalent circuit of the input clock buffer. The input signal must be AC-coupled and the common-mode voltage of the differential input stage is set via internal 5 kΩ resistors.



11.2.3 JESD204B harmonic clocking

The ADC1453D embeds an input clock divider that divides the incoming clock (clock frequency f_{clk}) by a factor of 1 to 8. The output of this divider is then used as sampling clock (sampling frequency f_s) (see bits CLK_DIV[2:0] in [Table 29](#)).

Caution must be taken to, first power the ADC1453D in «Power Down» mode by setting the CFG Pins to «1111» see [Table 19](#), second, program the clock divider to the wanted value (see bits CLK_DIV[1:0] in [Table 29](#)) and finally, set the ADC using the SPI register IP_CFG_SETUP [Table 43](#), to the wanted configuration.

11.2.4 JESD204B Deterministic Latency (pins SYSREFN and SYSREFP or SYNCBP and SYNCBN)

In the JESD204B standard 3 subclasses have been defined.

Subclass 0: No deterministic latency is required (equivalent to the JESD204A)

Subclass 1: Deterministic latency is required and is realized through the dedicated SYSREFP/N pins.

The deterministic latency can be controlled with a single-ended or a differential SYSREF signal.

When SYSREF is active (High by default), it resets the clock divider phase registers. In a multi-device application and when the clock divider factor is higher than 1, all sampling clock edges for multiple ADC1453D will be aligned (see [Table 8](#) and [Figure 3](#)).

On top of this, the SYSREFP/N pins initiates an internal LMFC clock (Local Multi-frame Clock), with a period of a multi-frame $F \cdot K$ (F: number of octets per frame, K: number of frames per multi-frame). See [Table 19](#) for examples.

A single pulse of SYSREF is needed for both clock divider reset and LMFC initialization. Because the SYSREF processing doesn't stop the data transmission, the signal can also be sent periodically at an harmonic frequency of the LMFC in order to change the alignment. In case of a periodic SYSREF not correlated to the LMFC, the user can program the LMFC to take into account only the first SYSREF pulse (see bit LMFC_periodic_rst in [Table 48](#)).

At a SYNC request from the receiver (on pins SYNCBP/N), K28.5 comma characters are sent over the serial lanes. When the receiver releases the SYNC request, then the Initial Lane Alignment (ILA) will start at an edge of the LMFC

At the receiver side, the different lanes are aligned using the ILA start of frame characters and fetched at the next LMFC boundary.

This operation ensures a deterministic latency. See the JESD204B JEDEC standard for more information.

Subclass2: Behavior is similar to Subclass1, but, instead of using a dedicated SYSREF signal, the SYNCBP/N is used for both SYNC request and deterministic latency.

The rising edge of the SYNCBP/N start the LMFC, while the falling edge set the SYNC request and hence start the Initial Lane Alignment according to the JEDEC JESD204B standard.

Below is an example of a Subclass1 ADC1453D registers programming:

Table 13. Subclass1 path activation

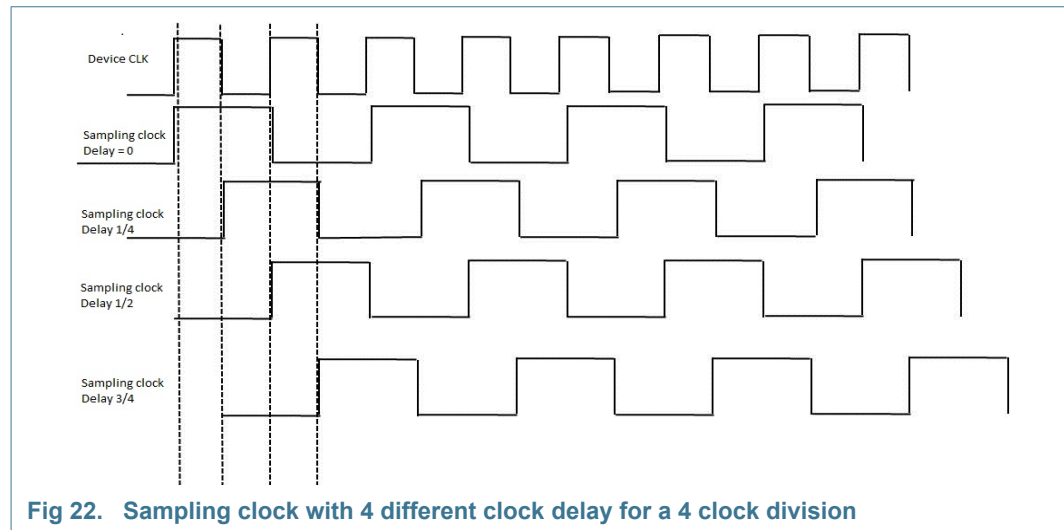
| Register | value | Comment |
|-----------------------|-------|--|
| DCS_CTRL (@0x043) | 0xC7 | Choose the SYSREFP/N on rising edge as DCS Reset |
| JESD204B_CTRL1 (@810) | 0xC0 | Enable an LMFC periodic reset |
| JESD204B_CTRL2 (@811) | 0x40 | Enable a one shot DCS reset |
| JESD204B_CTRL3 (@812) | 0x0A | Activate a Sync fetch at LMFC boundary |
| SYSREF_CFG (@81E) | 0x08 | Enable SYSREFP/N on differential mode |

11.2.5 Clock Group Delay

The ADC1453D has the ability to delay the sampling clock when derived from a harmonic clock within the range of a complete sampling clock period and with half harmonic clock period step

The delay can be adjusted over $2 \times N$ steps, where N is the clock divider ratio (bits CLK_DELAY[3:0] in [Table 38](#)).

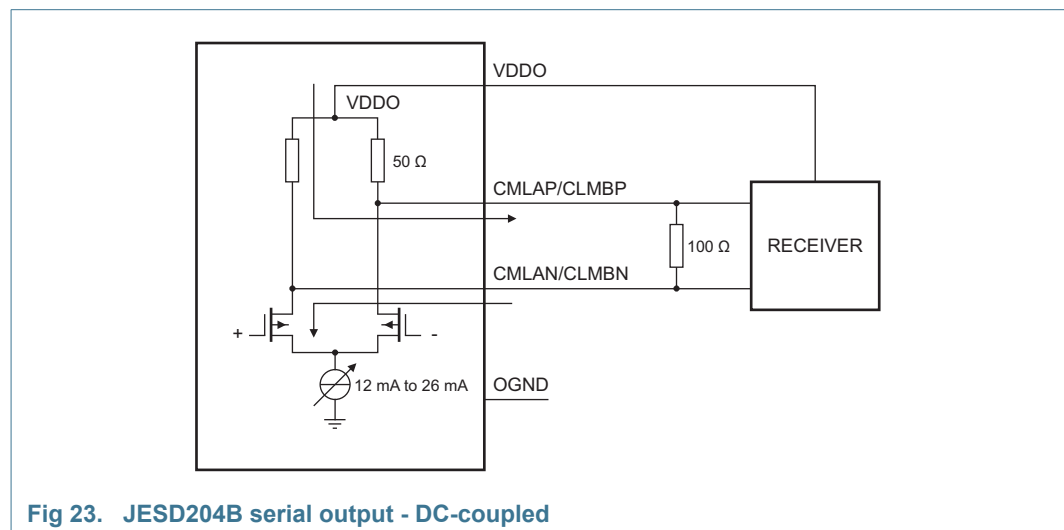
As an example: for a device clock of 500 Mhz and a clock division by 2 ($f_s = 250$ Msps), the sampling clock can be delayed over 4 steps of $1/(2 \times 500 \text{ Mhz}) = 1 \text{ ns}$.

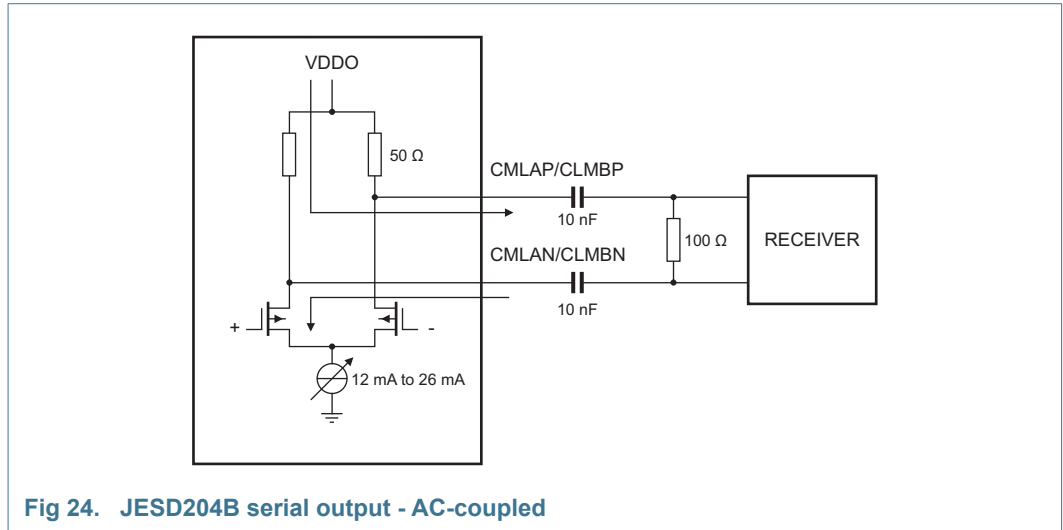


11.3 Digital outputs

11.3.1 Digital output buffers

The JESD204B standard specifies that both the receiver and the transmitter must share the same supply if they are connected in DC-coupling.



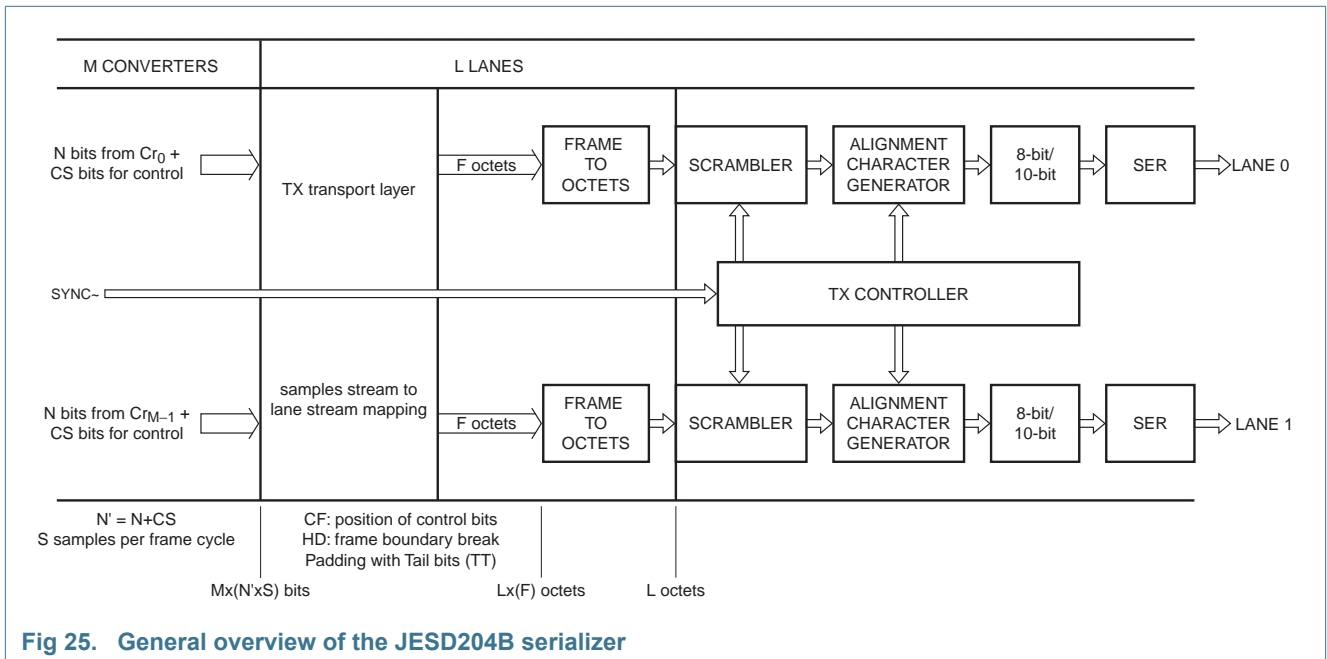


11.3.2 JESD204B serializer

11.3.2.1 Digital JESD204B formatter

The block placed after the ADC1453D cores implements all the JESD204B standard functionalities. This ensures signal integrity and guarantees the clock and the data recovery at the receiver side.

The block is highly configurable in various ways depending on the sampling frequency and the number of lanes used. All the processing and transmission are done with MSB first.



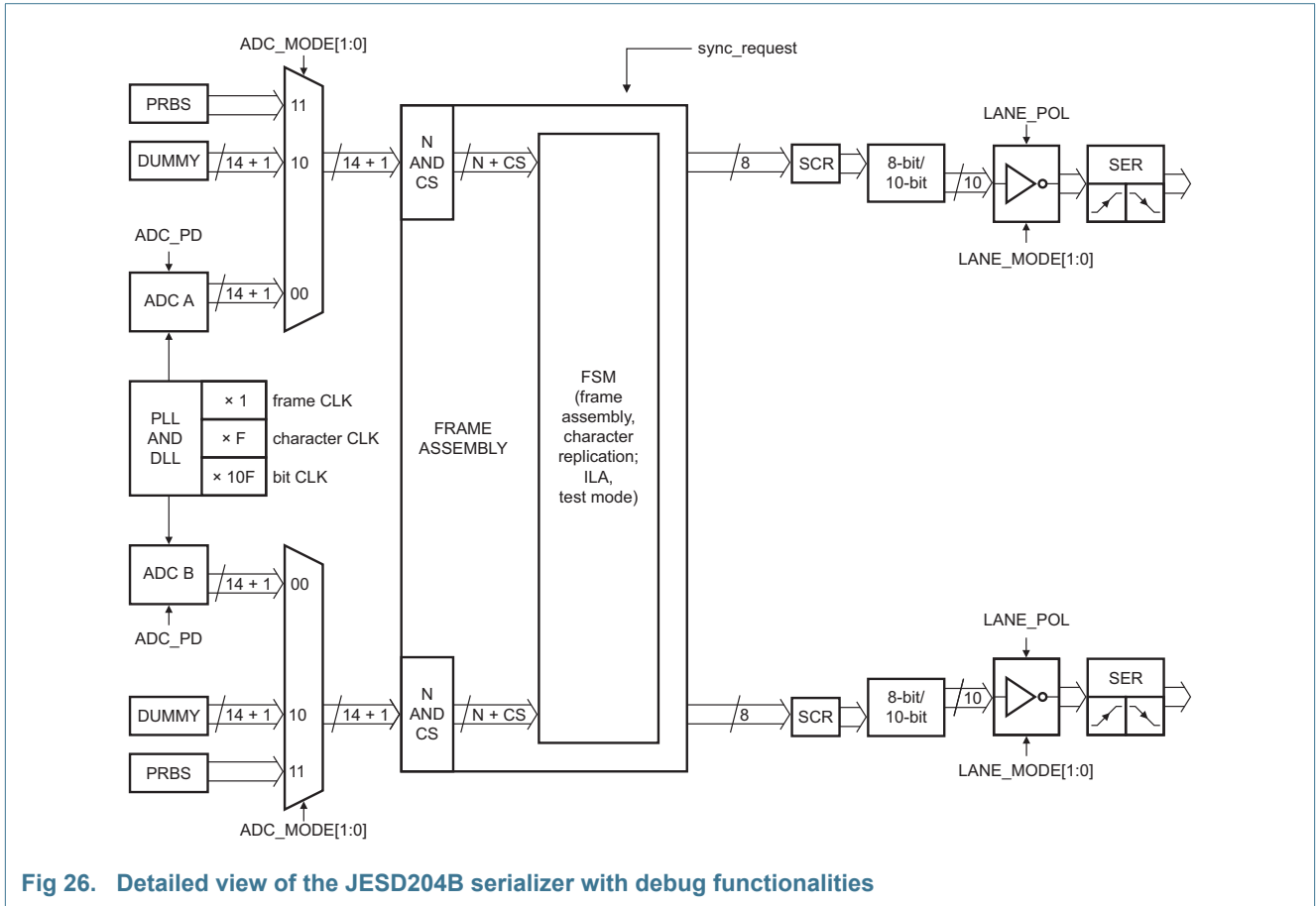


Fig 26. Detailed view of the JESD204B serializer with debug functionalities

11.3.2.2 Scrambler (SCR_EN)

The main purpose of scrambling is to avoid the spectral peaks that would be produced when the same data octet repeats from frame to frame. In general, scrambling makes the spectrum data-independent, so that possible frequency-selective effects on the electrical interface will not cause data-dependent errors. However, all digital operations in converters (including scrambling) cause some amount of switching noise, so there may be applications where it is of advantage to disable the scrambling.

The scrambler can be selected via the pin SCR_EN or the SPI registers (bit SCR_EN in [Table 58](#)).

Table 14. Scrambler configuration

| Pin SCR_EN | Scrambler |
|------------|-----------|
| HIGH | enabled |
| LOW | disabled |

An internal pull-up resistor (50 kΩ) sets pin SCR_EN to HIGH when no signal is connected to it. The pin SCR_EN is active only at start-up or after a JESD204B reset (bit SCR_EN in [Table 42](#)).

11.3.3 OuT-of-Range (OTR)

An out-of-range signal is provided on pins OTRA and OTRB. The OTR signal goes logic level HIGH when the input signal exceeds the maximum full scale range.

The latency of OTR is 31 clock cycles. The OTR response can be speeded up by enabling fast OTR using SPI local registers (bit FAST_OTR in [Table 37](#)). In this mode, the latency of OTR is reduced to only 11 clock cycles. The fast OTR detection threshold (below full-scale) can be programmed using the SPI local registers (bits FAST_OTR_DET[2:0] in [Table 37](#)).

Table 15. Fast OTR register threshold

| FAST_OTR_DET[2:0] | Detection level (dB) |
|-------------------|----------------------|
| 000 | -18.06 |
| 001 | -14.54 |
| 010 | -12.04 |
| 011 | -8.52 |
| 100 | -6.02 |
| 101 | -4.08 |
| 110 | -2.5 |
| 111 | -1.16 |

11.3.4 Digital offset

By default, the ADC1453D delivers an output code that corresponds to the analog input. However, it is possible to add a digital offset to the output code using the SPI local registers (bits DIG_OFFSET[5:0] in see [Table 16](#) and [Table 33](#)). The digital offset adjustment is coded in two's complement.

Table 16. Digital offset adjustment

Default values are shown highlighted.

| DIG_OFFSET[5:0] | Digital offset adjustment (LSB) |
|-----------------|---------------------------------|
| 10 0000 | -32 |
| 10 0001 | -31 |
| ... | ... |
| 11 1111 | -1 |
| 00 0000 | 0 |
| 00 0001 | +1 |
| ... | ... |
| 01 1110 | +30 |
| 01 1111 | +31 |

11.3.5 Test patterns

The ADC1453D can be configured to transmit a number of predefined test patterns using the SPI local registers (bits TEST_PAT_SEL[2:0] in [Table 17](#) and [Table 34](#)). The selected test pattern is transmitted regardless of the analog input.

Table 17. Digital test pattern selection

Default values are shown highlighted.

| TEST_PAT_SEL[2:0] | Digital test pattern |
|-------------------|----------------------------------|
| 000 | Off |
| 001 | Mid code |
| 010 | Min code |
| 011 | Max code |
| 100 | Toggle '1111..1111'/'0000..0000' |
| 101 | Custom test pattern |
| 110 | '0101..0101' |
| 111 | '1010..1010' |

A custom test pattern can be defined using the SPI local registers (bits TEST_PAT_USER[13:6] in [Table 35](#) and bits TEST_PAT_USER[5:0] in [Table 36](#)).

11.3.6 Output data format selection

The ADC1453D output data format can be selected (offset binary, two's complement or gray code) using the SPI local registers (bits DATA_FORMAT[1:0] in [Table 32](#)).

11.3.7 Output codes versus input voltage

Table 18. Output codes

| $V_{INP} - V_{INM}$ | Offset binary | Two's complement | Gray code | OTR |
|---------------------|-------------------|-------------------|-------------------|-----|
| < -1 | 00 0000 0000 0000 | 10 0000 0000 0000 | 00 0000 0000 0000 | 1 |
| -1 | 00 0000 0000 0000 | 10 0000 0000 0000 | 00 0000 0000 0000 | 0 |
| -0.99987793 | 00 0000 0000 0001 | 10 0000 0000 0001 | 00 0000 0000 0001 | 0 |
| -0.99975586 | 00 0000 0000 0010 | 00 0000 0000 0010 | 00 0000 0000 0011 | 0 |
| ... | ... | ... | ... | 0 |
| -0.00024414 | 01 1111 1111 1110 | 11 1111 1111 1110 | 01 0000 0000 0001 | 0 |
| -0.00012207 | 01 1111 1111 1111 | 11 1111 1111 1111 | 01 0000 0000 0000 | 0 |
| +0.00012207 | 10 0000 0000 0000 | 00 0000 0000 0000 | 11 0000 0000 0000 | 0 |
| +0.0.00024414 | 10 0000 0000 0001 | 00 0000 0000 0001 | 11 0000 0000 0001 | 0 |
| ... | ... | ... | ... | 0 |
| +0.99975586 | 11 1111 1111 1101 | 01 1111 1111 1101 | 10 0000 0000 0011 | 0 |
| +0.99987793 | 11 1111 1111 1110 | 01 1111 1111 1110 | 10 0000 0000 0001 | 0 |
| +1 | 11 1111 1111 1111 | 01 1111 1111 1111 | 10 0000 0000 0000 | 0 |
| > +1 | 11 1111 1111 1111 | 01 1111 1111 1111 | 10 0000 0000 0000 | 1 |

11.4 Configuration pins (CFG0, CFG1, CFG2, CFG3)

The configuration pins are only active as inputs at start-up. The values on those pins are read once to set up the device. Then the pins become outputs (OTRA and OTRB). Any further modification must be applied via SPI registers.

Each of these pins is internally connected to a 50 k Ω pull-down resistor. In case of harmonic sampling, it is recommended to connect externally a 1 k Ω pull-up resistor in order to start in power-down mode.

Table 19. JESD204B configuration table

| CFG 3 | CFG 2 | CFG 1 | CFG 0 | ADC A | ADC B | Lane A | Lane B | F ^[1] | HD ^[1] | K ^[1] | M ^[1] | L ^[1] |
|-------|-------|-------|-------|-------|-------|--------|----------|------------------|-------------------|------------------|------------------|------------------|
| 0 | 0 | 0 | 0 | ON | ON | ON | ON | 2 | 0 | 9 | 2 | 2 |
| 0 | 0 | 0 | 1 | ON | ON | ON | OFF | 4 | 0 | 5 | 2 | 1 |
| 0 | 0 | 1 | 0 | ON | ON | OFF | ON | 4 | 0 | 5 | 2 | 1 |
| 0 | 0 | 1 | 1 | | | | reserved | | | | | |
| 0 | 1 | 0 | 0 | | | | reserved | | | | | |
| 0 | 1 | 0 | 1 | ON | OFF | ON | OFF | 2 | 0 | 9 | 1 | 1 |
| 0 | 1 | 1 | 0 | ON | OFF | OFF | ON | 2 | 0 | 9 | 1 | 1 |
| 0 | 1 | 1 | 1 | | | | reserved | | | | | |
| 1 | 0 | 0 | 0 | | | | reserved | | | | | |
| 1 | 0 | 0 | 1 | ON | OFF | ON | ON | 1 | 1 | 17 | 1 | 2 |
| 1 | 0 | 1 | 0 | | | | reserved | | | | | |
| 1 | 0 | 1 | 1 | | | | reserved | | | | | |
| 1 | 1 | 0 | 0 | | | | reserved | | | | | |
| 1 | 1 | 0 | 1 | | | | reserved | | | | | |
| 1 | 1 | 1 | 0 | | | | reserved | | | | | |
| 1 | 1 | 1 | 1 | OFF | OFF | OFF | OFF | 2 | 0 | 9 | 2 | 2 |

- [1] F: Octets per frame clock cycle
 HD: High-density mode
 K: Frame per multi-frame
 M: Converters per device
 L: Lane per converter device

For all the configurations, the number of control bit per conversion sample (CS) is 1, the number of control words per frame clock cycle and link (CF) is 0, the number of samples transmitter per single converter per frame cycle (S) is 1 and the formula $(F \times K) \geq 17$ is always verified.

11.5 Serial Peripheral Interface (SPI)

11.5.1 Register description

The ADC1453D serial interface is a synchronous serial communication port, which allows easy interfacing with many commonly used microprocessors. It provides access to the registers controlling the operation of the chip.

The register bits are either global or local functions:

- A global function operates over the full IC behavior. A local function operates on one or several previously selected channels only. If a channel is selected, the next WRITE command in the local registers applies to the selected channel. The WRITE command has no impact on channels that are not selected. This makes it possible to apply different configurations on each channel by first selecting a specific channel and then all the related settings.
- Select only one channel during a READ operation of the local registers. If several channels are selected, the READ operation occurs on the channel A.

Programming all registers at the same time is required:

- The IC allows the storage of a set of settings for the addresses 06h to 23h, which enables the configuration of all registers simultaneously by setting bit TRANSFER to HIGH (see [Table 40](#)). This bit is auto-clearing. This function can be disabled using SPI (bit TRANS_DIS in [Table 40](#)). The registers are then updated at each WRITE operation.
- The transfer function does not apply to a READ operation.

The SPI interface is configured as a 3-wire type: pin SDIO is the bidirectional pin, pin SCLK is the serial clock input and SCS_N is the chip select pin.

A LOW level on pin SCS_N initiates each READ/WRITE operation. A minimum of 3 bytes is transmitted (two instruction bytes and at least 1 DATA byte; see [Table 21](#)).

Table 20. Instruction bytes for the SPI

| Bit: | 7 (MSB) | 6 | 5 | 4 | 3 | 2 | 1 | 0 (LSB) |
|-------------|-------------------|----|----|-----|-----|-----|----|---------|
| Description | R/ \overline{W} | W1 | W0 | A12 | A11 | A10 | A9 | A8 |
| | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |

- Bit R/ \overline{W} indicates whether it is a READ (when HIGH) or a WRITE (when LOW) operation.
- Bits W1 and W0 indicate the number of bytes to be transferred after both instruction bytes (see [Table 21](#)).

Table 21. Number of data bytes transferred

| W1 | W0 | Number of bytes transferred |
|----|----|-----------------------------|
| 0 | 0 | 1 byte |
| 0 | 1 | 2 bytes |
| 1 | 0 | 3 bytes |
| 1 | 1 | 4 or more bytes |

- Bits A12 to A0 indicate the address of the register being accessed. If it concerns a multiple byte transfer, this address is the first register accessed. An address counter is increased to access subsequent addresses.

The steps for a data transfer are:

1. Communication starts with the first rising edge on pin SCLK after a falling edge on pin SCS_N.
2. The first phase is the transfer of the 2-byte instruction.
3. The second phase is the transfer of the data. Its length varies, but it is always a multiple of 8 bits. The MSB is always sent first (for instruction and data bytes).
4. A rising edge on pin SCS_N indicates the end on data transmission.

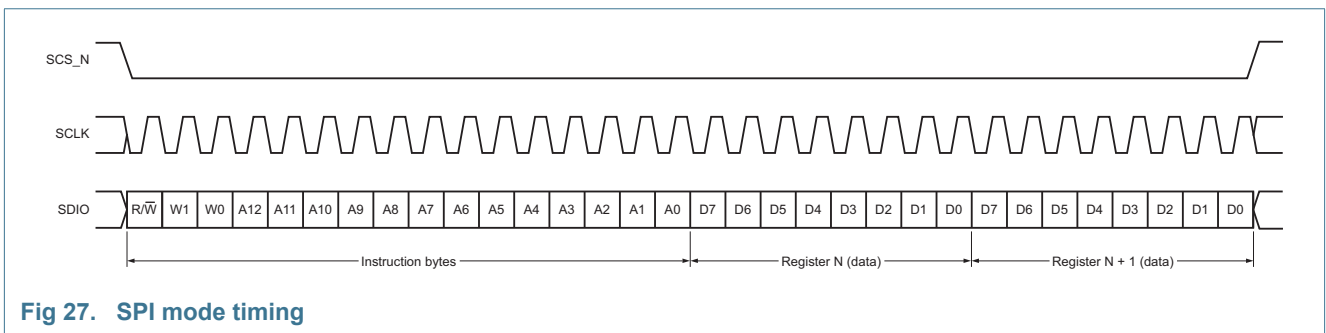


Fig 27. SPI mode timing

11.5.2 Start-up programming

At power-up or after a reset by SPI, the device needs a start-up programming for optimum performances. This initialization is done in 3 steps:

Table 22. Step 1 - Clock divider programming

| register address (hex) | value (hex) | comment |
|------------------------|--|------------------------------|
| 0007 | CLK_DIV[2:0] in Table 29 | in case of harmonic clocking |

Table 23. Step 2 - JESD204B initialization

| register address (hex) | value (hex) | comment |
|------------------------|--|--------------------------------|
| 080c | 01 | |
| 080c | 00 | |
| 0803 | CFG_SETUP[3:0] in Table 43 | JESD204B configuration |
| 0802 | 08 | frame assembler subclock reset |

Table 24. Step 3 - ADC core initialization

| register address (hex) | ADC1453D250 value (hex) | comment |
|------------------------|-------------------------|---|
| 0100 | d1 | |
| 0200 | 01 | |
| 00ff | 80 | registers updated on each WRITE command |
| 0012 | 0f | |
| 0024 | 01 | |
| 0040 | 80 | |
| 040a | 05 | |
| 0102 | 07 | |
| 0103 | 67 | |
| 0108 | 93 | |
| 0109 | 02 | |
| 010a | C5 | |
| 010b | 01 | |
| 0160 | ff | |
| 0161 | 1f | |
| 0170 | 10 | |
| 0171 | 10 | |
| 0400 | 00 | |
| 0401 | 18 | |
| 0409 | 10 | |
| - | - | wait for 200 ms |
| 0004 | 08 | |
| - | - | wait for 200 ms |
| 0004 | 40 | |
| - | - | wait for 200 ms |
| 0004 | 20 | |

Table 24. Step 3 - ADC core initialization

| register address (hex) | ADC1453D250 value (hex) | comment |
|------------------------|-------------------------|-----------------|
| - | - | wait for 200 ms |
| 0004 | 10 | |
| - | - | wait for 200 ms |
| 0409 | - | |

Those registers adjust some specific currents and timings. The programmed values should not be modified by the customer to ensure proper behavior over temperature and power supply variations.

11.5.3 Register allocation map

Table 25 shows an overview of all registers.

Table 25. Register allocation map

| Addr. (hex) | Register name | R/W | Bit definition | | | | | | | | Default |
|------------------------------|------------------|-----|-----------------------------|---------------|-------|----------|------------------|-------------------|-----------------------------|---------------|-----------|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| ADC control registers | | | | | | | | | | | |
| 0000h | CHIP_RST | RW | SW_RST[7:0] | | | | | | | | 0000 0000 |
| 0001h | CHIP_ID | R | CHIP_ID[7:0] ^[1] | | | | | | | | 0100 0011 |
| 0005h | SW_RST | R/W | SW_RST | - | - | - | - | - | - | - | 0000 0000 |
| 0006h | OP_MODE | R/W | - | - | - | - | - | - | OP_MODE[1:0] ^[3] | | 0000 0000 |
| 0007h | CLK_CFG | R/W | - | - | - | SE_SEL | DIFF_SE | CLK_DIV[2:0] | | | 0000 0000 |
| 0008h | INTERNAL_REF | R/W | - | - | - | - | - | INTREF[2:0] | | | 0000 0000 |
| 0009h | CHANNEL_SEL | R/W | - | - | - | - | - | - | ADC_B | ADC_A | 0000 1111 |
| 0011h | OUTPUT_CFG | R/W | - | - | - | - | - | DATA_SWAP | DATA_FORMAT[1:0] | | 0000 0000 |
| 0013h | DIG_OFFSET | R/W | DIG_OFFSET[5:0] | | | | | | - | - | 0000 0000 |
| 0014h | TEST_CFG_1 | R/W | - | - | - | - | - | TEST_PAT_SEL[2:0] | | | 0000 0000 |
| 0015h | TEST_CFG_2 | R/W | TEST_PAT_USER[13:6] | | | | | | | | 0000 0000 |
| 0016h | TEST_CFG_3 | R/W | TEST_PAT_USER[5:0] | | | | | | - | - | 0000 0000 |
| 0017h | OTR_CFG | R/W | - | - | - | RESERVED | FAST_OTR | FAST_OTR_DET[2:0] | | | 0001 0100 |
| 0042h | GRD_CTRL | R/W | RESERVED | | | | CLK_DELAY[3:0] | | | | 0000 0000 |
| 0043h | DCS_CTRL | R/W | RESERVED | | | | | | DIV_RESET_POL | DIV_RESET_SEL | 1100 0100 |
| 00Ffh | TRANS_CFG | R/W | TRANS_DIS | TRANSFER | - | - | - | - | - | - | 0000 0000 |
| JESD204B control | | | | | | | | | | | |
| 0801h | IP_STATUS | R | RXSYNC_ERR_FLG | RESERVED[5:0] | | | | | | PLL_LOCK | 0100 0010 |
| 0802h | IP_RST | R/W | SW_RST | - | - | - | ASSEMBLER_SW_RST | - | - | - | 0000 0000 |

Table 25. Register allocation map ...continued

| Addr. (hex) | Register name | R/W | Bit definition | | | | | | | Default | |
|----------------|------------------|-----|-------------------|------------------|---------------|-----------|-----------------|--------------|--------------------|-----------|-----------|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | | Bit 0 |
| 0803h | IP_CFG_SETUP | R/W | - | - | - | - | CFG_STP[3:0] | | | 0000 0000 | |
| 0805h | IP_CTRL1 | R/W | RESERVED | TRISTATE_CFG_PAD | SYNCB_POL | SYNCB_SE | EN_RXSYNC_ERR | RESERVED | | | 0000 1001 |
| 0806h | IP_CTRL2 | R/W | RESERVED | | | | | SWP_LANE_A_B | SWP_ADC_A_B | | 0011 0100 |
| 080Bh | IP_PRBS_CTRL | R/W | RESERVED | | | | | PRBS_TYPE | RES | | 0000 0000 |
| 0810h | JESD204B_C_TRL1 | R/W | LMFC_periodic_rst | LMFC_reset_en | - | - | - | - | - | 0000 0000 | |
| 0811h | JESD204B_C_TRL2 | R/W | DCS_periodic_rst | DCS_reset_en | - | - | - | - | - | 0000 0000 | |
| 0812h | JESD204B_C_TRL3 | R/W | - | - | - | - | sync_at_lmfc_en | - | sync_captur_e_path | 0000 0000 | |
| 0816h | IP_DEBUG_OUT1 | R/W | - | - | - | - | - | - | PAT_OUT[9:8] | 0000 0010 | |
| 0817h | IP_DEBUG_OUT2 | R/W | PAT_OUT[7:0] | | | | | | | 1010 1010 | |
| 0818h | IP_DEBUG_IN1 | R/W | PAT_IN[15:8] | | | | | | | 1110 0110 | |
| 0819h | IP_DEBUG_IN2 | R/W | PAT_IN[7:0] | | | | | | | 1110 1010 | |
| 081Bh | IP_TESTMODE | R/W | RESERVED | LOOP_ALIGN | DIS_REPL_CHAR | BYP_ALIGN | RESERVED | | | 0000 0000 | |
| 081Ch | IP_EXPERT_DOOR | R/W | KEY[7:0] | | | | | | | 0000 0000 | |
| 081Eh | SYSREF_CFG | R/W | - | - | - | - | SYSREF_EN | SYSREF_SE | - | 0000 0000 | |
| 0822h | SCR_L | R/W | SCR_EN | RESERVED | | | | | L | 0000 0001 | |
| 0824h | CFG_K | R/W | - | - | - | K[4:0] | | | | 000x xxxx | |
| 0827h | JESD_SUB | R/W | SUBCLASS[2:0] | | | RESERVED | | | | 000x xxxx | |
| 0828h | JESD_VER | R/W | VERSION[2:0] | | | - | - | RESERVED | | | 0000 0xxx |

Table 25. Register allocation map ...continued

| Addr. (hex) | Register name | R/W | Bit definition | | | | | | | | Default |
|----------------|--------------------|-----|----------------|-------|---------------|----------------|-------|------------|------------|-------------|-----------|
| | | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | |
| 086Bh | OUTBUF_A_ SWING | R/W | RESERVED | | | | | SWING[2:0] | | | 0000 0011 |
| 086Ch | OUTBUF_B_ SWING | R/W | RESERVED | | | | | | SWING[2:0] | | 0000 0011 |
| 0871h | LANE_A_0_ CTRL | R/W | RESERVED | | | LANE_MODE[1:0] | | LANE_POL | RESERVED | LANE_ PD | 0000 0000 |
| 0872h | LANE_B_0_ CTRL | R/W | RESERVED | | | LANE_MODE[1:0] | | LANE_POL | RESERVED | LANE_ PD | 0000 0000 |
| 0890h | ADC_A_0_ CTRL | R/W | - | - | ADC_MODE[1:0] | | - | - | - | ADC_ PD | 0000 0000 |
| 0891h | ADC_B_0_ CTRL | R/W | - | - | ADC_MODE[1:0] | | - | - | - | ADC_ PD | 0000 0000 |

- [1] The READ-ONLY and RESERVED registers.
 [2] The registers influenced by the TRANSFER function.
 [3] The LOCAL registers.

11.5.4 Detailed register description

The tables in this section contain detailed descriptions of the registers.

11.5.4.1 ADC control registers

Table 26. CHIP_RESET register (address 0000h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|-------|--|
| 7 to 0 | SW_RST | R/W | - | resets global and local registers for any value “1” written at any bit (auto-clear). |

Table 27. SW_RESET register (address 0005h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|-------|--|
| 7 | SW_RST | R/W | 0 | resets global and local registers no reset |
| | | | 1 | performs a reset to the default values (auto-clear) |
| 6 to 0 | - | - | - | not used |

Table 28. OP_MODE register (address 0006h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------------|--------|-------|---|
| 7 to 2 | - | - | - | not used |
| 1 to 0 | OP_MODE[1:0] ^[1] | R/W | 00 | operating mode for the selected channel normal (power-up) |
| | | | 01 | power-down |
| | | | 10 | sleep |
| | | | 11 | not used |

[1] Local register.

Table 29. CLK_CFG register (address 0007h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------|--------|-------|--|
| 7 to 5 | - | - | - | not used |
| 4 | SE_SEL | R/W | 0 | single-ended clock input pin selection CLKP |
| | | | 1 | CLKM |
| 3 | DIFF_SE | R/W | 0 | differential/single-ended clock input selection fully differential |
| | | | 1 | single-ended |

Table 29. CLK_CFG register (address 0007h) bit description ...continued

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|------------|-------------------------|
| 2 to 0 | CLK_DIV[2:0] | R/W | | clock divider selection |
| | | | 000 | divide by 1 |
| | | | 001 | divide by 2 |
| | | | 010 | divide by 3 |
| | | | 011 | divide by 4 |
| | | | 100 | divide by 5 |
| | | | 101 | divide by 6 |
| | | | 110 | divide by 7 |
| | | | 111 | divide by 8 |

Table 30. INTERNAL_REF register (address 0008h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------|--------|------------|------------------------------|
| 7 to 3 | - | - | - | not used |
| 2 to 0 | INTREF[2:0] ^[1] | R/W | 000 | see Table 11 |

[1] Local register

Table 31. CHANNEL_SEL register (address 0009h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|----------|---|
| 7 to 2 | - | - | - | not used |
| 1 | ADC_B | R/W | | channel B selection for next SPI operation in local registers |
| | | | 0 | not selected |
| | | | 1 | selected |
| 0 | ADC_A | R/W | | channel A selection for next SPI operation in local registers |
| | | | 0 | not selected |
| | | | 1 | selected |

Table 32. OUTPUT_CFG register (address 0011h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------------|--------|-----------|--------------------------|
| 7 to 3 | - | - | - | not used |
| 2 | DATA_SWAP ^[1] | R/W | | output data bits swapped |
| | | | 0 | no swapping |
| | | | 1 | MSBs swapped with LSBs |
| 1 to 0 | DATA_FORMAT[1:0:] ^[1] | R/W | | output data format |
| | | | 00 | offset binary |
| | | | 01 | two's complement |
| | | | 10 | gray code |
| | | | 11 | offset binary |

[1] Local register

Table 33. DIG_OFFSET register (address 0013h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------------------|--------|---------------|------------------------------|
| 7 to 2 | DIG_OFFSET[7:0] ^[1] | R/W | 000000 | see Table 16 |
| 1 to 0 | - | - | - | not used |

[1] Local register

Table 34. TEST_CFG_1 register (address 0014h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------------|--------|------------|------------------------------|
| 7 to 3 | - | - | - | not used |
| 2 to 0 | TEST_PAT_SEL[2:0] ^[1] | R/W | 000 | see Table 17 |

[1] Local register

Table 35. TEST_CFG_2 register (address 0015h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------------------------|--------|-----------------|--|
| 7 to 0 | TEST_PAT_USER[13:6] ^[1] | R/W | 00000000 | custom digital test pattern (bits 13 to 6) |

[1] Local register

Table 36. TEST_CFG_3 register (address 0016h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------------------|--------|---------------|---|
| 7 to 2 | TEST_PAT_USER[5:0] ^[1] | R/W | 000000 | custom digital test pattern (bits 5 to 0) |
| 1 to 0 | - | - | - | not used |

[1] Local register

Table 37. OTR_CFG register (address 0017h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------------|--------|------------|------------------------------------|
| 7 to 5 | - | - | - | not used |
| 4 | RESERVED | R/W | 1 | reserved |
| 3 | FAST_OTR ^[1] | R/W | 0 | Selection OTR full-scale/ fast OTR |
| | | | 1 | OTR full-scale fast OTR |
| 2 to 0 | FAST_OTR_DET[2:0] ^[1] | R/W | 100 | see Table 15 |

[1] Local register

Table 38. GRD_CTRL register (address 0042h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-------------|---|
| 7 to 4 | RESERVED | R/W | 0000 | reserved |
| 3 to 0 | CLK_DELAY[3:0] | R/W | 0000 | number of delay step expressed in half device clock period unit |

Table 39. DCS_CTRL register (address 0043h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|----------|---|
| 7 to 2 | RESERVED | R/W | 110001 | reserved |
| 1 | DIV_RESET_POL | R/W | 0 | Polarity of the DCS reset falling edge (Subclass 2) |
| | | | 1 | Rising edge (Subclass 1) |
| 0 | DIV_RESET_SEL | R/W | 0 | DCS reset selection SYNCBP/N is used (Subclass 2) |
| | | | 1 | SYSREFP/N is used (Subclass 1) |

Table 40. TRANS_CFG register (address 00FFh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|----------|---|
| 7 | TRANS_DIS | R/W | 0 | disable transfer function transfer function active |
| | | | 1 | registers updated on a WRITE command |
| 6 | TRANSFER | R/W | 0 | updates the registers with the written settings settings are stored |
| | | | 1 | registers updated (auto-clear) |
| 5 to 0 | - | - | - | not used |

11.5.4.2 JESD204B control registers

Table 41. IP_STATUS register (address 0801h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|---------------|---|
| 7 | RXSYNC_ERR_FLG | R | 0 1 | RX synchronization error no error synchronization error has occurred |
| 6 to 1 | RESERVED | R/W | 100001 | reserved |
| 0 | PLL_LOCK | R | 0 1 | JEDEC PLL lock unlocked locked |

Table 42. IP_RESET register (address 0802h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|---------------|--|
| 7 | SW_RST | R/W | 0 1 | resets All JESD204B sub-blocks and registers no reset performs a reset to the default values (auto-clear) |
| 6 to 4 | - | - | - | not used |
| 3 | ASSEMBLER_SW_RST | R/W | 0 1 | resets RXSYNC_ERR_FLG register bit and the frame assembler sub-block no reset performs a reset to the default values (auto-clear) |
| 2 to 0 | - | - | - | not used |

Table 43. IP_CFG_SETUP register (address 0803h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-------------|------------------------------|
| 7 to 4 | - | - | - | not used |
| 3 to 0 | CFG_SETUP[3:0] | R/W | 0000 | see Table 44 |

Table 44. JESD204B configuration table

| CFG_SETUP [3:0] | ADC A | ADC B | Lane A | Lane B | F ^[1] | HD ^[1] | K ^[1] | M ^[1] | L ^[1] | Lane A serial frequency | Lane B serial frequency |
|-----------------|-----------|-----------|-----------|-----------|------------------|-------------------|------------------|------------------|------------------|-------------------------|-------------------------|
| 0000 | ON | ON | ON | ON | 2 | 0 | 9 | 2 | 2 | 20 × f _s | 20 × f _s |
| 0001 | ON | ON | ON | OFF | 4 | 0 | 5 | 2 | 1 | 40 × f _s | 0 |
| 0010 | ON | ON | OFF | ON | 4 | 0 | 5 | 2 | 1 | 0 | 40 × f _s |
| 0011 | | | | | | | | | | reserved | |
| 0100 | | | | | | | | | | reserved | |
| 0101 | ON | OFF | ON | OFF | 2 | 0 | 9 | 1 | 1 | 20 × f _s | 0 |
| 0110 | ON | OFF | OFF | ON | 2 | 0 | 9 | 1 | 1 | 0 | 20 × f _s |
| 0111 | | | | | | | | | | reserved | |
| 1000 | | | | | | | | | | reserved | |
| 1001 | ON | OFF | ON | ON | 1 | 1 | 17 | 1 | 2 | 10 × f _s | 10 × f _s |

Table 44. JESD204B configuration table ...continued

| CFG_SETUP [3:0] | ADC A | ADC B | Lane A | Lane B | F ^[1] | HD ^[1] | K ^[1] | M ^[1] | L ^[1] | Lane A serial frequency | Lane B serial frequency |
|-----------------|-------|-------|--------|--------|------------------|-------------------|------------------|------------------|------------------|-------------------------|-------------------------|
| 1010 | | | | | | | | | | | reserved |
| 1011 | | | | | | | | | | | reserved |
| 1100 | | | | | | | | | | | reserved |
| 1101 | | | | | | | | | | | reserved |
| 1110 | | | | | | | | | | | reserved |
| 1111 | OFF | OFF | OFF | OFF | 2 | 0 | 9 | 2 | 2 | 0 | 0 |

[1] F: Octets per frame clock cycle

HD: High-density mode

K: Frame per multi-frame

M: Converters per device

L: Lane per converter device

For all the configurations, the number of control bit per conversion sample (CS) is 1, the number of control words per frame clock cycle and link (CF) is 0, the number of samples transmitter per single converter per frame cycle (S) is 1 and the formula $(F \times K) \geq 17$ is always verified.

Table 45. IP_CTRL1 register (address 0805h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|--|
| 7 | RESERVED | R/W | 0 | reserved |
| 6 | TRISTATE_CFG_PAD | R/W | 0 | CFG pad in tri-state mode |
| | | | 1 | CFG Pads in Output mode |
| | | | 1 | CFG Pads in Input mode; operating at power-up |
| 5 | SYNCB_POL | R/W | 0 | selects synchronization polarity |
| | | | 1 | synchronization active HIGH |
| | | | 0 | synchronization active LOW |
| 4 | SYNCB_SE | R/W | 0 | selects single-ended or differential synchronization |
| | | | 1 | single-ended synchronization on SYNCBP |
| | | | 0 | differential synchronization |
| 3 | EN_RXSYNC_ERR | R/W | 0 | SYNC error reporting |
| | | | 1 | disabled |
| | | | 1 | enabled |
| 2 to 0 | RESERVED | R/W | 001 | reserved |

Table 46. IP_CTRL2 register (address 0806h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|--------|---------------------------|
| 7 to 2 | RESERVED | R/W | 001101 | reserved |
| 1 | SWP_LANE_A_B | R/W | 0 | swaps the lanes |
| | | | 1 | no swap |
| | | | 1 | lane A and B are inverted |

Table 46. IP_CTRL2 register (address 0806h) bit description ...continued

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-------------|--------|-------|---|
| 0 | SWP_ADC_A_B | R/W | | swaps the ADC at the input of the frame assembler |
| | | | 0 | no swap |
| | | | 1 | ADC A and B are inverted |

Table 47. IP_PRBS_CTRL register (address 080Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|--------|--|
| 7 to 2 | RESERVED | R/W | 000000 | reserved |
| 1 | PRBS_TYPE | R/W | | Pseudo-Random Binary Sequence (PRBS) pattern selection |
| | | | 0 | PRBS-7; $1 + x^6 + x^7$ |
| | | | 1 | PRBS-23; $1 + x^{18} + x^{23}$ |
| 0 | RESERVED | R/W | 0 | reserved |

Table 48. JESD204B_CTRL1 register (address 0810h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|--|
| 7 | LMFC_periodic_rst | R/W | | LMFC mode definition |
| | | | 0 | LMFC reset is done once |
| | | | 1 | LMFC reset at each SYSREF or SYNC pulse |
| 6 | LMFC_reset_en | R/W | | LMFC reset selection |
| | | | 0 | LMFC reset is disabled (Subclass 0) |
| | | | 1 | LMFC reset is enabled (Subclass 1 and 2) |
| 5 to 0 | RESERVED | R/W | 00000 | reserved |

Table 49. JESD204B_CTRL2 register (address 0811h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|--|
| 7 | DCS_periodic_rst | R/W | | DCS mode definition |
| | | | 0 | DCS reset is done once |
| | | | 1 | DCS reset at each SYSREF or SYNC pulse |
| 6 | DCS_reset_en | R/W | | DCS reset selection |
| | | | 0 | DCS reset is disabled |
| | | | 1 | DCS reset is enabled |
| 5 to 0 | RESERVED | R/W | 00000 | reserved |

Table 50. JESD204B_CTRL3 register (address 0812h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|--|
| 7 to 4 | RESERVED | R/W | 0000 | reserved |
| 3 | sync_at_lmfc_en | R/W | 0 | defines the relation between SYNC and LMFC SYNC is fetched directly (Subclass 0) |
| | | | 1 | SYNC is taken at next LMFC boundary (Subclass 1 and Subclass 2) |
| 2 | RESERVED | R/W | 0 | reserved |
| 1 | sync_capture_path | R/W | 0 | selects SYNC mode Subclass 0 |
| | | | 1 | Subclass 1 and Subclass 2 |
| 0 | RESERVED | R/W | 0 | reserved |

Table 51. IP_DEBUG_OUT1 register (address 0816h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-----------|--|
| 7 to 2 | - | - | - | not used |
| 1 to 0 | PATTERN_OUT[9:8] | R/W | 10 | 2 most significant bits of output stage debug word (inserted just before serializer) |

Table 52. IP_DEBUG_OUT2 register (address 0817h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|------------------|---|
| 7 to 0 | PATTERN_OUT[7:0] | R/W | 1010 1010 | 8 least significant bits of output stage debug word (inserted just before serializer) |

Table 53. IP_DEBUG_IN1 register (address 0818h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|------------------|---|
| 7 to 0 | PATTERN_IN[15:8] | R/W | 1110 0110 | 8 most significant bits of input stage debug word (inserted in place of ADC data) |

Table 54. IP_DEBUG_IN2 register (address 0819h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|------------------|--|
| 7 to 0 | PATTERN_IN[7:0] | R/W | 1110 1010 | 8 least significant bits of input stage debug word (inserted in place of ADC data) |

Table 55. IP_TESTMODE register (address 081Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|------------|--------|-------|---|
| 7 | RESERVED | R/W | 0 | reserved |
| 6 | LOOP_ALIGN | R/W | 0 | continuous ILA ^[1] sequence normal operation |
| | | | 1 | ILA ^[1] repeated continuously |

Table 55. IP_TESTMODE register (address 081Bh) bit description ...continued

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|--|
| 5 | DIS_REPL_CHAR | R/W | | character replacement function selection |
| | | | 0 | normal operation |
| | | | 1 | character replacement disabled |
| 4 | BYP_ALIGN | R/W | | ILA ^[1] sequence function selection |
| | | | 0 | normal operation |
| | | | 1 | ILA ^[1] sequence disabled |
| 3 to 0 | RESERVED | R/W | 0000 | reserved |

[1] ILA = Initial Lane Alignment Sequence (see JESD204 JEDEC standard).

Table 56. IP_EXPERT_DOOR register (address 081Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------|--------|------------------|---|
| 7 to 0 | KEY[7:0] | R/W | 0000 0000 | 8-bit key (0x4a) to enable write access for scrambler (register 0822h) and parameter K (register 0824h) |

Table 57. SYSREF_CFG register (address 081Eh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|---|
| 7 to 4 | RESERVED | R/W | 0000 | reserved |
| 3 | SYSREF_EN | R/W | | enables SYSREFP/N path |
| | | | 0 | SYSREFP/N path disabled |
| | | | 1 | SYSREFP/N path enabled |
| 2 | SYSREF_SE | R/W | | selects single-ended or differential SYSREF |
| | | | 0 | SYSREFP/SYREFN are used as differential pair |
| | | | 1 | SYSREFP is used as single ended SYSREF input |
| 1 to 0 | RESERVED | R/W | 00 | reserved |

Table 58. SCR_L register (address 0822h) bit description (IP_EXPERT_DOOR write access needed, address 081Ch)

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------|--------|--------|--------------------------------|
| 7 | SCR_EN | R/W | | selects the scrambler function |
| | | | 0 | scrambler disabled |
| | | | 1 | scrambler enabled |
| 6 to 1 | RESERVED | R/W | 000000 | reserved |
| 0 | L | R/W | | lanes number minus 1 |
| | | | 0 | 1 lane |
| | | | 1 | 2 lanes |

Table 59. CFG_K register (address 0824h) bit description (IP_EXPERT_DOOR write access needed, address 081Ch)

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------|--------|------------------|---|
| 7 to 5 | - | - | - | not used |
| 4 to 0 | K[4:0] | R/W | 000x xxxx | Number of frames in a multi-frame. Default value depends on the JESD204B configuration. |

Table 60. JESD_SUB register (address 0827h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|------------|---|
| 7 to 5 | SUBCLASS[2:0] | R/W | 000 | JESD204 subclass information to be written for link configuration information |
| 4 to 0 | RESERVED | R/W | xxxxx | reserved |

Table 61. JESD_VER register (address 0828h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|------------|--|
| 7 to 5 | VERSION[2:0] | R/W | 000 | JESD204 version information to be written for link configuration information |
| 4 to 3 | - | - | - | not used |
| 2 to 0 | RESERVED | R/W | xxx | reserved |

Table 62. IP_OUTBUF_A_SWING register (address 086Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|------------|---|
| 7 to 3 | RESERVED[4:0] | R/W | 00000 | reserved |
| 2 to 0 | SWING[2:0] | R/W | | Configurable lane A output current |
| | | | 000 | 12 mA; ± 300 mV (p-p) |
| | | | 001 | 14 mA; ± 350 mV (p-p) |
| | | | 010 | 16 mA; ± 400 mV (p-p) |
| | | | 011 | 18 mA; ± 450 mV (p-p) |
| | | | 100 | 20 mA; ± 500 mV (p-p) |
| | | | 101 | 22 mA; ± 550 mV (p-p) |
| | | | 110 | 24 mA; ± 600 mV (p-p) |
| | | | 111 | 26 mA; ± 650 mV (p-p) |

Table 63. IP_OUTBUF_B_SWING register (address 086Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|------------|---|
| 7 to 3 | RESERVED[4:0] | R/W | 00000 | reserved |
| 2 to 0 | SWING[2:0] | R/W | | Configurable lane B output current |
| | | | 000 | 12 mA; ± 300 mV (p-p) |
| | | | 001 | 14 mA; ± 350 mV (p-p) |
| | | | 010 | 16 mA; ± 400 mV (p-p) |
| | | | 011 | 18 mA; ± 450 mV (p-p) |
| | | | 100 | 20 mA; ± 500 mV (p-p) |
| | | | 101 | 22 mA; ± 550 mV (p-p) |
| | | | 110 | 24 mA; ± 600 mV (p-p) |
| | | | 111 | 26 mA; ± 650 mV (p-p) |

Table 64. IP_LANE_A_0_CTRL register (address 0871h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-----------|---|
| 7 to 5 | RESERVED[2:0] | R/W | 000 | reserved |
| 4 to 3 | LANE_MODE[1:0] | R/W | | debug option directly before serializer |
| | | | 00 | normal mode, ADC path |
| | | | 01 | 0/1 toggle sent over the lanes |
| | | | 10 | IP_DEBUG_OUT value sent over the lanes |
| | | | 11 | 10-bit PRBS pattern is sent over the lane |
| 2 | LANE_POL | R/W | | selects lane polarity |
| | | | 0 | no inversion |
| | | | 1 | lane polarity P/N inverted |
| 1 | RESERVED | R/W | 0 | reserved |
| 0 | LANE_PD | R/W | | Selects lane power mode |
| | | | 0 | lane is powered-up |
| | | | 1 | lane is powered-down |

Table 65. IP_LANE_B_0_CTRL register (address 0872h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-----------|---|
| 7 to 5 | RESERVED[2:0] | R/W | 000 | reserved |
| 4 to 3 | LANE_MODE[1:0] | R/W | | debug option directly before serializer |
| | | | 00 | normal mode, ADC path |
| | | | 01 | 0/1 toggle sent over the lanes |
| | | | 10 | IP_DEBUG_OUT value sent over the lanes |
| | | | 11 | 10-bit PRBS pattern is sent over the lane |
| 2 | LANE_POL | R/W | | selects lane polarity |
| | | | 0 | no inversion |
| | | | 1 | lane polarity P/N inverted |
| 1 | RESERVED | R/W | 0 | reserved |

Table 65. IP_LANE_B_0_CTRL register (address 0872h) bit description ...continued

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|---------|--------|----------|---------------------------|
| 0 | LANE_PD | R/W | | Selects lane power mode |
| | | | 0 | lane is powered-up |
| | | | 1 | lane is powered-down |

Table 66. IP_ADC_A_0_CTRL register (address 0890h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-----------|---|
| 7 to 6 | RESERVED | R/W | 00 | reserved |
| 5 to 4 | ADC_MODE[1:0] | R/W | | debug option at ADC output |
| | | | 00 | normal mode, ADC path |
| | | | 01 | ramp pattern |
| | | | 10 | IP_DEBUG_IN value sent i.s.o. ADC data |
| | | | 11 | 16-bit PRBS pattern is sent i.s.o. ADC data |
| 3 to 1 | RESERVED | R/W | 000 | reserved |
| 0 | ADC_PD | R/W | | selects ADC power mode |
| | | | 0 | ADC is powered-up |
| | | | 1 | ADC is powered-down |

Table 67. IP_ADC_B_0_CTRL register (address 0891h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-----------|---|
| 7 to 6 | RESERVED | R/W | 00 | reserved |
| 5 to 4 | ADC_MODE[1:0] | R/W | | debug option at ADC output |
| | | | 00 | normal mode, ADC path |
| | | | 01 | ramp pattern |
| | | | 10 | IP_DEBUG_IN value sent i.s.o. ADC data |
| | | | 11 | 16-bit PRBS pattern is sent i.s.o. ADC data |
| 3 to 1 | RESERVED | R/W | 000 | reserved |
| 0 | ADC_PD | R/W | | selects ADC power mode |
| | | | 0 | ADC is powered-up |
| | | | 1 | ADC is powered-down |

12. Package outline

VFQFPN56 : plastic thermal enhanced low profile quad flat package; no leads; 56 terminals; resin based; body 8 x 8 x 1.35 mm

PSC-4449

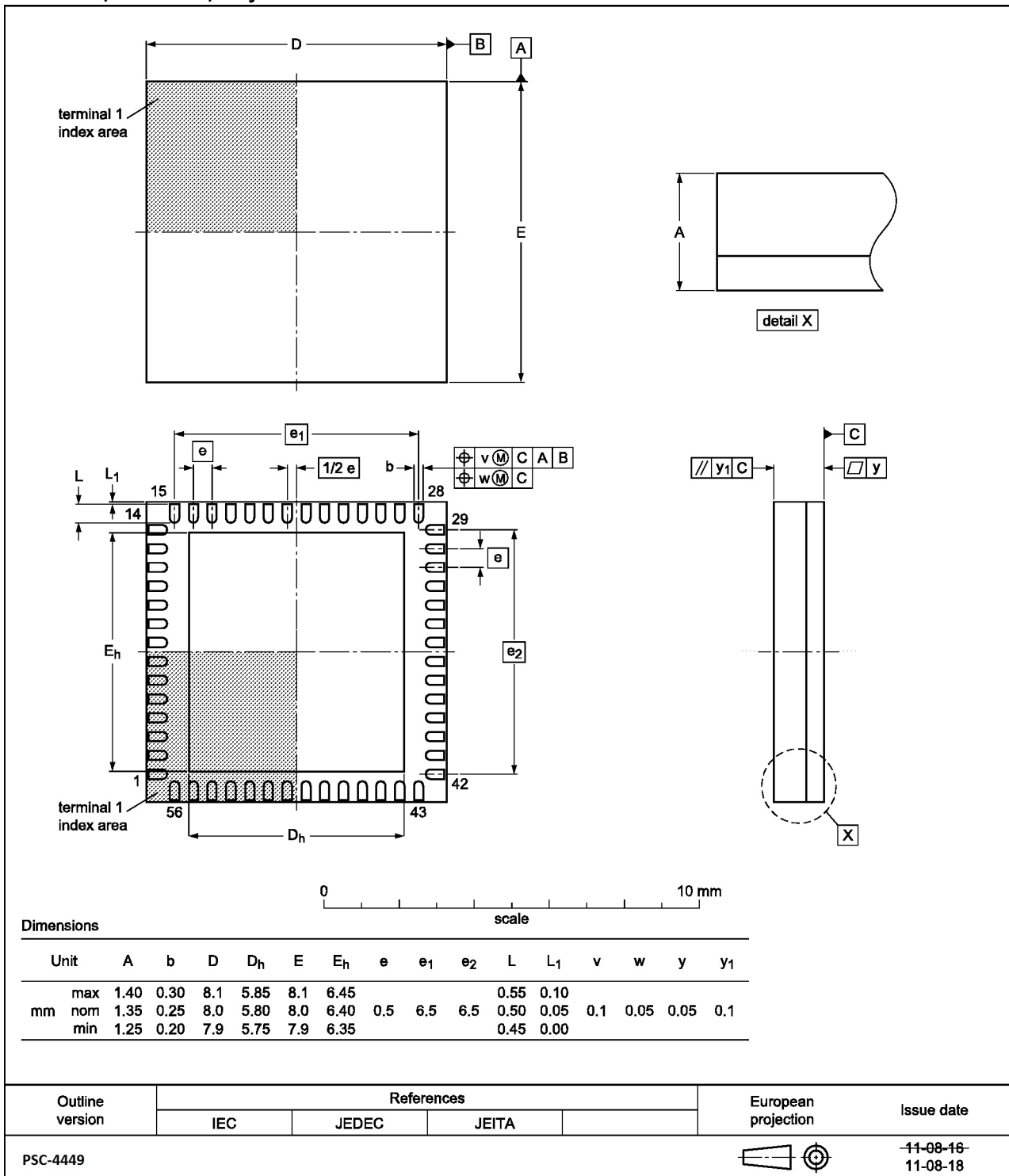


Fig 28. Package outline PSC-4449 (VFQFPN56)

13. Abbreviations

Table 68. Abbreviations

| Acronym | Description |
|----------|---|
| ADC | Analog-to-Digital Converter |
| CDMA | Code Division Multiple Access |
| DAV | DAta Valid |
| ESD | ElectroStatic Discharge |
| FFT | Fast Fourier Transform |
| GSM | Global System for Mobile communications |
| ILA | Initial Lane Alignment |
| IMD3 | third order InterMoDulation product |
| LSB | Least Significant Bit |
| LTE | Long-Term Evolution |
| LVDS DDR | Low Voltage Differential Signaling Double Data Rate |
| LVPECL | Low-Voltage Positive Emitter-Coupled Logic |
| MIMO | Multiple Input Multiple Output |
| MSB | Most Significant Bit |
| OTR | OuT-of-Range |
| SFDR | Spurious-Free Dynamic Range |
| SPI | Serial Peripheral Interface |
| SNR | Signal-to-Noise Ratio |
| TD-SCDMA | Time Division-Synchronous Code Division Multiple Access |
| WCDMA | Wideband Code Division Multiple Access |
| WiMAX | Worldwide interoperability for Microwave Access |
| Tclk | Period of the Sampling Clock |

14. Revision history

Table 69. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------------|--------------|------------------------|--|--------------------|
| ADC1453D250 v.3.2 | 20140606 | Preliminary data sheet | - Changed to Preliminary - ADC1453D160 removed - Registers updated - Offset error updated | ADC1453D_SER v.3.1 |
| ADC1453D_SER v.3.1 | 20140123 | Advance data sheet | - Pin 50 changed to VDDO - Min VDDO set to 1.8 V | ADC1453D_SER v.3.0 |
| ADC1453D_SER v.3.0 | 20131115 | Advance data sheet | - | ADC1453D_SER v.1.2 |
| ADC1453D_SER v.1.2 | 20130402 | Objective data sheet | New package outline | ADC1453D_SER v.1.1 |
| ADC1453D_SER v.1.1 | 20130316 | Objective data sheet | - | ADC1453D_SER v.1.0 |
| ADC1453D_SER v.1.0 | 20130227 | Objective data sheet | - | - |

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