ACS374MS

Radiation HardenedOctal D Flip-Flop, Three-State

FN3997
Rev 0.00
April 1995

Features

- 1.25 Micron Radiation Hardened SOS CMOS
- Total Dose 300K RAD (Si)
- Single Event Upset (SEU) Immunity <1 x 10^{-10} Errors/Bit-Day (Typ)
- SEU LET Threshold >80 MEV-cm^2/mg
- Dose Rate Upset >10^{11} RAD (Si)/s, 20ns Pulse
- Latch-Up Free Under Any Conditions
- Military Temperature Range: -55°C to +125°C
- Significant Power Reduction Compared to ALSTTL Logic
- DC Operating Voltage Range: 4.5V to 5.5V
- Input Logic Levels
  - VIL = 30% of VCC Max
  - VIH = 70% of VCC Min
- Input Current ≤1μA at VOL, VOH

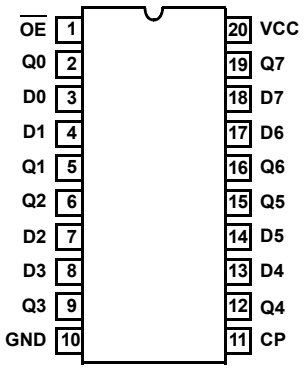
Description

The Intersil ACS374MS is a radiation hardened octal D-type flip-flop with three-state outputs. The eight edge-triggered flip-flops enter data into their registers on the low to high transition of clock (CP). The Output Enable (OEN) controls the three-state outputs and is independent of the register operation. When the OEN is high, the outputs will be in the high impedance state.

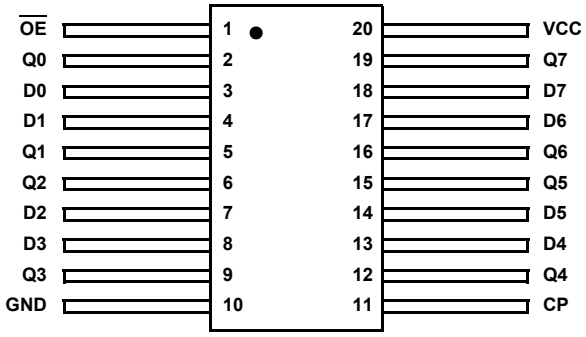
The ACS374MS utilizes advanced CMOS/SOS technology to achieve high-speed operation. This device is a member of the radiation hardened, high-speed, CMOS/SOS Logic Family.

Pinouts

20 LEAD CERAMIC DUAL-IN-LINE
MIL-STD-1835 DESIGNATOR CDIP2-T20, LEAD FINISH C
TOP VIEW



20 LEAD CERAMIC FLATPACK
MIL-STD-1835 DESIGNATOR CDFP4-F20, LEAD FINISH C
TOP VIEW



Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
ACS374DMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead SBDIP
ACS374KMSR	-55°C to +125°C	Intersil Class S Equivalent	20 Lead Ceramic Flatpack
ACS374D/Sample	+25°C	Sample	20 Lead SBDIP
ACS374K/Sample	+25°C	Sample	20 Lead Ceramic Flatpack
ACS374HMSR	+25°C	Die	Die

Truth Table

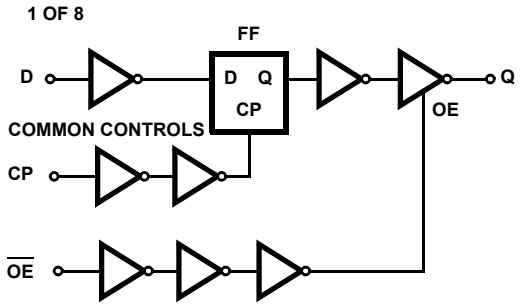
INPUTS			OUTPUTS
$\overline{OE}$	CP	Dn	Qn
L	↗	H	H
L	↗	L	L
L	X	X	Q0
H	X	X	Z

H = High Level
L = Low Level
X = Immaterial
Z = High Impedance

↗ = Transition from Low to High Level

Q0 = the level of Q before the indicated input conditions were established

Functional Diagram



Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.5V to +6.0V
Input Voltage Range . . . . . -0.5V to VCC +0.5V
DC Input Current, Any One Input . . . . . ±10mA
DC Drain Current, Any One Output . . . . . ±50mA
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (Soldering 10s) . . . . . +265°C
Junction Temperature (TJ) . . . . . +175°C
ESD Classification . . . . . Class 1
(All Voltages Reference to VSS)

Reliability Information

Thermal Impedance	θ_{JA}	θ_{JC}
DIP	72°C/W	24°C/W
Flatpack	107°C/W	28°C/W

Maximum Package Power Dissipation at +125°C
DIP 0.7W
Flatpack 0.5W
Maximum Device Power Dissipation . . . . . (TBD)W
Gate Count . . . . . 42 Gates

CAUTION: As with all semiconductors, stress listed under "Absolute Maximum Ratings" may be applied to devices (one at a time) without resulting in permanent damage. This is a stress rating only. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. The conditions listed under "Electrical Performance Characteristics" are the only conditions recommended for satisfactory device operation.

Operating Conditions

Supply Voltage . . . . . +4.5V to +5.5V
Input Rise and Fall Times at 4.5V VCC (TR, TF) . . . . . 10ns/V Max
Operating Temperature Range (T_A) . . . . . -55°C to +125°C
Input High Voltage (VIH) . . . . . VCC to 70% of VCC
Input Low Voltage (VIL) . . . . . 0V to 30% of VCC

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	20	µA
			2, 3	+125°C, -55°C	-	400	µA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0V, (Note 2)	1	+25°C	-12	-	mA
			2, 3	+125°C, -55°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0V, (Note 2)	1	+25°C	12	-	mA
			2, 3	+125°C, -55°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V VIL = 1.65V, IOH = -50µA	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	1, 2, 3	+25°C, +125°C, -55°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V VIL = 1.65V, IOH = 50µA	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = 50µA	1, 2, 3	+25°C, +125°C, -55°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	1	+25°C	-	±0.5	µA
			2, 3	+125°C, -55°C	-	±1.0	µA
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 3)	7, 8A, 8B	+25°C, +125°C, -55°C	-	-	V

NOTES:

1. All voltages referenced to device GND.
2. Force/measure functions may be interchanged.
3. For functional tests, VO ≥4.0V is recognized as a logic "1", and VO ≤0.5V is recognized as a logic "0".

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	14	ns
			10, 11	+125°C, -55°C	2	17	ns
	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	16	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPZL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	19	ns
	TPZH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	16	ns
			10, 11	+125°C, -55°C	2	20	ns
	TPLZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	19	ns
	TPHZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	9	+25°C	2	15	ns
			10, 11	+125°C, -55°C	2	19	ns

NOTES:

1. All voltages referenced to device GND.
2. AC measurements assume RL = 500Ω, CL = 50pF, Input TR = TF = 3ns.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Capacitance Power Dissipation	CPD	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	25	-	pF
				+125°C	-	30	-	pF
Input Capacitance	CIN	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	-	10	pF
				+125°C	-	-	10	pF
Output Capacitance	COUT	VCC = 5.0V, VIH = 5.0V, VIL = 0V, f = 1MHz	1	+25°C	-	-	20	pF
				+125°C	-	-	20	pF
Pulse Width Time	TW	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	4.5	-	-	ns
				+125°C	5	-	-	ns
Setup Time	TSU	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	3.5	-	-	ns
				+125°C	4	-	-	ns
Hold Time	TH	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	3.5	-	-	ns
				+125°C	4	-	-	ns
Maximum Frequency CP	FMAX	VCC = 4.5V, VIH = 4.5V, VIL = 0V	1	+25°C	0	-	100	MHz
				+125°C	0	-	100	MHz

NOTE:

1. The parameters listed in Table 3 are controlled via design or process parameters. Min and Max Limits are guaranteed but not directly tested. These parameters are characterized upon initial design release and upon design changes which affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	TEMP	RAD LIMITS		UNITS
				MIN	MAX	
Supply Current	ICC	VCC = 5.5V, VIN = VCC or GND	+25°C	-	400	µA
Output Current (Source)	IOH	VCC = VIH = 4.5V, VOUT = VCC -0.4V, VIL = 0	+25°C	-8	-	mA
Output Current (Sink)	IOL	VCC = VIH = 4.5V, VOUT = 0.4V, VIL = 0	+25°C	8	-	mA
Output Voltage High	VOH	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = -50µA	+25°C	VCC -0.1	-	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = -50µA	+25°C	VCC -0.1	-	V
Output Voltage Low	VOL	VCC = 5.5V, VIH = 3.85V, VIL = 1.65V, IOH = 50µA	+25°C	-	0.1	V
		VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, IOH = 50µA	+25°C	-	0.1	V
Input Leakage Current	IIN	VCC = 5.5V, VIN = VCC or GND	+25°C	-	±1	µA
Three-State Output Leakage Current	IOZ	VCC = 5.5V, Force Voltage = 0V or VCC	+25°C	-	±35	µA
Noise Immunity Functional Test	FN	VCC = 4.5V, VIH = 3.15V, VIL = 1.35V, (Note 2)	+25°C	-	-	V
Propagation Delay	TPHL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	17	ns
	TPLH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	20	ns
	TPZL1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	19	ns
	TPZH1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	20	ns
	TPLZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	19	ns
	TPHZ1	VCC = 4.5V, VIH = 4.5V, VIL = 0V	+25°C	2	19	ns

NOTES:

1. All voltages referenced to device GND.
2. For functional tests, VO ≥4.0V is recognized as a logic “1”, and VO ≤0.5V is recognized as a logic “0”.

TABLE 5. DELTA PARAMETERS (+25°C)

PARAMETER	SYMBOL	(NOTE1) DELTA LIMIT	UNITS
Supply Current	ICC	±4.0	µA
Three-State Leakage Current	IOZ	±200	nA
Output Current	IOL/IOH	±15	%

NOTE:

1. All delta calculations are referenced to 0 hour readings or pre-life readings.

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP		METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Preburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test 1 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
Interim Test 2 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Interim Test 3 (Postburn-In)		100%/5004	1, 7, 9	ICC, IOL/H, IOZL/H
PDA		100%/5004	1, 7, 9, Deltas	
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	
Group A (Note 1)		Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample/5005	1, 7, 9	
Group D		Sample/5005	1, 7, 9	

NOTE:

1. Alternate Group A testing may be exercised in accordance with MIL-STD-883, Method 5005.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUP	METHOD	TEST		READ AND RECORD	
		PRE RAD	POST RAD	PRE RAD	POST RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4 (Note 1)

NOTE:

1. Except FN test which will be performed 100% Go/No-Go.

TABLE 8. BURN-IN TEST CONNECTIONS (+125^{O}C < TA < 139^{O}C)

OPEN	GROUND	1/2 VCC = 3V ±0.5V	VCC = 6V ±0.5V	OSCILLATOR	
				50kHz	25kHz
STATIC BURN-IN 1 (Note 1)					
-	1, 3, 4, 7, 8, 10, 11, 13, 14, 17, 18	2, 5, 6, 9, 12, 15, 16, 19	20	-	-
STATIC BURN-IN 2 (Note 1)					
-	10	2, 5, 6, 9, 12, 15, 16, 19	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20	-	-
DYNAMIC BURN-IN (Note 1)					
-	1, 10	2, 5, 6, 9, 12, 15, 16, 19	20	11	3, 4, 7, 8, 13, 14, 17, 18

NOTE:

1. Each pin except VCC and GND will have a series resistor of 500Ω ±5%.

TABLE 9. IRRADIATION TEST CONNECTIONS (TA = +25^{O}C, ±5^{O}C)

FUNCTION	OPEN	GROUND	VCC = 5V ±0.5V
Irradiation Circuit (Note 1)	2, 5, 6, 9, 12, 15, 16, 19	10	1, 3, 4, 7, 8, 11, 13, 14, 17, 18, 20

NOTE:

1. Each pin except VCC and GND will have a series resistor of 47kΩ ±5%. Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures.

Intersil - Space Products MS Screening

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010

100% Temperature Cycling Method 1010 Condition C (-65^{o} to +150^{o}C)

100% Constant Acceleration

100% PIND Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In 1 Method 1015, 24 Hours at +125^{o}C Min

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2 Method 1015, 24 Hours at +125^{o}C Min

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In Method 1015, 240 Hours at +125^{o}C or 180 Hours at +135^{o}C

100% Interim Electrical Test 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012 (2 Views)

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Group B (Optional) Method 5005 (Class S) (Note 2)

Group D (Optional) Method 5005 (Class S) (Note 2)

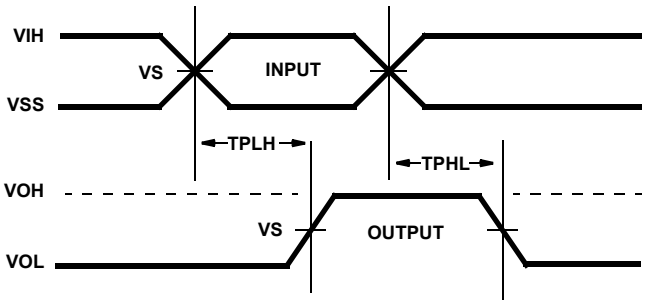
CSI and/or GSI (Optional) (Note 2)

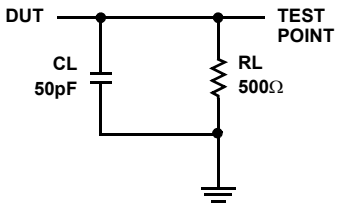
Data Package Generation (Note 3)

NOTES:

1. Failures from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. These steps are optional, and should be listed on the purchase order if required.
3. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Intersil Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include reproductions of SEM photos. NOTE: SEM photos to include percent of step coverage.
   X-Ray Report and Film, including penetrometer measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, RAD Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Intersil.

Propagation Delay Timing Diagram and Load Circuit

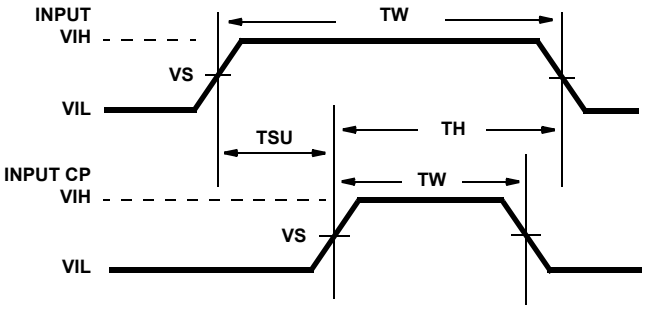




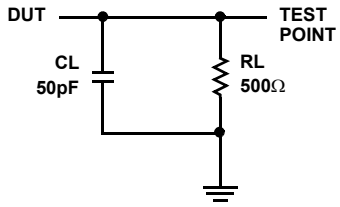
AC VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Pulse Width, Setup, Hold Timing Diagram Positive Edge Trigger and AC Load Circuit



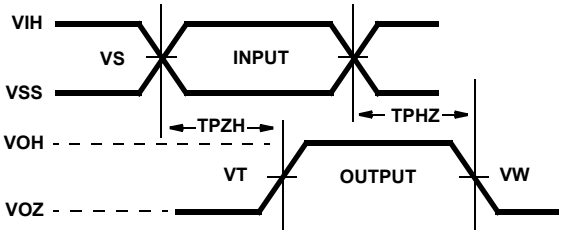
TH = HOLD TIME
TSU = SETUP TIME
TW = PULSE WIDTH

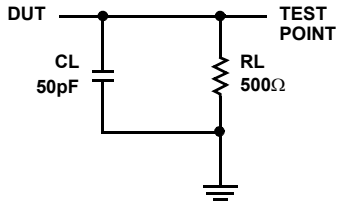


PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VIL	0	V
GND	0	V

Three-State High Timing Diagram and Load Circuit

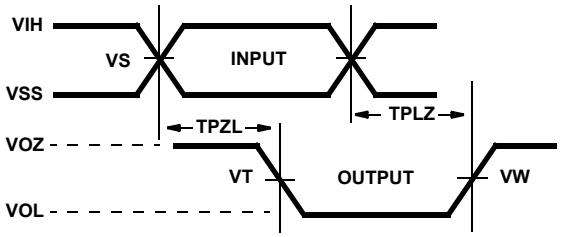


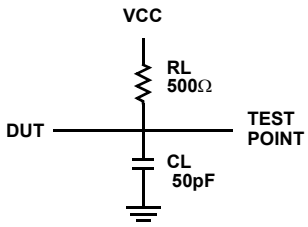


PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	3.60	V
GND	0	V

Three-State Low Timing Diagram and Load Circuit





PULSE WIDTH, SETUP, HOLD VOLTAGE LEVELS

PARAMETER	ACS	UNITS
VCC	4.50	V
VIH	4.50	V
VS	2.25	V
VT	2.25	V
VW	0.90	V
GND	0	V

Die Characteristics

DIE DIMENSIONS:

102 mils x 102 mils
2,600mm x 2,600mm

METALLIZATION:

Type: AlSiCu
Metal 1 Thickness: 6.75kÅ (Min), 8.25kÅ (Max)
Metal 2 Thickness: 9kÅ (Min), 11kÅ (Max)

GLASSIVATION:

Type: SiO_2
Thickness: 8kÅ ±1kÅ

DIE ATTACH:

Material: Silver Glass or JM 7000 after 7/1/95

WORST CASE CURRENT DENSITY:

$< 2.0 \times 10^5 A/cm^2$

BOND PAD SIZE:

> 4.3 mils x 4.3 mils
> 110µm x 110µm

Metallization Mask Layout