General Description

The 9ZXL1230 is a small-footprint, low power 12-output differential buffer that meets all the performance requirements of the Intel DB1900Z specification. It is pin compatible to the 9ZX21200. The 9ZXL1230 is backwards compatible to PCIe Gen2 and QPI 6.4GT/s specifications. A fixed, internal feedback path maintains low drift for critical QPI applications.

Recommended Application

12-output Low Power PCIe Gen3/QPI differential buffer for Romley

Output Features

- 12 - 0.7V low-power HCSL-compatible output pairs

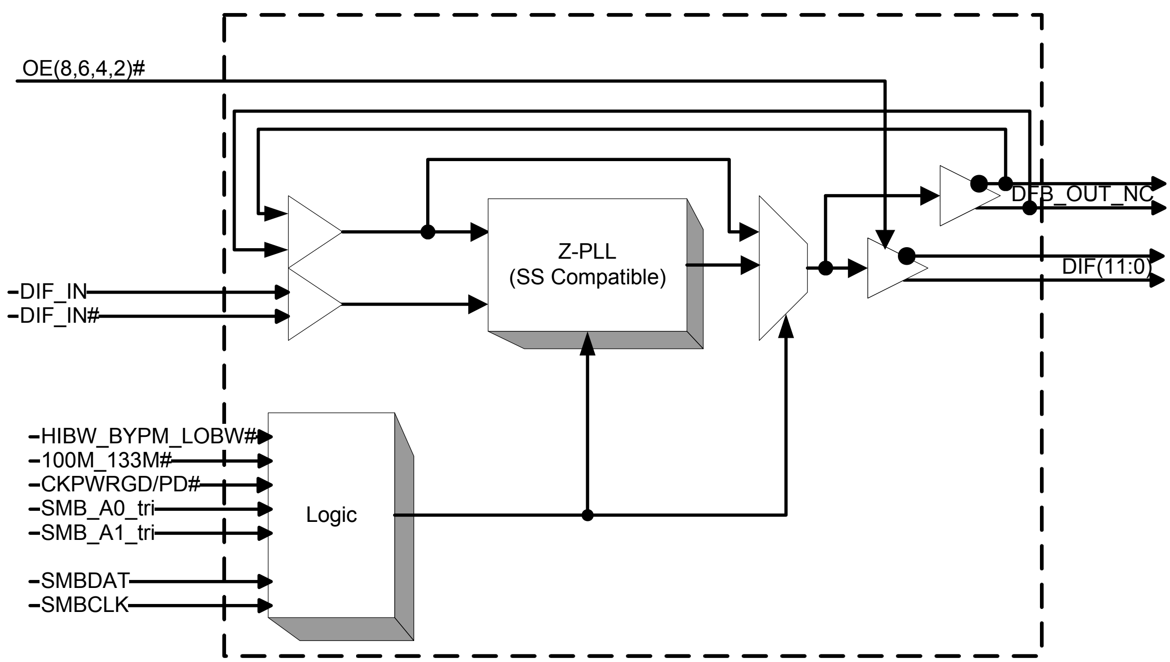
Features/Benefits

- Low-power push-pull outputs; Save power and board space - no Rp
- Pin compatible to 9ZX21200; easy path to >50% power savings
- Space-saving 56-pin QFN package
- Fixed feedback path for 0ps input-to-output delay
- 9 Selectable SMBus Addresses; Mulitple devices can share the same SMBus Segment
- 4 OE# pins; Hardware control of four outputs, other outputs free run
- PLL or bypass mode; PLL can dejitter incoming clock
- 100MHz or 133MHz PLL mode operation; supports PCIe and QPI applications
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible; tracks spreading input clock for low EMI

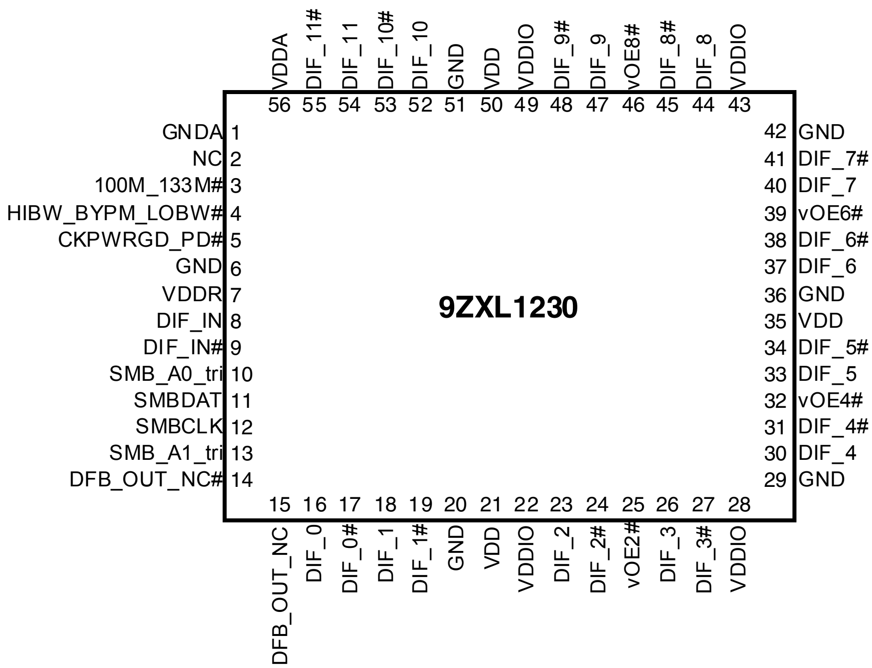
Key Specifications

- Cycle-to-cycle jitter <50ps
- Output-to-output skew <65 ps
- Input-to-output delay variation <50ps
- PCIe Gen3 phase jitter <1.0ps RMS
- QPI 9.6GT/s 12UI phase jitter <0.2ps RMS

Block Diagram



Pin Configuration



Note: Pins with ^ prefix have internal 120K pullup
Pins with v prefix have internal 120K pulldowm

Power Management Table

CKPWRGD_PD#	DIF_IN/ DIF_IN#	SMBus EN bit	DIF(11:0)/ DIF(11:0)#	PLL STATE IF NOT IN BYPASS MODE
0	X	X	Low/Low	OFF
1	Running	0	Low/Low	ON
		1	Running	ON

Functionality at Power-up (PLL mode)

100M_133M#	DIF_IN MHz	DIF(11:0)
1	100.00	DIF_IN
0	133.33	DIF_IN

Power Connections

Pin Number			Description
VDD	VDDIO	GND	
56		1	Analog PLL
7		6	Analog Input
21,35,50	22,28,43,49	20,29,36,42, 51	DIF clocks

PLL Operating Mode Readback Table

HiBW_BypM_LoBW#	Byte0, bit 7	Byte 0, bit 6
Low (Low BW)	0	0
Mid (Bypass)	0	1
High (High BW)	1	1

Tri-Level Input Thresholds

Level	Voltage
Low	<0.8V
Mid	1.2<Vin<1.8V
High	Vin > 2.2V

PLL Operating Mode

HiBW_BypM_LoBW#	MODE
Low	PLL Lo BW
Mid	Bypass
High	PLL Hi BW

NOTE: PLL is OFF in Bypass Mode

9ZXL1230 SMBus Addressing

Pin		
SMB_A1_tri	**SMB_A0_tri**	**SMBus Address**
0	0	D8
0	M	DA
0	1	DE
M	0	C2
M	M	C4
M	1	C6
1	0	CA
1	M	CC
1	1	CE

Pin Descriptions

PIN #	PIN NAME	TYPE	DESCRIPTION
1	GNDA	PWR	Ground pin for the PLL core.
2	NC	N/A	No Connection.
3	100M_133M#	IN	3.3V Input to select operating frequency See Functionality Table for Definition
4	HIBW_BYPM_LOBW#	IN	Trilevel input to select High BW, Bypass or Low BW mode. See PLL Operating Mode Table for Details.
5	CKPWRGD_PD#	IN	Notifies device to sample latched inputs and start up on first high assertion, or exit Power Down Mode on subsequent assertions. Low enters Power Down Mode.
6	GND	PWR	Ground pin.
7	VDDR	PWR	3.3V power for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately.
8	DIF_IN	IN	0.7 V Differential TRUE input
9	DIF_IN#	IN	0.7 V Differential Complementary Input
10	SMB_A0_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A1 to decode 1 of 9 SMBus Addresses.
11	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
12	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
13	SMB_A1_tri	IN	SMBus address bit. This is a tri-level input that works in conjunction with the SMB_A0 to decode 1 of 9 SMBus Addresses.
14	DFB_OUT_NC#	OUT	Complementary half of differential feedback output, provides feedback signal to the PLL for synchronization with input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package.
15	DFB_OUT_NC	OUT	True half of differential feedback output, provides feedback signal to the PLL for synchronization with the input clock to eliminate phase error. This pin should NOT be connected on the circuit board, the feedback is internal to the package.
16	DIF_0	OUT	0.7V differential true clock output
17	DIF_0#	OUT	0.7V differential Complementary clock output
18	DIF_1	OUT	0.7V differential true clock output
19	DIF_1#	OUT	0.7V differential Complementary clock output
20	GND	PWR	Ground pin.
21	VDD	PWR	Power supply, nominal 3.3V
22	VDDIO	PWR	Power supply for differential outputs
23	DIF_2	OUT	0.7V differential true clock output
24	DIF_2#	OUT	0.7V differential Complementary clock output
25	OE2#	IN	Active low input for enabling DIF pair 2. 1 =disable outputs, 0 = enable outputs
26	DIF_3	OUT	0.7V differential true clock output
27	DIF_3#	OUT	0.7V differential Complementary clock output
28	VDDIO	PWR	Power supply for differential outputs
29	GND	PWR	Ground pin.
30	DIF_4	OUT	0.7V differential true clock output
31	DIF_4#	OUT	0.7V differential Complementary clock output

Pin Descriptions (cont.)

32	OE4#	IN	Active low input for enabling DIF pair 4 1 =disable outputs, 0 = enable outputs
33	DIF_5	OUT	0.7V differential true clock output
34	DIF_5#	OUT	0.7V differential Complementary clock output
35	VDD	PWR	Power supply, nominal 3.3V
36	GND	PWR	Ground pin.
37	DIF_6	OUT	0.7V differential true clock output
38	DIF_6#	OUT	0.7V differential Complementary clock output
39	OE6#	IN	Active low input for enabling DIF pair 6. 1 =disable outputs, 0 = enable outputs
40	DIF_7	OUT	0.7V differential true clock output
41	DIF_7#	OUT	0.7V differential Complementary clock output
42	GND	PWR	Ground pin.
43	VDDIO	PWR	Power supply for differential outputs
44	DIF_8	OUT	0.7V differential true clock output
45	DIF_8#	OUT	0.7V differential Complementary clock output
46	OE8#	IN	Active low input for enabling DIF pair 8. 1 =disable outputs, 0 = enable outputs
47	DIF_9	OUT	0.7V differential true clock output
48	DIF_9#	OUT	0.7V differential Complementary clock output
49	VDDIO	PWR	Power supply for differential outputs
50	VDD	PWR	Power supply, nominal 3.3V
51	GND	PWR	Ground pin.
52	DIF_10	OUT	0.7V differential true clock output
53	DIF_10#	OUT	0.7V differential Complementary clock output
54	DIF_11	OUT	0.7V differential true clock output
55	DIF_11#	OUT	0.7V differential Complementary clock output
56	VDDA	PWR	3.3V power for the PLL core.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9ZXL1230. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
3.3V Core Supply Voltage	VDD, VDDA	VDD for core logic and PLL			4.6	V	1,2
IO Supply Voltage	VDD_IO	VDD for differential IO			4.6	V	1,2
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface			V_{DD}+0.5V	V	1
Input High Voltage	V_{IHSMB}	SMBus clock and data pins			5.5V	V	1
Storage Temperature	Ts		-65		150	°C	1
Junction Temperature	Tj				125	°C	1
Input ESD protection	ESD prot	Human Body Model	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics–DIF_IN Clock Input Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%, VDD_IO = 1.05 to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Input Crossover Voltage - DIF_IN	V_{CROSS}	Cross Over Voltage	150		900	mV	1
Input Swing - DIF_IN	V_{SWING}	Differential value	300			mV	1
Input Slew Rate - DIF_IN	dv/dt	Measured differentially	0.4		8	V/ns	1,2
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5		5	uA	
Input Duty Cycle	d_{tin}	Measurement from differential wavefrom	45		55	%	1
Input Jitter - Cycle to Cycle	J_{DIFIn}	Differential Measurement	0		125	ps	1

[1] Guaranteed by design and characterization, not 100% tested in production.

[2]Slew rate measured through +/-75mV window centered around differential zero

Electrical Characteristics–Input/Supply/Common Output Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%, VDD_IO = 1.05 to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Ambient Operating Temperature	T_{COM}	Commmercial range	0		70	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = VDD	-5		5	uA	1
	I_{INP}	Single-ended inputs V_{IN} = 0 V; Inputs with internal pull-up resistors V_{IN} = VDD; Inputs with internal pull-down resistors	-200		200	uA	1
Input Frequency	F_{ibyp}	V_{DD} = 3.3 V, Bypass mode	33		150	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 100MHz PLL mode	90	100.00	110	MHz	2
	F_{ipll}	V_{DD} = 3.3 V, 133.33MHz PLL mode	120	133.33	147	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic Inputs, except DIF_IN	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock			1	ms	1,2
Input SS Modulation Frequency	f_{MODIN}	Allowable Frequency (Triangular Modulation)	30		33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion DIF stop after OE# deassertion	4		12	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# de-assertion			300	us	1,3
Tfall	t_F	Fall time of control inputs			10	ns	1,2
Trise	t_R	Rise time of control inputs			10	ns	1,2
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	@ I_{PULLUP}			0.4	V	1
SMBus Sink Current	I_{PULLUP}	@ V_{OL}	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V +/- 10%	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency			100	kHz	1,5

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are >200 mV

[4] DIF_IN input

[5] The differential input clock must be running for the SMBus to be active

Electrical Characteristics–DIF 0.7V Low Power Differential Outputs

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%, VDD_IO = 1.05 to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Slew rate	Trf	Scope averaging on	1	3.3	4	V/ns	1, 2, 3
Slew rate matching	ΔTrf	Slew rate matching, Scope averaging on		7	20	%	1, 2, 4
Voltage High	VHigh	Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on)	660	778	850	mV	1
Voltage Low	VLow		-150	0	150		1
Max Voltage	Vmax	Measurement on single ended signal using absolute value. (Scope averaging off)		985	1150	mV	1
Min Voltage	Vmin		-300	-91			1
Vswing	Vswing	Scope averaging off	300	1556		mV	1, 2
Crossing Voltage (abs)	Vcross_abs	Scope averaging off	300	458	550	mV	1, 5
Crossing Voltage (var)	Δ-Vcross	Scope averaging off		17	140	mV	1, 6

[1]Guaranteed by design and characterization, not 100% tested in production. C_L = 2pF with R_S = 33Ω for Zo = 50Ω (100Ω differential trace impedance).

[2] Measured from differential waveform

[3] Slew rate is measured through the Vswing voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

Electrical Characteristics–Current Consumption

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%, VDD_IO = 1.05 to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Operating Current	I_{DDVDD}	133MHz, C_L = Full load; VDD rail		18	25	mA	1
	I_{DDVDDA}	133MHz, C_L = Full load; VDDA+VDDR rail		16	20	mA	1
	$I_{DDVDDIO}$	133MHz, C_L = Full load; VDD IO rail		101	106	mA	1
Powerdown Current	$I_{DDVDDPD}$	Power Down, VDD Rail		0.01	1	mA	1
	$I_{DDVDDAPD}$	Power Down, VDDA+VDDR Rail		3	5	mA	1
	$I_{DDVDDIOPD}$	Power Down, VDD_IO Rail		0.01	0.2	mA	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Skew and Differential Jitter Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%, VDD_IO = 1.05 to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
CLK_IN, DIF[x:0]	t_{SPO_PLL}	Input-to-Output Skew in PLL mode nominal value @ 25°C, 3.3V	-100	-60	100	ps	1,2,4,5,8
CLK_IN, DIF[x:0]	t_{PD_BYP}	Input-to-Output Skew in Bypass mode nominal value @ 25°C, 3.3V	2.5	3.2	4.5	ns	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_PLL}	Input-to-Output Skew Varation in PLL mode across voltage and temperature	-50	0	50	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSPO_BYP}	Input-to-Output Skew Varation in Bypass mode across voltage and temperature	-250		250	ps	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DTE}	Random Differential Tracking error beween two 9ZX devices in Hi BW Mode		3	5	ps (rms)	1,2,3,5,8
CLK_IN, DIF[x:0]	t_{DSSTE}	Random Differential Spread Spectrum Tracking error beween two 9ZX devices in Hi BW Mode		10	75	ps	1,2,3,5,8
DIF{x:0]	t_{SKEW_ALL}	Output-to-Output Skew across all outputs (Common to Bypass and PLL mode)		60	65	ps	1,2,3,8
PLL Jitter Peaking	$j_{peak-hibw}$	LOBW#_BYPASS_HIBW = 1	0	1.2	2.5	dB	7,8
PLL Jitter Peaking	$j_{peak-lobw}$	LOBW#_BYPASS_HIBW = 0	0	0.76	2	dB	7,8
PLL Bandwidth	pll_{HIBW}	LOBW#_BYPASS_HIBW = 1	2	3	4	MHz	8,9
PLL Bandwidth	pll_{LOBW}	LOBW#_BYPASS_HIBW = 0	0.7	1.1	1.4	MHz	8,9
Duty Cycle	t_{DC}	Measured differentially, PLL Mode	45	50.1	55	%	1
Duty Cycle Distortion	t_{DCD}	Measured differentially, Bypass Mode @100MHz	-2	0	2	%	1,10
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	PLL mode		34	50	ps	1,11
		Additive Jitter in Bypass Mode		17	50	ps	1,11

Notes for preceding table:

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.

[2] Measured from differential cross-point to differential cross-point. This parameter can be tuned with external feedback path, if present.

[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.

[4] This parameter is deterministic for a given device

[5] Measured with scope averaging on to find mean value.

[6.] t is the period of the input clock

[7] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.

[8.] Guaranteed by design and characterization, not 100% tested in production.

[9] Measured at 3 db down or half power point.

[10] Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

[11] Measured from differential waveform

Electrical Characteristics–Phase Jitter Parameters

$T_A = T_{COM}$; Supply Voltage V_{DD} = 3.3 V +/-5%, VDD_IO = 1.05 to 3.3V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
[4]DIF_IN input	$t_{jphPCIeG1}$	PCIe Gen 1		34	86	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		1.2	3	ps (rms)	1,2
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		2.2	3.1	ps (rms)	1,2
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.5	1	ps (rms)	1,2,4
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.24	0.5	ps (rms)	1,5
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.14	0.3	ps (rms)	1,5
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.12	0.2	ps (rms)	1,5
	$t_{jphPCIeG1}$	PCIe Gen 1		3.7	10	ps (p-p)	1,2,3
	$t_{jphPCIeG2}$	PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz		0.1	0.1	ps (rms)	1,2,6
		PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz)		0.4	0.5	ps (rms)	1,2,6
	$t_{jphPCIeG3}$	PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz)		0.09	0.2	ps (rms)	1,2,4,6
	t_{jphQPI_SMI}	QPI & SMI (100MHz or 133MHz, 4.8Gb/s, 6.4Gb/s 12UI)		0.14	0.1	ps (rms)	1,5,6
		QPI & SMI (100MHz, 8.0Gb/s, 12UI)		0.01	0.1	ps (rms)	1,5,6
		QPI & SMI (100MHz, 9.6Gb/s, 12UI)		0.01	0.1	ps (rms)	1,5,6

[1] Applies to all outputs.

[2] See http://www.pcisig.com for complete specs

[3] Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

[4] Subject to final radification by PCI SIG.

[5] Calculated from Intel-supplied Clock Jitter Tool v 1.6.3

[6] For RMS figures, additive jitter is calculated by solving the following equation: (Additive jitter)^2 = (total jittter)^2 - (input jitter)^2

Clock Periods–Differential Outputs with Spread Spectrum Disabled

SSC OFF	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter	-SSC Sh	- ppm L	0 ppm Period Nominal	+ ppm L	+SSC Sh	+c2c jitter		
DIF	100.00	9.94900		9.99900	10.00000	10.00100		10.05100	ns	1,2,3
	133.33	7.44925		7.49925	7.50000	7.50075		7.55075	ns	1,2,4

Clock Periods–Differential Outputs with Spread Spectrum Enabled

SSC ON	Center Freq. MHz	Measurement Window							Units	Notes
		1 Clock	1us	0.1s	0.1s	0.1s	1us	1 Clock		
		-c2c jitter AbsPer Min	-SSC Short-Term Average Min	- ppm Long-Term Average Min	0 ppm Period Nominal	+ ppm Long-Term Average Max	+SSC Short-Term Average Max	+c2c jitter AbsPer Max		
DIF	99.75	9.94906	9.99906	10.02406	10.02506	10.02607	10.05107	10.10107	ns	1,2,3
	133.00	7.44930	7.49930	7.51805	7.51880	7.51955	7.53830	7.58830	ns	1,2,4

Notes:

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy specifications are guaranteed with the assumption that the input clock complies with CK420BQ/CK410B+ accuracy requirements (+/-100ppm). The 9ZXL1230 itself does not contribute to ppm error.

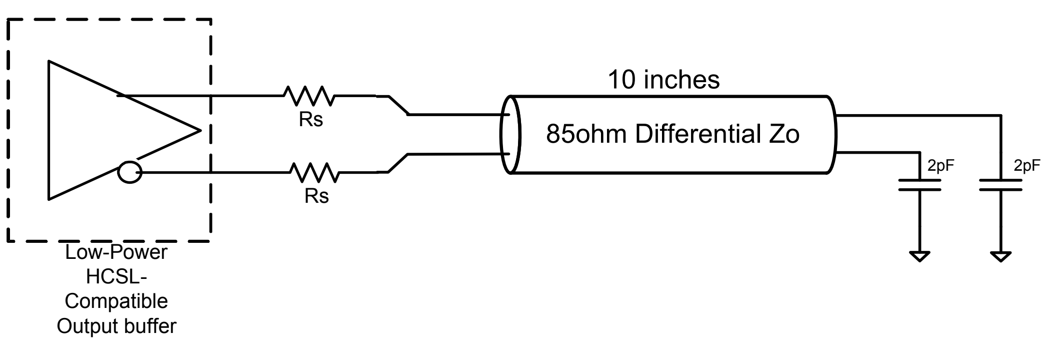
[3] Driven by SRC output of main clock, 100 MHz PLL Mode or Bypass mode

[4] Driven by CPU output of main clock, 133 MHz PLL Mode or Bypass mode

Differential Output Terminations

DIF Zo (Ω)	Rs (Ω)
100	33
85	27

9ZXL Differential Test Loads



General SMBus Serial Interface Information for 9ZXL1230

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) sends the byte count = X
- IDT clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- IDT clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a Stop bit

Index Block Write Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- IDT clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- IDT clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- IDT clock will **acknowledge**
- IDT clock will send the data byte count = X
- IDT clock sends Byte **N+X-1**
- IDT clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**IDT (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

SMBusTable: PLL Mode, and Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	3	PLL Mode 1	PLL Operating Mode Rd back 1	R	See PLL Operating Mode Readback Table		Latch
Bit 6	3	PLL Mode 0	PLL Operating Mode Rd back 0	R			Latch
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		PLL_SW_EN	Enable S/W control of PLL BW	RW	HW Latch	SMBus Control	0
Bit 2		PLL Mode 1	PLL Operating Mode 1	RW	See PLL Operating Mode Readback Table		1
Bit 1		PLL Mode 0	PLL Operating Mode 1	RW			1
Bit 0	4	100M_133M#	Frequency Select Readback	R	133MHz	100MHz	Latch

Note: Setting bit 3 to '1' allows the user to overide the Latch value from pin 5 via use of bits 2 and 1. Use the values from the PLL Operating Mode Readback Table. Note that Bits 7 and 6 will keep the value originally latched on pin 5. A warm reset of the system will have to accomplished if the user changes these bits.

SMBusTable: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	42/41	DIF_7_En	Output Control overrides OE# pin	RW	Low/Low	Enable	1
Bit 6	38/37	DIF_6_En	Output Control overrides OE# pin	RW			1
Bit 5	34/35	DIF_5_En	Output Control overrides OE# pin	RW			1
Bit 4	30/29	DIF_4_En	Output Control overrides OE# pin	RW			1
Bit 3	25/26	DIF_3_En	Output Control	RW			1
Bit 2	23/24	DIF_2_En	Output Control	RW			1
Bit 1	18/19	DIF_1_En	Output Control	RW			1
Bit 0	16/17	DIF_0_En	Output Control	RW			1

SMBusTable: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3	55/54	DIF_11_En	Output Control	RW	Low/Low	Enable	1
Bit 2	53/52	DIF_10_En	Output Control	RW			1
Bit 1	48/47	DIF_9_En	Output Control	RW			1
Bit 0	46/45	DIF_8_En	Output Control	RW			1

SMBusTable: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Reserved Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

SMBusTable: Vendor & Revision ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	RID3	REVISION ID	R	A rev = 0000		X
Bit 6	-	RID2		R			X
Bit 5	-	RID1		R			X
Bit 4	-	RID0		R			X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

SMBusTable: DEVICE ID

Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	-	Device ID 7 (MSB)		R	1230 is 230 Decimal or E6 Hex		1
Bit 6	-	Device ID 6		R			1
Bit 5	-	Device ID 5		R			1
Bit 4	-	Device ID 4		R			0
Bit 3	-	Device ID 3		R			0
Bit 2	-	Device ID 2		R			1
Bit 1	-	Device ID 1		R			1
Bit 0	-	Device ID 0		R			0

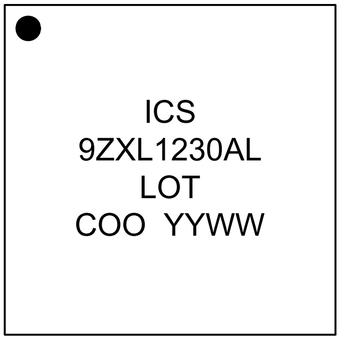
SMBusTable: Byte Count Register

Byte 7	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4	-	BC4	Writing to this register configures how many bytes will be read back.	RW	Default value is 8 hex, so 9 bytes (0 to 8) will be read back by default.		0
Bit 3	-	BC3		RW			1
Bit 2	-	BC2		RW			0
Bit 1	-	BC1		RW			0
Bit 0	-	BC0		RW			0

SMBusTable: Reserved Register

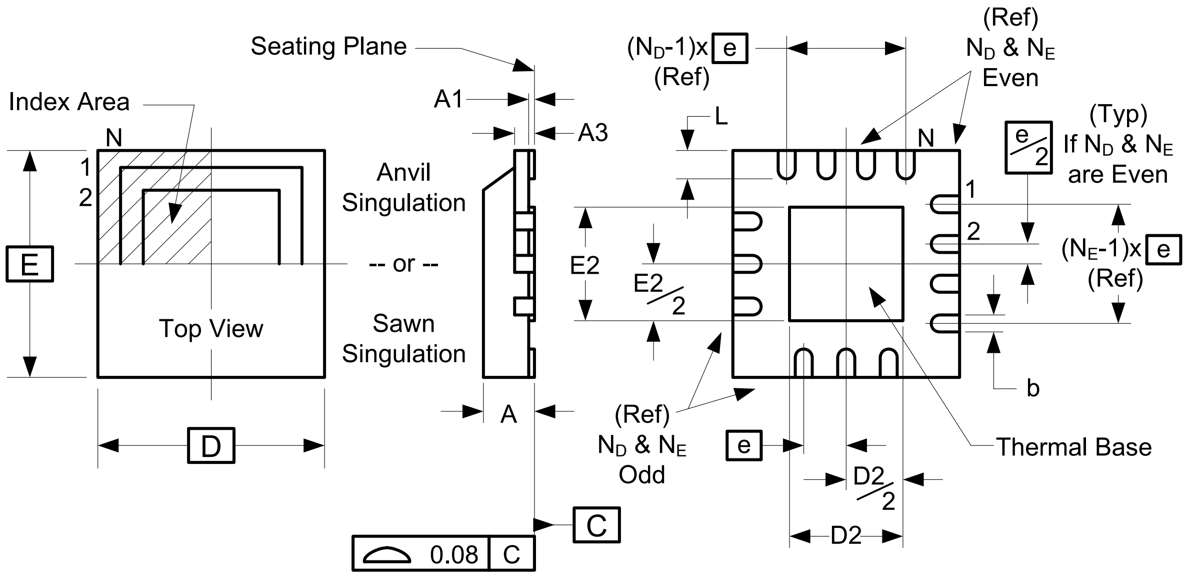
Byte 8	Pin #	Name	Control Function	Type	0	1	Default
Bit 7		Reserved					0
Bit 6		Reserved					0
Bit 5		Reserved					0
Bit 4		Reserved					0
Bit 3		Reserved					0
Bit 2		Reserved					0
Bit 1		Reserved					0
Bit 0		Reserved					0

Marking Diagram



Notes:
1. ‘LOT” is the lot number.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. “L” denotes RoHS compliant package.
4. ‘COO” denotes country of origin.

Package Outline and Package Dimensions (56-pin MLF)



	Millimeters	
Symbol	**Min**	**Max**
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.3
e	0.50 BASIC	
D x E BASIC	8.00 x 8.00	
D2 MIN./MAX.	4.35	4.65
E2 MIN./MAX.	5.05	5.35
L MIN./MAX.	0.30	0.50
N	56	
N_D	14	
N_E	14	

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
9ZXL1230AKLF	see page 15	Trays	56-pin MLF	0 to +70° C
9ZXL1230AKLFT		Tape and Reel	56-pin MLF	0 to +70° C

"LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator (will not correlate with the datasheet revision).

Revision History

Rev.	Issuer	Issue Date	Description	Page #
A	RDW	12/8/2011	1. Changed Output Features description 2. Corrected Title of SMBus Addressing Table 3. Updated tDSPO_BYP to +/-250ps and all Electrical tables with typical values. IDD specs revised downward. 4. Updated Differential Test Loads Figure to indicate impedance and trace length. 5. Removed SMBus Address info on page 12, SMBus address is selectable as indicated on page 3. 6. Mark spec added. 7. Move to final	1,3,6-10,11, 12,15
B	RDW	4/11/2012	1. Updated VDD and VDDIO pin numbers in the Power Connections Table, pinout is correct.	2
C	RDW	11/20/2015	1. Updated QPI references to QPI/UPI 2. Updated DIF_IN table to match PCI SIG specification, no silicon change	1,6

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