Description

The 9SQ445 is a single-chip, PCIe Gen7 clock synthesizer providing a subset of the 9SQ440 outputs. It is designed to work as a complete clock solution or in combination with DB2000Q-compliant clock buffers to provide point-to-point clocks to multiple receiving agents. It is part of the next generation clock generator family supporting the latest dual and multi-socket Intel server platforms.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- CK440Q Lite

Key Specifications

- PCIe Gen7 CC Phase Jitter < 25fs rms

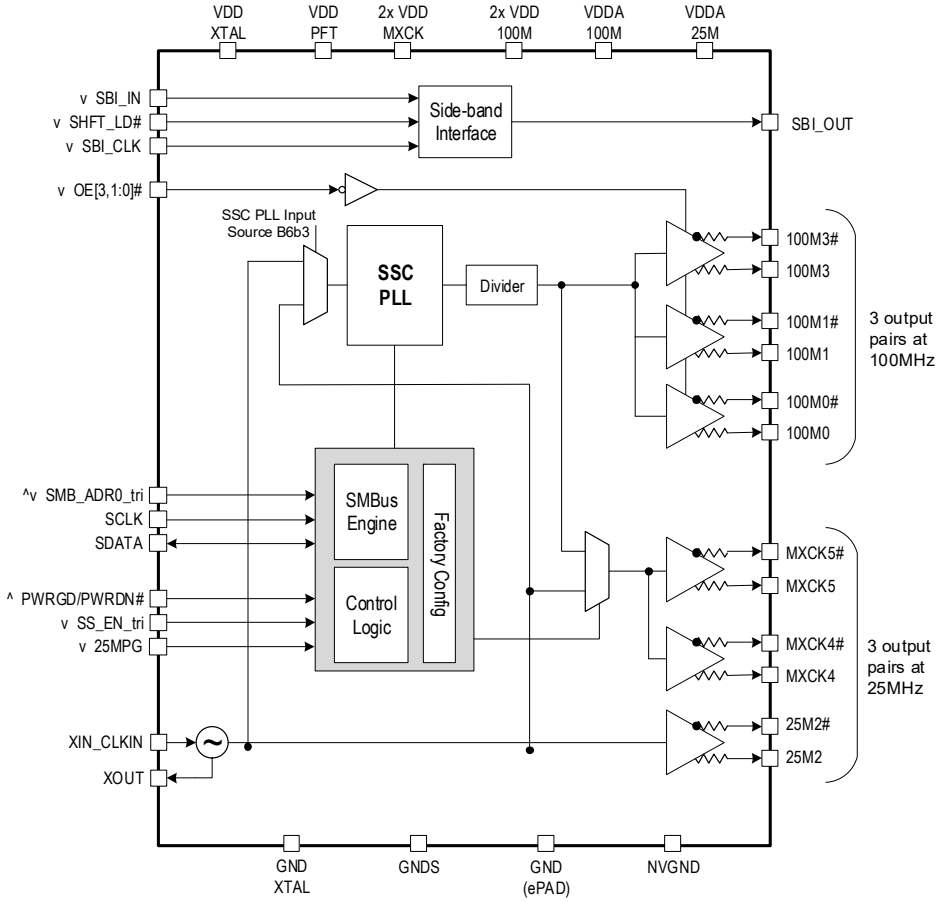
Features

- 3.3V operation
- Side-Band Interface allows real-time hardware control of all output enables
- OE# pin control of 100M outputs
- 85Ω differential Low-Power HCSL (LP-HCSL) outputs eliminate 24 resistors, saving 39mm^2 of area
- Differential outputs drive both source terminated and double (receiver) terminated loads
- 3 selectable SMBus addresses
- Supports 0%, -0.3% and -0.5% spread-spectrum amounts
- Packaged in 5 × 5 mm 40-VFQFPN

Output Features

- Three 25MHz output pairs (1 × 25MHz and 2 × MXCLK set to 25MHz)
- Three 100MHz output pairs with individual OE# pins

Block Diagram

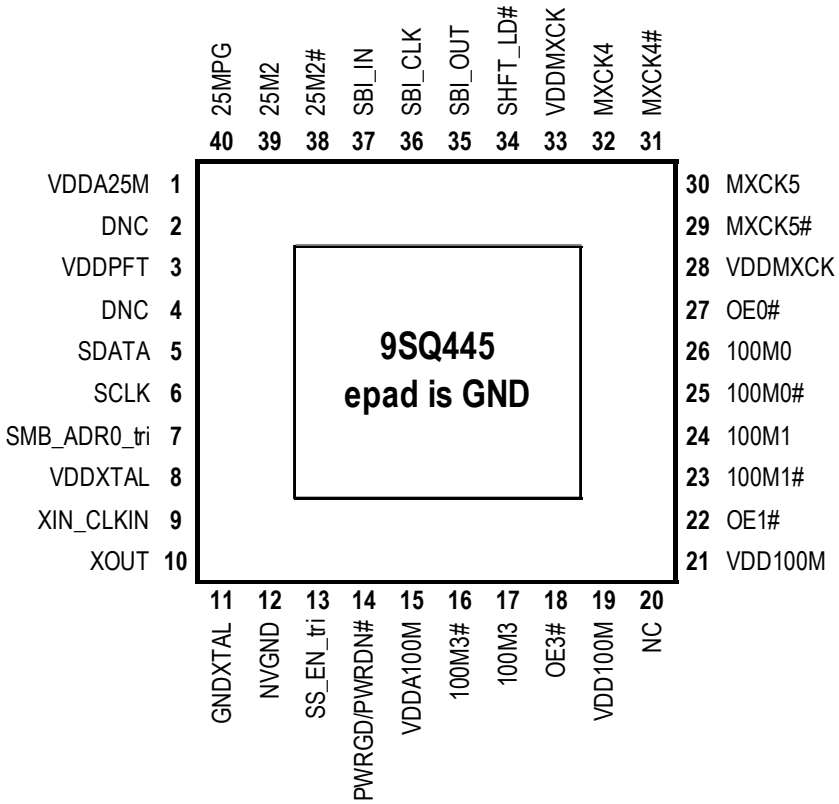


v indicates internal pull down
^ indicates internal pull up
^v indicates internal pull up/down (bias to VDD/2)
See electrical tables for values.

Contents

Pin Assignments

Figure 1. Pin Assignments for 5 × 5 mm 40-VFQFPN Package – Top View



40-VFQFPN

5 × 5 mm, 0.4mm pin pitch

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	VDDA25M	Power	Analog power supply for 25M outputs.
2	DNC	—	Do not connect anything to this pin.
3	VDDPFT	Power	Power supply for platform time circuit and digital.
4	DNC	—	Do not connect anything to this pin.
5	SDATA	I/O, SE, OD, PDT	Data pin for SMBus interface.
6	SCLK	I, SE, PDT	Clock pin of SMBus interface.
7	SMB_ADR0_tri	I, SE, PD, PU	3.3V tri-level LVTTL input to select SMBus address. Refer to tri-level input threshold table.
8	VDDXTAL	Power	Power supply for internal crystal oscillator and CLK_IN.
9	XIN_CLKIN	I, SE, PDT	Crystal input/single-ended input.
10	XOUT	O, SE	Output of internal crystal oscillator. This pin should be left floating if CLK_IN function is being used.
11	GNDXTAL	GND	GND for XTAL.
12	NVGND	GND	Ground.
13	SS_EN_tri	I, SE, PD	Tri-level input to enable or disable spread spectrum. Refer to tri-level input threshold table. 0 = SSC off, MID = -0.3% max, and HIGH = -0.5% max.
14	PWRGD/PWRDN#	I, SE, PU	3.3V LVTTL input to power up or power down the device.
15	VDDA100M	Power	Analog power supply for 100M outputs.
16	100M3#	O, DIF	±0.7V LP-HCSL Differential 100MHz clock complement output.
17	100M3	O, DIF	±0.7V LP-HCSL Differential 100MHz clock true output.
18	OE3#	I, SE, PDT, PD	Active low input for enabling output 3. 1 = disable output, 0 = enable output.
19	VDD100M	Power	Power supply for 100M outputs.
20	NC	—	No connect.
21	VDD100M	Power	Power supply for 100M outputs.
22	OE1#	I, SE, PDT, PD	Active low input for enabling output 1. 1 = disable output, 0 = enable output.
23	100M1#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
24	100M1	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
25	100M0#	O, DIF	±0.7V LP-HCSL differential 100MHz clock complement output.
26	100M0	O, DIF	±0.7V LP-HCSL differential 100MHz clock true output.
27	OE0#	I, SE, PDT, PD	Active low input for enabling output 0. 1 = disable output, 0 = enable output.
28	VDDMXCK	Power	Power supply for MXCK outputs.
29	MXCK5#	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
30	MXCK5	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
31	MXCK4#	O, DIF	±0.7V LP-HCSL differential multiplexable clock complement output.
32	MXCK4	O, DIF	±0.7V LP-HCSL differential multiplexable clock true output.
33	VDDMXCK	Power	Power supply for MXCK outputs.
34	SHFT_LD#	I, SE, PDT, PD	3.3V LVTTL input to control shifting and loading of the Side-Band Interface to the Output Enable Control register.
35	SBI_OUT	O, SE	3.3V LVTTL Side Band Interface data output.
36	SBI_CLK	I, SE, PDT, PD	3.3V LVTTL Side Band Interface clock input for shifting/loading the SBI interface.
37	SBI_IN	I, SE, PDT, PD	3.3V LVTTL Side Band Interface data input.
38	25M2#	O, DIF	±0.7V LP-HCSL differential 25MHz complement output.
39	25M2	O, DIF	±0.7V LP-HCSL differential 25MHz true output.
40	25MPG	I, SE, PDT, PD	3.3V LVTTL input to assert power good for the 25M2 output pair before PWRGD is asserted.
41	EPAD	GND	Ground pin.

Table 2. Signal Types

Term	Description
I	Input
O	Output
OD	Open Drain Output
I/O	Bi-Directional
PD	Pull-down
PU	Pull-up
Z	Tristate
D	Driven
X	Don’t care
SE	Single-ended
DIF	Differential
Power	3.3V power
GND	Ground
PDT	Power Down Tolerant: These signals must tolerate being driven when the device is powered down.

OE Functionality

Table 3. OE Functionality for 100M Outputs

PWRGD/PWRDN#	OEx# Pin	SMBus OE Bit	SBI Mask Bit	SBI Output Control Register	100M
0	X	X	X	X	Disabled
1	1	X	X	X	Disabled
	1	0	X	X	Disabled
	1	1	0	0	Disabled
	0	1	X	1	Running
	0	1	1	X	Running

Note: Disabled in this table means both the true and complement output are low.

Table 4. OE Functionality for 25M and MXCK Outputs

PWRGD/PWRDN#	SMBus OE Bit	SBI Mask Bit	SBI Output Control Register	25M MXCK Outputs
0	X	X	X	Disabled
1	0	X	X	Disabled
	1	0	0	Disabled
	1	X	1	Running
	1	1	X	Running

Note: Disabled in this table means both the true and complement output are low.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9SQ445 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 5. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDX}		—	—	3.9	V	1
3.3V Input High Voltage	V_{IH}		—	—	3.9	V	2
3.3V Input Low Voltage	V_{IL}		-0.5	—	—	V	
Storage Temperature	T_S		-65	—	150	°C	
Junction Temperature	T_J	Maximum operating junction temperature.	—	—	125	°C	
Input ESD Protection	ESD Prot	Human Body Model.	2000	—	—	V	

[1] Operation under these conditions is neither implied nor guaranteed.

[2] Maximum V_{IH} is not to exceed maximum V_{DD}.

Electrical Characteristics

All electrical characteristics are guaranteed over the operating conditions specified in Table 7 unless noted otherwise. See Test Loads for loading conditions

Table 6. PCIe Phase Jitter

Parameter	Symbol	Conditions	Typical	Maximum	Specification Limit	Unit	Notes
PCIe Phase Jitter Common Clocked Architecture (SSC off)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s).	1534	5035	86,000	fs Pk-Pk	1,2
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Hi Band (5.0 GT/s).	127	325	3,100	fs RMS	1,2
		PCIe Gen2 Lo Band (5.0 GT/s).	70	89	3,000		1,2
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s).	43	111	1,000		1,2
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s).	43	111	500		1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s).	17.1	50.0	150		1,2,3,5
	$t_{jphPCIeG6-CC}$	PCIe Gen6 (64.0 GT/s).	10.1	27.0	100		1,2,3,6
	$t_{jphPCIeG7-CC}$	PCIe Gen7 (128.0 GT/s).	7.0	18.9	67		1,2,3,7
PCIe Phase Jitter IR Architectures (SSC off)	$t_{jphPCIeG2-IR}$	PCIe Gen2 (5.0 GT/s).	120	209	N/A		1,2,8
	$t_{jphPCIeG3-IR}$	PCIe Gen3 (8.0 GT/s).	47	87			1,2,8
	$t_{jphPCIeG4-IR}$	PCIe Gen4 (16.0 GT/s).	48	88			1,2,3,4,8
	$t_{jphPCIeG5-IR}$	PCIe Gen5 (32.0 GT/s).	13.7	31.0			1,2,3,5,8
	$t_{jphPCIeG6-IR}$	PCIe Gen6 (64.0 GT/s).	9.6	17.6			1,2,3,5,8
	$t_{jphPCIeG7-IR}$	PCIe Gen7(128.0 GT/s).	6.8	12.4			1,2,3,5,8
PCIe Phase Jitter Common Clocked Architecture (SSC-0.5%)	$t_{jphPCIeG1-CC}$	PCIe Gen1 (2.5 GT/s).	3217	5902	86,000	fs Pk-Pk	1,2,3
	$t_{jphPCIeG2-CC}$	PCIe Gen2 Hi Band (5.0 GT/s).	270	414	3,100	fs RMS	1,2,3
		PCIe Gen2 Lo Band (5.0 GT/s).	188	566	3,000		1,2,3
	$t_{jphPCIeG3-CC}$	PCIe Gen3 (8.0 GT/s).	91	140	1,000		1,2,3
	$t_{jphPCIeG4-CC}$	PCIe Gen4 (16.0 GT/s).	91	140	500		1,2,3,4
	$t_{jphPCIeG5-CC}$	PCIe Gen5 (32.0 GT/s).	38.1	58.6	150		1,2,3,5
	$t_{jphPCIeG6-CC}$	PCIe Gen6 (64.0 GT/s).	21.1	32.4	100		1,2,3,5,6
	$t_{jphPCIeG7-CC}$	PCIe Gen7 (128.0 GT/s).	14.8	25	67		1,2,3,5,7
PCIe Phase Jitter IR Architectures (SSC -0.5%)	$t_{jphPCIeG2-IR}$	PCIe Gen2 (5.0 GT/s).	1322	1365	N/A		1,2,8
	$t_{jphPCIeG3-IR}$	PCIe Gen3 (8.0 GT/s).	470	488			1,2,8
	$t_{jphPCIeG4-IR}$	PCIe Gen4 (16.0 GT/s).	267	292			1,2,8
PCIe Phase Jitter IR Architectures (SSC -0.3%)	$t_{jphPCIeG5-IR}$	PCIe Gen5 (32.0 GT/s).	70.1	74.7			1,2,8
	$t_{jphPCIeG6-IR}$	PCIe Gen6 (64.0 GT/s).	59.3	61.6			1,2,8
PCIe Phase Jitter IR Architectures (SSC -0.15%)	$t_{jphPCIeG7-IR}$	PCIe Gen7 (128.0 GT/s).	31.8	33.7			1,2,8

[1] The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 7.0, Revision 1.0*. See the Test Loads section of the data sheet for the exact measurement setup. If oscilloscope data is used, equipment noise is removed from all results.

[2] Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak to peak jitter using a multiplication factor of 8.83. In the case where real-time oscilloscope and PNA measurements have both been done and produce different results, the RTO result must be used.

[3] SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.

[4] The CK440Q specification calls out a maximum of 400fs RMS. Note that 700fs RMS is to be used in channel simulations to account for additional noise in a real system.

[5] The CK440Q specification calls out a maximum of 80fs RMS. Note that 250fs RMS is to be used in channel simulations to account for additional noise in a real system.

[6] Note that 150fs RMS is to be used in channel simulations to account for additional noise in a real system.

[7] Note that 100fs RMS is to be used in channel simulations to account for additional noise in a real system.

[8] The *PCI Express Base Specification 7.0, Revision 1.0* provides the filters necessary to calculate IR jitter values, however, it does not provide specification limits, hence the n/a in the Limit column. IR values are informative only. Generally, a clock operating in an IR system must be twice as good as a clock operating in a Common Clock system. For RMS values, twice as good is equivalent to dividing the CC value by √2. For IR architectures operating at Gen4, Gen5 or Gen6 data rates, an additional consideration is which jitter value to divide by √2. The conservative approach is to divide the ref clock jitter limit. However, if the clock is close to the SOC, the case can be made for allocating the channel noise budget to the ref clock jitter budget. Then the channel simulation values mentioned above would be divided by √2. An example for Gen4 is as follows. A "rule-of-thumb" IR limit would be either 0.5ps RMS/√2 = 0.35ps RMS or 0.7ps RMS/√2 = 0.5ps RMS depending on whether the ref clock jitter limit, or channel noise budget were used (the ref clock is close to the SOC).

Table 7. Input/Supply/Common Parameters

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Supply Voltage	V_{DDX}	3.3V ±5%.	3.135	3.3	3.465	V	
Ambient Operating Temperature	T_{AMB}	No airflow.	-40	25	85	°C	
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, and tri-level inputs.	2	—	V_{DD} + 0.3	V	
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, and tri-level inputs.	GND - 0.3	—	0.8	V	
Input High Voltage	V_{IH}	Tri-level inputs.	2.4	—	V_{DD} + 0.3	V	
Input Mid Voltage	V_{IM}	Tri-level inputs.	1.2	VDD/2	1.8	V	
Input Low Voltage	V_{IL}	Tri-level inputs.	GND - 0.3	—	0.8	V	
Input Current	I_{IN}	Single-ended inputs, V_{IN} = GND, V_{IN} = V_{DD}.	-5	—	5	µA	4
	I_{INPUPD}	Single-ended inputs. V_{IN} = 0 V; Inputs with internal pull-up resistors. V_{IN} = V_{DD}; Inputs with internal pull-down resistors.	-50	6	50	µA	
Internal Resistor Values	P_{UP}/P_{DN}	Value of internal pull-up and pull-down resistors, except PFT_IN/PFT_IN#.	—	128	—	kΩ	
	$P_{DN\_PFT\_IN}$	Value of internal pull-down resistor on PFT_IN.	—	60	—	kΩ	
	$P_{UP\_PFT\_IN\#}$	Value of internal pull-up resistor on PFT_IN#.	—	56	—	kΩ	
Input Frequency	F_{IN}		—	25	—	MHz	
Pin Inductance	L_{pin}		—	—	7	nH	1

Table 7. Input/Supply/Common Parameters (Cont.)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	—	—	4.5	pF	1
	C_{INDIF_IN}	Differential clock inputs.	—	—	2.7	pF	1
	C_{OUT}	Output pin capacitance.	—	—	4.5	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or de-assertion of PWRDN# to valid outputs.	—	2.2	5	ms	1,2
OE# Latency	$t_{LATOE\#}$	100M[x] start after OE[x]# pin assertion. 100M[x] stop after OE[x]# pin deassertion.	4	5	10	clocks	1,2,3
Tdrive_PD#	t_{DRVPD}	Differential output enable after PWRDN# de-assertion.	—	107	300	µs	1,3
Tfall	t_F	Fall time of control inputs.	—	—	5	ns	2
Trise	t_R	Rise time of control inputs.	—	—	5	ns	2

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Time from deassertion until outputs are > 200mV.

[4] Applies to single-ended inputs without pull-up or pull-down resistors.

Table 8. Skew, Jitter and Duty Cycle

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Output to Output Skew	t_{SKEW}	100M[3,1:0]	15	27	57	N/A	ps	1,2
		MXCK[5:4]	110	195	285			
		25M2 + MXCK[5:4]	198	302	434			
Cycle to Cycle Jitter	t_{JCC100}	100M[3,1:0]	—	22	38	50	ps	1,2
	t_{JCC25}	25M2 + MXCK[5:4]	—	30	49	125		
Duty Cycle	t_{DC100}	100M[3,1:0]	49.0	50.3	52.0	45 to 55	%	1,2
	t_{DC25}	25M2 and MXCLK[5:4] set to 25MHz	49.0	50.1	51.0	45 to 55		
	t_{DC25}	25M2 and MXCLK[5:4] set to 25MHz with XO as source on XIN_ CLKIN with 44/55% duty cycle.	49.0	50.1	51.0	43 to 57		

[1] Measured into AC test load.

[2] Measured from differential cross-point to differential cross-point.

Table 9. Differential Clock Outputs Driving High Impedance Receiver

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	2.0	3.1	4.0	2 to 4	V/ns	1,2,3
Rise/Fall Matching	ΔtR/tF	Single-ended measurement.	—	6	19	20	%	4
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value. (scope averaging off).	800	877	970	1150	mV	1,7,8
Minimum Voltage	Vmin		-150	-67	0	-300		1,5,7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	363	443	505	250 to 550	mV	1,6,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.	20	25	35	140	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] Includes 300mV of overshoot for Vmax and 300mV of undershoot for Vmin.

Table 10. Differential Clock Outputs Driving Terminated Receiver (Double Termination)

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Slew Rate	dV/dt	Scope averaging on.	1.5	1.8	2.4	1 to 3	V/ns	1,2,3
Rise/Fall Matching	ΔtR/tF	Single-ended measurement.	—	11	19	20	%	4
Maximum Voltage	Vmax	Measurement on single-ended signal using absolute value. (scope averaging off).	—	428	485	330 to 575	mV	7,8
Minimum Voltage	Vmin		-50	-4	—	-150		1,5,7,8
Crossing Voltage (abs)	Vcross_abs	Scope averaging off.	170	211	260	125 to 275	mV	1,6,7
Crossing Voltage (var)	Δ-Vcross	Scope averaging off.	—	8	12	70	mV	1,6,7

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Measured from differential waveform.

[3] Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a ±75mV window around differential 0V.

[4] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±37mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

[5] Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

[6] The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting Δ-Vcross to be smaller than Vcross absolute.

[7] At default SMBus settings.

[8] Includes 150mV of overshoot for Vmax and 150mV of undershoot for Vmin.

Table 11. Current Consumption

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	$I_{DDMXCK25}$	Sum of VDDMXCK pins, MXCK at 25MHz.	—	22	24	mA	1, 3
	I_{DD100M}	Sum of VDD100M pins.	—	39	48	mA	1
	I_{DDXTAL}	VDDXTAL, 25MHz XTAL.	—	1.3	2	mA	1
	I_{DDPFT}	VDDPFT.	—	12.1	15	mA	1,3
	I_{DDA25M}	VDDA25M, 25M[2] on.	—	22.1	24	mA	1
	$I_{DDA100M}$	VDDA100M, SSC on.	—	24.6	26	mA	2
Power Down Supply Current	I_{DDMXCK}	Sum of VDDMXCK pins.	—	8.1	9	mA	2
	I_{DD100M}	Sum of VDD100M pins.	—	7.8	9	mA	2
	I_{DDXTAL}	VDDXTAL, 25MHz XTAL.	—	1.4	2	mA	2
	I_{DDPFT}	VDDPFT.	—	1.3	3	mA	2,4
	I_{DDA25M}	VDDA25M, 25M[2] on (25MPG = 1).	—	19.4	21	mA	2
		VDDA25M, 25M[2] off (25MPG = 0).	—	9.9	11	mA	2
	$I_{DDA100M}$	VDDA100M.	—	3.8	5	mA	1, 3

[1] PWRGD/PWRGDN# = 1, all outputs enabled.

[2] PWRGD/PWRGDN# = 0.

[3] For outputs are driving source-terminated high-impedance loads. Add 7mA for each output at 25M driving a double-terminated load and 2.5mA for each output at 100M driving a double-terminated load.

Table 12. Power Supply Noise Profile

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Power Supply Noise	V_{DD_AC}	Single tone AC noise, swept.	—	50	—	mV	1
	V_{DDA_AC}	V_{DD} electrical noise > 20MHz.	—	50	—	mV	1
	V_{DDXTAL}	V_{DD} electrical noise 12kHz to 25MHz.	—	50	—	mV	1

[1] Peak-to-peak values. The device meets all AC/DC parameters in the presence of at least this much noise.

Table 13. SMBus

Parameter	Symbol	100kHz Class Operation		400kHz Class Operation		Units	Notes
		Minimum	Maximum	Minimum	Maximum		
SMBus Operating Frequency	f_{SMB}	10	100	10	400	kHz	
Bus Free Time between STOP and START Condition	t_{BUF}	4.7	—	1.3	—	µs	
Hold Time after (REPEATED) START Condition	$t_{HD:STA}$	4	—	0.6	—	µs	1
REPEATED START Condition Setup Time	$t_{SU:STA}$	4.7	—	0.6	—	µs	
STOP Condition Setup Time	$t_{SU:STO}$	4	—	0.6	—	µs	
Data Hold Time	$t_{HD:DAT}$	300	—	0	—	ns	2
Data Setup Time	$t_{SU:DAT}$	250	—	100	—	ns	
Detect SMBDAT Low Timeout	$t_{TIMEOUT}$	25	35	25	35	ms	3
Detect Clock Low Timeout	$t_{TIMEOUT}$	25	35	25	35	ms	4
Clock Low Period	t_{LOW}	4.7	—	1.3	—	µs	
Clock High Period	t_{HIGH}	4	50	0.6	50	µs	5
Clock/Data Fall Time	t_F	—	300	—	300	ns	6
Clock/Data Rise Time	t_R	—	1000	—	300	ns	6
Time in which a device must be operational after power-on reset	t_{POR}	—	500	—	500	ms	7

[1] After this period, the first clock is generated.

[2] The 9SQ44x device maintains 300ns data hold time for backwards compatibility with the SMBus 2.0 specification. Newer versions of the SMBus specification call out 0ns data hold time for both 100kHz and 400kHz classes.

[3] The 9SQ44x provided additional SMBus protection by implementing a timeout for SMBDATA being held low in excess of $t_{TIMEOUT}$, in addition to the SMBCLK low timeout.

[4] Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT}$, Minimum. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT}$, Maximum. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT}$, Maximum or longer.

[5] t_{HIGH}, Maximum provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than t_{HIGH}, Maximum.

[6] The rise and fall time measurement limits are defined as follows:

Rise Time Limits: (V_{IL}, MAX - 0.15V) to (V_{IH},MIN + 0.15V)

Fall Time Limits: (V_{IH},MIN + 0.15 V) to (V_{IL},MAX - 0.15V)

[7] The default configuration requires power to be applied with PWRGD/PWRDN# = 1 for the SMBus to be active.

Table 14. Side Band Interface

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Clock Period	t_{PERIOD}	Clock period.	40	—	—	ns	
Setup Time to Clock	t_{SETUP}	SHFT setup to CLK rising edge.	10	—	—	ns	1
Data set up time	t_{DSU}	DATA setup to CLK rising edge.	5	—	—	ns	1
Data hold time	t_{DHOLD}	DATA hold after CLK rising edge.	2	—	—	ns	1
Delay time	t_{DELAY}	Delay from CLK rising edge to LD# falling edge.	10	—	—	ns	1
Propagation Delay	t_{PD}	Delay from LD# falling edge to next output configuration taking effect.	1	—	12	clocks	3
Slew Rate	t_{SLEW}	CLK input (between 20% and 80%).	0.7	0.9	1.5	V/ns	2
Output Impedance	Z_{OUT}	SBI_OUT output impedance.	—	41	—	Ω	

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Control input must be monotonic from 20% to 80% of input swing.

[3] Refers to device differential output clock.

Figure 2. Side Band Interface Timing Diagram

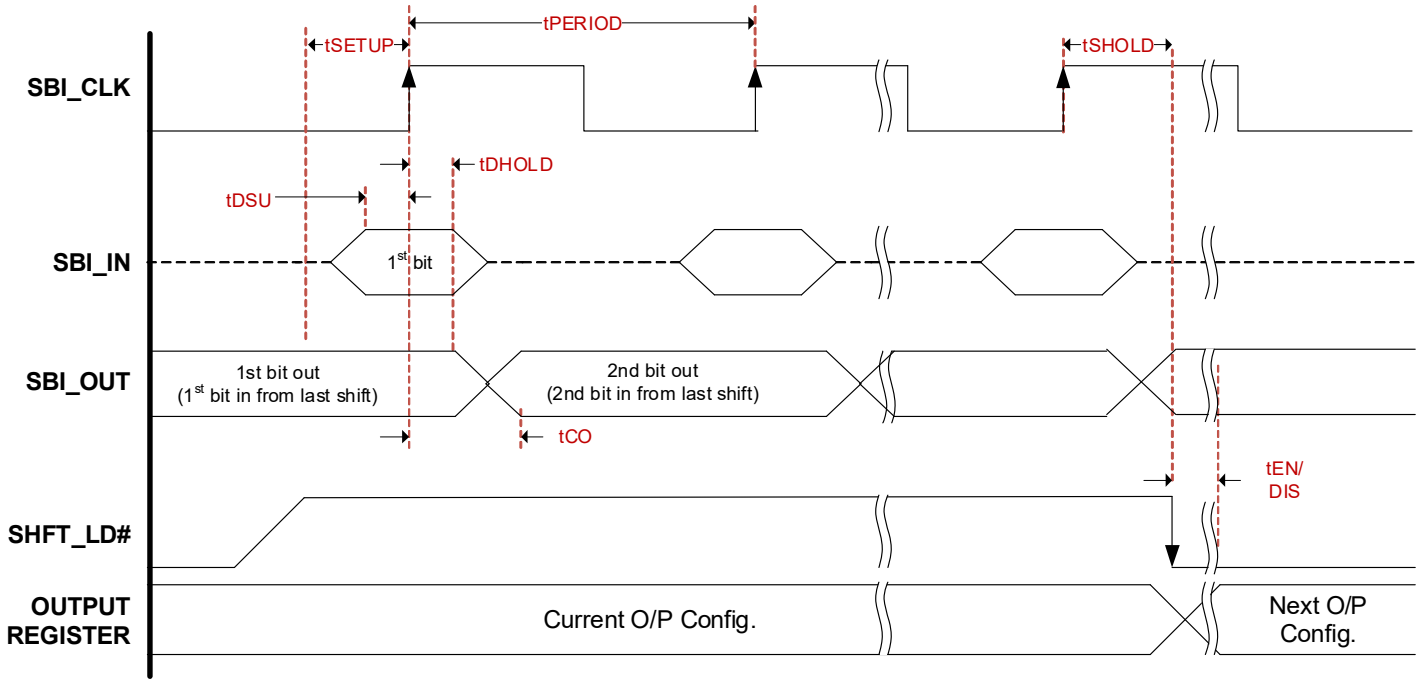


Table 15. Recommended Crystal Characteristics [1]

Parameter	Value	Units
Frequency	25	MHz
Resonance Mode	Fundamental	—
Equivalent Series Resistance (ESR)	50	Ω Max
Shunt Capacitance (C_O)	4	pF Max
Load Capacitance (C_L)	8	pF Max
Drive Level	200	µW Max
Frequency Tolerance at 25°C [2]	±20	PPM Max
Frequency Stability, ref at 25°C Over Operating Temperature Range [2]	±20	PPM Max
Temperature Range (commercial) [2]	0 to 70	°C
Temperature Range (industrial) [2]	-40 to 85	°C
Aging Per Year [2]	±5	PPM Max

1 When driven by an external oscillator via the XIN/CLKIN_25 pin, X2 should be floating.

2. These parameters depend on specific customer requirements and may differ from the values listed here.

Test Loads

Figure 3. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)

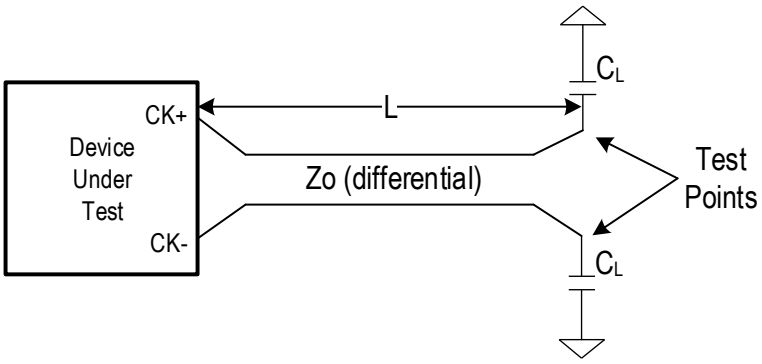


Table 16. AC/DC Test Load Parameters for Differential Outputs

Rs (Ω)	Zo (Ω)	L (cm)	C_L (pF)
Internal	85	25.4	2

Figure 4. AC/DC Test Load for Differential Outputs (Double-Terminated)

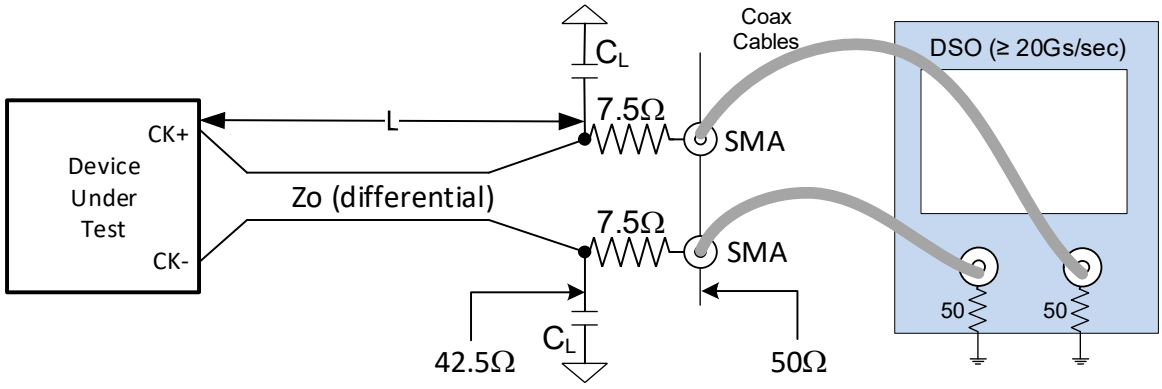


Figure 5. Test Load for PCIe Phase Jitter Measurements

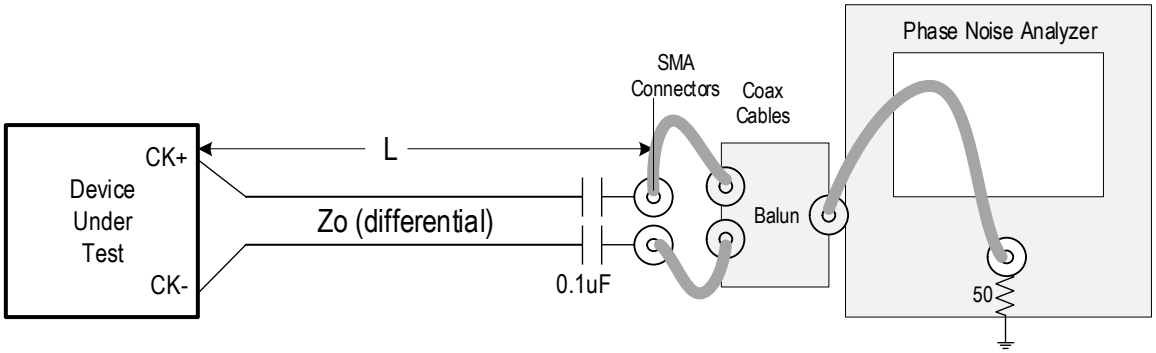


Table 17. Test Load Parameters for PCIe Gen5 Jitter Measurement

Rs (Ω)	Zo (Ω)	L (cm) *	C_L (pF)
Internal	85	25.4	N/A

* Note: PCIe Gen5 specifies L = 0cm. L = 25.4cm is more conservative.

Figure 6. AC/DC Test Load for SBI OUT

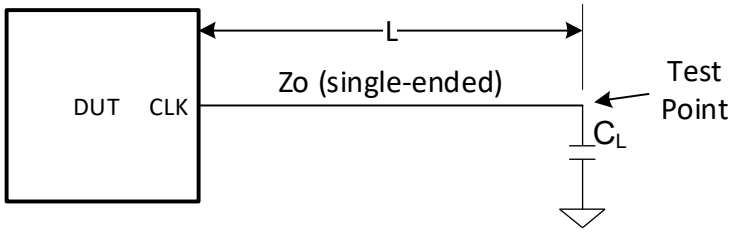


Table 18. AC/DC Test Load Parameters for SBI_OUT

Rs (Ω)	Zo (Ω)	L (cm) *	C_L (pF)
Internal	50	25.4	2pF

* Note: PCIe Gen5 specifies L = 0cm. L = 25.4cm is more conservative.

Output Enable Control on CK440Q

Traditional Method

The CK440BQ has two methods for enabling and disabling outputs. The first is the traditional method of OE# pins and SMBus output enable bits. Outputs 100M[6:0] have dedicated output enable pins for PCIe slot applications. All outputs have dedicated SMBus output enable bits in Bytes [2:0] of the SMBus register set.

Side-Band Interface

The second method is a simple serial interface referred to as the Side-Band Interface (SBI). In the DB2000QL, this is a 3-wire interface consisting of SBI_DATA (input), SBI_CLK and SHFT_LD# pins. The CK440Q adds an additional pin - SBI_OUT. This output is the last stage of the internal 20-bit shift register. The SBI_DATA pin is renamed to SBI_IN. When the SHFT_LD# pin is high, the rising edge of SBI_CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# loads the shift register contents to the output control register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable of outputs, regardless of the method used.

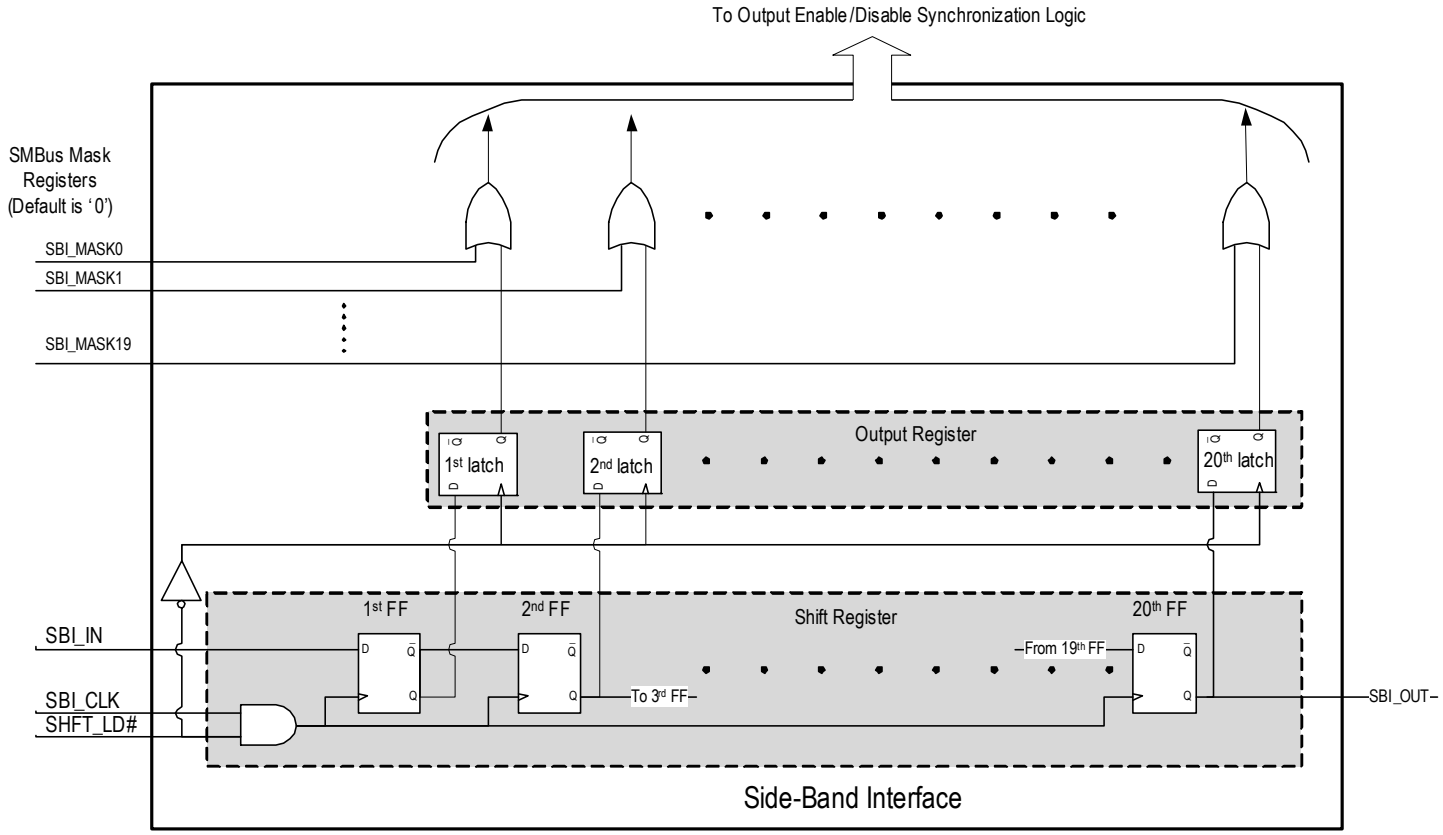
Since the CK440Q has dedicated pins for the SBI, both SBI and the traditional SMBus methods are active at the same time. This is different from the DB2000QL, which requires a strapping pin to select the active interface. There are SMBus registers for masking off the disable function of the SBI interface. When set to a one, the mask register forces the SBI interface for its respective output to indicate 'enabled'. This prevents accidentally disabling critical outputs when using the SBI. The traditional SMBus enable bits and the OE# pins may still disable an output.

If the application does not use the SBI, the SBI input pins may be tied 'Low'.

After applying power, the SBI is active, even if the PWRGD/PWRDN# pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output control register before the assertion of PWRGD/PWRDN#. Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the PWRGD/PWRDN# is low. The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The SBI mask registers default to zero at power-up, allowing the shift register bits to disable their respective output.

An additional feature in the CK440BQ is the ability to read back the contents of the shift register from the SMBus. The SMBus values update on each falling edge of SHFT_LD#. Note: The SBI shift register may only be loaded via the serial interface. Figure 7 provides a high-level functional description of the SBI.

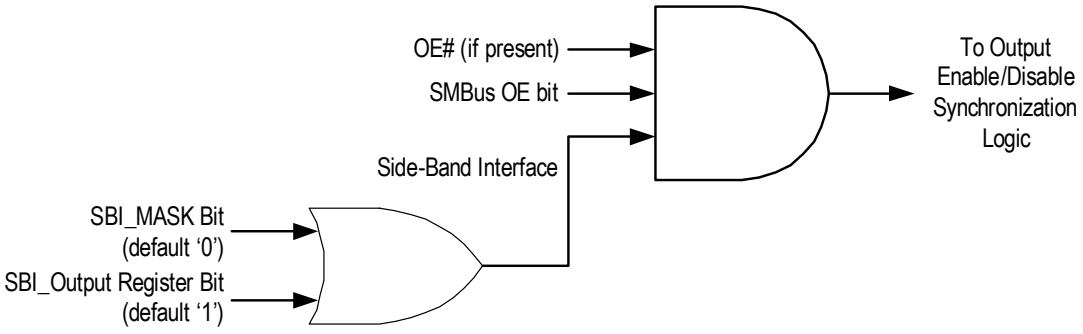
Figure 7. Side Band Interface High-Level Functional Description



Output Enable/Disable Priority

The CK440Q outputs require that outputs be enabled by an 'AND' function of all methods of enabling the output. Figure 8 illustrates this. There are three enable/disable paths: OE# pin (if present), an SMBus OE bit and the Side-Band Interface. All three must indicate 'enable' for the output to be enabled. Conversely, any single enable/disable path can disable an output if it indicates 'disable'.

Figure 8. Output Enable Logic (per output)



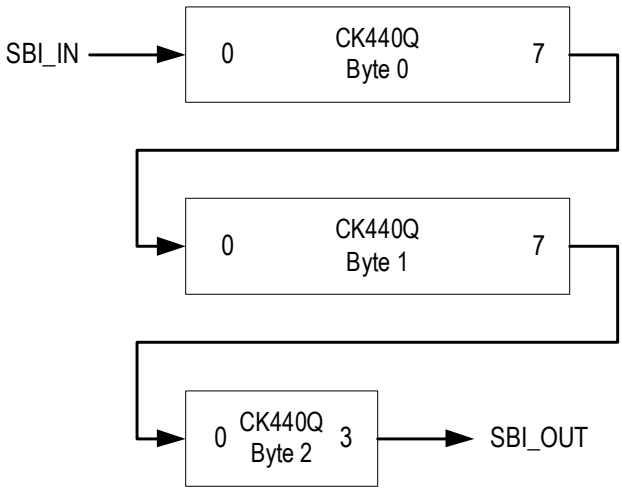
A closer study of Figure 8 shows the following must be true to enable an output:

- OE# pin (if present) must be 'low'
- SMBus OE bit must be 'high'
- Side-Band Interface must be 'high'

Additionally, one can see that the Side-Band Interface indicates a 'high' if the SBI_Mask_Bit OR the SBI_Output Register Bit are 'high'. This means that the SBI_MASK_Bit can prevent the SBI interface from disabling an output. Recall that the SBI_MASK_Bits are SMBus registers.

The shift order follows the order of the SMBus enable bits in Byte[2:0] as shown in Figure 9. The first bit shifted in would be the output enable for the PFT_OUT, which is in Byte 2 bit 3. The last bit shifted in would be the output enable for 100M0, which is in Byte 0, bit 0.

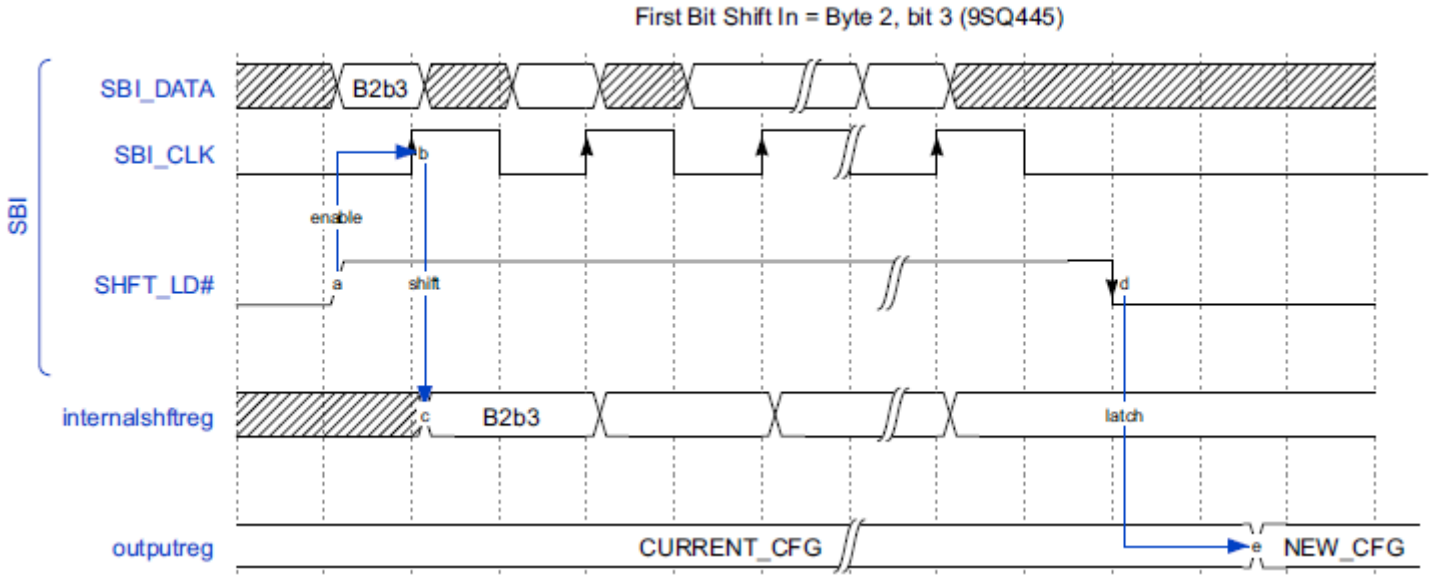
Figure 9. CK440Q Side-Band Shift Order



The SMBus registers for the SBI Output and SBI_Mask follow the same bit order. Note that the SBI Output register contains the value latched from the shift register. Software must apply the SBI Mask bits to this value to get the output of the Side-Band Interface OR gate in Figure 8.

Figure 10 shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the SBI_CLK input. Next, the rising edge of SBI_CLK clocks SBI_IN data into the shift register. After the 20th clock, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# latches the shift register contents to the output control register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

Figure 10. Side-Band Interface Functional Timing



The SBI interface supports clock rates up to 25MHz. The CK440Q allows two SBI connection topologies - star and daisy chain. In a star topology (Figure 11), multiple devices may share SBI_CLK and SBI_IN pins. In this topology, each CK440Q has a dedicated SHFT_LD# pin. In a daisy-chain topology, the SBI_OUT of one device connects to the SBI_IN device of a downstream device. When using the daisy chain topology (Figure 12), the user must shift a complete set of bits for the combined devices. Two daisy-chained CK440Q devices require shifting of 40 bits. When the SHFT_LD# pin is low, the SBI interface ignores any activity on the SBI_CLK and SBI_IN pins.

Figure 11 illustrates a star topology connection for the CK440Q SBI interface. The star topology allows independent configuration of each device. For CK440Q, this means shifting 20 bits at a time. A disadvantage is that a separate SHFT_LD# pin is required for each device.

Figure 11. Star SBI Topology for CK440Q

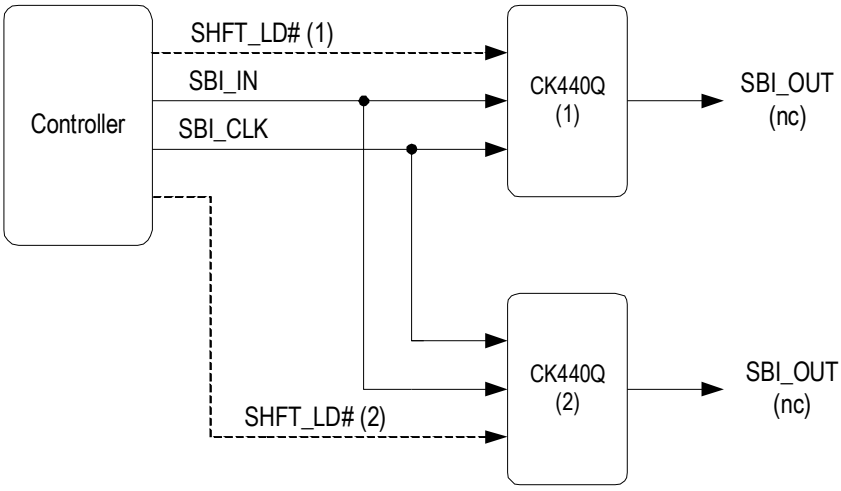
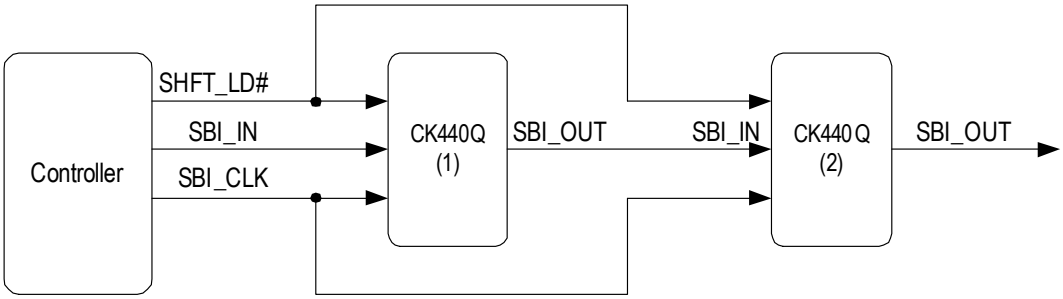


Figure 12. Daisy-Chain SBI Topology for CK440Q



The daisy chain topology allows configuration of any number of devices with only three signals from the SBI controller. It utilizes the SBI_OUT pin of one device to drive the SBI_IN pin of the next device in the daisy chain. Users must take care to shift the proper number of bits in this configuration. For the example shown in Figure 12, the SBI bit stream consists of 40 bits.

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledg**e each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if $X_{(H)}$ was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas (Slave/Receiver)**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

Table 19. SMBus Address Selection

SMB_ADR0_tri	SMBus Address
L	B2
M	B4
H	B6

Table 20. Byte 0: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	RW	0	—
6	Reserved	—	—	RW	0	—
5	Reserved	—	—	RW	0	—
4	Reserved	—	—	RW	0	—
3	Output Enable 100M3	Disabled	Enabled	RW	1	100M3
2	Reserved	—	—	RW	0	—
1	Output Enable 100M1	Disabled	Enabled	RW	1	100M1
0	Output Enable 100M0	Disabled	Enabled	RW	1	100M0

Table 21. Byte 1: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	RW	0	—
6	Reserved	—	—	RW	0	—
5	Output Enable MXCK5	Disabled	Enabled	RW	1	MXCK5
4	Output Enable MXCK4	Disabled	Enabled	RW	1	MXCK4
3	Reserved	—	—	RW	0	—
2	Reserved	—	—	RW	0	—
1	Reserved	—	—	RW	0	—
0	Reserved	—	—	RW	0	—

Table 22. Byte 2: Output Enable Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	MXCK_SEL	100MHz	25MHz	R/W	1	MXCK
6	MXCK_SEL Control	Pin control	Register control	R/W	1	MXCK
5	Reserved	—	—	—	0	—
4	Reserved	—	—	—	0	—
3	Reserved	—	—	—	0	—
2	Output Enable 25M2	Disabled	Enabled	RW	1	25M2
1	Output Enable 25M1	Disabled	Enabled	RW	0	25M1
0	Output Enable 25M0	Disabled	Enabled	RW	0	25M0

Table 23. Byte 3: Reserved Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	R	0	—
6	Reserved	—	—	R/W	0	—
5	Reserved	—	—	RW	0	—
4	Reserved	—	—	RW	0	—
3	Reserved	—	—	RW	0	—
2	Reserved	—	—	RW	0	—
1	Reserved	—	—	RW	0	—
0	Reserved	—	—	RW	0	—

Table 24. Byte 4: Reserved Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	R	N/A	—
6	Reserved	—	—	R	N/A	—
5	Reserved	—	—	R	N/A	—
4	Reserved	—	—	R	N/A	—
3	Reserved	—	—	R	N/A	—
2	Reserved	—	—	R	N/A	—
1	Reserved	—	—	R	N/A	—
0	Reserved	—	—	R	N/A	—

Table 25. Byte 5: Reserved Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	R	N/A	—
6	Reserved	—	—	R	N/A	—
5	Reserved	—	—	R	N/A	—
4	Reserved	—	—	R	N/A	—
3	Reserved	—	—	R	N/A	—
2	Reserved	—	—	R	N/A	—
1	Reserved	—	—	R	N/A	—
0	Reserved	—	—	R	N/A	—

Table 26. Byte 6: SSC PLL Control Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	—	Reserved	—
6	Reserved	—	—	—	Reserved	—
5	Readback of SSC_ENABLE pin	Bit[1:0]: SSC State 00: SSC Off, 01: SSC = -0.3% 10: Reserved, 11: SSC = -0.5%		R	Realtime	100M and MXCK if Byte2[7] = 0
4				R	Realtime	
3	SSC PLL Input Source	Xtal	Filter PLL	RW	0	
2	SSC Pin Control	Pin Control	Software Control	RW	0	
1	SSC Select	Bit[1:0]: SSC State 00: SSC Off, 01: SSC = -0.3% 10: Reserved, 11: SSC = -0.5%		RW	Latch SSC pin on power-up	
0				RW	Latch SSC pin on power-up	

Table 27. Byte 7: OE# Pin Realtime Readback Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	R	0	—
6	Reserved	—	—	R	0	—
5	Reserved	—	—	R	0	—
4	Reserved	—	—	R	0	—
3	Realtime Readback of OE3# pin	OE3# Low	OE3# High	R	Realtime	100M3
2	Reserved	—	—	R	0	—
1	Realtime Readback of OE1# pin	OE1# Low	OE1# High	R	Realtime	100M1
0	Realtime Readback of OE0# pin	OE0# Low	OE0# High	R	Realtime	100M0

Table 28. Byte 8: Vendor/Revision Identification Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Revision Code Bit 3	0000 is 1st Silicon		R	0	—
6	Revision Code Bit 2			R	0	—
5	Revision Code Bit 1			R	0	—
4	Revision Code Bit 0			R	0	—
3	Vendor ID Bit 3	0001 is Renesas		R	0	—
2	Vendor ID Bit 2			R	0	—
1	Vendor ID Bit 1			R	0	—
0	Vendor ID Bit 0			R	1	—

Table 29. Byte 9: Device ID Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Device ID 7 (MSB)	9SQ445 is TBD		R	TBD	—
6	Device ID 6			R	TBD	—
5	Device ID 5			R	TBD	—
4	Device ID 4			R	TBD	—
3	Device ID 3			R	TBD	—
2	Device ID 2			R	TBD	—
1	Device ID 1			R	TBD	—
0	Device ID 0			R	TBD	—

Table 30. Byte 10: Byte Count Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—		0	—
6	Reserved	—	—		0	—
5	BC5 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
4	BC4 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
3	BC3 - Writing to this register configures how many bytes will be read back	—	—	RW	1	—
2	BC2 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
1	BC1 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—
0	BC0 - Writing to this register configures how many bytes will be read back	—	—	RW	0	—

Table 31. Byte 11: Side-Band Interface Mask Register 0

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	RW	0	—
6	Reserved	—	—	RW	0	—
5	Reserved	—	—	RW	0	—
4	Reserved	—	—	RW	0	—
3	SBI Mask 100M3	SBI May Disable the Output	SBI Always Indicates Enable	RW	0	100M3
2	Reserved	—	—	RW	0	—
1	SBI Mask 100M1	SBI May Disable the Output	SBI Always Indicates Enable	RW	0	100M1
0	SBI Mask 100M0	SBI May Disable the Output	SBI Always Indicates Enable	RW	0	100M0

Note:

If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit, or OE# pin (present only for 100M outputs).

Table 32. Byte 12: Side-Band Interface Mask Register 1

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	RW	0	—
6	SBI Mask MXCK5	SBI May Disable the Output	SBI Always Indicates Enable	RW	0	MXCK5
5	SBI Mask MXCK4	SBI May Disable the Output	SBI Always Indicates Enable	RW	0	MXCK4
4	Reserved	—	—	RW	0	—
3	Reserved	—	—	RW	0	—
2	Reserved	—	—	RW	0	—
1	Reserved	—	—	RW	0	—
0	Reserved	—	—	RW	0	—

Note:

If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit, or OE# pin (present only for 100M outputs).

Table 33. Byte 13: Side-Band Interface Mask Register 2

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—		0	—
6	Reserved	—	—		0	—
5	Reserved	—	—		0	—
4	Reserved	—	—		0	—
3	Reserved	—	—	RW	0	—
2	SBI Mask 25M2	SBI May Disable the Output	SBI Always Indicates Enable	RW	0	25M2
1	Reserved	—	—	RW	0	—
0	Reserved	—	—	RW	0	—

Note:

If '0', the Side-Band Interface register may disable the output. If '1', the Side-Band Interface cannot disable the output. Such an output may only be disabled by the respective SMBus bit, or OE# pin (present only for 100M outputs).

Table 34. Byte 14: Side-Band Interface Readback Register 0

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	R	1	Reserved
6	Reserved	—	—	R	1	Reserved
5	Reserved	—	—	R	1	Reserved
4	Reserved	—	—	R	1	Reserved
3	SBI Readback 100M3	Disabled	Enabled	R	1	100M3
2	Reserved	—	—	R	1	Reserved
1	SBI Readback 100M1	Disabled	Enabled	R	1	100M1
0	SBI Readback 100M0	Disabled	Enabled	R	1	100M0

Note:

If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high and OE# pin (present only for 100M outputs) is pulled low.

Table 35. Byte 15: Side-Band Interface Readback Register 1

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	R	1	Reserved
6	Reserved	—	—	R	1	Reserved
5	SBI Readback MXCK5	Disabled	Enabled	R	1	MXCK5
4	SBI Readback MXCK4	Disabled	Enabled	R	1	MXCK4
3	Reserved	—	—	R	1	Reserved
2	Reserved	—	—	R	1	Reserved
1	Reserved	—	—	R	1	Reserved
0	Reserved	—	—	R	1	Reserved

Note:

If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high and OE# pin (present only for 100M outputs) is pulled low.

Table 36. Byte 16: Side-Band Interface Readback Register 2

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
7	Reserved	—	—	R	0	—
6	Reserved	—	—	R	0	—
5	Reserved	—	—	R	0	—
4	Reserved	—	—	R	1	—
3	SBI Readback 25M2	Disabled	Enabled	R	1	25M2
2	Reserved	—	—	R	1	—
1	Reserved	—	—	R	1	—
0	Reserved	—	—	R	0	—

Note:

If the Side-Band interface is used, this register latches the content of the shift register. A '0' indicates that the corresponding differential output is disabled unless the bit has been masked off in SBI Mask register. A '1' indicates that the output is enabled if the corresponding SMBus OE bit is set high and OE# pin (present only for 100M outputs) is pulled low.

Thermal Characteristics

Table 37. Thermal Characteristics

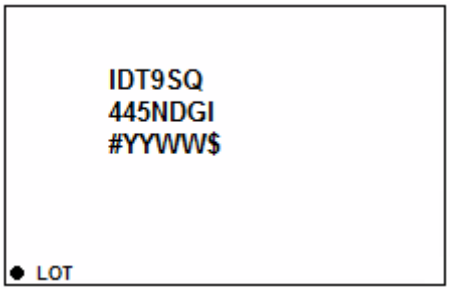
Parameter	Symbol	Conditions	Package	Typical Value	Units	Notes
Thermal Resistance	θ_{JC}	Junction to case.	NDG40	32	°C/W	1
	θ_{Jb}	Junction to base.		2	°C/W	1
	θ_{JA0}	Junction to air, still air.		44	°C/W	1
	θ_{JA1}	Junction to air, 1 m/s air flow.		37	°C/W	1
	θ_{JA3}	Junction to air, 3 m/s air flow.		33	°C/W	1
	θ_{JA5}	Junction to air, 5 m/s air flow.		31	°C/W	1

[1] EPAD soldered to board.

Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Marking Diagram

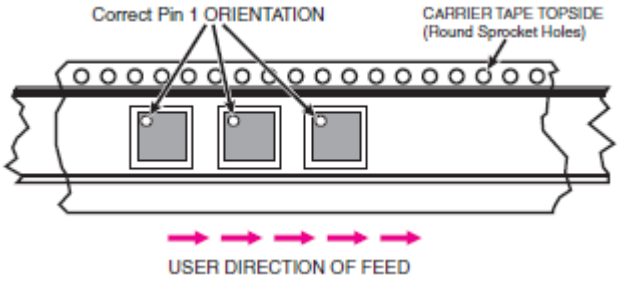


- Line 1 and 2: part number
  - "I" denotes industrial temperature.
- Line 3:
  - "#" denotes the stepping number.
  - "YYWW" is the last digits of the year and week that the part was assembled.
  - "$" denotes mark code.
- "LOT" denotes the lot sequence code.

Ordering Information

Part Number	Package	Carrier Type	Temperature
9SQ445NDGI	5 × 5 mm, 0.4mm pitch 40-VFQFPN	Tray	-40° to +85°C
9SQ445NDGI8	5 × 5 mm, 0.4mm pitch 40-VFQFPN	Tape and Reel (EIA-481-C)	-40° to +85°C

Table 38. Pin 1 Orientation in Tape and Reel Packaging

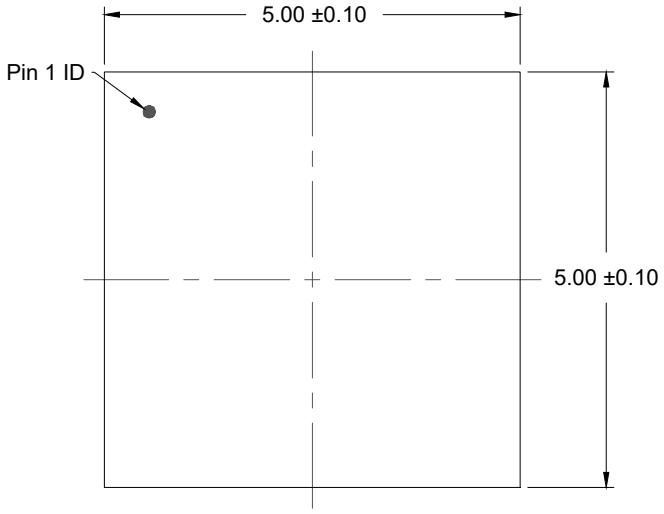
Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	

Revision History

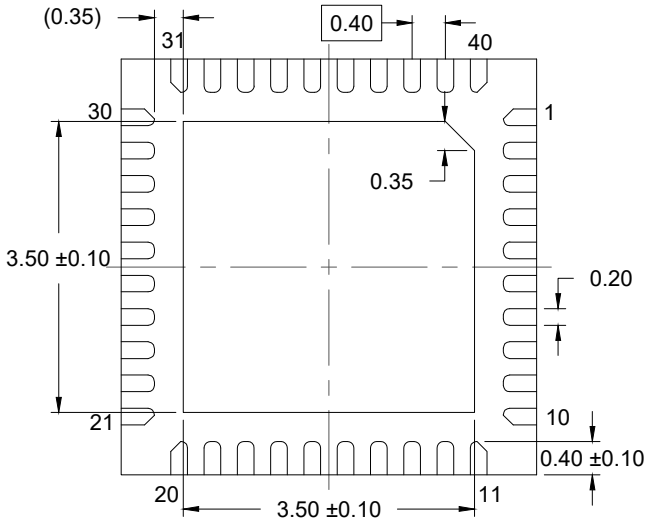
Revision Date	Description of Change
August 5, 2026	▪ Updated Table 6 and footnotes. ▪ Updated front page to reflect Gen7.
May 8, 2023	Corrected Byte 7, bit 3 to indicate OE3# real time read back.
February 14, 2022	▪ Updated front page text to indicate PCIe Gen6 support. ▪ Added PCIe Gen6 parameters to Table 6 and changed all units to fs RMS except for PCIe Gen1, which remains ps (Pk-Pk). ▪ Updated footnotes.
July 26, 2021	Removed “A” from the orderable part numbers.
July 14, 2021	Initial release

Package Outline Drawing

PSC-4292-02
NDG40P2
40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch
Rev.03, May 20, 2025

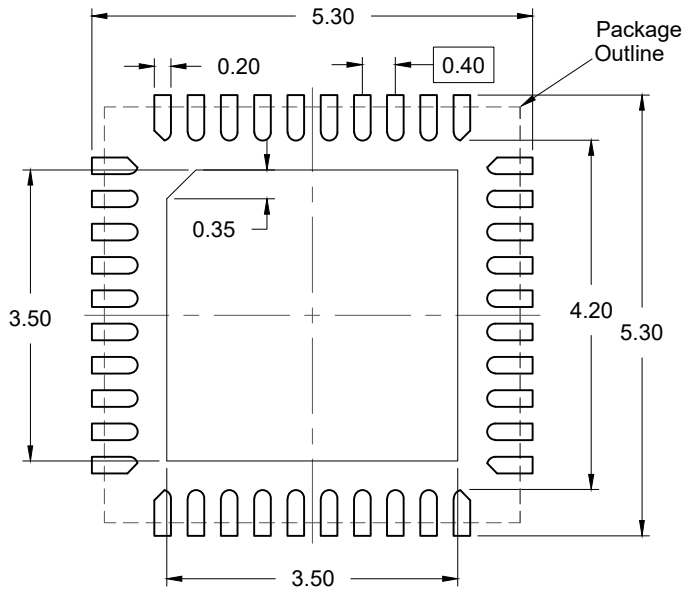


TOP VIEW



BOTTOM VIEW

SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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