

9QXL2002B

20-Output DB2000QL PCIe Clock Buffer

Description

The **9QXL2002B** is a 20-output very-low-additive phase jitter fanout buffer for PCIe Gen1-7 and UPI applications. The **9QXL2002B** provides three methods to control output enables; standard OE# pins, SMBus enable bits, or a simple 3-wire serial interface that is independent of the SMBus. The OE Control Mode is set via a hardware strap. It offers integrated terminations for 85Ω transmission lines.

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum

Typical Applications

- Servers, Storage, Networking, Accelerators

Key Specifications

- PCIe Gen7 additive phase jitter: 4fs RMS
- DB2000Q additive phase jitter: 17fs RMS
- 12kHz to 20MHz additive phase jitter: 62fs RMS at 156.25MHz

Features

- 3.3V tolerant outputs support M-XIO applications
- Power Down Tolerant (PDT) inputs
- Flexible Startup Sequencing (FSS)
- Automatic Clock Parking (ACP) upon loss of input clock
- Three Output Enable Control modes:
 - Traditional 8 OE# pins allow hardware control of 8 outputs
 - 20 SMBus bits allow software control of each output
 - Simple 3-wire Side-Band Interface allows real-time control of all 20 outputs
- Outputs remain Low/Low when powered up with floating input clock
- Nine selectable SMBus addresses
- Spread-spectrum compatible
- 6 × 6 mm dual-row 80-GQFN
- 20 Low-Power HCSL (LP-HCSL) 85Ω output pairs
- Operating Temperature Range -40° to +105°C

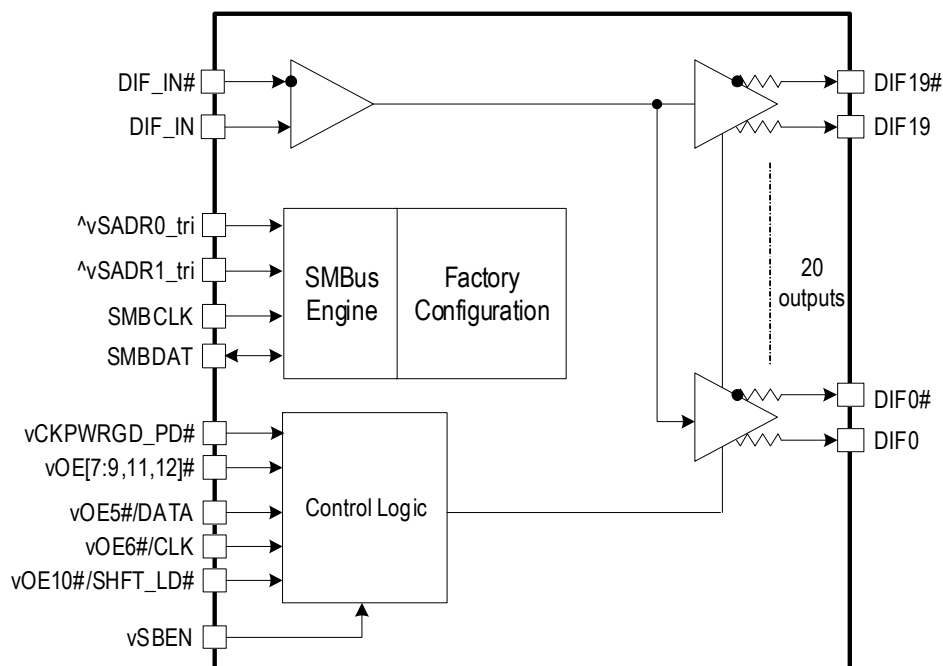
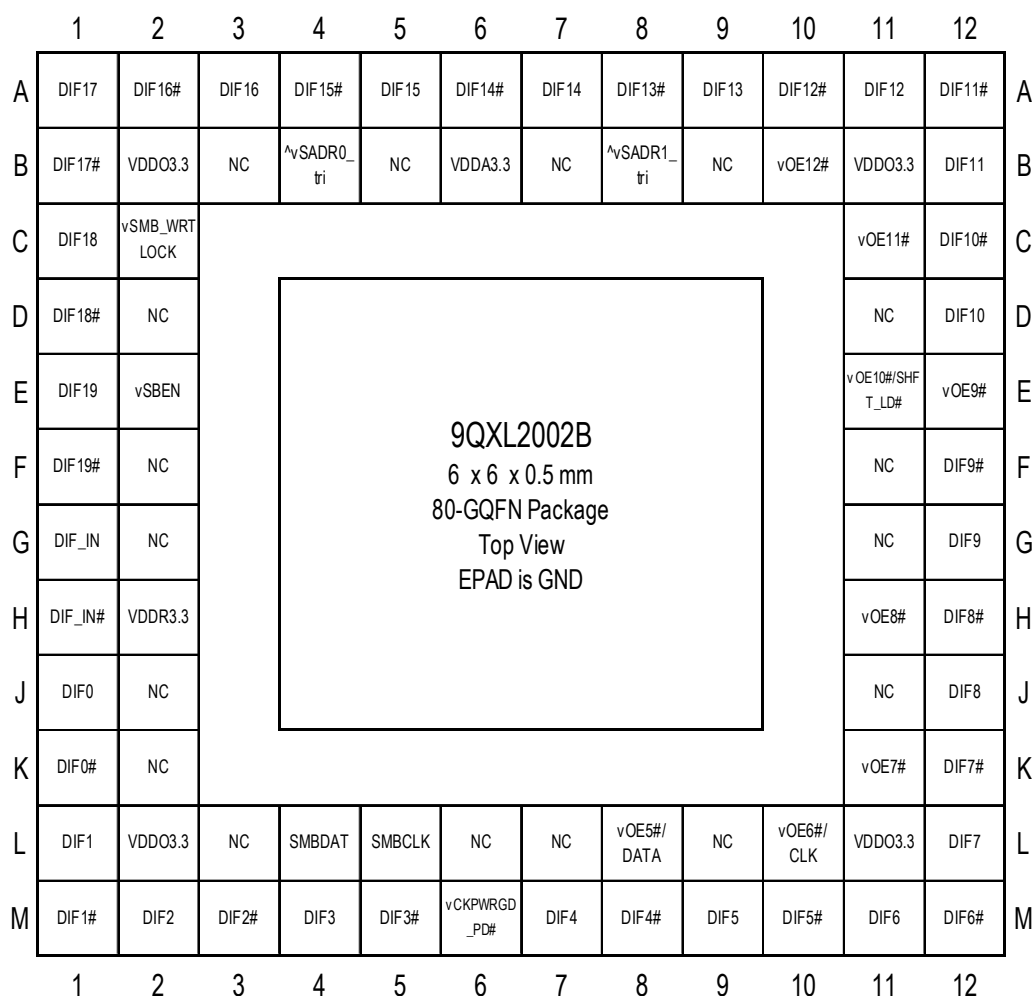


Figure 1. Block Diagram

Contents

1. Pin Information	3
1.1 Power Down Tolerant Pins	6
1.2 Signal Types	6
2. Output Control	6
3. Power Management	7
4. Output Enable Control	7
4.1 Traditional Method	7
4.2 Side-Band Interface	7
4.3 Automatic Clock Parking	9
5. Absolute Maximum Ratings	10
6. Thermal Characteristics	10
7. Electrical Specifications	11
7.1 Phase Jitter	11
7.2 Output Frequencies, Startup Time and OE Timing	13
7.3 Output Characteristics	13
7.4 Input Clock AC/DC Characteristics	15
7.5 Output-to-Output and Input-to-Output Skew	15
7.6 I/O Electrical Characteristics	15
7.7 Power Supply Current	16
7.8 SMBus Electrical Characteristics	17
8. Test Loads	19
9. Alternate Terminations	19
10. SMBus Addressing	20
11. General SMBus Serial Interface Information	21
11.1 How to Write	21
11.2 How to Read	21
12. Registers	23
13. PCB Layout Recommendations	27
14. Package Outline Drawings	27
15. Ordering Information	28
16. Revision History	29

1. Pin Information



Note: Pins with ^ prefix have internal 120kOhm pull-up
 Pins with v prefix have internal 120kOhm pull-down
 Pins with ^v prefix have internal 120kOhm pull-up/pull-down network biasing input to VDD/2

Figure 2. 9QXL2002B Pin Assignments

Table 1. 9QXL2002B Pin Descriptions

Pin #	Pin Name	Pin Type	Description
A 1	DIF17	O	Differential true clock output.
A 2	DIF16#	O	Differential complimentary clock output.
A 3	DIF16	O	Differential true clock output.
A 4	DIF15#	O	Differential complimentary clock output.
A 5	DIF15	O	Differential true clock output.
A 6	DIF14#	O	Differential complimentary clock output.
A 7	DIF14	O	Differential true clock output.
A 8	DIF13#	O	Differential complimentary clock output.
A 9	DIF13	O	Differential true clock output.
A 10	DIF12#	O	Differential complimentary clock output.

Table 1. 9QXL2002B Pin Descriptions

Pin #		Pin Name	Pin Type	Description
A	11	DIF12	O	Differential true clock output.
A	12	DIF11#	O	Differential complimentary clock output.
B	1	DIF17#	O	Differential complimentary clock output.
B	2	VDDO3.3	PWR	Power supply for outputs. Nominally 3.3V
B	3	NC	NC	No connection.
B	4	$\wedge$ vSADR0_tri	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to $V_{DD}/2$. See the SMBus Address Selection table.
B	5	NC	NC	No connection.
B	6	VDDA3.3	PWR	3.3V power for the PLL core.
B	7	NC	NC	No connection.
B	8	$\wedge$ vSADR1_tri	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to $V_{DD}/2$. See the SMBus Address Selection table.
B	9	NC	NC	No connection.
B	10	vOE12#	I, SE, PD, PU	Active low input for enabling output 12. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
B	11	VDDO3.3	PWR	Power supply for outputs. Nominally 3.3V.
B	12	DIF11	O	Differential true clock output.
C	1	DIF18	O	Differential true clock output.
C	2	NC	NC	No connection.
C	11	vOE11#	I, SE, PD, PU	Active low input for enabling output 11. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
C	12	DIF10#	O	Differential complementary clock output.
D	1	DIF18#	O	Differential complementary clock output.
D	2	NC	NC	No connection.
D	11	NC	NC	No connection.
D	12	DIF10	O	Differential true clock output.
E	1	DIF19	O	Differential true clock output.
E	2	vSBEN	I	Input that enables the Side-Band Interface for controlling output enables. This pin disables the output enable pins when asserted. It has an internal pull-down resistor. 0 = OE pins and SMBus enable bits control outputs, Side-band interface disabled. 1 = Side-Band Interface controls output enables, OE pins and SMBus enable bits are disabled.
E	11	vOE10#SHFT_LD#	I, SE, PD, PU, PDT	Active low input for enabling output 10 or SHFT_LD# pin for the Side-Band Interface. Refer to the Side-Band Interface section for details. This pin has an internal pull-down. OE mode: 1 = disable output, 0 = enable output. Side-Band Mode: 1 = enable Side-Band Interface shift register, 0 = disable Side-Band Interface shift register. A falling edge transfers Side-Band shift register contents to output register.
E	12	vOE9#	I, SE, PD, PDT	Active low input for enabling output 9. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
F	1	DIF19#	O	Differential complementary clock output.
F	2	NC	NC	No connection.
F	11	NC	NC	No connection.
F	12	DIF9#	O	Differential complementary clock output.
G	1	DIF_IN	O	HCSL true input.
G	2	NC	NC	No connection.

Table 1. 9QXL2002B Pin Descriptions

Pin #		Pin Name	Pin Type	Description
G	11	NC	NC	No connection.
G	12	DIF9	O	Differential true clock output.
H	1	DIF_IN#	I, DIF, PDT	HCSL complementary input.
H	2	VDDR3.3	PWR	Power supply for differential input clock (receiver). This V_{DD} should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
H	11	vOE8#	I, SE, PD, PDT	Active low input for enabling output 8. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
H	12	DIF8#	O	Differential complementary clock output.
J	1	DIF0	O	Differential true clock output.
J	2	NC	NC	No connection.
J	11	NC	NC	No connection.
J	12	DIF8	O	Differential true clock output.
K	1	DIF0#	O	Differential complementary clock output.
K	2	NC	NC	No connection.
K	11	vOE7#	I, SE, PD, PDT	Active low input for enabling output 7. This pin has an internal pull-down. 1 = disable output, 0 = enable output.
K	12	DIF7#	O	Differential complementary clock output.
L	1	DIF1	O	Differential true clock output.
L	2	VDDO3.3	PWR	Power supply for outputs. Nominally 3.3V.
L	3	NC	NC	No connection.
L	4	SMBDAT	I/O, SE, OD, PDT	Data pin of SMBUS circuitry.
L	5	SMBCLK	I, SE, PDT	Clock pin of SMBUS circuitry.
L	6	NC	NC	No connection.
L	7	NC	NC	No connection.
L	8	vOE5#/DATA	I, SE, PD, PU, PDT	Active low input for enabling output 5 or the data pin for the Side-Band Interface. Refer to the Side-Band Interface section for details. This pin has an internal pull-down. OE mode: 1 = disable output, 0 = enable output. Side-Band mode: Data pin.
L	9	NC	NC	No connection.
L	10	vOE6#/CLK	I, SE, PD, PU, PDT	Active low input for enabling output 6 or the clock pin for the Side-Band Interface shift register. Refer to the Side-Band Interface section for details. This pin has an internal pull-down. OE mode: 1 = disable output, 0 = enable output. Side Band mode: Clocks data into the Side-Band Interface shift register on the rising edge.
L	11	VDDO3.3	PWR	Power supply for outputs. Nominally 3.3V.
L	12	DIF7	O	Differential true clock output.
M	1	DIF1#	O	Differential complementary clock output.
M	2	DIF2	O	Differential true clock output.
M	3	DIF2#	O	Differential complementary clock output.
M	4	DIF3	O	Differential true clock output.
M	5	DIF3#	O	Differential complementary clock output.
M	6	vCKPWRGD_PD#	I, SE, PD, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down mode, subsequent high assertions exit Power Down mode. This pin has internal pull-down resistor.
M	7	DIF4	O	Differential true clock output.

Table 1. 9QXL2002B Pin Descriptions

Pin #	Pin Name	Pin Type	Description
M 8	DIF4#	O	Differential complementary clock output.
M 9	DIF5	O	Differential true clock output.
M 10	DIF5#	O	Differential complementary clock output.
M 11	DIF6	O	Differential true clock output.
M 12	DIF6#	O	Differential complementary clock output.
N/A	EPAD	GND	Connect epad to ground.

1.1 Power Down Tolerant Pins

Pins that are Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the devices and it will power up normally. PDT pins are indicated in the pin descriptions for each device (See Section 1 Pin Information).

1.2 Signal Types

Table 2. Pin Type Definitions

Term	Description
I	Input
O	Output
PU	Pull Up
PD	Pull Down
SE	Single ended
DIF	Differential
GND	Ground
PWR	Power
PDT	Power Down Tolerant
NC	No Connect

2. Output Control

Table 3. Output Control (SBEN = 0)

CKPWRGD_PD#	DIF_IN	Traditional Interface		Side Band Interface		Outputs
		OEx bit Byte[2:0]	OEx# Pin	MASKx Byte[10:8]	Qx	DIFx
0	X	X	X	X	X	Low/Low
1	Running	0	X	X	X	Low/Low
		1	0	X	X	Running
		1	1	X	X	Low/Low
1	Stopped	1	0	X	X	Stopped
		1	1	X	X	Low/Low

Table 4. Output Control (SBEN = 1)

		Traditional Interface		Side Band Interface		Outputs
CKPWRGD_PD#	DIF_IN	OEx bit Byte[2:0]	OEx# Pin	MASKx Byte[10:8]	Qx	DIFx
0	X	X	X	X	X	Low/Low
1	Running	X	X	0	0	Low/Low
		X	X	0	1	Running
		X	X	1	X	Running
1	Stopped	X	X	0	0	Low/Low
		X	X	0	1	Stopped

3. Power Management

Table 5. Power Connections

Pin Number		Description
VDD	VND	
B6, H2	EPAD	Analog
B2, B11, L2, L11	EPAD	Outputs

4. Output Enable Control

4.1 Traditional Method

The 20-output 9QXL2002B has two methods for enabling and disabling outputs. The first is the traditional method of OE# pins and SMBus output enable bits. Outputs 5 through 12 have dedicated output enable pins and each of the 20 outputs have dedicated SMBus output enable bits in Bytes[0:2] of the SMBus register set.

4.2 Side-Band Interface

The second method is a simple 3-wire serial interface referred to as the Side-Band Interface (SBI). This interface consists of DATA, CLK and SHFT_LD# pins. When the SHFT_LD# pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT_LD# clocks the shift register contents to the Output register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable of outputs, regardless of the method used.

Both interfaces are not active at the same time, and the SBEN pin selects which interface is active. Tying the SBEN high enables the SBI. Tying the SBEN pin low enables the traditional OE# pin/SMBus output enable interface. When the SBI is enabled, OE[7:9, 11,12]# are disabled and DATA, CLK and SHFT_LD# are enabled on OE5#, OE6# and OE10# respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active. When set to a one, the mask register forces its respective output to 'enabled'. This prevents accidentally disabling critical outputs when using the SBI.

An SMBus read back bit in Byte 4 indicates which output enable control interface is enabled.

When the SBI is enabled, and power has been applied, the SBI is active, even if the CKPWRGD_PD# pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output register before the assertion of CKPWRGD. Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the CKPWRGD_PD# is low. Figure 1 provides a functional description of the SBI.

The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The mask registers default to zero at power-up, allowing the shift register bits to disable their respective output. See [Figure 3](#).

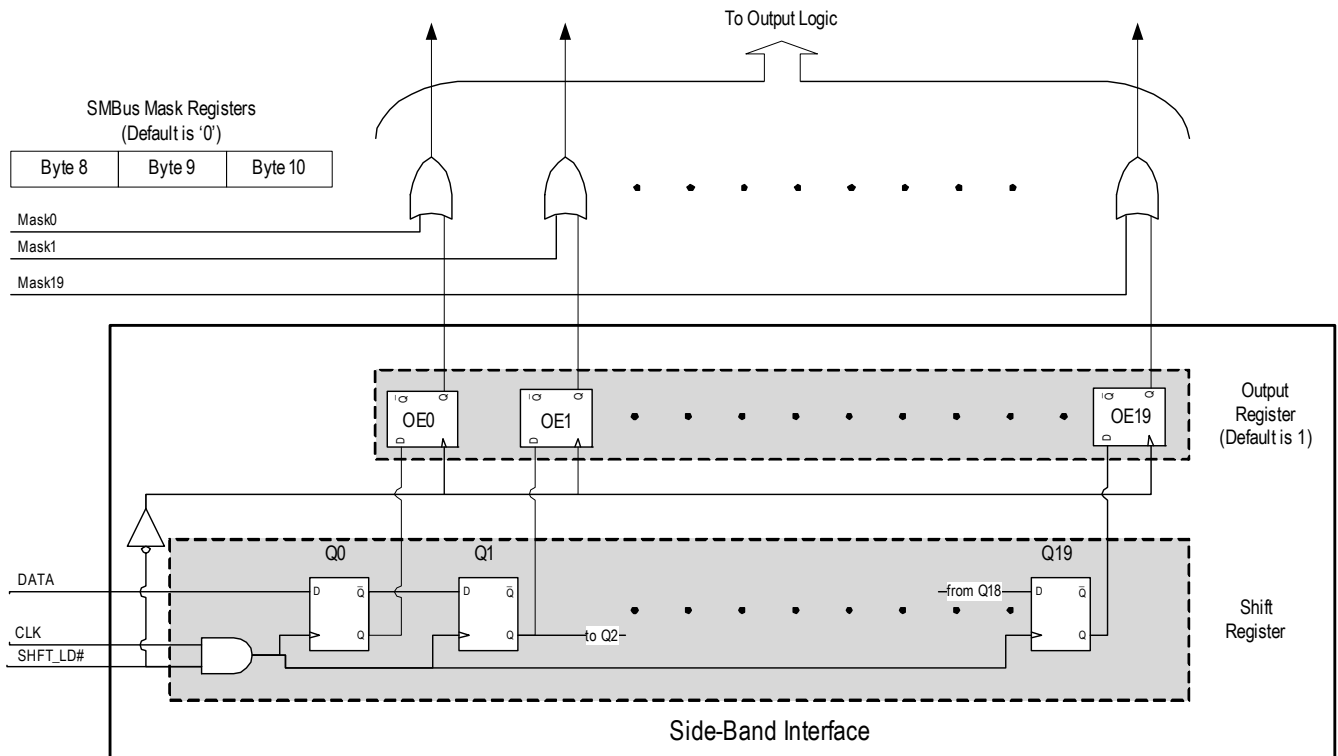


Figure 3. Side Band Interface Control Logic - Functional Description

[Figure 4](#) shows the basic timing of the side-band interface. The SHFT_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable DATA into the shift register. After the 20th clock, stop the clock low and drive the SHFT_LD# pin low. The falling edge of SHFT_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

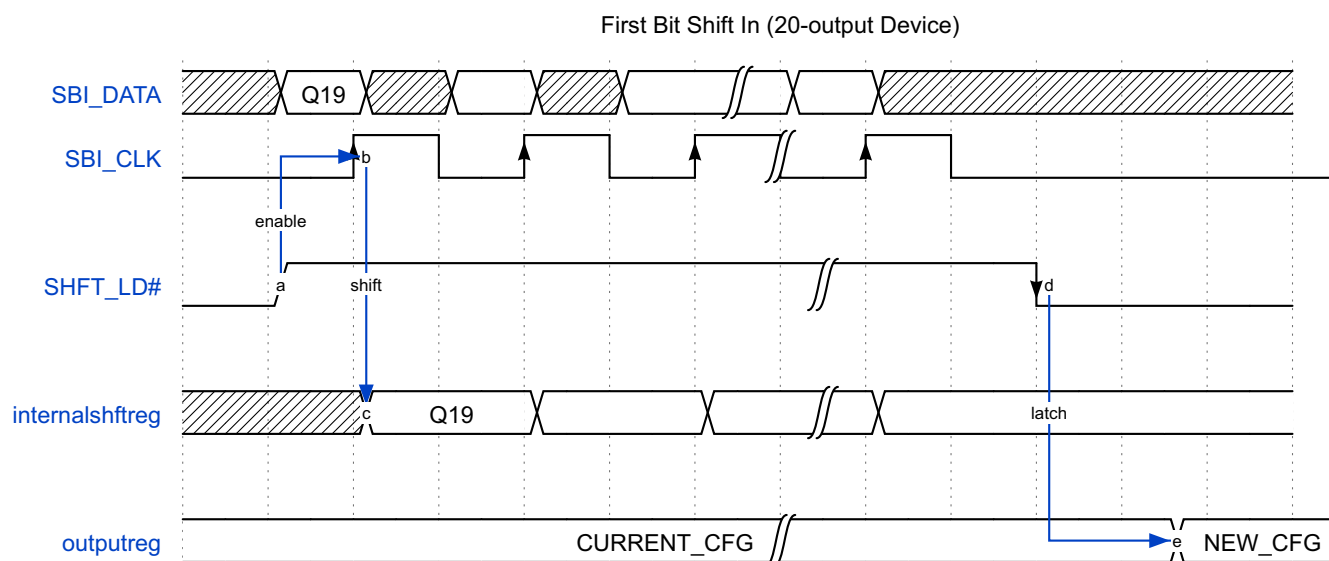


Figure 4. Side Band Interface Functional Timing

The SBI interface supports clock rates up to 25MHz. Multiple devices may share CLK and DATA pins. Dedicating a SHFT_LD# pin to each device allows its use as a chip-select pin. When the SHFT_LD# pin is low, the 9QXL2002B ignores any activity on the SBI_CLK and SBI_DATA pins.

4.3 Automatic Clock Parking

Automatic Clock Parking brings the outputs to a Low/Low state if the input signal is lost. Figure 5 shows the output clock behavior when the input signal is lost. For exact timing see [Electrical Specifications](#).

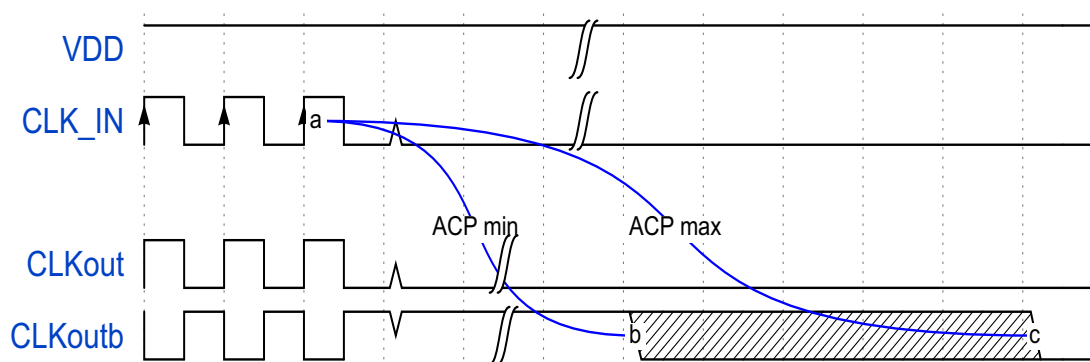


Figure 5. ACP Timing

5. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the 9QXL2002B at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin	-0.5	3.9	V
V_{IN}	Input Voltage for non-PDT inputs	Input pins not labeled as PDT [1]	-0.5	3.6	V
V_{INPDT}	Input Voltage for PDT inputs	PDT input pins, see below for LOSb output pin [2]			V
V_{PUPSMB}	Pull up resistor voltage for SMBus interface	SCLK, SDATA pins			
I_{IN}	Input Current	All SE inputs and CLKIN [1]	-	±50	mA
I_{OUT}	Output Current – Continuous	CLK	-	30	mA
		SDATA	-	25	mA
	Output Current – Surge	CLK	-	60	mA
		SDATA	-	50	mA
T_S	Storage Temperature	Storage Temperature	-65	150	°C
ESD	Human Body Model	JESD22-A114 (JS-001) Classification	-	2000	V
	Charged Device Model	JESD22-C101 Classification	-	500	V

1. Inputs not designated Power Down Tolerant (PDT) in the pin description tables.

2. Inputs designated Power Down Tolerant (PDT) in the pin description tables.

Table 7. Recommended Operation Conditions

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature	-	-	-	125	°C
T_A	Ambient Operating Temperature	-	-40	25	105	°C
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin, 3.3V ±5% supply.	3.135	3.3	3.465	V
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic).	0.05	-	5	ms

6. Thermal Characteristics

Package [1]	Symbol	Condition	Typical Value (°C/W)
8 × 8 mm 80-VFQFPN (5.1 × 5.1 mm ePad)	θ_{JC}	Junction to Case	44
	θ_{JB}	Junction to Base	2
	θ_{JA0}	Junction to Ambient, still air	33
	θ_{JA1}	Junction to Ambient, 1 m/s air flow	29
	θ_{JA3}	Junction to Ambient, 3 m/s air flow	28
	θ_{JA5}	Junction to Ambient, 5 m/s air flow	27

1. ePad soldered to board.

7. Electrical Specifications

7.1 Phase Jitter

Table 8. Filtered Additive Phase Jitter - Normal Conditions [1][2][3] [4]

Parameter	Paramter	Condition	Min.	Typ.	Max.	Ind. Spec	Unit
$t_{jphPCleG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC = 0 or -0.5%	PCIe Gen1 (2.5 GT/s)	-	687	941	86000	fs pk-pk
$t_{jphPCleG2-CC}$		PCIe Gen2 Hi Band (5 GT/s)	-	78	113	3100	fs RMS
$t_{jphPCleG3-CC}$		PCIe Gen2 Lo Band (5 GT/s)	-	26	34	3000	
$t_{jphPCleG4-CC}$		PCIe Gen3 (8 GT/s)	-	26	34	1000	
$t_{jphPCleG5-CC}$		PCIe Gen4 (16 GT/s) [5]	-	26	34	500	
$t_{jphPCleG6-CC}$		PCIe Gen5 (32 GT/s) [6]	-	10.3	13.3	150	
$t_{jphPCleG7-CC}$		PCIe Gen6 (64 GT/s) [7]	-	6.1	8.0	100	
$t_{jphPCleG7-CC}$		PCIe Gen7 (128 GT/s) [8]	-	4.3	5.5	67	
$t_{jphPCleG2-IR}$	Additive Phase Jitter - PCIe Independent Reference Clocked	PCIe Gen2 (5 GT/s) [9]	-	69	116	N/A	fs RMS
$t_{jphPCleG3-IR}$		PCIe Gen3 (8 GT/s) [9]	-	27	35		
$t_{jphPCleG4-IR}$		PCIe Gen4 (16 GT/s) [9]	-	28	36		
$t_{jphPCleG5-IR}$		PCIe Gen5 (32 GT/s) [9]	-	7.9	10.2		
$t_{jphPCleG6-IR}$		PCIe Gen6 (64 GT/s) [9]	-	5.6	7.2		
$t_{jphPCleG7-IR}$		PCIe Gen7 (128 GT/s) [9]	-	4.0	5.2		
$t_{jphDB2000Qadd}$	Additive Phase Jitter - DB2000Q	100MHz, DB2000Q Filter	-	17	22	80	fs RMS

1. Measured using SMA100B signal source, or equivalent and a phase noise analyzer.
2. The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 7.0, Revision 1.0*. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
3. Jitter measurements are made using a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
4. Differential input swing $\geq 1600\text{mV}$ and input slew rate $\geq 3.5\text{V/ns}$. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
5. 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. The PCI Express Base Specification provides the filters necessary to calculate IR jitter values; it does not provide specification limits, hence the n/a in the Limit column. IR values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the channel simulation specification, which includes an allocation for the jitter added by the channel. Using 32GT/s as an example, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an IR system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.

Table 9. Filtered Additive Phase Jitter - Degraded Conditions [1][2][3] [4]

Parameter	Paramter	Condition	Min.	Typ.	Max.	Ind. Spec	Unit
t _{jphPCleG1-CC}	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC = 0 or -0.5%	PCIe Gen1 (2.5 GT/s)	-	656	1055	86000	fs pk-pk
t _{jphPCleG2-CC}		PCIe Gen2 Hi Band (5 GT/s)	-	88	127	3100	fs RMS
		PCIe Gen2 Lo Band (5 GT/s)	-	33	45	3000	
t _{jphPCleG3-CC}		PCIe Gen3 (8 GT/s)	-	30	43	1000	
t _{jphPCleG4-CC}		PCIe Gen4 (16 GT/s) ^[5]	-	30	43	500	
t _{jphPCleG5-CC}		PCIe Gen5 (32 GT/s) ^[6]	-	11.6	16.6	150	
t _{jphPCleG6-CC}		PCIe Gen6 (64 GT/s) ^[7]	-	7.0	10.0	100	
t _{jphPCleG7-CC}			PCIe Gen7 (128 GT/s) ^[8]	-	4.9	7.0	67
t _{jphPCleG2-IR}	Additive Phase Jitter - PCIe Independent Reference Clocked	PCIe Gen2 (5 GT/s) ^[9]	-	82	116	N/A	fs RMS
t _{jphPCleG3-IR}		PCIe Gen3 (8 GT/s) ^[9]	-	32	45		
t _{jphPCleG4-IR}		PCIe Gen4 (16 GT/s) ^[9]	-	33	47		
t _{jphPCleG5-IR}		PCIe Gen5 (32 GT/s) ^[9]	-	9.1	12.9		
t _{jphPCleG6-IR}		PCIe Gen6 (64 GT/s) ^[9]	-	6.6	9.3		
t _{jphPCleG7-IR}		PCIe Gen7 (128 GT/s) ^[9]	-	4.7	6.6		
t _{jphDB2000Qadd}	Additive Phase Jitter - DB2000Q	100MHz, DB2000Q Filter	-	20	28	80	fs RMS

1. Measured using SMA100B signal source, or equivalent and a phase noise analyzer.
2. The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 7.0, Revision 1.0*. See the [Test Loads](#) section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
3. Jitter measurements are made using a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
4. Differential input swing $\geq 800\text{mV}$ and input slew rate $\geq 1.5\text{V/ns}$. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
5. 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. The PCI Express Base Specification provides the filters necessary to calculate IR jitter values; it does not provide specification limits, hence the n/a in the Limit column. IR values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the channel simulation specification, which includes an allocation for the jitter added by the channel. Using 32GT/s as an example, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an IR system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.

Table 10. Unfiltered Additive Phase Jitter [1] [2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$t_{jph12k-20Madd}$	Additive Phase Jitter - Normal Conditions	100MHz	-	78	110	fs
		156.25MHz	-	62	77	RMS
$t_{jph12k-20Madd}$	Additive Phase Jitter - Degraded	100MHz	-	88	117	fs
		156.25MHz	-	74	93	RMS

1. Measured using SMA100B signal source, or equivalent and a phase noise analyzer.
2. 12kHz - 20MHz brick wall filter.

7.2 Output Frequencies, Startup Time and OE Timing

Table 11. Start-Up Time and OE Timing

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{OP}	Output Frequency		1	-	400	MHz
$t_{STARTUP}$	Start-up Time [1]	[2]	-	210	500	μs
		[3]	-	35	100	μs
$t_{LATOE\#}$	OE# Latency [1][1][4]	DIF start after OE# assertion. DIF stop after OE# deassertion.	4	5	10	clks
t_{DRVPD}	Tdrive_PD# [1][4]	DIF output enable after PD# de-assertion.	-	76	300	μs
t_{ACP_ON}	ACP Latency	Time from disappearance of input clock to DIF stop.		123	200	ns
t_{ACP_OFF}		Time from appearance of input clock to DIF start.		6	9	clks

- Control input must be monotonic from 20% to 80% of input swing.
- Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. PWRGD_PWRDNb tied to VDD in this case.
- VDD stable, measured from de-assertion of PWRGD_PWRDNb.
- Time from deassertion until outputs are > 200mV.

7.3 Output Characteristics

Table 12. 85 Ω CLK AC/DC Characteristics – Source-Terminated 100MHz PCIe Applications[1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Specification Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	884	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-114	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	580	752	831	-	mV
V_{LOW}	Voltage Low [3]		-101	-3	150	-	
V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 800mV, scope averaging off.	325	416	441	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		17	24	40	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, Fast slew rate, scope averaging on.	1.2	2.2	3.2	0.6 to 4	V/ns
		V_{HIGH} set to 800mV, Slow slew rate, scope averaging on.	0.9	1.9	2.9		
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Fast slew rate.	-	5	18	20	%
		V_{HIGH} set to 800mV. Slow slew rate.	-	3	20	20	%
t_{DC}	Output Duty Cycle [9]	$V_T = 0V$ differential.	47.0	49.8	53.0	45 to 55	%

- Standard high impedance load with $C_L = 2pF$. For more information, see [Figure 9](#).
- The specification limits are taken from either the *PCIe Base Specification Revision 7* or from relevant x86 processor specifications, whichever is more stringent.
- Measured from single-ended waveform.
- Defined as the maximum instantaneous voltage including overshoot.

5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a $\pm 75\text{mV}$ window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 13. 85 ohm CLK AC/DC Characteristics – Source-Terminated, Non-PCIe Applications ^[1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage ^[2]	$V_{HIGH} = 800\text{mV}$, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	600	757	880	mV
V_{OL}	Output Low Voltage ^[2]		-126	8	180	
V_{CROSS}	Crossing Voltage (abs) ^[3]		270	390	465	
ΔV_{CROSS}	Crossing Voltage (var) ^{[3][4][5]}		19	24	40	
t_R, t_F	Rise/Fall Time ^[2] $V_T = 20\%$ to 80% of swing		177	450	1100	ps
t_{DC}	Output Duty Cycle ^[6]	Across all settings in this table, $V_T = 0\text{V}$.	45.0	49.4	55.0	%

1. Standard high impedance load with $C_L = 2\text{pF}$. For more information, see [Figure 9](#).
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

7.4 Input Clock AC/DC Characteristics

Table 14. Input Clock AC/DC Parameters

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CROSS}	Input Crossover Voltage [1]	Crossover voltage.	100	-	900	mV
V_{SWING}	Input Swing [1]		200	-	-	mV
dv/dt	Input Slew Rate [1][2]		0.7	-	-	V/ns
d_{in}	Input Duty Cycle	Measurement from differential waveform.	45	-	55	%

1. Differential value.

2. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero-crossing.

7.5 Output-to-Output and Input-to-Output Skew

Table 15. Output-to-Output and Input-to-Output Skew [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-Output Skew [2]	Any two outputs, all outputs at fast slew rate.	-	25	50	ps
		Any two outputs, all outputs at slow slew rate.	-	28	44	ps
t_{PD}	Input-to-Output Delay [3]	Clock in to any output, all outputs at fast slew rate.	1.9	2.6	3.2	ns
		Clock in to any output, all outputs at slow slew rate.	2.0	2.8	3.5	ns
Δt_{PD}	Input-to-Output Delay Variation [3]	A single device, over temperature and voltage.	1.7	-	2.1	ps/°C

1. These parameters are measured with the loads in Figure 10.

2. This parameter is defined in accordance with JEDEC Standard 65.

3. Defined as the time between to output rising edge and the input rising edge that caused it.

7.6 I/O Electrical Characteristics

Table 16. I/O Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage [1][2]	Single-ended inputs, unless otherwise listed.	2	-	$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage [1][2]		GND - 0.3	-	0.8	V
V_{IH}	Input High Voltage	SADR_tri[1:0].	2.2	-	$V_{DD} + 0.3$	V
V_{IM}	Input Mid Voltage		1.2	$V_{DD}/2$	1.8	V
V_{IL}	Input Low Voltage		GND - 0.3	-	0.8	V
I_{IH}	Input Leakage Current High, $V_{IN} = V_{DD}$	DIF_IN	10	-	50	μA
		DIF_IN#				
		vCKPWRGD_PD#				
		SADR_tri[1:0]				
		Single-ended inputs not otherwise listed				
I_{IL}	Input Leakage Current Low, $V_{IN} = 0V$	DIF_IN	-12	-	-6	μA
		DIF_IN#	-3	-	3	
		vCKPWRGD_PD#	-3	-	3	
		SADR_tri[1:0]	-35	-	-20	
		Single-ended inputs not otherwise listed	-3	-	3	

Table 16. I/O Electrical Characteristics (Cont.)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
Rp	PD_DIFIN	Value of internal pull-up resistor to 0.5V (DIFIN)	-	51	-	kΩ
	PU_DIFIN#	Value of internal pull-down resistor to ground (DIFINb).	-	54	-	
	Pull-up/Pull-down Resistor	Single-ended inputs.	-	125	-	
Zo	Output Impedance [3]	DIF/DIF# single-ended impedance, 85Ω setting	37.2	41.5	46.5	Ω
I _{OL}	Output Leakage Current	Outputs Tri-stated. Single Ended Measurement. 3.3V applied to pin.	-10	-	10	-

1. For SCLK and SDATA, see the [SMBus DC Electrical Characteristics](#) table.
2. These values are compliant with JESD8-7A 1.8V Normal Range.
3. Measured at V_{cross_abs}.

7.7 Power Supply Current

Table 17. Power Supply Current [1][2][3]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I _{DD_VDDO}	V _{VDDO} Operating Current per Output Pair, 85Ω impedance [4][5]	Fast slew rate, source-terminated load at 100MHz.	-	9.9	10.7	mA
		Fast slew rate, source-terminated load at maximum output frequency.	-	12.7	13.2	
I _{DD_A/R}	V _{VDDA/R} Core Operating Current, All Outputs Disabled.	CKPWRGD_PD = 1, all outputs disabled, CLKIN = 100MHz.	-	1.5	2	mA
		CKPWRGD_PD = 1, all outputs disabled, CLKIN = 400MHz.	-	1.7	3	
I _{DD_VDDO_PD}	V _{VDDO} Power-down Current	CKPWRGD_PD = 0	-	1.0	5	mA
I _{DD_A/R_PD}	V _{VDDA/R} Power-down Current	CKPWRGD_PD = 0	-	1.4	2	mA
I _{DD_R}	Input Low/Low Current	Input driven Low/Low	-	0.2	0.3	mA

1. For more information, see [Test Loads](#).
2. Slew rate has negligible effect on current consumption, so only fast is listed.
3. Total operating current is obtained by adding (I_{DD_VDDO} × number of outputs used) + I_{DD_A/R}. Power down current is obtained by adding I_{DD_VDDO_PD} + I_{DD_A/R_PD}. For example let's assume that the 9QXL2002B is being used at 100MHz and that only 6 outputs are used. The operating current would be I_{DD_VDDO} × 6 + I_{DD_A/R}.
4. The value specified is for one output pair. Multiply this value by the number of outputs in use.
5. The value I_{DD_VDDO} per output, is the calculated by total I_{DD_VDDO} of all outputs running divided by 20

7.8 SMBus Electrical Characteristics

Table 18. SMBus DC Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	High-level Input Voltage for SMBCLK and SMBDAT	$V_{DD} = 1.8V$	$0.8 V_{DD}$	-	3.4	V
V_{IL}	Low-level Input Voltage for SMBCLK and SMBDAT	$V_{DD} = 1.8V$	-	-	$0.3 V_{DD}$	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	-	$0.05 V_{DD}$	-	-	
V_{OL}	Low-level Output Voltage for SMBCLK and SMBDAT	$I_{OL} = 4mA$	-	0.21	0.4	
I_{IN}	Input Leakage Current per Pin	-	[2]	-	[2]	μA
C_B	Capacitive Load for Each Bus Line	-	-	-	400	pF

1. V_{OH} is governed by the V_{PUP} , the voltage rail to which the pull-up resistors are connected. The maximum V_{PUP} voltage is 3.6V.

2. See [I/O Electrical Characteristics](#).

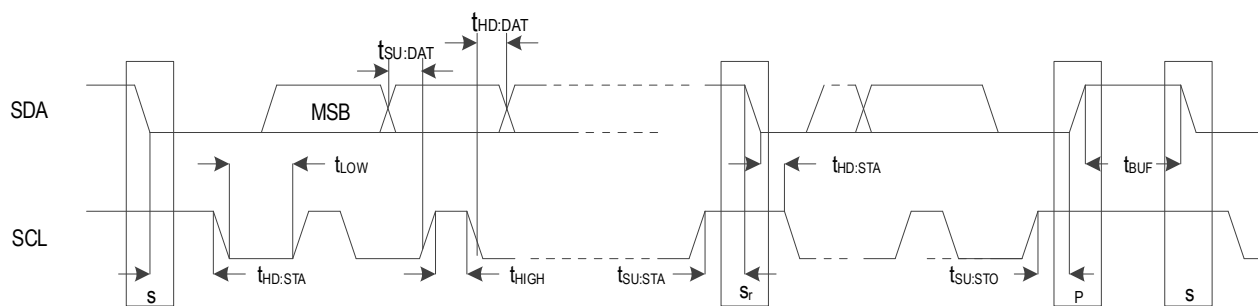


Figure 6. SMBus Target Timing Diagram

Table 19. SMBus AC Electrical Characteristics

Symbol	Parameter	Condition	100kHz Class		400kHz Class		Unit
			Minimum	Maximum	Minimum	Maximum	
f_{SMB}	SMBus Operating Frequency	[1]	10	100	10	400	kHz
t_{BUF}	Bus free time between STOP and START Condition	-	4.7	-	1.3	-	μs
$t_{HD:STA}$	Hold Time after (REPEATED) START Condition	[2]	4	-	0.6	-	μs
$t_{SU:STA}$	REPEATED START Condition Setup Time	-	4.7	-	0.6	-	μs
$t_{SU:STO}$	STOP Condition Setup Time	-	4	-	0.6	-	μs
$t_{HD:DAT}$	Data Hold Time	[3]	300	-	300	-	ns
$t_{SU:DAT}$	Data Setup Time	-	250	-	100	-	ns
$t_{TIMEOUT}$	Detect SCL_SCLK Low Timeout	[4]	25	35	25	35	ms
$t_{TIMEOUT}$	Detect SDA_nCS Low Timeout	[5]	25	35	25	35	ms
t_{LOW}	Clock Low Period	-	4.7	-	1.3	-	μs
t_{HIGH}	Clock High Period	[6]	4	50	0.6	-	μs
$t_{LOW:SEXT}$	Cumulative Clock Low Extend Time - Target (Slave)	[7]	N/A		N/A		ms
$t_{LOW:MEXT}$	Cumulative Clock Low Extend Time - Host (Master)	[8]	N/A		N/A		ms
t_F	Clock/Data Fall Time	[9]	-	300	-	300	ns
t_R	Clock/Data Rise Time	[9]	-	1000	-	300	ns
t_{SPIKE}	Noise Spike Suppression Time	[10]	-	-	0	50	ns

1. Power must be applied and CKPWRGD_PD must be a 1 for the SMBus to be active.

2. A host (master) should not drive the clock at a frequency below the minimum f_{SMB} . Further, the operating clock frequency should not be reduced below the minimum value of f_{SMB} due to periodic clock extending by target devices as defined in Section 5.3.3 of System Management Bus (SMBus) Specification, Version 3.2, dated 12 Jan, 2022. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW:SEXT}$ and $t_{LOW:MEXT}$ limits. For example, if the SMBCLK is high for $t_{HIGH,MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB,MIN} - t_{HIGH,MAX}$. This requirement does not pertain to a device that extends the SMBCLK low for data processing of a received byte, data buffering and so forth for longer than 100 μs in a non-periodic way.
3. A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the $V_{IH,MIN}$ of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
4. Target devices may have caused other target devices to hold SDA low. This is the maximum time that a device can hold SMBDAT low after the host raises SMBCLK after the last bit of a transaction. A target device may detect how long SDA is held low and release SDA after the time out period.
5. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the host in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can host the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT,MAX}$ or longer.
6. The device has the option of detecting a timeout if the SMBDATA pin is also low for this time.
7. $t_{HIGH,MAX}$ provides a simple guaranteed method for hosts to detect bus idle conditions. A host can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH,MAX}$.
8. $t_{LOW:MEXT}$ is the cumulative time a host device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a target device or another host will also extend the clock causing the combined clock low time to be greater than $t_{LOW:MEXT}$ on a given byte. This parameter is measured with a full-speed target device as the sole target of the host.
9. The rise and fall time measurement limits are defined as follows:
 Rise Time Limits: ($V_{IL,MAX} - 0.15 V$) to ($V_{IH,MIN} + 0.15 V$)
 Fall Time Limits: ($V_{IH,MIN} + 0.15 V$) to ($V_{IL,MAX} - 0.15 V$)
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

8. Test Loads

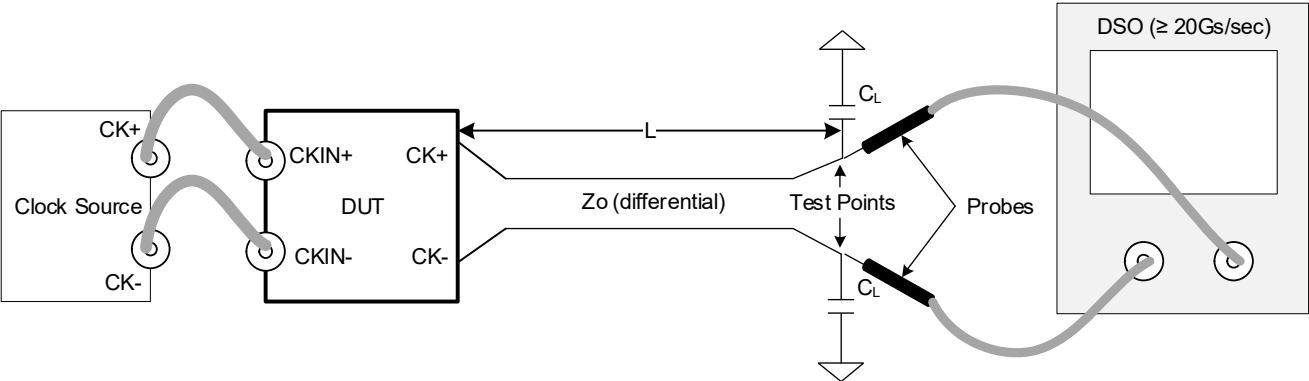


Figure 7. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)

Table 20. Parameters for AC/DC Test Load (Standard PCIe Source-Terminated)

Device	Clock Source	Zo (ohms)	Rs (ohms)	L (cm)	CL (pF)
All	SMA100B	85	Internal	25.4	2

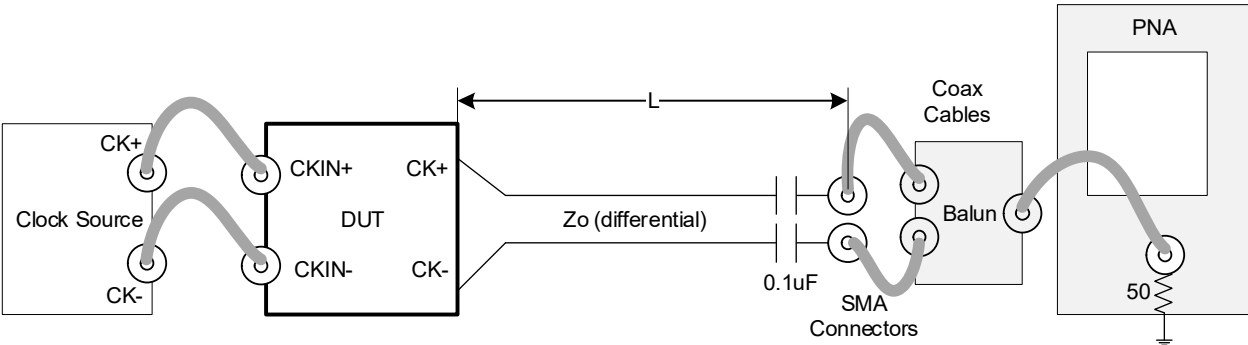


Figure 8. Test Load for PCIe Phase Jitter Measurements

Table 21. Parameters for PCIe Jitter Measurement

Device	Clock Source	Zo (ohms)	Rs (ohms)	L (cm) [1]	CL (pF)
All	SMA100B	85	Internal	25.4	2

1. PCIe Base Specification 7.0 specifies L = 0cm for 32, 64 and 128GT/s jitter measurements. L = 25.4cm is more conservative.

9. Alternate Terminations

The LP-HCSL output can easily drive other logic families. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with “Universal” Low-Power HCSL Outputs”](#) for termination schemes for LVPECL, LVDS, CML and SSTL.

10. SMBus Addressing

Table 22. SMBus Addressing

SADR(1:0)_tri	SMBus Address (Read/Write bit = 0)
00	D8
0M	DA
01	DE
M0	C2
MM	C4
M1	C6
10	CA
1M	CC
11	CE

11. General SMBus Serial Interface Information

11.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending **Byte N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

Table 23. Index Block Write Operation

Controller (Host)			Renesas (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

11.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**

- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte 0 through Byte X (if X(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Table 24. Index Block Read Operation

Controller (Host)			Renesas (Slave/Receiver)
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat		
Slave Address			
RD	ReaD		
			ACK
		Data Byte Count=X	
ACK			
		X Byte	Beginning Byte N
ACK			
			0
0			0
0			0
0			
			Byte N + X - 1
N	Not		
P	stoP bit		

12. Registers

Table 25. 9QXL2002B SMBus Registers

Byte	Register	Name	Bit	Type	Default	Description	Definition
0	OUTPUT_ENABLE_2	RESERVED	[7]	RW	0	RESERVED	0 = output is disabled (low/low) 1 = output is enabled
		DIF19_EN	[6]	RW	1	Output Enable for DIF19	
		DIF18_EN	[5]	RW	1	Output Enable for DIF18	
		DIF17_EN	[4]	RW	1	Output Enable for DIF17	
		DIF16_EN	[3]	RW	1	Output Enable for DIF16	
		RESERVED	[2:0]	RW	0	RESERVED	
1	OUTPUT_ENABLE_0	DIF7_EN	[7]	RW	1	Output Enable for DIF7	0 = output is disabled (low/low) 1 = output is enabled
		DIF6_EN	[6]	RW	1	Output Enable for DIF6	
		DIF5_EN	[5]	RW	1	Output Enable for DIF5	
		DIF4_EN	[4]	RW	1	Output Enable for DIF4	
		DIF3_EN	[3]	RW	1	Output Enable for DIF3	
		DIF2_EN	[2]	RW	1	Output Enable for DIF2	
		DIF1_EN	[1]	RW	1	Output Enable for DIF1	
		DIF0_EN	[0]	RW	1	Output Enable for DIF0	
2	OUTPUT_ENABLE_1	DIF15_EN	[7]	RW	1	Output Enable for DIF15	0 = output is disabled (low/low) 1 = output is enabled
		DIF14_EN	[6]	RW	1	Output Enable for DIF14	
		DIF13_EN	[5]	RW	1	Output Enable for DIF13	
		DIF12_EN	[4]	RW	1	Output Enable for DIF12	
		DIF11_EN	[3]	RW	1	Output Enable for DIF11	
		DIF10_EN	[2]	RW	1	Output Enable for DIF10	
		DIF9_EN	[1]	RW	1	Output Enable for DIF9	
		DIF8_EN	[0]	RW	1	Output Enable for DIF8	
3	OE_B_PIN_READBACK	RB_OEb_12	[7]	RO	1'bX	Status of OEb12	0 = pin low 1 = pin high
		RB_OEb_11	[6]	RO	1'bX	Status of OEb11	
		RB_OEb_10 ^[1]	[5]	RO	1'bX	Status of OEb10	
		RB_OEb_9	[4]	RO	1'bX	Status of OEb9	
		RB_OEb_8	[3]	RO	1'bX	Status of OEb8	
		RB_OEb_7	[2]	RO	1'bX	Status of OEb7	
		RB_OEb_6 ^[1]	[1]	RO	1'bX	Status of OEb6	
		RB_OEb_5 ^[1]	[0]	RO	1'bX	Status of OEb5	
4	SBI_EN_RDBK	RESERVED	[7:1]	RW	0x0	RESERVED	-
		RB_SBI_ENQ	[0]	RO	1'bX	Status of SBI_EN	0 = pin low 1 = pin high
5	VENDOR_REVISION_ID	RID	[7:4]	RO	0x3	REVISION ID	-
		VID	[3:0]	RO	0x1	VENDOR ID, ICS/IDT/Renesas	-
6	DEVICE_ID	DEVICE_ID	[7:0]	RO	0xC9	Device ID	-
7	READ_BYTE_COUNT	RESERVED	[7:5]	RW	0x0	RESERVED	-
		BC	[4:0]	RW	0x8	Writing to this register configures how many bytes will be read back.	-

Table 25. 9QXL2002B SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
8	SBI_MASK_0 [2]	MASK7	[7]	RW	0	Masks off Side-band Disable for DIF7	0 = Side-band shift register may disable the output 1 = Side-band shift register may not disable the output
		MASK6	[6]	RW	0	Masks off Side-band Disable for DIF6	
		MASK5	[5]	RW	0	Masks off Side-band Disable for DIF5	
		MASK4	[4]	RW	0	Masks off Side-band Disable for DIF4	
		MASK3	[3]	RW	0	Masks off Side-band Disable for DIF3	
		MASK2	[2]	RW	0	Masks off Side-band Disable for DIF2	
		MASK1	[1]	RW	0	Masks off Side-band Disable for DIF1	
		MASK0	[0]	RW	0	Masks off Side-band Disable for DIF0	
9	SBI_MASK_1 [2]	MASK15	[7]	RW	0	Masks off Side-band Disable for DIF15	0 = Side-band shift register may disable the output 1 = Side-band shift register may not disable the output
		MASK14	[6]	RW	0	Masks off Side-band Disable for DIF14	
		MASK13	[5]	RW	0	Masks off Side-band Disable for DIF13	
		MASK12	[4]	RW	0	Masks off Side-band Disable for DIF12	
		MASK11	[3]	RW	0	Masks off Side-band Disable for DIF11	
		MASK10	[2]	RW	0	Masks off Side-band Disable for DIF10	
		MASK9	[1]	RW	0	Masks off Side-band Disable for DIF9	
		MASK8	[0]	RW	0	Masks off Side-band Disable for DIF8	
10	SBI_MASK_2 [2]	RESERVED	[7:4]	RW	0	RESERVED	-
		MASK19	[3]	RW	0	Masks off Side-band Disable for DIF19	0 = Side-band shift register may disable the output 1 = Side-band shift register may not disable the output
		MASK18	[2]	RW	0	Masks off Side-band Disable for DIF18	
		MASK17	[1]	RW	0	Masks off Side-band Disable for DIF17	
		MASK16	[0]	RW	0	Masks off Side-band Disable for DIF16	

Table 25. 9QXL2002B SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
11	SLEW_RATE_7_0	DIF7_SLEWRATE	[7]	RW	1	DIF7 Slewrate Control	0 = low slew rate 1 = high slew rate
		DIF6_SLEWRATE	[6]	RW	1	DIF6 Slewrate Control	
		DIF5_SLEWRATE	[5]	RW	1	DIF5 Slewrate Control	
		DIF4_SLEWRATE	[4]	RW	1	DIF4 Slewrate Control	
		DIF3_SLEWRATE	[3]	RW	1	DIF3 Slewrate Control	
		DIF2_SLEWRATE	[2]	RW	1	DIF2 Slewrate Control	
		DIF1_SLEWRATE	[1]	RW	1	DIF1 Slewrate Control	
		DIF0_SLEWRATE	[0]	RW	1	DIF0 Slewrate Control	
12	SLEW_RATE_15_8	DIF15_SLEWRATE	[7]	RW	1	DIF15 Slewrate Control	0 = low slew rate 1 = high slew rate
		DIF14_SLEWRATE	[6]	RW	1	DIF14 Slewrate Control	
		DIF13_SLEWRATE	[5]	RW	1	DIF13 Slewrate Control	
		DIF12_SLEWRATE	[4]	RW	1	DIF12 Slewrate Control	
		DIF11_SLEWRATE	[3]	RW	1	DIF11 Slewrate Control	
		DIF10_SLEWRATE	[2]	RW	1	DIF10 Slewrate Control	
		DIF9_SLEWRATE	[1]	RW	1	DIF9 Slewrate Control	
		DIF8_SLEWRATE	[0]	RW	1	DIF8 Slewrate Control	
13	SLEW_RATE_23_16	RESERVED	[7:4]	RW	0x0	RESERVED	0 = low slew rate 1 = high slew rate
		DIF19_SLEWRATE	[3]	RW	1	DIF19 Slewrate Control	
		DIF18_SLEWRATE	[2]	RW	1	DIF18 Slewrate Control	
		DIF17_SLEWRATE	[1]	RW	1	DIF17 Slewrate Control	
		DIF16_SLEWRATE	[0]	RW	1	DIF16 Slewrate Control	
14 - 19	RESERVED	-	-	-	-	RESERVED	-
20	OUTPUT_AMP_CTRL	AMP	[7:5]	RW	0x5	Global Differential output Control (signed-ended value) 0.55V~0.9V 50mV/step Default = 0.8V	000 = 550mV 001 = 600mV 010 = 650mV 011 = 700mV 100 = 750mV 101 = 800mV 110 = 850mV 111 = 900mV
		RESERVED	[4:0]	RW	0x7	RESERVED	-
21	PD_RESTORE_LOSb_R DBK	RESERVED	[7:4]	RO	0x4	RESERVED	-
		PD_RESTORE_B	[3]	RW	1	Save Configuration in Power Down	0 = Config Cleared 1 = Config Saved
		RESERVED	[2:1]	RW	0x0	RESERVED	-
		LOSb_RB	[0]	RO	1'bX	real time read back of loss detect block output	0 = LOS event detected 1 = NO LOS event detected.
22-32	RESERVED	-	-	-	-	RESERVED	-

Table 25. 9QXL2002B SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
33	SBI_READBACK_0 [2]	SBI_CK7	[7]	RO	1'bX	Readback of Side-band Disable for DIF7	0 = bit low 1 = bit high
		SBI_CK6	[6]	RO	1'bX	Readback of Side-band Disable for DIF6	
		SBI_CK5	[5]	RO	1'bX	Readback of Side-band Disable for DIF5	
		SBI_CK4	[4]	RO	1'bX	Readback of Side-band Disable for DIF4	
		SBI_CK3	[3]	RO	1'bX	Readback of Side-band Disable for DIF3	
		SBI_CK2	[2]	RO	1'bX	Readback of Side-band Disable for DIF2	
		SBI_CK1	[1]	RO	1'bX	Readback of Side-band Disable for DIF1	
		SBI_CK0	[0]	RO	1'bX	Readback of Side-band Disable for DIF0	
34	SBI_READBACK_1 [2]	SBI_CK15	[7]	RO	1'bX	Readback of Side-band Disable for DIF15	0 = bit low 1 = bit high
		SBI_CK14	[6]	RO	1'bX	Readback of Side-band Disable for DIF14	
		SBI_CK13	[5]	RO	1'bX	Readback of Side-band Disable for DIF13	
		SBI_CK12	[4]	RO	1'bX	Readback of Side-band Disable for DIF12	
		SBI_CK11	[3]	RO	1'bX	Readback of Side-band Disable for DIF11	
		SBI_CK10	[2]	RO	1'bX	Readback of Side-band Disable for DIF10	
		SBI_CK9	[1]	RO	1'bX	Readback of Side-band Disable for DIF9	
		SBI_CK8	[0]	RO	1'bX	Readback of Side-band Disable for DIF8	
35	SBI_READBACK_2 [2]	RESERVED	[7:4]	RO	1'bXXX	RESERVED	0 = bit low 1 = bit high
		SBI_CK19	[3]	RO	1'bX	Readback of Side-band Disable for DIF19	
		SBI_CK18	[2]	RO	1'bX	Readback of Side-band Disable for DIF18	
		SBI_CK17	[1]	RO	1'bX	Readback of Side-band Disable for DIF17	
		SBI_CK16	[0]	RO	1'bX	Readback of Side-band Disable for DIF16	
36-37	RESERVED	RESERVED	[7:0]	RW	0xXX	RESERVED	RESERVED

Table 25. 9QXL2002B SMBus Registers (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
38	WRITE_LOCK	RESERVED	[7:1]	RW	0x0	RESERVED	-
		WRITE_LOCK	[0]	RW	0	Non-clearable SMBus Write Lock bit. When written to one, the SMBus registers can only be read, not written. This bit can be cleared in two ways: by cycling power or by setting the PD_RESTORE_B to 1 prior to setting WRITE_LOCK to 1 and then toggling the PWRGD_PDb pin to 0 and then 1.	0 = SMBus not locked for writing 1 = SMBus locked for writing
39	RESERVED	RESERVED	[7:0]	RO	0x0	RESERVED	RESERVED

1. Register is only valid when the Side-Band Interface is not enabled (SBI_ENQ = 0).
2. Register only valid when the Side-Band Interface is enabled (SBI_ENQ = 1).

13. PCB Layout Recommendations

Proper PCB layout is critical to achieving the full functionality and efficiency of the device. For more information pertaining to optimal electrical performance, effective thermal management, and overall system reliability, see [layout recommendations](#).

14. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see [Ordering Information](#) for POD links). The package information is the most current data available and is subject to change without revision of this document.

15. Ordering Information

IDT9QXL2
002BNHGI
#YYWW\$

● LOT

- Lines 1 and 2: part number
 - “I” denotes industrial temperature
- Line 3:
 - “#” denotes the stepping number.
 - “YYWW” is the last digits of the year and work week that the part was assembled.
 - “\$” denotes mark code.
- “LOT” denotes the lots sequence code.

Table 26. Ordering information

Part Number	Package	Carrier Type	Operating Temperature
9QXL2002BNHKGK	6 × 6 mm, 0.5mm pitch 80-GQFN	Tray	-40° to +105°C
9QXL2002BNHKGK8	6 × 6 mm, 0.5mm pitch 80-GQFN	Tape and Reel, Pin 1 Orientation: EIA-481-C (see Table 27)	-40° to +105°C
9QXL2002BNHKGK8/W	6 × 6 mm, 0.5mm pitch 80-GQFN	Tape and Reel, Pin 1 Orientation: EIA-481-D (see Table 27)	-40° to +105°C

Table 27. Pin 1 Orientation

Part Number Suffix	Pin 1 Orientation	Illustration
8	Quadrant 1 (EIA-481-C)	
/W	Quadrant 2 (EIA-481-D)	

16. Revision History

Revision	Date	Description
1.01	Jun 8, 2026	▪ Updated Table 26. ▪ Added Table 27.
1.00	May 29, 2026	Initial Release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.