

# 9QXL2001C

20-Output Enhanced DB2000QL

## Description

The 9QXL2001C is an enhanced-performance 9QXL2001B with ultra-low-additive phase jitter for PCIe Gen5, Gen6, Gen7 and UPI applications. The 9QXL2001C also reduces propagation delay by approximately 50% with respect to the 9QXL2001B.

## PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) – SRNS, SRIS

## Applications

- Servers, Storage, Networking, Accelerators

## Key Specifications

- Output-to-output skew: < 50ps
- PCIe Gen5 additive phase jitter: 6.6fs RMS
- PCIe Gen6 additive phase jitter: 3.9fs RMS
- PCIe Gen7 additive phase jitter: 2.8fs RMS
- DB2000Q additive phase jitter: 10fs RMS
- 12kHz–20MHz additive jitter: 23fs RMS at 156.25MHz
- Propagation delay: 1.4ns typical

## Features

- 8 OE# pins provide hardware control of 8 outputs
- SMBus allows software control of each output
- 25MHz Side-Band Interface allows real-time control of all 20 outputs
- Outputs remain Low/Low when powered up with floating input clock
- Power Down Tolerant (PDT) inputs
- 85Ω Low-Power HCSL (LP-HCSL) outputs:
  - Eliminate 80 resistors, saving 130mm<sup>2</sup> of area
  - Power consumption reduced by 50%
- 9 selectable SMBus addresses
- Spread spectrum compatible
- 6.00 × 6.00 mm dual-row 80-VFQFPN
- 40° to +105°C, 3.3V ±10% operation

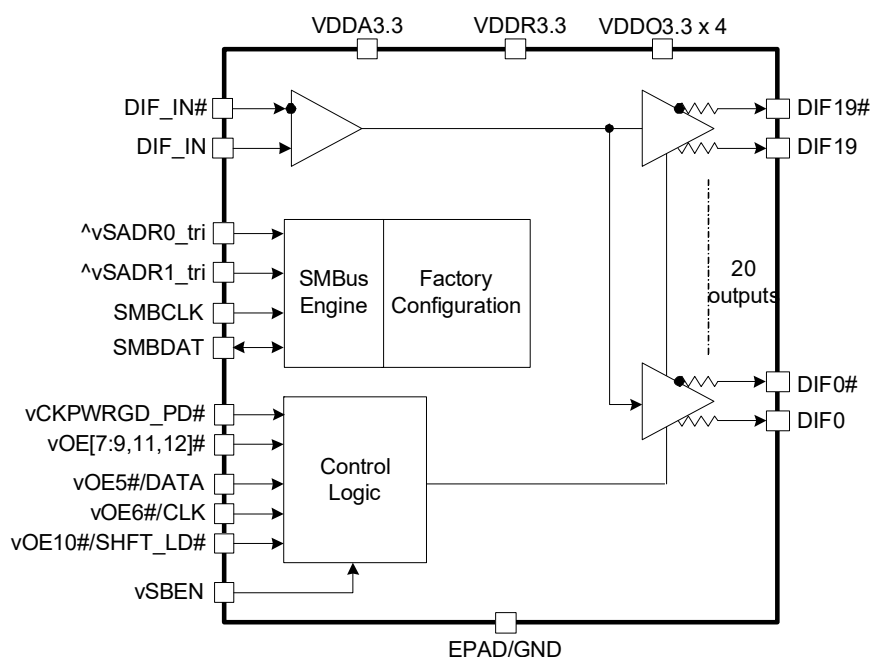


Figure 1. Block Diagram

## Contents

|                                                         |           |
|---------------------------------------------------------|-----------|
| <b>1. Pin Information</b>                               | <b>3</b>  |
| 1.1 Signal Types                                        | 3         |
| 1.2 Pin Assignments                                     | 4         |
| 1.3 Pin Descriptions                                    | 4         |
| <b>2. Specifications</b>                                | <b>8</b>  |
| 2.1 Absolute Maximum Ratings                            | 8         |
| 2.2 Thermal Specifications                              | 8         |
| 2.3 Electrical Specifications                           | 8         |
| <b>3. Output Control</b>                                | <b>14</b> |
| <b>4. Power Management</b>                              | <b>15</b> |
| <b>5. Output Enable Control on 9QXL2001C (DB2000QL)</b> | <b>15</b> |
| 5.1 Traditional Method                                  | 15        |
| 5.2 Side-Band Interface                                 | 15        |
| <b>6. Test Loads</b>                                    | <b>17</b> |
| 6.1 Alternate Terminations                              | 17        |
| <b>7. General SMBus Serial Interface Information</b>    | <b>18</b> |
| 7.1 How to Write                                        | 18        |
| 7.2 How to Read                                         | 18        |
| 7.3 SMBus Addressing                                    | 19        |
| <b>8. Application Information</b>                       | <b>23</b> |
| 8.1 PCB Layout Recommendations                          | 23        |
| <b>9. Package Outline Drawings</b>                      | <b>24</b> |
| <b>10. Marking Diagram</b>                              | <b>24</b> |
| <b>11. Ordering Information</b>                         | <b>24</b> |
| <b>12. Revision History</b>                             | <b>25</b> |

# 1. Pin Information

## 1.1 Signal Types

Table 1. Signal Types

| Term | Description                                                                                    |
|------|------------------------------------------------------------------------------------------------|
| I    | Input                                                                                          |
| O    | Input                                                                                          |
| OD   | Open Drain Output                                                                              |
| I/O  | Bi-Directional                                                                                 |
| PD   | Pull-down                                                                                      |
| PU   | Pull-up                                                                                        |
| Z    | Tristate                                                                                       |
| D    | Driven                                                                                         |
| X    | Don't care                                                                                     |
| SE   | Single ended                                                                                   |
| DIF  | Differential                                                                                   |
| PWR  | 3.3 V power                                                                                    |
| GND  | Ground                                                                                         |
| PDT  | Power Down Tolerant: These signals must tolerate being driven when the device is powered down. |

*Note:* Some pins have both internal pull-up and pull-down resistors which bias the pins to VDD/2.

## 1.2 Pin Assignments

|   | 1       | 2       | 3                                                                                                                                                         | 4                           | 5      | 6                | 7     | 8                           | 9     | 10        | 11                  | 12     |   |
|---|---------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|--------|------------------|-------|-----------------------------|-------|-----------|---------------------|--------|---|
| A | DIF17   | DIF16#  | DIF16                                                                                                                                                     | DIF15#                      | DIF15  | DIF14#           | DIF14 | DIF13#                      | DIF13 | DIF12#    | DIF12               | DIF11# | A |
| B | DIF17#  | VDDO3.3 | NC                                                                                                                                                        | <sup>^</sup> vSADR0_t<br>ri | NC     | VDDA3.3          | NC    | <sup>^</sup> vSADR1_t<br>ri | NC    | vOE12#    | VDDO3.3             | DIF11  | B |
| C | DIF18   | NC      | <div style="text-align: center;"> <p>9QXL2001</p> <p>6.00 x 6.00 mm, x 0.5mm pitch</p> <p>80-VFQFPN Package</p> <p>Top View</p> <p>EPAD is GND</p> </div> |                             |        |                  |       |                             |       |           | vOE11#              | DIF10# | C |
| D | DIF18#  | NC      |                                                                                                                                                           |                             |        |                  |       |                             |       |           | NC                  | DIF10  | D |
| E | DIF19   | vSBEN   |                                                                                                                                                           |                             |        |                  |       |                             |       |           | vOE10#/SH<br>FT_LD# | vOE9#  | E |
| F | DIF19#  | NC      |                                                                                                                                                           |                             |        |                  |       |                             |       |           | NC                  | DIF9#  | F |
| G | DIF_IN  | NC      |                                                                                                                                                           |                             |        |                  |       |                             |       |           | NC                  | DIF9   | G |
| H | DIF_IN# | VDDR3.3 |                                                                                                                                                           |                             |        |                  |       |                             |       |           | vOE8#               | DIF8#  | H |
| J | DIF0    | NC      |                                                                                                                                                           |                             |        |                  |       |                             |       |           | NC                  | DIF8   | J |
| K | DIF0#   | NC      |                                                                                                                                                           |                             |        |                  |       |                             |       |           | vOE7#               | DIF7#  | K |
| L | DIF1    | VDDO3.3 | NC                                                                                                                                                        | SMBDAT                      | SMBCLK | NC               | NC    | vOE5#/DAT<br>A              | NC    | vOE6#/CLK | VDDO3.3             | DIF7   | L |
| M | DIF1#   | DIF2    | DIF2#                                                                                                                                                     | DIF3                        | DIF3#  | vCKPWRG<br>D_PD# | DIF4  | DIF4#                       | DIF5  | DIF5#     | DIF6                | DIF6#  | M |
|   | 1       | 2       | 3                                                                                                                                                         | 4                           | 5      | 6                | 7     | 8                           | 9     | 10        | 11                  | 12     |   |

**Note:** Pins with a ^ prefix have an internal pull-up resistor.  
Pins with a v prefix have an internal pull-down resistor.  
Pins with a ^v prefix have an internal pull-up/down resistor biasing network.

**Figure 2. Pin Assignments – Top View**

## 1.3 Pin Descriptions

**Table 2. Pin Descriptions**

| Number | Name   | Type   | Description                              |
|--------|--------|--------|------------------------------------------|
| A 1    | DIF17  | O, DIF | Differential true clock output.          |
| A 2    | DIF16# | O, DIF | Differential complementary clock output. |
| A 3    | DIF16  | O, DIF | Differential true clock output.          |
| A 4    | DIF15# | O, DIF | Differential complementary clock output. |

Table 2. Pin Descriptions (Cont.)

| Number |    | Name                | Type           | Description                                                                                                                                                                                                                                        |
|--------|----|---------------------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A      | 5  | DIF15               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |
| A      | 6  | DIF14#              | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                           |
| A      | 7  | DIF14               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |
| A      | 8  | DIF13#              | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                           |
| A      | 9  | DIF13               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |
| A      | 10 | DIF12#              | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                           |
| A      | 11 | DIF12               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |
| A      | 12 | DIF11#              | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                           |
| B      | 1  | DIF17#              | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                           |
| B      | 2  | VDDO3.3             | PWR            | Power supply for outputs. Nominally 3.3V.                                                                                                                                                                                                          |
| B      | 3  | NC                  | NC             | No connection.                                                                                                                                                                                                                                     |
| B      | 4  | $\wedge$ vSADR0_tri | I, SE, PD, PU  | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to $V_{DD}/2$ . See the <a href="#">SMBus Addressing</a> table. |
| B      | 5  | NC                  | NC             | No connection.                                                                                                                                                                                                                                     |
| B      | 6  | VDDA3.3             | PWR            | 3.3V power for the PLL core.                                                                                                                                                                                                                       |
| B      | 7  | NC                  | NC             | No connection.                                                                                                                                                                                                                                     |
| B      | 8  | $\wedge$ vSADR1_tri | I, SE, PD, PU  | SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus addresses. It has internal pull-up/down resistors to bias to $V_{DD}/2$ . See the <a href="#">SMBus Addressing</a> table. |
| B      | 9  | NC                  | NC             | No connection.                                                                                                                                                                                                                                     |
| B      | 10 | vOE12#              | I, SE, PD, PDT | Active low input for enabling output 12. This pin has an internal pull-down. 1 = disable output, 0 = enable output.                                                                                                                                |
| B      | 11 | VDDO3.3             | PWR            | Power supply for outputs. Nominally 3.3V.                                                                                                                                                                                                          |
| B      | 12 | DIF11               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |
| C      | 1  | DIF18               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |
| C      | 2  | NC                  | NC             | No connection.                                                                                                                                                                                                                                     |
| C      | 11 | vOE11#              | I, SE, PD, PDT | Active low input for enabling output 11. This pin has an internal pull-down. 1 = disable output, 0 = enable output.                                                                                                                                |
| C      | 12 | DIF10#              | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                           |
| D      | 1  | DIF18#              | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                           |
| D      | 2  | NC                  | NC             | No connection.                                                                                                                                                                                                                                     |
| D      | 11 | NC                  | NC             | No connection.                                                                                                                                                                                                                                     |
| D      | 12 | DIF10               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |
| E      | 1  | DIF19               | O, DIF         | Differential true clock output.                                                                                                                                                                                                                    |

Table 2. Pin Descriptions (Cont.)

| Number |    | Name            | Type           | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|----|-----------------|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| E      | 2  | vSBEN           | I, SE, PD, PDT | Input that enables the Side-Band Interface for controlling output enables. This pin disables the output enable pins when asserted. It has an internal pull-down resistor.<br>0 = OE pins and SMBus enable bits control outputs, Side-band interface disabled.<br>1 = Side-Band Interface controls output enables, OE pins and SMBus enable bits are disabled.                                                                                                    |
| E      | 11 | vOE10#/SHFT_LD# | I, SE, PD, PDT | Active low input for enabling output 10 or SHFT_LD# pin for the Side-Band Interface. Refer to the <a href="#">Side-Band Interface</a> section for details. This pin has an internal pull-down.<br><b>OE mode:</b> 1 = disable output, 0 = enable output.<br><b>Side-Band Mode:</b> 1 = enable Side-Band Interface shift register, 0 = disable Side-Band Interface shift register. A falling edge transfers Side-Band shift register contents to output register. |
| E      | 12 | vOE9#           | I, SE, PD, PDT | Active low input for enabling output 9. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output.                                                                                                                                                                                                                                                                                                                                            |
| F      | 1  | DIF19#          | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| F      | 2  | NC              | NC             | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| F      | 11 | NC              | NC             | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| F      | 12 | DIF9#           | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| G      | 1  | DIF_IN          | I, DIF, PDT    | HCSL true input.                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
| G      | 2  | NC              | NC             | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| G      | 11 | NC              | O, OD, PDT     | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| G      | 12 | DIF9            | O, DIF         | Differential true clock output.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| H      | 1  | DIF_IN#         | I, DIF, PDT    | HCSL complementary input.                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| H      | 2  | VDDR3.3         | PWR            | Power supply for differential input clock (receiver). This V <sub>DD</sub> should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.                                                                                                                                                                                                                                                                                                 |
| H      | 11 | vOE8#           | I, SE, PD, PDT | Active low input for enabling output 8. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output.                                                                                                                                                                                                                                                                                                                                            |
| H      | 12 | DIF8#           | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| J      | 1  | DIF0            | O, DIF         | Differential true clock output.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| J      | 2  | NC              | NC             | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| J      | 11 | NC              | NC             | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| J      | 12 | DIF8            | O, DIF         | Differential true clock output.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| K      | 1  | DIF0#           | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| K      | 2  | NC              | NC             | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| K      | 11 | vOE7#           | I, SE, PD, PDT | Active low input for enabling output 7. This pin has an internal pull-down.<br>1 = disable output, 0 = enable output.                                                                                                                                                                                                                                                                                                                                            |
| K      | 12 | DIF7#           | O, DIF         | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                                                                                                         |
| L      | 1  | DIF1            | O, DIF         | Differential true clock output.                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| L      | 2  | VDDO3.3         | PWR            | Power supply for outputs. Nominally 3.3V.                                                                                                                                                                                                                                                                                                                                                                                                                        |
| L      | 3  | NC              | NC             | No connection.                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

Table 2. Pin Descriptions (Cont.)

| Number |    | Name         | Type             | Description                                                                                                                                                                                                                                                                                                                                                                   |
|--------|----|--------------|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| L      | 4  | SMBDAT       | I/O, SE, OD, PDT | Data pin of SMBUS circuitry.                                                                                                                                                                                                                                                                                                                                                  |
| L      | 5  | SMBCLK       | I, SE, PDT       | Clock pin of SMBUS circuitry.                                                                                                                                                                                                                                                                                                                                                 |
| L      | 6  | NC           | NC               | No connection.                                                                                                                                                                                                                                                                                                                                                                |
| L      | 7  | NC           | NC               | No connection.                                                                                                                                                                                                                                                                                                                                                                |
| L      | 8  | vOE5#/DATA   | I, SE, PD, PDT   | Active low input for enabling output 5 or the data pin for the Side-Band Interface. Refer to the <a href="#">Side-Band Interface</a> section for details. This pin has an internal pull-down.<br><b>OE mode:</b> 1 = disable output, 0 = enable output.<br><b>Side-Band mode:</b> Data pin.                                                                                   |
| L      | 9  | NC           | NC               | No connection.                                                                                                                                                                                                                                                                                                                                                                |
| L      | 10 | vOE6#/CLK    | I, SE, PD, PDT   | Active low input for enabling output 6 or the clock pin for the Side-Band Interface shift register. Refer to the <a href="#">Side-Band Interface</a> section for details. This pin has an internal pull-down.<br><b>OE mode:</b> 1 = disable output, 0 = enable output.<br><b>Side-Band mode:</b> Clocks data into the Side-Band Interface shift register on the rising edge. |
| L      | 11 | VDDO3.3      | PWR              | Power supply for outputs. Nominally 3.3V.                                                                                                                                                                                                                                                                                                                                     |
| L      | 12 | DIF7         | O, DIF           | Differential true clock output.                                                                                                                                                                                                                                                                                                                                               |
| M      | 1  | DIF1#        | O, DIF           | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                      |
| M      | 2  | DIF2         | O, DIF           | Differential true clock output.                                                                                                                                                                                                                                                                                                                                               |
| M      | 3  | DIF2#        | O, DIF           | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                      |
| M      | 4  | DIF3         | O, DIF           | Differential true clock output.                                                                                                                                                                                                                                                                                                                                               |
| M      | 5  | DIF3#        | O, DIF           | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                      |
| M      | 6  | vCKPWRGD_PD# | I, SE, PD, PDT   | Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down mode, subsequent high assertions exit Power Down mode. This pin has internal pull-down resistor.                                                                                                                                                                   |
| M      | 7  | DIF4         | O, DIF           | Differential true clock output.                                                                                                                                                                                                                                                                                                                                               |
| M      | 8  | DIF4#        | O, DIF           | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                      |
| M      | 9  | DIF5         | O, DIF           | Differential true clock output.                                                                                                                                                                                                                                                                                                                                               |
| M      | 10 | DIF5#        | O, DIF           | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                      |
| M      | 11 | DIF6         | O, DIF           | Differential true clock output.                                                                                                                                                                                                                                                                                                                                               |
| M      | 12 | DIF6#        | O, DIF           | Differential complementary clock output.                                                                                                                                                                                                                                                                                                                                      |
| -      | -  | EPAD         | GND              | Connect EPAD to ground.                                                                                                                                                                                                                                                                                                                                                       |

## 2. Specifications

### 2.1 Absolute Maximum Ratings

**Caution:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

| Parameter                           | Symbol      | Conditions                              | Minimum   | Typical | Maximum        | Unit |
|-------------------------------------|-------------|-----------------------------------------|-----------|---------|----------------|------|
| Supply Voltage <sup>[1][2]</sup>    | $V_{DDx}$   | -                                       | -         | -       | 3.9            | V    |
| Input Low Voltage <sup>[1]</sup>    | $V_{IL}$    | -                                       | GND - 0.5 | -       | -              | V    |
| Input High Voltage <sup>[3]</sup>   | $V_{IH}$    | Except for SMBus interface.             | -         | -       | $V_{DD} + 0.5$ | V    |
| Input High Voltage <sup>[1]</sup>   | $V_{IHSMB}$ | SMBus clock and data pins.              | -         | -       | 3.9            | V    |
| Storage Temperature <sup>[1]</sup>  | $T_S$       | -                                       | -65       | -       | 150            | °C   |
| Junction Temperature <sup>[1]</sup> | $T_J$       | Maximum operating junction temperature. | -         | -       | 125            | °C   |
| Human Body Model <sup>[1]</sup>     | ESD         | JESD22-A114 (JS-001) Classification.    | 2000      | -       | -              | V    |
| Charged Device Model <sup>[1]</sup> |             | JESD22-C101 Classification.             | 500       | -       | -              | V    |

1. Confirmed by design and characterization, not 100% tested in production.
2. Operation under these conditions is neither implied nor guaranteed.
3. Not to exceed 3.9V.

### 2.2 Thermal Specifications

Table 3. Thermal Characteristics

| Parameter          | Symbol         | Conditions                       | Package              | Typical Value | Unit |
|--------------------|----------------|----------------------------------|----------------------|---------------|------|
| Thermal Resistance | $\theta_{JC}$  | Junction to case.                | NHG80 <sup>[1]</sup> | 44            | °C/W |
|                    | $\theta_{Jb}$  | Junction to base.                |                      | 2             | °C/W |
|                    | $\theta_{JA0}$ | Junction to air, still air.      |                      | 33            | °C/W |
|                    | $\theta_{JA1}$ | Junction to air, 1 m/s air flow. |                      | 29            | °C/W |
|                    | $\theta_{JA3}$ | Junction to air, 3 m/s air flow. |                      | 28            | °C/W |
|                    | $\theta_{JA5}$ | Junction to air, 5 m/s air flow. |                      | 27            | °C/W |

1. EPAD soldered to board.

### 2.3 Electrical Specifications

$T_A = T_{AMB}$ . Supply voltages per normal operation conditions; see [Test Loads](#) for loading conditions.

Table 4. SMBus

| Parameter                           | Symbol       | Conditions                                          | Minimum | Typical | Maximum     | Unit |
|-------------------------------------|--------------|-----------------------------------------------------|---------|---------|-------------|------|
| SMBus Input Low Voltage             | $V_{ILSMB}$  | -                                                   | -       | -       | 0.8         | V    |
| SMBus Input High Voltage            | $V_{IHSMB}$  | -                                                   | 2.1     | -       | $V_{DDSMB}$ | V    |
| SMBus Output Low Voltage            | $V_{OLSMB}$  | At $I_{PULLUP}$ .                                   | -       | -       | 0.4         | V    |
| SMBus Sink Current                  | $I_{PULLUP}$ | At $V_{OL}$ .                                       | 4       | -       | -           | mA   |
| Nominal Bus Voltage <sup>[1]</sup>  | $V_{DDSMB}$  | -                                                   | 2.7     | -       | 3.6         | V    |
| SCLK/SDATA Rise Time <sup>[1]</sup> | $t_{RSMB}$   | (Max $V_{IL} - 0.15V$ ) to (Min $V_{IH} + 0.15V$ ). | -       | -       | 1000        | ns   |

Table 4. SMBus (Cont.)

| Parameter                                | Symbol     | Conditions                                        | Minimum | Typical | Maximum | Unit |
|------------------------------------------|------------|---------------------------------------------------|---------|---------|---------|------|
| SCLK/SDATA Fall Time <sup>[1]</sup>      | $t_{FSMB}$ | (Min $V_{IH}$ + 0.15V) to (Max $V_{IL}$ - 0.15V). | -       | -       | 300     | ns   |
| SMBus Operating Frequency <sup>[2]</sup> | $f_{SMB}$  | SMBus operating frequency.                        | -       | -       | 400     | kHz  |

1. Confirmed by design and characterization, not 100% tested in production.
2. The device must be powered up with CKPWRGD\_PD# = '1' for the SMBus to be active.
3. Control input must be monotonic from 20% to 80% of input swing.
4. Time from deassertion until outputs are > 200mV.
5. DIF\_IN input.

Table 5. DIF\_IN Clock Input Parameters

| Parameter                                       | Symbol      | Conditions                                                | Minimum | Typical | Maximum | Unit    |
|-------------------------------------------------|-------------|-----------------------------------------------------------|---------|---------|---------|---------|
| Input Crossover Voltage – DIF_IN <sup>[1]</sup> | $V_{CROSS}$ | Crossover voltage.                                        | 100     | -       | 900     | mV      |
| Input Swing – DIF_IN <sup>[1]</sup>             | $V_{SWING}$ | Differential value.                                       | 200     | -       | -       | mV      |
| Input Slew Rate – DIF_IN <sup>[1][2]</sup>      | $dv/dt$     | Measured differentially.                                  | 0.7     | -       | -       | V/ns    |
| Input Leakage Current                           | $I_{IN}$    | CLK_IN#, $V_{IN} = 0.8V$ ,<br>CLK_IN, $V_{IN} = V_{DD}$ . | -150    | -       | 40      | $\mu A$ |
| Input Duty Cycle <sup>[1]</sup>                 | $d_{tin}$   | Measurement from differential waveform.                   | 45      | -       | 55      | %       |

1. Confirmed by design and characterization, not 100% tested in production.
2. Slew rate measured through  $\pm 75mV$  window centered around differential zero.

Table 6. Input/Supply/Common Parameters

| Parameter                     | Symbol          | Conditions                                                                                                                                       | Minimum   | Typical    | Maximum        | Unit        |
|-------------------------------|-----------------|--------------------------------------------------------------------------------------------------------------------------------------------------|-----------|------------|----------------|-------------|
| Supply Voltage                | $V_{DDx}$       | Supply voltage for core and analog.                                                                                                              | 2.97      | 3.3        | 3.63           | V           |
| Ambient Operating Temperature | $T_{AMB}$       | Industrial range.                                                                                                                                | -40       | 25         | 105            | $^{\circ}C$ |
| Input High Voltage            | $V_{IH}$        | Single-ended inputs, except SMBus, tri-level inputs.                                                                                             | 2         | -          | $V_{DD} + 0.3$ | V           |
| Input Low Voltage             | $V_{IL}$        | Single-ended inputs, except SMBus, tri-level inputs.                                                                                             | GND - 0.3 | -          | 0.8            | V           |
| Input High Voltage            | $V_{IH}$        | Tri-level inputs.                                                                                                                                | 2.2       | -          | $V_{DD} + 0.3$ | V           |
| Input Mid Voltage             | $V_{IM}$        | Tri-level inputs.                                                                                                                                | 1.2       | $V_{DD}/2$ | 1.8            | V           |
| Input Low Voltage             | $V_{IL}$        | Tri-level inputs.                                                                                                                                | GND - 0.3 | -          | 0.8            | V           |
| Input Current                 | $I_{IN}$        | Single-ended inputs, $V_{IN} = GND$ , $V_{IN} = V_{DD}$ .                                                                                        | -5        | -          | 5              | $\mu A$     |
|                               | $I_{INP}$       | Single-ended inputs.<br>$V_{IN} = 0V$ ; inputs with internal pull-up resistors.<br>$V_{IN} = V_{DD}$ ; inputs with internal pull-down resistors. | -50       | -          | 50             | $\mu A$     |
| Input Frequency               | $F_{IN}$        | $V_{DD} = 3.3V$ .                                                                                                                                | 1         | -          | 400            | MHz         |
| Pin Inductance <sup>[1]</sup> | $L_{pin}$       |                                                                                                                                                  | -         | -          | 7              | nH          |
| Capacitance                   | $C_{IN}$        | Logic inputs, except DIF_IN. <sup>[1]</sup>                                                                                                      | 1.5       | -          | 5              | pF          |
|                               | $C_{INDIF\_IN}$ | DIF_IN differential clock inputs. <sup>[1][2]</sup>                                                                                              | 1.5       | -          | 2.7            | pF          |
|                               | $C_{OUT}$       | Output pin capacitance. <sup>[1]</sup>                                                                                                           | -         | -          | 6              | pF          |

Table 6. Input/Supply/Common Parameters (Cont.)

| Parameter                | Symbol       | Conditions                                                                                     | Minimum | Typical | Maximum | Unit   |
|--------------------------|--------------|------------------------------------------------------------------------------------------------|---------|---------|---------|--------|
| Clk Stabilization [1][3] | $T_{STAB}$   | From $V_{DD}$ power-up and after input clock stabilization or deassertion of PD# to 1st clock. | -       | 1.2     | 3       | ms     |
| OE# Latency [1][3][4]    | $t_{LATO\#}$ | DIF start after OE# assertion.<br>DIF stop after OE# deassertion.                              | 4       | 5       | 10      | clocks |
| Tdrive_PD# [1][4]        | $t_{DRVPD}$  | DIF output enable after PD# deassertion.                                                       | -       | 0.3     | 1       | ms     |
| Tfall [3]                | $t_F$        | Fall time of control inputs.                                                                   | -       | -       | 5       | ns     |
| Trise [3]                | $t_R$        | Rise time of control inputs.                                                                   | -       | -       | 5       | ns     |

1. Confirmed by design and characterization, not 100% tested in production.

2. DIF\_IN input.

3. Time from deassertion until outputs are > 200mV.

4. Control input must be monotonic from 20% to 80% of input swing.

Table 7. Side-Band Interface

| Parameter             | Symbol       | Conditions                                                              | Minimum | Typical | Maximum | Unit   |
|-----------------------|--------------|-------------------------------------------------------------------------|---------|---------|---------|--------|
| Clock Period          | $t_{PERIOD}$ | Clock period.                                                           | 40      | -       | -       | ns     |
| Setup Time to Clock   | $t_{SETUP}$  | SHFT setup to CLK rising edge.                                          | 10      | -       | -       | ns     |
| Data Setup Time       | $t_{DSU}$    | DATA setup to CLK rising edge.                                          | 5       | -       | -       | ns     |
| Data Hold Time [1]    | $t_{DHOLD}$  | DATA hold after CLK rising edge.                                        | 2       | -       | -       | ns     |
| Delay Time [1]        | $t_{DELAY}$  | Delay from CLK rising edge to LD# falling edge.                         | 10      | -       | -       | ns     |
| Propagation Delay [2] | $t_{PD}$     | Delay from LD# falling edge to next output configuration taking effect. | 4       | -       | 10      | clocks |
| Slew Rate [3]         | $t_{SLEW}$   | CLK input (between 20% and 80%).                                        | 0.7     | -       | 4       | V/ns   |

1. Confirmed by design and characterization, not 100% tested in production.

2. Refers to device differential input clock.

3. Control input must be monotonic from 20% to 80% of input swing.

Table 8. LP-HCSL Outputs Driving High Impedance Receiver at 100MHz

| Parameter                        | Symbol             | Conditions                                                                      | Minimum | Typical | Maximum | Industry Limit | Unit     |
|----------------------------------|--------------------|---------------------------------------------------------------------------------|---------|---------|---------|----------------|----------|
| Maximum Voltage [1][2]           | $V_{max}$          | Measurement on single ended signal using absolute value. (scope averaging off). | -       | 875     | 1010    | 1150           | mV       |
| Minimum Voltage [1][2][3][4]     | $V_{min}$          |                                                                                 | -91     | 6       | -       | -300           |          |
| Voltage High [1][2]              | $V_{high}$         | $V_{high}$ set to 800mV.                                                        | 678     | 810     | 903     | N/A            | mV       |
| Voltage Low [1][2][3][4]         | $V_{low}$          |                                                                                 | -88     | 35      | 123     | N/A            |          |
| Slew Rate [1][3][5][6]           | $dV/dt$            | Scope averaging on, fast setting.                                               | 2       | 2.6     | 3.4     | 2 to 5         | V/ns     |
| Rise/Fall Matching [1][7]        | $\Delta t_R/t_F$   | Single-ended measurement.                                                       | -       | 3.6     | 19      | 20             | %        |
| Crossing Voltage (abs) [1][3][8] | $V_{cross\_abs}$   | Scope averaging off.                                                            | 278     | 412     | 543     | 250 to 550     | mV       |
| Crossing Voltage (var) [1][3][8] | $\Delta V_{cross}$ | Scope averaging off.                                                            | -       | 10      | 57      | 140            | mV       |
| Output Impedance [9]             | $Z_o$              | DIF outputs (differential value).                                               | 75      | 79      | 84      | 64 to 102      | $\Omega$ |

1. At default SMBus settings.
2. Includes 300mV of overshoot for Vmax and 300mV of undershoot for Vmin.
3. Confirmed by design and characterization, not 100% tested in production.
4. Vcross is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).
5. Measured from differential waveform.
6. Slew rate is measured through the Vswing voltage range centered around differential 0 V. This results in a  $\pm 150\text{mV}$  window around differential 0V.
7. Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a  $\pm 75\text{mV}$  window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.
8. The total variation of all Vcross measurements in any particular system. Note that this is a subset of Vcross\_min/max (Vcross absolute) allowed. The intent is to limit Vcross induced modulation by setting  $\Delta\text{-Vcross}$  to be smaller than Vcross absolute.
9. Measured at Vcross\_abs.

Table 9. Current Consumption

| Parameter                | Symbol             | Conditions                                                                      | Minimum | Typical | Maximum | Unit |
|--------------------------|--------------------|---------------------------------------------------------------------------------|---------|---------|---------|------|
| Operating Supply Current | $I_{DDVDD + VDDA}$ | Source termination, all outputs 100MHz, $C_L = 2\text{pF}$ ; $Z_0 = 85\Omega$ . | -       | 218     | 234     | mA   |
|                          | $I_{DDR}$          |                                                                                 | -       | 0.45    | 0.6     |      |
| Powerdown Current        | $I_{DD\_PD}$       | All VDD's except VDDR, CKPWRGD_PD# = 0.                                         | -       | 3.3     | 5       | mA   |
|                          | $I_{DDR\_PD}$      | VDDR, CKPWRGD_PD# = 0.                                                          | -       | 0.6     | 1       |      |

Table 10. Skew and Differential Jitter Parameters

| Parameter                              | Symbol                   | Conditions                                                                       | Minimum | Typical | Maximum | Unit  |
|----------------------------------------|--------------------------|----------------------------------------------------------------------------------|---------|---------|---------|-------|
| CLK_IN, DIF[x:0]<br>[1][2][3][4][5][6] | $t_{PD}$                 | Input-to-output skew.                                                            | 1.2     | 1.4     | 1.6     | ns    |
| CLK_IN, DIF[x:0]<br>[1][2][3][5][7]    | $t_{PD\text{VARIATION}}$ | Input-to-output skew variation for a single device over temperature and voltage. | 1.1     | 1.2     | 1.4     | ps/°C |
| DIF[x:0] [1][2][3][6]                  | $t_{SKEW\_ALL}$          | Output-to-output skew across all outputs.                                        | -       | 37      | 50      | ps    |
| Duty Cycle Distortion<br>[1][6][8]     | $t_{DCD}$                | Measured differentially at 100MHz.                                               | -0.5    | -0.1    | 0.5     | %     |

1. Measured into fixed 2pF load cap. Input to output skew is measured at the first output edge following the corresponding input. Default SMBus settings unless otherwise noted.
2. Measured from differential cross-point to differential cross-point.
3. All input-to-output specs refer to the timing between an input edge and the specific output edge created by it.
4. Measured with scope averaging on to find mean value.
5. Confirmed by design and characterization, not 100% tested in production.
6. Measured from differential waveform.
7. This is the amount of input-to-output delay variation with respect to temperature. This is equivalent to 250ps from -40°C to +85°C.
8. Duty cycle distortion is the difference in duty cycle between the output and the input clock.

Table 11. PCIe Refclk Phase Jitter - Normal Conditions <sup>[1]</sup>

| Parameter                                                           | Symbol             | Conditions                                       | Typical | Maximum | Specification Limits | Unit     |
|---------------------------------------------------------------------|--------------------|--------------------------------------------------|---------|---------|----------------------|----------|
| Additive PCIe Phase Jitter<br>(Common Clock Architecture)           | $t_{jphPCleG1-CC}$ | PCIe Gen1 (2.5GT/s) <sup>[2][3][4]</sup>         | 292     | 415     | 86,000               | fs pk-pk |
|                                                                     | $t_{jphPCleG2-CC}$ | PCIe Gen2 Low Band (5GT/s) <sup>[2][3][4]</sup>  | 39      | 50      | 3100                 | fs RMS   |
|                                                                     |                    | PCIe Gen2 High Band (5GT/s) <sup>[2][3][4]</sup> | 15      | 18      | 3000                 |          |
|                                                                     | $t_{jphPCleG3-CC}$ | PCIe Gen3 (8GT/s) <sup>[2][3][4]</sup>           | 13      | 17      | 1000                 |          |
|                                                                     | $t_{jphPCleG4-CC}$ | PCIe Gen4 (16GT/s) <sup>[2][3][4][5][6]</sup>    | 13      | 17      | 500                  |          |
|                                                                     | $t_{jphPCleG5-CC}$ | PCIe Gen5 (32GT/s) <sup>[2][3][4][5][7]</sup>    | 5.0     | 6.6     | 150                  |          |
|                                                                     | $t_{jphPCleG6-CC}$ | PCIe Gen6 (64GT/s) <sup>[2][3][4][5][8]</sup>    | 3.0     | 3.9     | 100                  |          |
|                                                                     | $t_{jphPCleG7-CC}$ | PCIe Gen7 (128GT/s) <sup>[2][3][4][5][9]</sup>   | 2.1     | 2.8     | 67                   |          |
| Additive PCIe Phase Jitter<br>(IR Clock Architectures - SRIS, SRNS) | $t_{jphPCleG2-IR}$ | PCIe Gen2 (5GT/s) <sup>[10]</sup>                | 37      | 46      | [10]                 | fs RMS   |
|                                                                     | $t_{jphPCleG3-IR}$ | PCIe Gen3 (8GT/s) <sup>[10]</sup>                | 14      | 18      |                      |          |
|                                                                     | $t_{jphPCleG4-IR}$ | PCIe Gen4 (16GT/s) <sup>[6][10]</sup>            | 15      | 18      |                      |          |
|                                                                     | $t_{jphPCleG5-IR}$ | PCIe Gen5 (32GT/s) <sup>[7][10]</sup>            | 4.0     | 6.6     |                      |          |
|                                                                     | $t_{jphPCleG6-IR}$ | PCIe Gen6 (64GT/s) <sup>[8][10]</sup>            | 2.9     | 3.9     |                      |          |
|                                                                     | $t_{jphPCleG7-IR}$ | PCIe Gen7 (128GT/s) <sup>[9][10]</sup>           | 2.1     | 2.6     |                      |          |

- Differential input swing = 1600mV and input slew rate = 3.5V/ns.
- The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0. For the exact measurement setup, see Test Loads in the data sheet. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
- Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
- The RMS sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
- SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- Note that 700fs RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 250fs RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 150fs RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 100fs RMS is to be used in channel simulations to account for additional noise in a real system.
- The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 12. PCIe Refclk Phase Jitter - Degraded Conditions [1]

| Parameter                                                           | Symbol             | Conditions                            | Typical | Maximum | Specification Limits | Unit     |
|---------------------------------------------------------------------|--------------------|---------------------------------------|---------|---------|----------------------|----------|
| Additive PCIe Phase Jitter<br>(Common Clock Architecture)           | $t_{jphPCleG1-CC}$ | PCIe Gen1 (2.5GT/s) [2][3][4]         | 442     | 722     | 86,000               | fs pk-pk |
|                                                                     | $t_{jphPCleG2-CC}$ | PCIe Gen2 Low Band (5GT/s) [2][3][4]  | 53      | 79      | 3100                 | fs RMS   |
|                                                                     |                    | PCIe Gen2 High Band (5GT/s) [2][3][4] | 20      | 28      | 3000                 |          |
|                                                                     | $t_{jphPCleG3-CC}$ | PCIe Gen3 (8GT/s) [2][3][4]           | 18      | 26      | 1000                 |          |
|                                                                     | $t_{jphPCleG4-CC}$ | PCIe Gen4 (16GT/s) [2][3][4][5][6]    | 18      | 26      | 500                  |          |
|                                                                     | $t_{jphPCleG5-CC}$ | PCIe Gen5 (32GT/s) [2][3][4][5][7]    | 6.9     | 10.3    | 150                  |          |
|                                                                     | $t_{jphPCleG6-CC}$ | PCIe Gen6 (64GT/s) [2][3][4][5][8]    | 4.2     | 6.2     | 100                  |          |
|                                                                     | $t_{jphPCleG7-CC}$ | PCIe Gen7 (128GT/s) [2][3][4][5][9]   | 2.9     | 4.3     | 67                   |          |
| Additive PCIe Phase Jitter<br>(IR Clock Architectures - SRIS, SRNS) | $t_{jphPCleG2-IR}$ | PCIe Gen2 (5GT/s) [10]                | 49      | 72      | [10]                 | fs RMS   |
|                                                                     | $t_{jphPCleG3-IR}$ | PCIe Gen3 (8GT/s) [10]                | 19      | 28      |                      |          |
|                                                                     | $t_{jphPCleG4-IR}$ | PCIe Gen4 (16GT/s) [6][10]            | 20      | 29      |                      |          |
|                                                                     | $t_{jphPCleG5-IR}$ | PCIe Gen5 (32GT/s) [7][10]            | 5.4     | 8.0     |                      |          |
|                                                                     | $t_{jphPCleG6-IR}$ | PCIe Gen6 (64GT/s) [8][10]            | 4.0     | 5.8     |                      |          |
|                                                                     | $t_{jphPCleG7-IR}$ | PCIe Gen6 (128GT/s) [9][10]           | 2.8     | 4.1     |                      |          |

- Differential input swing = 800mV and input slew rate = 1.5V/ns.
- The Refclk jitter is measured after applying the filter functions found in the PCI Express Base Specification 7.0. For the exact measurement setup, see Test Loads in the data sheet. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
- Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
- The RMS sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
- SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
- Note that 700fs RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 250fs RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 150fs RMS is to be used in channel simulations to account for additional noise in a real system.
- Note that 100fs RMS is to be used in channel simulations to account for additional noise in a real system.
- The PCI Express Base Specification 7.0 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 13. Non-PCIe Refclk Phase Jitter

| Parameter                                                | Symbol           | Conditions                                            | Typical | Maximum | Specification Limit | Unit   |
|----------------------------------------------------------|------------------|-------------------------------------------------------|---------|---------|---------------------|--------|
| Additive Phase Jitter–Normal Conditions <sup>[1]</sup>   | $t_{jphDB2000Q}$ | 100MHz, Intel-supplied filter <sup>[2][3][4][5]</sup> | 10      | 12      | 80                  | fs RMS |
|                                                          | $t_{jph12k-20M}$ | 156.25MHz (12kHz to 20MHz) <sup>[2][3]</sup>          | 30      | 36      | N/A                 |        |
| Additive Phase Jitter–Degraded Conditions <sup>[6]</sup> | $t_{jphDB2000Q}$ | 100MHz, Intel-supplied filter <sup>[2][3][4][5]</sup> | 13      | 15      | 80                  |        |
|                                                          | $t_{jph12k-20M}$ | 156.25MHz (12kHz to 20MHz) <sup>[2][3]</sup>          | 40      | 47      | N/A                 |        |

1. Differential input swing = 1600mV and input slew rate = 3.5V/ns.
2. See [Test Loads](#) for test configuration.
3. SMA100B used as signal source.
4. The 9QXL2001C meets all legacy QPI/UPI specifications by meeting the PCIe and DB2000Q specifications listed in this document.
5. The RMS sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
6. Differential input swing = 800mV and input slew rate = 1.5V/ns.

### 3. Output Control

Table 14. Output Control (SBEN = 0)

|             |         | Traditional Interface |          | Side-Band Interface |    | Outputs |
|-------------|---------|-----------------------|----------|---------------------|----|---------|
| CKPWRGD_PD# | DIF_IN  | OEx bit Byte[2:0]     | OEx# Pin | MASKx Byte[10:8]    | Qx | DIFx    |
| 0           | X       | X                     | X        | X                   | X  | Low/Low |
| 1           | Running | 0                     | X        | X                   | X  | Low/Low |
|             |         | 1                     | 0        | X                   | X  | Running |
|             |         | 1                     | 1        | X                   | X  | Low/Low |
| 1           | Stopped | 1                     | 0        | X                   | X  | Stopped |
|             |         | 1                     | 1        | X                   | X  | Low/Low |

Table 15. Output Control (SBEN = 1)

|             |         | Traditional Interface |          | Side-Band Interface |    | Outputs |
|-------------|---------|-----------------------|----------|---------------------|----|---------|
| CKPWRGD_PD# | DIF_IN  | OEx bit Byte[2:0]     | OEx# Pin | MASKx Byte[10:8]    | Qx | DIFx    |
| 0           | X       | X                     | X        | X                   | X  | Low/Low |
| 1           | Running | X                     | X        | 0                   | 0  | Low/Low |
|             |         | X                     | X        | 0                   | 1  | Running |
|             |         | X                     | X        | 1                   | X  | Running |
| 1           | Stopped | X                     | X        | 0                   | 0  | Low/Low |
|             |         | X                     | X        | 0                   | 1  | Stopped |
|             |         | X                     | X        | 1                   | X  | Stopped |

## 4. Power Management

Table 16. Power Connections

| Pin Number       |      | Description |
|------------------|------|-------------|
| V <sub>DD</sub>  | GND  |             |
| B6, H2           | EPAD | Analog      |
| B2, B11, L2, L11 | EPAD | Outputs     |

## 5. Output Enable Control on 9QXL2001C (DB2000QL)

### 5.1 Traditional Method

The 20-output 9QXL2001C has two methods for enabling and disabling outputs. The first is the traditional method of OE# pins and SMBus output enable bits. Outputs 5 through 12 have dedicated output enable pins and each of the 20 outputs have dedicated SMBus output enable bits in Bytes[0:2] of the SMBus register set.

### 5.2 Side-Band Interface

The second method is a simple 3-wire serial interface referred to as the Side-Band Interface (SBI). This interface consists of DATA, CLK and SHFT\_LD# pins. When the SHFT\_LD# pin is high, the rising edge of CLK can shift DATA into the shift register. After shifting data, the falling edge of SHFT\_LD# clocks the shift register contents to the Output register.

Both the SBI and the traditional interface feed common output enable/disable synchronization logic ensuring glitch free enable and disable of outputs, regardless of the method used.

Both interfaces are not active at the same time, and the SBEN pin selects which interface is active. Tying the SBEN high enables the SBI. Tying the SBEN pin low enables the traditional OE# pin/SMBus output enable interface. When the SBI is enabled, OE[7:9, 11,12]# are disabled and DATA, CLK and SHFT\_LD# are enabled on OE5#, OE6# and OE10# respectively. Additionally, SMBus registers for masking off the disable function of the shift register (0 value of a bit) become active. When set to a one, the mask register forces its respective output to 'enabled'. This prevents accidentally disabling critical outputs when using the SBI.

An SMBus read back bit in Byte 4 indicates which output enable control interface is enabled.

When the SBI is enabled, and power has been applied, the SBI is active, even if the CKPWRGD\_PD# pin indicates the part is in power down. This allows loading the shift register and transferring the contents to the output register before the assertion of CKPWRGD. Note that the mask registers are part of the normal SMBus interface and cannot be accessed when the CKPWRGD\_PD# is low. [Figure 3](#) provides a functional description of the SBI.

The SBI and the traditional SMBus output enable registers both default to the 'output enabled' state at power-up. The mask registers default to zero at power-up, allowing the shift register bits to disable their respective output. See [Figure 3](#).

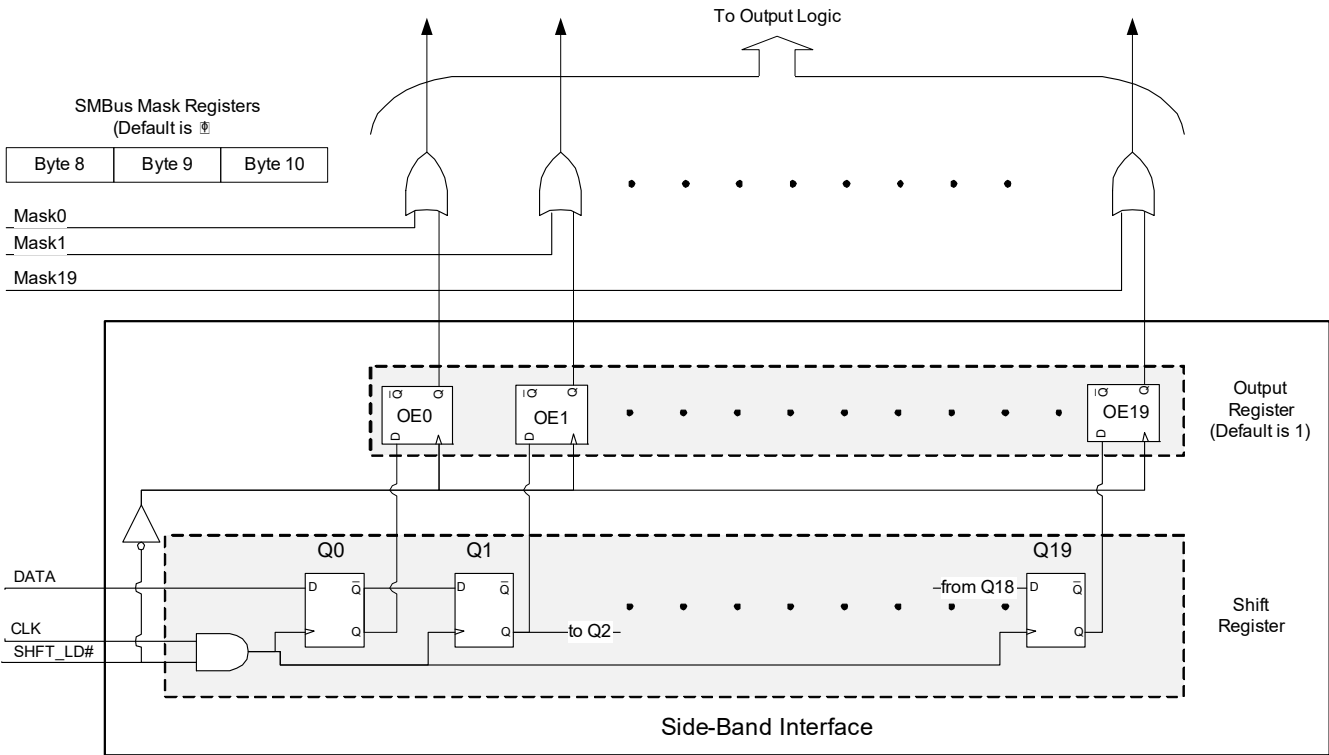


Figure 3. Side-Band Interface Control Logic – Functional Description

Figure 4 shows the basic timing of the side-band interface. The SHFT\_LD# pin goes high to enable the CLK input. Next, the rising edge of CLK clocks enable DATA into the shift register. After the 20th clock, stop the clock low and drive the SHFT\_LD# pin low. The falling edge of SHFT\_LD# clocks the shift register contents to the output register, enabling or disabling the outputs. Always shift 20 bits of data into the shift register to control the outputs.

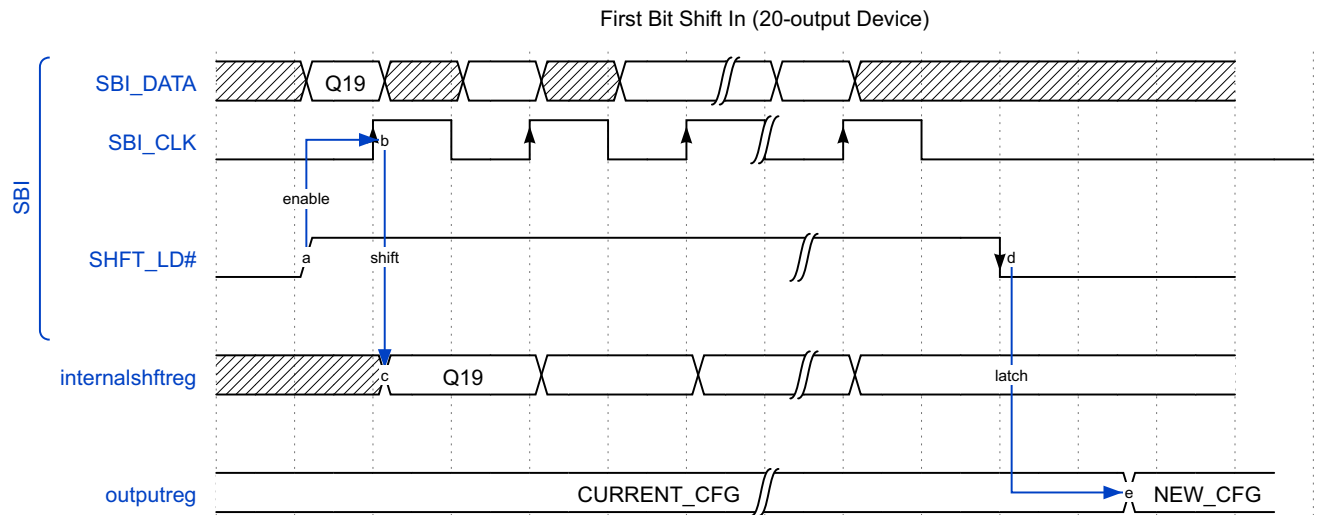


Figure 4. Side-Band Interface Functional Timing

The SBI interface supports clock rates up to 25MHz. Multiple devices may share CLK and DATA pins. Dedicating a SHFT\_LD# pin to each devices allows its use as a chip-select pin. When the SHFT\_LD# pin is low, the 9QXL2001 ignores any activity on the CLK and DATA pins.

## 6. Test Loads

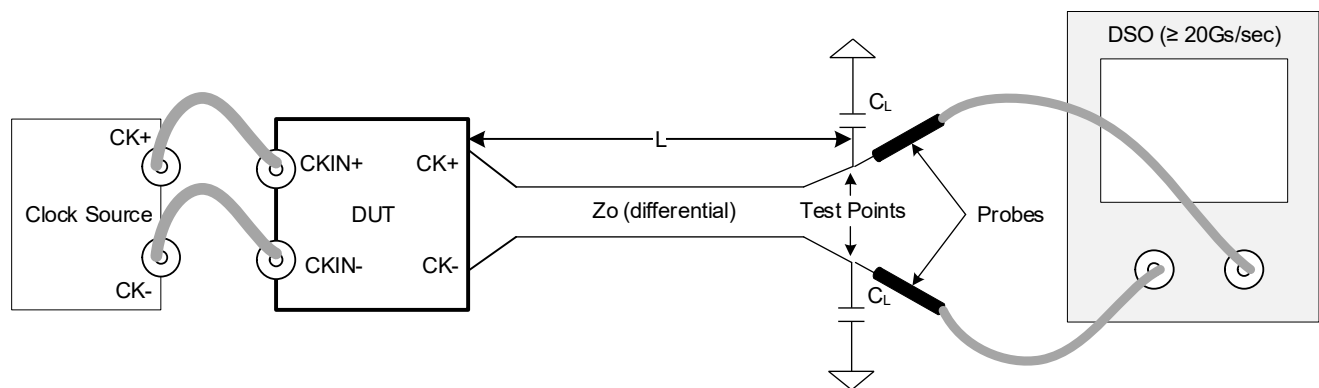


Figure 5. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Termination)

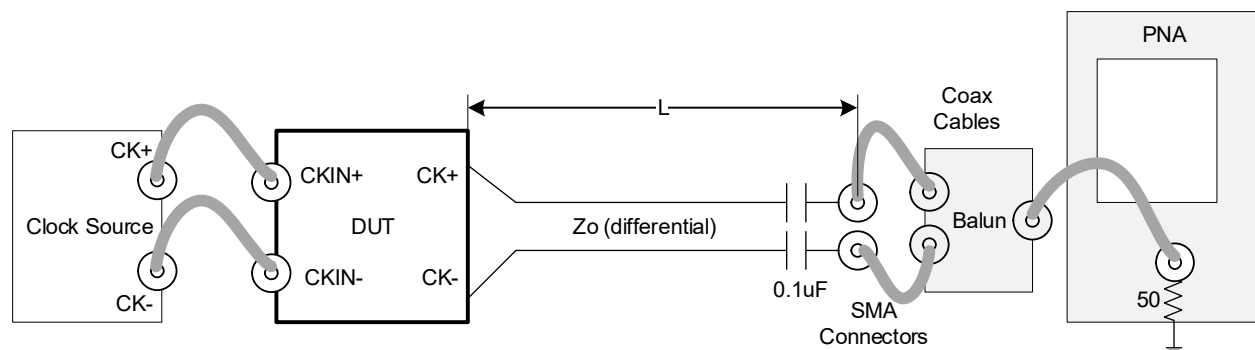


Figure 6. Test Load for Additive Phase Jitter Measurements

Table 17. Parameters for Test Loads

| Clock Source | Rs (Ω)   | Zo (Ω) | L (cm) | CL (pF) |
|--------------|----------|--------|--------|---------|
| SMA100B      | Internal | 85     | 25.4   | 2       |

Note: PCIe Gen6 specifies L = 0cm for 32 and 64 GT/s. L = 25.4cm is more conservative.

### 6.1 Alternate Terminations

The LP-HCSL output can easily drive other logic families. See [“AN-891 Driving LVPECL, LVDS, and CML Logic with “Universal” Low-Power HCSL Outputs”](#) for termination schemes for LVPECL, LVDS, CML and SSTL.

## 7. General SMBus Serial Interface Information

### 7.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

| Index Block Write Operation |           |        |                          |  |
|-----------------------------|-----------|--------|--------------------------|--|
| Controller (Host)           |           | X Byte | Renesas (Slave/Receiver) |  |
| T                           | starT bit |        |                          |  |
| Slave Address               |           |        |                          |  |
| WR                          | WRite     |        |                          |  |
|                             |           |        | ACK                      |  |
| Beginning Byte = N          |           |        |                          |  |
|                             |           |        | ACK                      |  |
| Data Byte Count = X         |           |        |                          |  |
|                             |           |        | ACK                      |  |
| Beginning Byte N            |           |        |                          |  |
|                             |           |        | ACK                      |  |
| O                           |           |        |                          |  |
| O                           |           |        | O                        |  |
| O                           |           | O      |                          |  |
|                             |           | O      |                          |  |
| Byte N + X - 1              |           |        |                          |  |
|                             |           | ACK    |                          |  |
| P                           | stoP bit  |        |                          |  |

### 7.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte N+X-1
- Renesas clock sends **Byte 0 through Byte X (if X<sub>(H)</sub> was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

| Index Block Read Operation |              |                  |                     |
|----------------------------|--------------|------------------|---------------------|
| Controller (Host)          |              |                  | Renesas             |
| T                          | starT bit    |                  |                     |
| Slave Address              |              |                  |                     |
| WR                         | WRite        |                  |                     |
|                            |              |                  | ACK                 |
| Beginning Byte = N         |              |                  |                     |
|                            |              |                  | ACK                 |
| RT                         | Repeat starT |                  |                     |
| Slave Address              |              |                  |                     |
| RD                         | ReaD         |                  |                     |
|                            |              |                  | ACK                 |
|                            |              |                  |                     |
| ACK                        |              |                  | Data Byte Count = X |
|                            |              |                  |                     |
|                            |              | Beginning Byte N |                     |
| ACK                        |              |                  |                     |
|                            |              | O                |                     |
| O                          |              | O                |                     |
| O                          |              | O                |                     |
| O                          |              |                  |                     |
|                            |              | Byte N + X - 1   |                     |
| N                          | Not          |                  |                     |
| P                          | stoP bit     |                  |                     |

## 7.3 SMBus Addressing

Table 18. SMBus Address Selection

| SADR(1:0)_tri | SMBus Address (Read/Write bit = 0) |
|---------------|------------------------------------|
| 00            | D8                                 |
| 0M            | DA                                 |
| 01            | DE                                 |
| M0            | C2                                 |
| MM            | C4                                 |
| M1            | C6                                 |
| 10            | CA                                 |
| 1M            | CC                                 |
| 11            | CE                                 |

SMBus Table: Output Enable Register (functional only when SBEN = 0)

| Byte 0 | Name      | Control Function | Type | 0       | 1      | Default |
|--------|-----------|------------------|------|---------|--------|---------|
| Bit 7  | Reserved  |                  |      |         |        | 0       |
| Bit 6  | DIF_19_En | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 5  | DIF_18_En | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 4  | DIF_17_En | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 3  | DIF_16_En | Output Enable    | RW   | Low/Low | Enable | 1       |
| Bit 2  | Reserved  |                  |      |         |        | 0       |
| Bit 1  | Reserved  |                  |      |         |        | 0       |
| Bit 0  | Reserved  |                  |      |         |        | 0       |

SMBus Table: Output Enable Register (functional only when SBEN = 0)

| Byte 1 | Name     | Control Function | Type | 0                   | 1             | Default |
|--------|----------|------------------|------|---------------------|---------------|---------|
| Bit 7  | DIF_7_En | Output Enable    | RW   | Disabled<br>Low/Low | OE7# Controls | 1       |
| Bit 6  | DIF_6_En | Output Enable    | RW   |                     | OE6# Controls | 1       |
| Bit 5  | DIF_5_En | Output Enable    | RW   |                     | OE5# Controls | 1       |
| Bit 4  | DIF_4_En | Output Enable    | RW   |                     | Enabled       | 1       |
| Bit 3  | DIF_3_En | Output Enable    | RW   |                     | Enabled       | 1       |
| Bit 2  | DIF_2_En | Output Enable    | RW   |                     | Enabled       | 1       |
| Bit 1  | DIF_1_En | Output Enable    | RW   |                     | Enabled       | 1       |
| Bit 0  | DIF_0_En | Output Enable    | RW   |                     | Enabled       | 1       |

**SMBus Table: Output Enable Register (functional only when SBEN = 0)**

| Byte 2 | Name      | Control Function | Type | 0       | 1              | Default |
|--------|-----------|------------------|------|---------|----------------|---------|
| Bit 7  | DIF_15_En | Output Enable    | RW   | Low/Low | Enabled        | 1       |
| Bit 6  | DIF_14_En | Output Enable    | RW   |         | Enabled        | 1       |
| Bit 5  | DIF_13_En | Output Enable    | RW   |         | Enabled        | 1       |
| Bit 4  | DIF_12_En | Output Enable    | RW   |         | OE12# Controls | 1       |
| Bit 3  | DIF_11_En | Output Enable    | RW   |         | OE11# Controls | 1       |
| Bit 2  | DIF_10_En | Output Enable    | RW   |         | OE10# Controls | 1       |
| Bit 1  | DIF_9_En  | Output Enable    | RW   |         | OE9# Controls  | 1       |
| Bit 0  | DIF_8_En  | Output Enable    | RW   |         | OE8# Controls  | 1       |

**SMBus Table: OE# Pin Readback Register**

| Byte 3 | Name    | Control Function | Type | 0       | 1        | Default   |
|--------|---------|------------------|------|---------|----------|-----------|
| Bit 7  | RB_OE12 | Status of OE12#  | R    | Pin Low | Pin High | Real-time |
| Bit 6  | RB_OE11 | Status of OE11#  | R    |         |          | Real-time |
| Bit 5  | RB_OE10 | Status of OE10#  | R    |         |          | Real-time |
| Bit 4  | RB_OE9  | Status of OE9#   | R    |         |          | Real-time |
| Bit 3  | RB_OE8  | Status of OE8#   | R    |         |          | Real-time |
| Bit 2  | RB_OE7  | Status of OE7#   | R    |         |          | Real-time |
| Bit 1  | RB_OE6  | Status of OE6#   | R    |         |          | Real-time |
| Bit 0  | RB_OE5  | Status of OE5#   | R    |         |          | Real-time |

**SMBus Table: SBEN Readback Register**

| Byte 4 | Name     | Control Function | Type | 0       | 1        | Default   |
|--------|----------|------------------|------|---------|----------|-----------|
| Bit 7  | Reserved |                  |      |         |          | 0         |
| Bit 6  | Reserved |                  |      |         |          | 0         |
| Bit 5  | Reserved |                  |      |         |          | 0         |
| Bit 4  | Reserved |                  |      |         |          | 0         |
| Bit 3  | Reserved |                  |      |         |          | 0         |
| Bit 2  | Reserved |                  |      |         |          | 0         |
| Bit 1  | Reserved |                  |      |         |          | 0         |
| Bit 0  | RB_SBEN  | Status of SBEN   | R    | Pin Low | Pin High | Real-time |

**SMBus Table: Vendor and Revision ID Register**

| Byte 5 | Name | Control Function | Type | 0             | 1 | Default |
|--------|------|------------------|------|---------------|---|---------|
| Bit 7  | RID3 | REVISION ID      | R    | C rev is 0010 |   | 0       |
| Bit 6  | RID2 |                  | R    |               |   | 0       |
| Bit 5  | RID1 |                  | R    |               |   | x       |
| Bit 4  | RID0 |                  | R    |               |   | x       |
| Bit 3  | VID3 | VENDOR ID        | R    | IDT/Renesas   |   | 0       |
| Bit 2  | VID2 |                  | R    |               |   | 0       |
| Bit 1  | VID1 |                  | R    |               |   | 0       |
| Bit 0  | VID0 |                  | R    |               |   | 1       |

**SMBus Table: Device ID**

| Byte 6 | Name              | Control Function | Type | 0  | 1 | Default |
|--------|-------------------|------------------|------|----|---|---------|
| Bit 7  | Device ID 7 (MSB) |                  | R    | C9 |   | 1       |
| Bit 6  | Device ID 6       |                  | R    |    |   | 1       |
| Bit 5  | Device ID 5       |                  | R    |    |   | 0       |
| Bit 4  | Device ID 4       |                  | R    |    |   | 0       |
| Bit 3  | Device ID 3       |                  | R    |    |   | 1       |
| Bit 2  | Device ID 2       |                  | R    |    |   | 0       |
| Bit 1  | Device ID 1       |                  | R    |    |   | x       |
| Bit 0  | Device ID 0       |                  | R    |    |   | 1       |

**SMBus Table: Byte Count Register**

| Byte 7 | Name     | Control Function                                                      | Type | 0                   | 1 | Default |
|--------|----------|-----------------------------------------------------------------------|------|---------------------|---|---------|
| Bit 7  | Reserved |                                                                       |      |                     |   | 0       |
| Bit 6  | Reserved |                                                                       |      |                     |   | 0       |
| Bit 5  | Reserved |                                                                       |      |                     |   | 0       |
| Bit 4  | BC4      | Writing to this register configures how many bytes will be read back. | RW   | Default value is 7. |   | 0       |
| Bit 3  | BC3      |                                                                       | RW   |                     |   | 0       |
| Bit 2  | BC2      |                                                                       | RW   |                     |   | 1       |
| Bit 1  | BC1      |                                                                       | RW   |                     |   | 1       |
| Bit 0  | BC0      |                                                                       | RW   |                     |   | 1       |

**SMBus Table: Side-Band Mask Register (functional only when SBEN = 1)**

| Byte8 | Name  | Control Function            | Type | 0                                               | 1                                                                               | Default |
|-------|-------|-----------------------------|------|-------------------------------------------------|---------------------------------------------------------------------------------|---------|
| Bit 7 | Mask7 | Masks off Side-band Disable | RW   | Side-band shift register may disable the output | Forces output to always be enabled regardless of side-band shift register value | 0       |
| Bit 6 | Mask6 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 5 | Mask5 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 4 | Mask4 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 3 | Mask3 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 2 | Mask2 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 1 | Mask1 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 0 | Mask0 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |

**SMBus Table: Side-Band Mask Register (functional only when SBEN = 1)**

| Byte 9 | Name   | Control Function            | Type | 0                                               | 1                                                                               | Default |
|--------|--------|-----------------------------|------|-------------------------------------------------|---------------------------------------------------------------------------------|---------|
| Bit 7  | Mask15 | Masks off Side-band Disable | RW   | Side-band shift register may disable the output | Forces output to always be enabled regardless of side-band shift register value | 0       |
| Bit 6  | Mask14 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 5  | Mask13 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 4  | Mask12 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 3  | Mask11 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 2  | Mask10 | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 1  | Mask9  | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 0  | Mask8  | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |

**SMBus Table: Side-Band Mask Register (functional only when SBEN = 1)**

| Byte 10 | Name     | Control Function            | Type | 0                                               | 1                                                                               | Default |
|---------|----------|-----------------------------|------|-------------------------------------------------|---------------------------------------------------------------------------------|---------|
| Bit 7   | Reserved |                             |      |                                                 |                                                                                 | 0       |
| Bit 6   | Reserved |                             |      |                                                 |                                                                                 | 0       |
| Bit 5   | Reserved |                             |      |                                                 |                                                                                 | 0       |
| Bit 4   | Reserved |                             |      |                                                 |                                                                                 | 0       |
| Bit 3   | Mask19   | Masks off Side-band Disable | RW   | Side-band shift register may disable the output | Forces output to always be enabled regardless of side-band shift register value | 0       |
| Bit 2   | Mask18   | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 1   | Mask17   | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |
| Bit 0   | Mask16   | Masks off Side-band Disable | RW   |                                                 |                                                                                 | 0       |

**Bytes 11 through 19 are Reserved.**

SMBus Table: Amplitude Configuration Register

| Byte 20 | Name     | Control Function                   | Type | 0                                     | 1 | Default |
|---------|----------|------------------------------------|------|---------------------------------------|---|---------|
| Bit 7   | AMP[3]   | Global Differential output Control | RW   | 0.6V – 1V, 25mV/step<br>Default=800mV |   | 0       |
| Bit 6   | AMP[2]   |                                    | RW   |                                       |   | 1       |
| Bit 5   | AMP[1]   |                                    | RW   |                                       |   | 1       |
| Bit 4   | AMP[0]   |                                    | RW   |                                       |   | 1       |
| Bit 3   | Reserved |                                    |      |                                       |   | 0       |
| Bit 2   | Reserved |                                    |      |                                       |   | 1       |
| Bit 1   | Reserved |                                    |      |                                       |   | 1       |
| Bit 0   | Reserved |                                    |      |                                       |   | 1       |

SMBus Table: PD\_RESTORE

| Byte 21 | Name        | Control Function                 | Type | 0              | 1            | Default |
|---------|-------------|----------------------------------|------|----------------|--------------|---------|
| Bit 7   | Reserved    |                                  |      |                |              | 0       |
| Bit 6   | Reserved    |                                  |      |                |              | 0       |
| Bit 5   | Reserved    |                                  |      |                |              | 0       |
| Bit 4   | Reserved    |                                  |      |                |              | 0       |
| Bit 3   | PD_RESTORE# | Save Configuration in Power Down | RW   | Config Cleared | Config Saved | 1       |
| Bit 2   | Reserved    |                                  |      |                |              | 0       |
| Bit 1   | Reserved    |                                  |      |                |              | 0       |
| Bit 0   | Reserved    |                                  |      |                |              | 0       |

## 8. Application Information

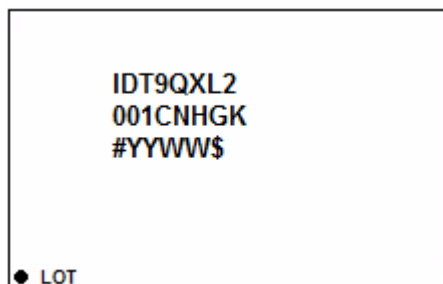
### 8.1 PCB Layout Recommendations

Proper PCB layout is critical to achieving the full functionality and efficiency of the device. For more information pertaining to optimal electrical performance, effective thermal management, and overall system reliability, see [layout recommendations](#).

## 9. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

## 10. Marking Diagram



- Lines 1 and 2: part number
  - “K” denotes temperature rating.
- Line 3:
  - “#” denotes the stepping number.
  - “YYWW” is the last digits of the year and work week that the part was assembled.
  - “\$” denotes mark code.
- “LOT” denotes the lot sequence code.

## 11. Ordering Information

| Part Number [1][2]   | Package Description                       | Carrier Type                                                     | Temperature Range |
|----------------------|-------------------------------------------|------------------------------------------------------------------|-------------------|
| 9QXL2001CNHGK        | 6.00 × 6.00 mm, 0.50mm pitch<br>80-VFQFPN | Tray                                                             | -40° to +105°C    |
| 9QXL2001CNHGK8       | 6.00 × 6.00 mm, 0.50mm pitch<br>80-VFQFPN | Tape and Reel                                                    | -40° to +105°C    |
| 9QXL2001CNHGK/n [3]  | 6.00 × 6.00 mm, 0.50mm pitch<br>80-VFQFPN | Tray                                                             | -40° to +105°C    |
| 9QXL2001CNHGK8/n [3] | 6.00 × 6.00 mm, 0.50mm pitch<br>80-VFQFPN | Tape and Reel                                                    | -40° to +105°C    |
| 9QXL2001CNHGK8/W     | 6.00 × 6.00 mm, 0.50mm pitch<br>80-VFQFPN | Tape and Reel, Pin 1<br>Orientation: EIA-481-D<br>(see Table 19) | -40° to +105°C    |

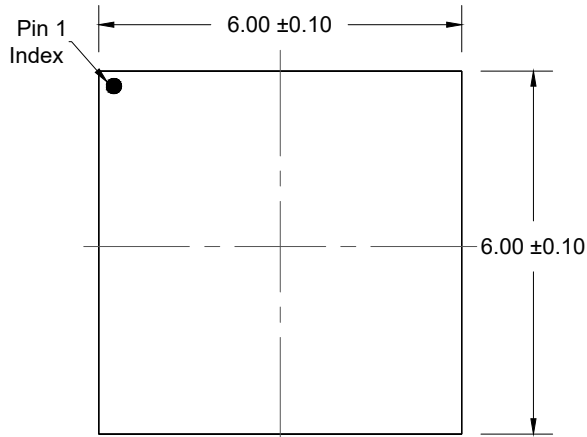
1. “C” is the device revision designator (will not correlate with the datasheet revision).
2. “G” designates PB-free configuration, RoHS compliant.
3. “n” is an alphanumeric character for specific customer requests or tracking.

Table 19. Pin 1 Orientation in Tape and Reel Packaging

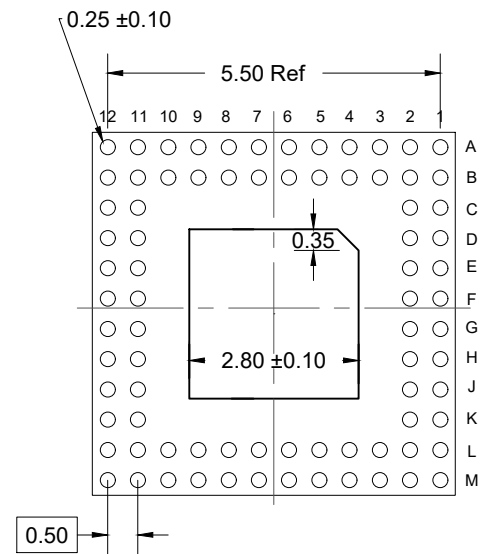
| Part Number Suffix | Pin 1 Orientation      | Illustration |
|--------------------|------------------------|--------------|
| 8                  | Quadrant 1 (EIA-481-C) |              |
| /W                 | Quadrant 2 (EIA-481-D) |              |

## 12. Revision History

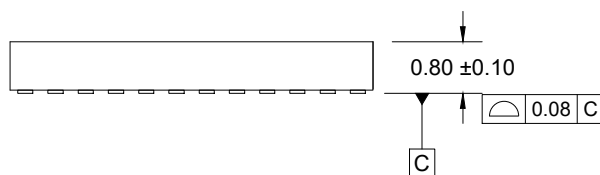
| Revision | Date         | Description                                                                                                                                                                                                                                                                                          |
|----------|--------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 1.13     | Sep 22, 2026 | <ul style="list-style-type: none"> <li>Added PCIe Gen7 specifications on front page under <a href="#">Key Specifications</a>.</li> <li>Updated PCIe Gen5 and Gen 6 maximum values in <a href="#">Table 11</a>.</li> </ul>                                                                            |
| 1.12     | Sep 11, 2026 | Corrected PCIe data due to calculation changes.                                                                                                                                                                                                                                                      |
| 1.11     | Jun 20, 2025 | Added <a href="#">Application Information</a> section.                                                                                                                                                                                                                                               |
| 1.10     | Jan 14, 2025 | Added Output Impedance parameter to <a href="#">Table 8</a> .                                                                                                                                                                                                                                        |
| 1.09     | Sep 27, 2024 | Updated <a href="#">Table 13</a> .                                                                                                                                                                                                                                                                   |
| 1.08     | Jul 30, 2024 | Changed POD nomenclature to 80-VFQFPN from 80-GQFN in <a href="#">Ordering Information</a> .                                                                                                                                                                                                         |
| 1.07     | Sep 27, 2023 | Reformatted to the latest template.                                                                                                                                                                                                                                                                  |
| -        | Jul 19, 2023 | <ul style="list-style-type: none"> <li>Updated Clk Stabilization and Tdrive_PD# values in <a href="#">Table 6</a>.</li> <li>Updated Maximum/Minimum Voltage and Slew Rate values in <a href="#">Table 8</a>.</li> <li>Updated Operating Supply Current values in <a href="#">Table 9</a>.</li> </ul> |
| -        | May 19, 2023 | <ul style="list-style-type: none"> <li>Added 9QXL2001CNHGK8/W part number in <a href="#">Ordering Information</a>.</li> <li>Added <a href="#">Table 19</a>.</li> </ul>                                                                                                                               |
| -        | Oct 6, 2022  | Added 9QXL2001CNHGK/n and 9QXL2001CNHGK8/n to <a href="#">Ordering Information</a> .                                                                                                                                                                                                                 |
| -        | Apr 8, 2022  | Added <a href="#">Signal Types</a> table and updated <a href="#">Pin Descriptions</a> table with latest nomenclature.                                                                                                                                                                                |
| -        | Nov 9, 2021  | Updated with characterization data; move to final.                                                                                                                                                                                                                                                   |
| -        | Jul 19, 2023 | <ul style="list-style-type: none"> <li>Updated Clk Stabilization and Tdrive_PD# values in <a href="#">Table 6</a>.</li> <li>Updated Maximum/Minimum Voltage and Slew Rate values in <a href="#">Table 8</a>.</li> <li>Updated Operating Supply Current values in <a href="#">Table 9</a>.</li> </ul> |
| -        | Oct 4, 2021  | Initial release.                                                                                                                                                                                                                                                                                     |



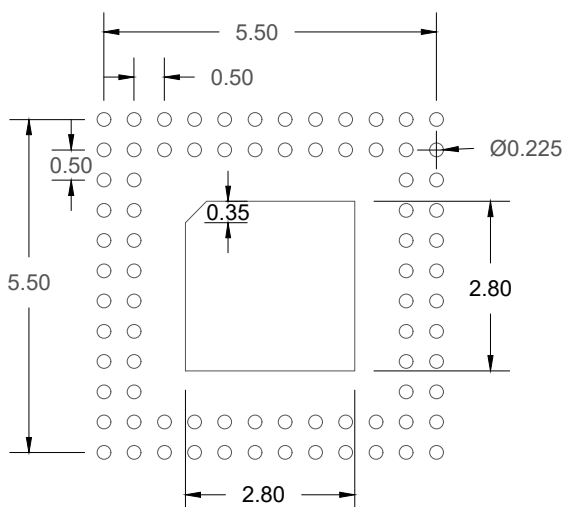
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

(PCB Top View, NSMD Design)

## NOTES:

1. JEDEC compatible
2. All dimensions are in mm and angles are in degrees
3. Use  $\pm 0.05$  mm tolerance for all other dimensions
4. Numbers in ( ) are for reference only

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