ICS9LPRS535
Datasheet

48-pin CK505 for Intel Systems

Recommended Application:
48-pin Low Cost CK505 w/fully integrated VREG and series resistors on differential outputs

Output Features:
- Integrated Series Resistors on differential outputs
- 2 - CPU differential push-pull pairs
- 4 - SRC differential push-pull pairs
- 1 - CPU/SRC selectable differential push-pull pair
- 1 - SRC/DOT selectable differential push-pull pair
- 1- SRC/Stop_Inputs selectable differential push-pull pair
- 1 - 25MHz SE1 output for Wake-on-Lan applications
- 3 - PCI, 33MHz
- 1 - USB, 48MHz
- 1 - REF, 14.31818MHz

Key Specifications:
- CPU outputs cycle-cycle jitter < 85ps
- SRC output cycle-cycle jitter < 125ps
- PCI outputs cycle-cycle jitter < 250ps
- +/-100ppm frequency accuracy on all clocks

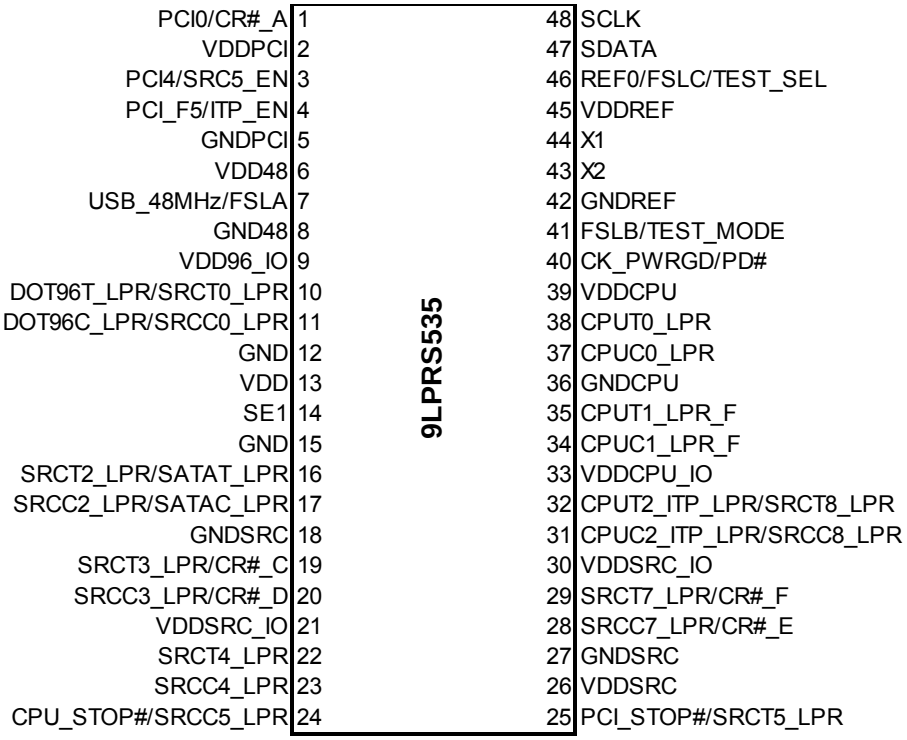
Features/Benefits:
- Supports spread spectrum modulation, default is 0.5% down spread
- Uses external 14.318MHz crystal, external crystal load caps are required for frequency tuning

Table 1: CPU Frequency Select Table

FS_LC^2 B0b7	FS_LB^1 B0b6	FS_LA^1 B0b5	CPU MHz	SRC MHz	PCI MHz	REF MHz	USB MHz	DOT MHz
0	0	0	266.66	100.00	33.33	14.318	48.00	96.00
0	0	1	133.33					
0	1	0	200.00					
0	1	1	166.66					
1	0	0	333.33					
1	0	1	100.00					
1	1	0	400.00					
1	1	1	Reserved					

1. FS_LA and FS_LB are low-threshold inputs.Please see V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values. Also refer to the Test Clarification Table.
2. FS_LC is a three-level input. Please see the V_{IL_FS} and V_{IH_FS} specifications in the Input/Supply/Common Output Parameters Table for correct values.

Pin Configuration



48-SSOP/TSSOP

* Internal Pull-Up Resistor

** Internal Pull-Down Resistor

1461A—07/28/09

SSOP/TSSOP Pin Description

PIN #	PIN NAME	TYPE	DESCRIPTION
1	PCI0/CR#_A	I/O	3.3V PCI clock output or CR#_A input. Default is PCI0. To configure this pin as CR#_A, the PCI output must first be disabled in Byte 2, bit 0. Byte 5, bit 7: 0 = PCI0 enabled (default), 1= CR#_A enabled. Byte 5, bit 6: 0 = CR#_A controls SRC0 (default), 1= CR#_A# controls SRC2.
2	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
3	PCI4/SRC5_EN	I/O	3.3V PCI clock output / SRC5 enable strap. On powerup, the logic value on this pin determines if SRC5 or CPU_STOP#/PCI_STOP# is enabled. The latched value controls the pin function as follows 0 = PCI_STOP#/CPU_STOP# 1 = SRC5/SRC5#
4	PCI_F5/ITP_EN	I/O	Free running PCI clock output and ITP/SRC8 enable strap. This output is not affected by the state of the PCI_STOP# pin. On powerup, the state of this pin determines whether pins 38 and 39 are an ITP or SRC pair. 0 =SRC8/SRC8# 1 = ITP/ITP#
5	GNDPCI	PWR	Ground pin for the PCI outputs
6	VDD48	PWR	Power pin for the 48MHz output.3.3V
7	USB_48MHz/FSLA	I/O	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. / Fixed 48MHz USB clock output. 3.3V.
8	GND48	PWR	Ground pin for the 48MHz outputs
9	VDD96_IO	PWR	Power pin for the DOT96 clocks, nominal 1.05V to 3.3V.
10	DOT96T_LPR/SRCT0_LPR	OUT	True clock of push-pull SRC or DOT96 with integrated series resistor. No 50 ohm pull down needed. Default is SRCT0. After powerup, this pin function may be changed to DOT96T via SMBus Byte 1, bit 7 as follows: 0= SRC0T 1=DOT96T
11	DOT96C_LPR/SRCC0_LPR	OUT	Complementary clock of push-pull SRC or DOT96 with integrated series resistor. No 50 ohm pull down needed. Default is SRC0C. After powerup, this pin function may be changed to DOT96C via SMBus Byte 1, bit 7 as follows: 0= SRC0C 1=DOT96C
12	GND	PWR	Ground pin.
13	VDD	PWR	Power supply, nominal 3.3V
14	SE1	OUT	CK505 Singled Ended Output 1. 3.3V.
15	GND	PWR	Ground pin.
16	SRCT2_LPR/SATAT_LPR	OUT	True clock of differential 0.8V push-pull SRC/SATA output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
17	SRCC2_LPR/SATAC_LPR	OUT	Complementary clock of differential 0.8V push-pull SRC/SATA output with integrated 33ohm series resistor. No 50ohm resistor to GND needed.
18	GNDSRC	PWR	Ground pin for the SRC outputs
19	SRCT3_LPR/CR#_C	I/O	True clock of push-pull SRC output with int. 33ohm series resistor/CR#_C input. Disable SRC3 via Byte 4, bit 7, before using as CR#_C. Byte 5, bit 3: 0=SRC3 (default), 1=CR#_C. Byte 5, bit 2: 0=CR#_C controls SRC0 (default), 1=CR#_C controls SRC2
20	SRCC3_LPR/CR#_D	I/O	Complementary clock of push-pull SRC output with int. 33ohm series resistor/CR#_D input. Disable SRC3 via Byte 4, bit 7, before using as CR#_D. Byte 5, bit 1: 0=SRC3 (default),1=CR#_D. Byte 5, bit 0: 0=CR#_D controls N/A (default), 1=CR#_D controls SRC4
21	VDDSRC_IO	PWR	1.05V to 3.3V from external power supply
22	SRCT4_LPR	OUT	True clock of push-pull SRC output with int. 33ohm series resistor.
23	SRCC4_LPR	OUT	Complementary clock of push-pull SRC output with int. 33ohm series resistor.
24	CPU_STOP#/SRCC5_LPR	I/O	Stops all CPUCLK, except those set to be free running clocks / Complementary clock of push-pull SRC pair with int. 33ohm series resistor.

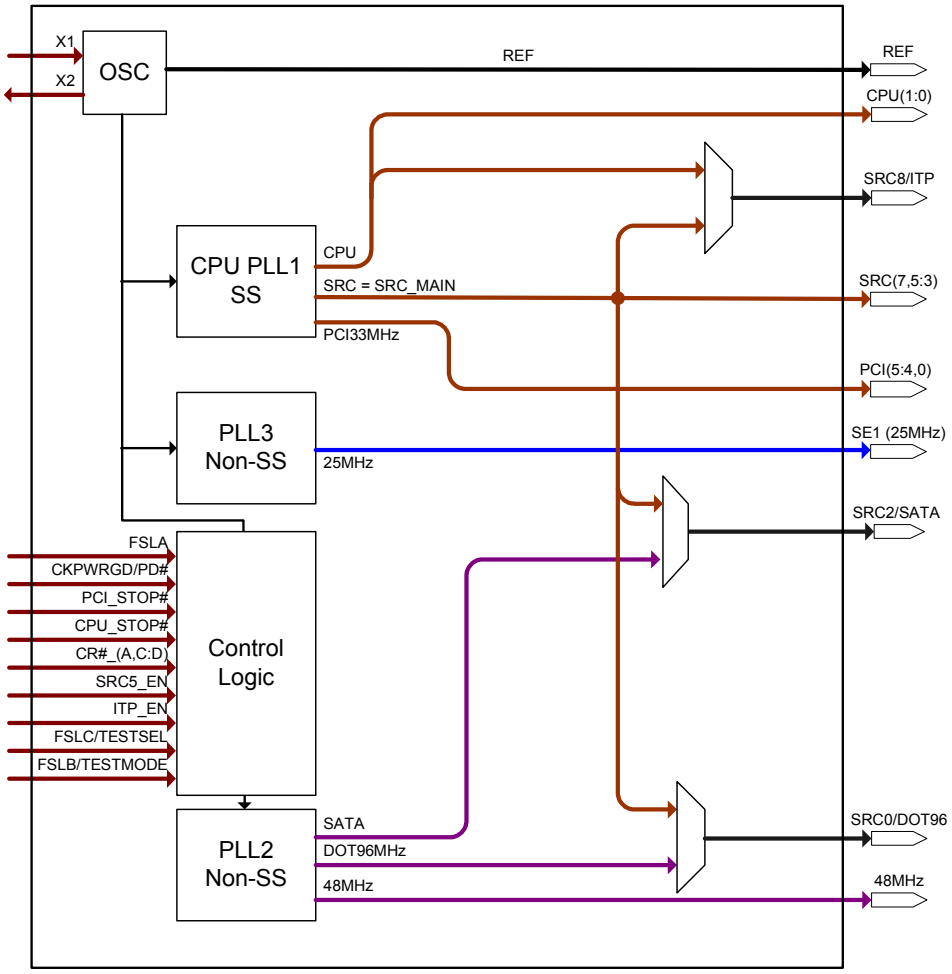
SSOP/TSSOP Pin Description (Continued)

25	PCI_STOP#/SRCT5_LPR	I/O	Stops all PCICLKs at logic 0 level, when low. Can also stop SRC clocks. Free running PCICLKs are not effected by this input. / True clock of push-pull SRC pair with int. 33ohm series resistor.
26	VDDSRC	PWR	Supply for SRC clocks, 3.3V nominal
27	GNDSRC	PWR	Ground pin for the SRC outputs
28	SRCC7_LPR/CR#_E	I/O	Complementary clock of push-pull SRC output with int. 33ohm series resistor/CR#_E input. Disable SRC7 via Byte 3, bit 3 before using as CR#_E. Byte 6, bit 7: 0=SRC7 (default), 1=CR#_E Outputs controlled by CR#_E are not present on this device
29	SRCT7_LPR/CR#_F	I/O	True clock of push-pull SRC output with int. 33 ohm series resistor/CR#_F input. Disable SRC7 via Byte 3, bit 3 before using CR#_F. Byte 6, bit 6: 0 = SRC7 (default),1 = CR#_F enabled to control SRC8.
30	VDDSRC_IO	PWR	1.05V to 3.3V from external power supply
31	CPUC2_ITP_LPR/SRCC8_LPR	OUT	Complementary clock of low power differential CPU2_ITP/SRC pair. No Rs needed. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8# 1 = ITP#
32	CPUT2_ITP_LPR/SRCT8_LPR	OUT	True clock of low power differential CPU2_ITP/SRC8 pair. No Rs needed. The function of this pin is determined by the latched input value on pin 7, PCIF5/ITP_EN on powerup. The function is as follows: Pin 7 latched input Value 0 = SRC8 1 = ITP
33	VDDCPU_IO	PWR	1.05V to 3.3V from external power supply
34	CPUC1_LPR_F	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. Free running during iAMT. No 50ohm resistor to GND needed.
35	CPUT1_LPR_F	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. Free running during iAMT No 50 ohm resistor to GND needed.
36	GNDCPU	PWR	Ground pin for the CPU outputs
37	CPUC0_LPR	OUT	Complementary clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
38	CPUT0_LPR	OUT	True clock of differential pair 0.8V push-pull CPU outputs with integrated 33ohm series resistor. No 50 ohm resistor to GND needed.
39	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
40	CK_PWRGD/PD#	IN	Notifies CK505 to sample latched inputs, or iAMT entry/exit, or PWRDWN# mode
41	FSLB/TEST_MODE	IN	3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. TEST_MODE is a real time input to select between Hi-Z and REF/N divider mode while in test mode. Refer to Test Clarification Table.
42	GNDREF	PWR	Ground pin for the REF outputs.
43	X2	OUT	Crystal output, Nominally 14.318MHz
44	X1	IN	Crystal input, Nominally 14.318MHz.
45	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
46	REF0/FSLC/TEST_SEL	I/O	14.318 MHz reference clock./ 3.3V tolerant input for CPU frequency selection. Refer to input electrical characteristics for Vil_FS and Vih_FS values. /TEST_Sel: 3-level latched input to enable test mode. Refer to Test Clarification Table
47	SDATA	I/O	Data pin for SMBus circuitry, 3.3V tolerant.
48	SCLK	IN	Clock pin of SMBus circuitry, 5V tolerant.

General Description

ICS9LPRS535 is compliant to the Intel CK505 Yellow Cover specification. This clock synthesizer provides a single chip solution for Intel desktop chipsets. **ICS9LPRS535** is driven with a 14.318MHz crystal. It also provides a tight ppm accuracy output for Serial ATA and PCI-Express support.

Block Diagram



Power Groups

Pin Number		Description
VDD	GND	
33	36	CPU Outputs
39	36	CPU/SRC Analog
30, 21	18, 27	SRC Outputs
13	15	PLL3 25MHz
9	12	DOT96 outputs
6	8	USB 48 Output/Analog
45	42	Xtal, REF
2	5	PCI outputs

Absolute Maximum Ratings - DC Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Maximum Supply Voltage	VDDxxx	Supply Voltage		4.6	V	7
Maximum Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply		3.8	V	7
Maximum Input Voltage	V_{IH}	3.3V Inputs		4.6	V	4,5,7
Minimum Input Voltage	V_{IL}	Any Input	GND - 0.5		V	4,7
Storage Temperature	Ts	-	-65	150	°C	4,7
Input ESD protection	ESD prot	Human Body Model	2000		V	6,7

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Operation under these conditions is neither implied, nor guaranteed.

[3] Maximum input voltage is not to exceed VDD

AC Electrical Characteristics - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Rising Edge Slew Rate	tSLR	Averaging on	2.5	4	V/ns	2, 3
Falling Edge Slew Rate	tFLR	Averaging on	2.5	4	V/ns	2, 3
Slew Rate Variation	tSLVAR	Averaging on		20	%	1, 10
Differential Voltage Swing	VSWING	Averaging off	300		mV	2
Crossing Point Voltage	VXABS	Averaging off	300	550	mV	1,4,5
Crossing Point Variation	VXABSVAR	Averaging off		140	mV	1,4,9
Maximum Output Voltage	VHIGH	Averaging off		1150	mV	1,7
Minimum Output Voltage	VLOW	Averaging off	-300		mV	1,8
Duty Cycle	DCYC	Averaging on	45	55	%	2
CPU[1:0] Skew	CPUSKEW10	Differential Measurement		100	ps	1
CPU[2_ITP:0] Skew	CPUSKEW20	Differential Measurement		150	ps	1
SRC[10:0] Skew	SRCSKEW	Differential Measurement		3000	ps	1,6,11

NOTES on DIF Output AC Specs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]Measurement taken for single ended waveform on a component test board (not in system)

[2] Measurement taken from differential waveform on a component test board. (not in system)

[3] Slew rate emastured through V_swing voltage range centered about differential zero

[4] Vcross is defined at the voltage where Clock = Clock#, measured on a component test board (not in system)

[5] Only applies to the differential rising edge (Clock rising, Clock# falling)

[6] Total distributed intentional SRC to SRC skew. PCIE Gen2 outputs (SRC3, 4, 6 and 7) will have 0 nominal skew. Maximum allowable interpair skew is 150 ps.

[7] The max voltage including overshoot.

[8] The min voltage including undershoot.

[9] The total variation of all Vcross measurements in any particular system. Note this is a subset of V_cross min/mas (V_Cross absolute) allowed. The intent is to limit Vcross

[10] Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a +/-75mV window centered on the average cross point where Clock rising

[11] For PCIe Gen2 compliant devices, SRC 3, 4, 6, and 7 will have 0 ps nominal skew.

Electrical Characteristics - PCICLK/PCICLK_F

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	1,2
Clock period	T_{period}	33.33MHz output no spread	29.99700	30.00300	ns	2
		33.33MHz output spread	30.08421	30.23459	ns	2
Absolute min/max period	T_{abs}	33.33MHz output no spread	29.49700	30.50300	ns	2
		33.33MHz output nominal/spread	29.56617	30.58421	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.55	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33		mA	1
		V_{OH}@MAX = 3.135 V		-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30		mA	1
		V_{OL} @ MAX = 0.4 V		38	mA	1
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Pin to Pin Skew	t_{skew}	V_T = 1.5 V		250	ps	2
Intential PCI to PCI delay	t_{skew}	V_T = 1.5 V	100	200	ps	2
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	2
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		500	ps	2

Electrical Characteristics - Input/Supply/Common Output DC Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Ambient Operating Temp	Tambient	-	0	70	°C	
Supply Voltage	VDDxxx	Supply Voltage	3.135	3.465	V	
Supply Voltage	VDDxxx_IO	Low-Voltage Differential I/O Supply	0.9975	3.465	V	10
Input High Voltage	V_{IHSE}	Single-ended 3.3V inputs	2	V_{DD} + 0.3	V	3
Input Low Voltage	V_{ILSE}	Single-ended 3.3V inputs	V_{SS} - 0.3	0.8	V	3
Low Threshold Input- High Voltage	$V_{IH\_FS\_TEST}$	3.3 V +/-5%	2	VDD + 0.3	V	8
Low Threshold Input- FSC = '1' Voltage	$V_{IH\_FS\_FSC}$	3.3 V +/-5%	0.7	1.5	V	8
Low Threshold Input- FSA,FSB = '1' Voltage	$V_{IH\_FS\_FSAB}$	3.3 V +/-5%	0.7	VDD+0.3	V	
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3	0.35	V	
Input Leakage Current	I_{IN}	$V_{IN} = V_{DD}$, V_{IN} = GND	-5	5	uA	2
Input Leakage Current	I_{INRES}	Inputs with pull up or pull down resistors $V_{IN} = V_{DD}$, V_{IN} = GND	-200	200	uA	
Output High Voltage	V_{OHSE}	Single-ended outputs, I_{OH} = -1mA	2.4		V	1
Output Low Voltage	V_{OLSE}	Single-ended outputs, I_{OL} = 1 mA		0.4	V	1
Operating Supply Current	$I_{DDOP3.3}$	Full Active, C_L = Full load; Idd 3.3V		125	mA	
	I_{DDOPIO}	Full Active, C_L = Full load; IDD IO		50	mA	10
iAMT Mode Current	$I_{DDiAMT3.3}$	M1 mode, 3.3V Rail		40	mA	
	$I_{DDiAMTIO}$	M1 Mode, IO Rail		10	mA	
Powerdown Current	$I_{DDPD3.3}$	Power down mode, 3.3V Rail		5	mA	
	I_{DDPDIO}	Power down mode, IO Rail		0.1	mA	10
Input Frequency	F_i	V_{DD} = 3.3 V		15	MHz	
Pin Inductance	L_{pin}			7	nH	
Input Capacitance	C_{IN}	Logic Inputs	1.5	5	pF	
	C_{OUT}	Output pin capacitance		6	pF	
	C_{INX}	X1 & X2 pins		6	pF	
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock		1.8	ms	
Tdrive_CR_off	$T_{DRCROFF}$	Output stop after CR deasserted		400	ns	
Tdrive_CR_on	T_{DRCRON}	Output run after CR asserted		0	us	
Tdrive_CPU	T_{DRSRC}	CPU output enable after PCI_STOP# de-assertion		10	ns	
Tfall_SE	T_{FALL}	Fall/rise time of all 3.3V control inputs from 20-80%		10	ns	
Trise_SE	T_{RISE}			10	ns	
SMBus Voltage	V_{DD}		2.7	5.5	V	
Low-level Output Voltage	V_{OLSMB}	@ I_{PULLUP}		0.4	V	
Current sinking at V_{OLSMB} = 0.4 V	I_{PULLUP}	SMB Data Pin	4		mA	
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)		1000	ns	
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)		300	ns	
Maximum SMBus Operating Frequency	F_{SMBUS}			100	kHz	
Spread Spectrum Modulation Frequency	f_{SSMOD}	Triangular Modulation	30	33	kHz	

NOTES on Input/Supply/Common Output DC Parameters: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1] Signal is required to be monotonic in this region.

[2] input leakage current does not include inputs with pull-up or pull-down resistors

[3] 3.3V referenced inputs are: PCI_STOP#, CPU_STOP#, TME, SRC5_EN, ITP_EN, SCLKL, SDATA, TESTMODE, TESTSEL, CKPWRGD and CR# inputs if selected.

[4] Intentionally blank

[5] Maximum VIH is not to exceed VDD

[6] Human Body Model

[7] Operation under these conditions is neither implied, nor guaranteed.

[8] Frequency Select pins which have tri-level input

[9] PCI3/CFG0 is optional

[10] If present. Not all parts have this feature.

Electrical Characteristics - USB48MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	2,4
Clock period	T_{period}	48.00MHz output nominal	20.83125	20.83542	ns	2,3
Absolute min/max period	T_{abs}	48.00MHz output nominal	20.48125	21.18542	ns	2
CLK High Time	T_{HIGH}		8.216563	11.15198	V	
CLK Low time	T_{LOW}		7.816563	10.95198	V	
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4		V	
Output Low Voltage	V_{OL}	I_{OL} = 1 mA		0.55	V	
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29		mA	
		V_{OH}@MAX = 3.135 V		-23	mA	
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29		mA	
		V_{OL} @ MAX = 0.4 V		27	mA	
Rising Edge Slew Rate	t_{SLR}	Measured from 0.8 to 2.0 V	1	2	V/ns	1
Falling Edge Slew Rate	t_{FLR}	Measured from 2.0 to 0.8 V	1	2	V/ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	55	%	2
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		350	ps	2

Electrical Characteristics - REF-14.318MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-100	100	ppm	2, 4
Clock period	Tperiod	14.318MHz output nominal	69.82033	69.86224	ns	2, 3
Absolute min/max period	Tabs	14.318MHz output nominal	69.83400	70.84800	ns	2
CLK High Time	THIGH		29.97543	38.46654	V	
CLK Low time	TLOW		29.57543	38.26654	V	
Output High Voltage	VOH	IOH = -1 mA	2.4		V	
Output Low Voltage	VOL	IOL = 1 mA		0.4	V	
Output High Current	IOH	VOH @MIN = 1.0 V, VOH@MAX = 3.135 V	-33	-33	mA	
Output Low Current	IOL	VOL @MIN = 1.95 V, VOL @MAX = 0.4 V	30	38	mA	
Rising Edge Slew Rate	tSLR	Measured from 0.8 to 2.0 V	1	4	V/ns	1
Falling Edge Slew Rate	tFLR	Measured from 2.0 to 0.8 V	1	4	V/ns	1
Duty Cycle	dt1	VT = 1.5 V	45	55	%	2
Jitter, Cycle to cycle	tjcyc-cyc	VT = 1.5 V		1000	ps	2

NOTES on SE outputs: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]Edge rate in system is measured from 0.8V to 2.0V.

[2] Duty cycle, Peroid and Jitter are measured with respect to 1.5V

[3] The average period over any 1us period of time

[4] Using frequency counter with the measurment interval equal or greater that 0.15s, target frequencies are 14.318180 MHz, 33.333333MHz and 48.000000MHz

Clock Jitter Specs - Low Power Differential Outputs

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS	NOTES
CPU Jitter - Cycle to Cycle	CPUJC2C	Differential Measurement		85	ps	1
SRC Jitter - Cycle to Cycle	SRCJC2C	Differential Measurement		125	ps	1,2
DOT Jitter - Cycle to Cycle	DOTJC2C	Differential Measurement		250	ps	1

NOTES on DIF Output Jitter: (unless otherwise noted, guaranteed by design and characterization, not 100% tested in production).

[1]JItter specs are specified as measured on a clock characterization board. System designers need to take special care not to use these numbers, as the in-system performance will be somewhat degraded. The receiver EMTS (chispet or CPU) will have the rece

[2] Phase jitter requirement: The deisgnated Ge2 outputs will meet the reference clock jitter requiremernts from the PCI Express Gen2 Base Spec. The test is performed on a componnet test board under quiet conditttions with all outputs on. Jitter analysis is performed using a standardized tool provided by the PCI SIG or equivalent. Measurement methodology is as defined by the PCI SIG.

Table 2: PLL3 Quick Configuration (Read Only)

B1b4	B1b3	B1b2	B1b1	Pin 14	Spread	Comment
				MHz	%	
0	0	0	0	**N/A**	**N/A**	**N/A**
0	0	0	1	**N/A**	**N/A**	**N/A**
0	0	1	0	**N/A**	**N/A**	**N/A**
0	0	1	1	**N/A**	**N/A**	**N/A**
0	1	0	0	**N/A**	**N/A**	**N/A**
0	1	0	1	**N/A**	**N/A**	**N/A**
0	1	1	0	**N/A**	**N/A**	**N/A**
0	1	1	1	**N/A**	**N/A**	**N/A**
1	0	0	0	**N/A**	**N/A**	**N/A**
1	0	0	1	**N/A**	**N/A**	**N/A**
1	0	1	0	**N/A**	**N/A**	**N/A**
1	0	1	1	**N/A**	**N/A**	**N/A**
1	**1**	**0**	**0**	25.000	None	25Mhz on SE1
1	1	0	1	**N/A**	**N/A**	**N/A**
1	1	1	0	**N/A**	**N/A**	**N/A**
1	1	1	1	**N/A**	**N/A**	**N/A**

Table 3: Vswing Select Table

B9b2	B9b1	B9b0	Vswing
0	0	0	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V
1	1	0	0.9V
1	1	1	1.0V

Table 4: Device ID table

B8b7	B8b6	B8b5	B8b4	Comment
0	**1**	**1**	**0**	**48 SSOP/TSSOP**

PCI_STOP# Power Management

		Single-ended Clocks		Differential Clocks (Except CPU)	
SMBus OE Bit	**PCI_STOP#**	**Stoppable**	**Free running**	**Stoppable**	**Free running**
Enable	**1**	Running	Running	Running	Running
	0	Low	Running	CK= High CK# = Low	Running
Disable	**X**	Low		CK= Pull down, CK# = Low	

CPU_STOP# Power Management

		CPU Clocks	
SMBus OE Bit	**CPU_STOP#**	**Stoppable**	**Free running**
Enable	**1**	Running	Running
	0	CK= High CK# = Low	Running
Disable	**X**	Low	

CR# Power Management

		Differential Clocks (Except CPU)	
SMBus OE Bit	**CR#**	**CR# controlled**	**Free running**
Enable	**1**	Running	Running
	0	CK= Pull down, CK# = Low	
Disable	**X**	CK = Pull down, CK# = Low	

PD# Power Management

	Single-ended Clocks (Except SE1)		SE1 w/B11b5 = 0	SE1 w/B11b5 = 1	Differential Clocks (Except CPU1)	CPU1
Device State	w/o Latched input	w/Latched input				
Latches Open	Low	Hi-Z	Low	Low	CK= Pull down, CK# = Low	CK= Pull down, CK# = Low
Power Down				25MHz	CK= Pull down CK# = Low	CK= Pull down CK# = Low
M1				25MHz	CK= Pull down CK# = Low	Running
Virtual Power Cycle to Latches Open				25MHz	CK= Pull down, CK# = Low	CK= Pull down, CK# = Low

General SMBus serial interface information for the ICS9LPRS535

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D2 $_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D3 $_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X$_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2$_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
Data Byte Count = X		
		ACK
Beginning Byte N	X Byte	
		ACK
O		
O		O
O		O
		O
Byte N + X - 1		
		ACK
P	stoP bit	

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)
T	starT bit	
Slave Address D2$_{(H)}$		
WR	WRite	
		ACK
Beginning Byte = N		
		ACK
RT	Repeat starT	
Slave Address D3$_{(H)}$		
RD	ReaD	
		ACK
		Data Byte Count = X
ACK		
	X Byte	Beginning Byte N
ACK		
		O
O		O
O		O
O		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

Byte 0 FS Readback and PLL Selection Register

Bit	Pin	Name	Description	Type	0	1	Default
7	-	FSLC	CPU Freq. Sel. Bit (Most Significant)	R	See Table 1 : CPU Frequency Select Table		Latch
6	-	FSLB	CPU Freq. Sel. Bit	R			Latch
5	-	FSLA	CPU Freq. Sel. Bit (Least Significant)	R			Latch
4	-	iAMT_EN	Set via SMBus or dynamically by CK505 if detects dynamic M1	RW	Legacy Mode	iAMT Enabled	0
3		Reserved	Reserved	RW			0
2	-	SRC_Main_SEL	Select source for SRC Main	R	SRC Main = PLL1	SRC Main = PLL3	0
1	-	SATA_SEL	Select source for SATA clock	RW	SATA = SRC_Main	SATA = PLL2	0
0	-	PD_Restore	1 = on Power Down de-assert return to last known state 0 = clear all SMBus configurations as if cold power-on and go to latches open state This bit is ignored and treated at '1' if device is in iAMT mode.	RW	Configuration Not Saved	Configuration Saved	1

Byte 1 DOT96 Select and PLL3 Quick Config Register

Bit	Pin	Name	Description	Type	0	1	Default
7	13/14	SRC0_SEL	Select SRC0 or DOT96	RW	SRC0	DOT96	0
6	-	PLL1_SSC_SEL	Select 0.5% down or center SSC	RW	Down spread	Center spread	0
5		Reserved	Reserved	RW			1
4		PLL3_CF3	PLL3 Quick Config Bit 3	R	25MHz from PLL3 Quick Config		1
3		PLL3_CF2	PLL3 Quick Config Bit 2	R			1
2		PLL3_CF1	PLL3 Quick Config Bit 1	R			0
1		PLL3_CF0	PLL3 Quick Config Bit 0	R			0
0		PCI_SEL	PCI_SEL	R	PCI from PLL1	PCI from SRC_MAIN	1

Byte 2 Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		REF_OE	Output enable for REF, if disabled output is tri-stated	RW	Output Disabled	Output Enabled	1
6		USB_OE	Output enable for USB	RW	Output Disabled	Output Enabled	1
5		PCIF5_OE	Output enable for PCI5	RW	Output Disabled	Output Enabled	1
4		PCI4_OE	Output enable for PCI4	RW	Output Disabled	Output Enabled	1
3		Reserved	Reserved	RW			1
2		Reserved	Reserved	RW			1
1		Reserved	Reserved	RW			1
0		PCI0_OE	Output enable for PCI0	RW	Output Disabled	Output Enabled	1

Byte 3 Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW			1
6		Reserved	Reserved	RW			1
5		Reserved	Reserved	RW			1
4		SRC8/ITP_OE	Output enable for SRC8 or ITP	RW	Output Disabled	Output Enabled	1
3		SRC7_OE	Output enable for SRC7	RW	Output Disabled	Output Enabled	1
2		Reserved	Reserved	RW			1
1		SRC5_OE	Output enable for SRC5	RW	Output Disabled	Output Enabled	1
0		SRC4_OE	Output enable for SRC4	RW	Output Disabled	Output Enabled	1

Byte 4 Output Enable and Spread Spectrum Disable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		SRC3_OE	Output enable for SRC3	RW	Output Disabled	Output Enabled	1
6		SATA/SRC2_OE	Output enable for SATA/SRC2	RW	Output Disabled	Output Enabled	1
5		Reserved	Reserved	RW			0
4		SRC0/DOT96_OE	Output enable for SRC0/DOT96	RW	Output Disabled	Output Enabled	1
3		CPU1_OE	Output enable for CPU1	RW	Output Disabled	Output Enabled	1
2		CPU0_OE	Output enable for CPU0	RW	Output Disabled	Output Enabled	1
1		PLL1_SSC_ON	Enable PLL1's spread modulation	RW	Spread Disabled	Spread Enabled	1
0		Reserved	Reserved	RW			0

Byte 5 Clock Request Enable/Configuration Register

Bit	Pin	Name	Description	Type	0	1	Default
7		CR#_A_EN	Enable CR#_A (clk req), PCI0_OE must be = 1 for this bit to take effect	RW	Disable CR#_A	Enable CR#_A	0
6		CR#_A_SEL	Sets CR#_A to control either SRC0 or SRC2	RW	CR#_A -> SRC0	CR#_A -> SRC2	0
5		Reserved	Reserved	RW			0
4		Reserved	Reserved	RW			0
3		CR#_C_EN	Enable CR#_C (clk req)	RW	Disable CR#_C	Enable CR#_C	0
2		CR#_C_SEL	Sets CR#_C -> SRC0 or SRC2	RW	CR#_C -> SRC0	CR#_C -> SRC2	0
1		CR#_D_EN	Enable CR#_D (clk req)	RW	Disable CR#_D	Enable CR#_D	0
0		CR#_D_SEL	Sets CR#_D -> SRC1 or SRC4	RW	NA, SRC1 not present	CR#_D -> SRC4	0

Byte 6 Clock Request Enable/Configuration and Stop Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW			0
6		CR#_F_EN	Enable CR#_F (clk req) -> SRC8	RW	Disable CR#_F	Enable CR#_F	0
5		Reserved	Reserved	RW			0
4		Reserved	Reserved	RW			0
3		Reserved	Reserved	RW			0
2		Reserved	Reserved	RW			0
1		Reserved	Reserved	RW			0
0		SRC_STP_CRTL	If set, SRCs (except SRC1) stop with PCI_STOP#	RW	Free Running	Stops with PCI_STOP# assertion	0

Byte 7 Vendor ID/ Revision ID

Bit	Pin	Name	Description	Type	0	1	Default
7		Rev Code Bit 3	Revision ID Rev B = 0001 Rev C = 0010	R	B rev = 0001 C rev = 0010		X
6		Rev Code Bit 2		R			X
5		Rev Code Bit 1		R			X
4		Rev Code Bit 0		R			X
3		Vendor ID bit 3	Vendor ID ICS is 0001, binary	R	ICS is 0001		0
2		Vendor ID bit 2		R			0
1		Vendor ID bit 1		R			0
0		Vendor ID bit 0		R			1

Byte 8 Device ID and Output Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		**Device_ID3**	**Table of Device identifier codes, used for differentiating between CK505 package options, etc.**	**R**	**See Device ID Table**		**0**
6		**Device_ID2**		**R**			**1**
5		**Device_ID1**		**R**			**1**
4		**Device_ID0**		**R**			**0**
3		Reserved	Reserved	RW	-	-	0
2		Reserved	Reserved	RW	-	-	0
1		SE1_OE	Output enable for SE1	RW	Disabled	Enabled	1
0		Reserved	Reserved	RW	-	-	0

Byte 9 Output Control Register

Bit	Pin	Name	Description	Type	0	1	Default
7		PCIF5 STOP EN	Allows control of PCIF5 with assertion of PCI_STOP#	RW	Free running	Stops with PCI_STOP# assertion	0
6		TME_Readback	Truested Mode Enable (TME) strap status	**R**	normal operation	no overclocking	0
5		REF Strength	Sets the REF output drive strength	RW	1X (2Loads)	2X (3 Loads)	1
4		Test Mode Select	Allows test select, ignores REF/FSC/TestSel	RW	Outputs HI-Z	Outputs = REF/N	0
3		Test Mode Entry	Allows entry into test mode, ignores FSB/TestMode	RW	Normal operation	Test mode	0
2		IO_VOUT2	IO Output Voltage Select (Most Significant Bit)	RW	See Table 3: V_IO Selection (Default is 0.8V)		1
1		IO_VOUT1	IO Output Voltage Select	RW			0
0		IO_VOUT0	IO Output Voltage Select (Least Significant Bit)	RW			1

Byte 10 Stop Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		SRC5_EN Readback	Readback of SRC5 enable latch	**R**	CPU/PCI Stop Enabled	SRC5 Enabled	Latch
6		Reserved	Reserved	RW	TBD	TBD	0
5		Reserved		RW	TBD	TBD	0
4		Reserved		RW	TBD	TBD	0
3		Reserved		RW	TBD	TBD	0
2		Reserved		RW	TBD	TBD	0
1		CPU 1 Stop Enable	Enables control of CPU1 with CPU_STOP#	RW	Free Running	Stoppable	1
0		CPU 0 Stop Enable	Enables control of CPU 0 with CPU_STOP#	RW	Free Running	Stoppable	1

Byte 11 iAMT Enable Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved	Reserved	RW	-	-	0
6		Reserved	Reserved	RW	-	-	0
5		WOL_STOP_EN	Enable 25MHz WLAN clock during M1 or Power Down. This bit is sticky 1.	RW	25MHz disabled in Powerdown or M1	25MHz enabled in Powerdown or M1	**NOTE**
4		Reserved	Reserved	RW	-	-	1
3		CPU2_AMT_EN	M1 mode clk enable, only if ITP_EN=1	RW	Disable	Enable	0
2		CPU1_AMT_EN	M1 mode clk enable	RW	Disable	Enable	1
1		PCI-E_GEN2	Determines if PCI-E Gen2 compliant	**R**	non-Gen2	PCI-E Gen2 Compliant	1
0		**CPU 2 Stop Enable**	Enables control of CPU 2 (ITP)with CPU_STOP#	RW	Free Running	Stoppable	1

Note Rev B device default is 0. Rev C device is 1

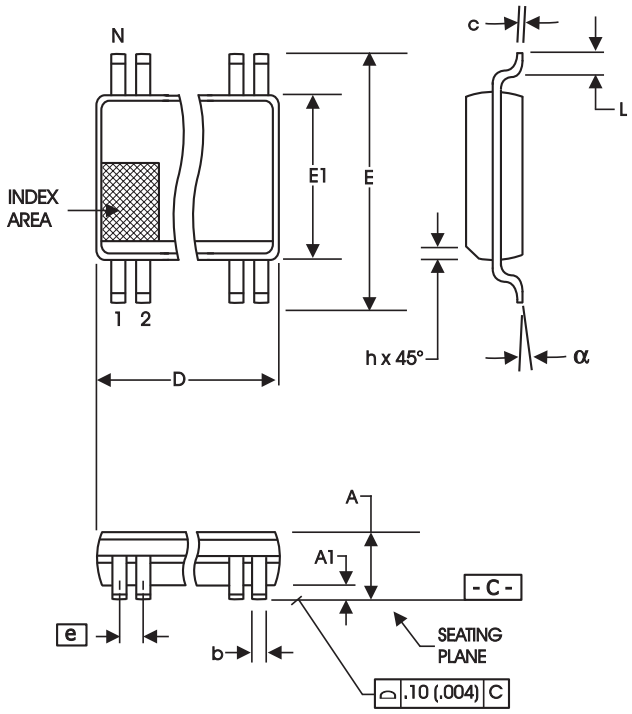
Byte 12 Byte Count Register

Bit	Pin	Name	Description	Type	0	1	Default
7		Reserved		RW			0
6		Reserved		RW			0
5		BC5	Read Back byte count register, max bytes = 32	RW	Byte count is 13 decimal.		0
4		BC4		RW			0
3		BC3		RW			1
2		BC2		RW			1
1		BC1		RW			0
0		BC0		RW			1

Test Clarification Table

Comments	HW		SW		
	FSLC/ TEST_SEL HW PIN	FSLB/ TEST_MODE HW PIN	TEST ENTRY BIT B9b3	REF/N or HI-Z B9b4	OUTPUT
	<2.0V	X	0	0	NORMAL
Power-up w/ TEST_SEL = 1 to enter test mode Cycle power to disable test mode FSLC./TEST_SEL -->3-level latched input If power-up w/ V>2.0V then use TEST_SEL If power-up w/ V<2.0V then use FSLC FSLB/TEST_MODE -->low Vth input TEST_MODE is a real time input	>2.0V	0	X	0	HI-Z
	>2.0V	0	X	1	REF/N
	>2.0V	1	X	0	REF/N
	>2.0V	1	X	1	REF/N
If TEST_SEL HW pin is 0 during power-up, test mode can be invoked through B9b3. If test mode is invoked by B9b3, only B9b4 is used to select HI-Z or REF/N FSLB/TEST_Mode pin is not used. Cycle power to disable test mode, one shot control	<2.0V	X	1	0	HI-Z
	<2.0V	X	1	1	REF/N

B9b3: 1= ENTER TEST MODE, Default = 0 (NORMAL OPERATION)
B9b4: 1= REF/N, Default = 0 (HI-Z)



300 mil SSOP

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	15.75	16.00	.620	.630

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

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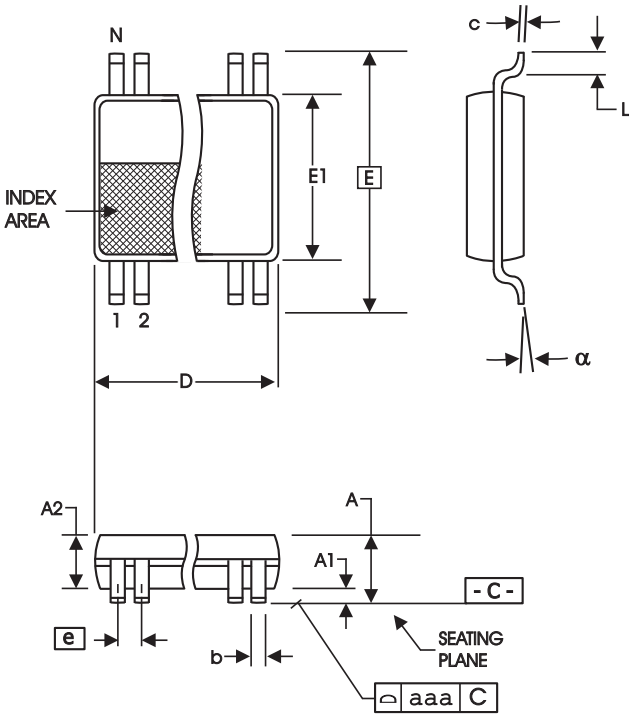

6.10 mm. Body, 0.50 mm. Pitch TSSOP
(240 mil) (20 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
48	12.40	12.60	.488	.496

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature	Wake-on LAN Default
9LPRS535BFLF	Tubes	48-pin SSOP	0 to +70°C	Disabled
9LPRS535BFLFT	Tape and Reel	48-pin SSOP	0 to +70°C	
9LPRS535BGLF	Tubes	48-pin TSSOP	0 to +70°C	
9LPRS535BGLFT	Tape and Reel	48-pin TSSOP	0 to +70°C	
9LPRS535CFLF	Tubes	48-pin SSOP	0 to +70°C	Enabled
9LPRS535CFLFT	Tape and Reel	48-pin SSOP	0 to +70°C	
9LPRS535CGLF	Tubes	48-pin TSSOP	0 to +70°C	
9LPRS535CGLFT	Tape and Reel	48-pin TSSOP	0 to +70°C	

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Revision History

Rev.	Issue Date	Description	Page #
0.1	3/10/2008	1. Intial release	
0.2	4/23/2008	1. Updated SMBus, front page, block diagram and deleted page 5	1, 4, 12-13
0.3	5/7/2008	1. Corrected typo in CPU power management table. Wrong column heading 2. Corrected typo in PD# Power Management Table SE1 should be low when B11b5 = 0 3. Corrected Byte 5 bit 0 to be NA when set to 0. SRC1 is not present. 4. Byte 6, bit 6 restored. CR_F# is present and can control SRC8	Various
0.4	7/7/2008	1. Corrected Power management table to remove the stop mode drive bits, which do not exist in this device. 2. Updated Differential clock period table.	Various
0.5	7/10/2008	1. Updated pin names to reflect LPR output type. Pin descriptions updated too. 2. SMBus updated to indicate PCIe Gen2 status	Various
0.6	7/13/2009	1. Removed references to CR# inputs that do not exist in this part. 2. Clarified functionality of Byte 11, bit 5.	Various
0.7	7/21/2009	1. Lowered Idd values to reflect performance of the device.	
A	7/28/2009	1. Moved to final 2. Added "Wake-on LAN Default" parameter to ordering info table.	

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