

Description

The 9DB836 is a zero delay/fanout buffer for PCI Express™ clocking. It supports PCIe Gen1–3 in zero-delay mode and PCIe Gen1–4 in fanout mode. The 9DB836 is a pin-compatible upgrade to the 9DB833 and 9DB834 with a Safe Power Sequence (SPS) clock input.

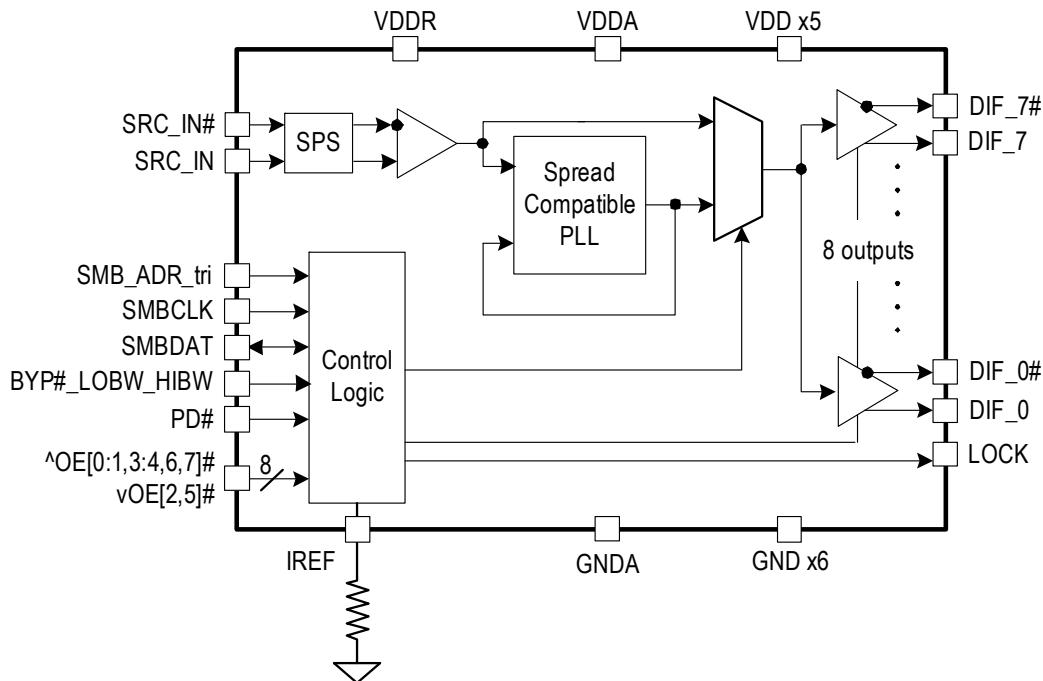
Typical Applications

- Riser cards
- Storage
- Networking
- JBOD

Output Features

- Eight 0.7V current-mode differential HCSL output pairs
- Supports zero delay buffer (ZDB) mode and fanout mode
- Selectable bandwidth for zero delay mode
- 50–110 MHz operation in PLL mode
- 5–166 MHz operation in Bypass mode

Block Diagram



Features

- SPS internal receiver bias network keeps input clock parked when input is floating
- Supports both 85Ω and 100Ω output impedance with appropriate resistor selection
- OE# pins default to controlling outputs
- PLL or Bypass mode; PLL can dejitter incoming clock
- Selectable PLL bandwidth; minimizes jitter peaking in downstream PLLs
- Spread spectrum compatible
- Outputs default to Hi-Z when disabled or when device is powered down
- SMBus interface; unused outputs can be disabled
- 3 selectable SMBus addresses

Key Specifications

- PCIe Gen3 jitter < 0.6ps rms in ZDB mode
- PCIe Gen4 additive jitter < 0.1ps rms in fanout mode
- Output cycle-to-cycle jitter < 50ps
- Output-to-output skew < 50ps

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Pin Assignments

Figure 1. Pin Assignments for 48TSSOP Package – Top View

NC	1	48	VDDA
VDDR	2	47	GNDA
GND	3	46	IREF
SRC_IN	4	45	LOCK
SRC_IN#	5	44	^OE7#
^OE0#	6	43	^OE4#
^OE3#	7	42	DIF_7
DIF_0	8	41	DIF_7#
DIF_0#	9	40	PD#
GND	10	39	VDD
VDD	11	38	DIF_6
DIF_1	12	37	DIF_6#
DIF_1#	13	36	^OE6#
^OE1#	14	35	vOE5#
vOE2#	15	34	DIF_5
DIF_2	16	33	DIF_5#
DIF_2#	17	32	GND
GND	18	31	VDD
VDD	19	30	DIF_4
DIF_3	20	29	DIF_4#
DIF_3#	21	28	SMB_ADR_tri
BYP#_HIBW_LOBW	22	27	VDD
SMBCLK	23	26	GND
SMBDAT	24	25	GND

v indicates internal pull-down resistor
 ^ indicates internal pull-up resistor

Pin 22 and pin 28 are latched on power-up. Ensure that the power supply to the pull-up/pull-down resistors ramps at the same time as the main supply to the chip.

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type	Description
1	NC	—	No connection.
2	VDDR	Power	Power supply for differential input clock (receiver). This VDD should be treated as an analog power rail and filtered appropriately. Nominally 3.3V.
3	GND	GND	Ground pin.
4	SRC_IN	Input	HCSL SRC true input.
5	SRC_IN#	Input	HCSL SRC complementary input.
6	^OE0#	Input	Active low input for enabling output 0. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
7	^OE3#	Input	Active low input for enabling output 3. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
8	DIF_0	Output	HCSL true clock output.
9	DIF_0#	Output	HCSL complementary clock output.
10	GND	GND	Ground pin.
11	VDD	Power	Power supply, nominally 3.3V.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
12	DIF_1	Output	HCSL true clock output.
13	DIF_1#	Output	HCSL complementary clock output.
14	^OE1#	Input	Active low input for enabling output 1. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
15	vOE2#	Input	Active low input for enabling output 2. This pin has an internal pull-down resistor. 1 = disable output, 0 = enable output.
16	DIF_2	Output	HCSL true clock output.
17	DIF_2#	Output	HCSL complementary clock output.
18	GND	GND	Ground pin.
19	VDD	Power	Power supply, nominally 3.3V.
20	DIF_3	Output	HCSL true clock output.
21	DIF_3#	Output	HCSL complementary clock output.
22	BYP#_HIBW_LOBW	Input	Tri-level input to select bypass mode, Hi BW PLL, or Lo BW PLL mode.
23	SMBCLK	Input	Clock pin of SMBUS circuitry.
24	SMBDAT	I/O	Data pin of SMBUS circuitry.
25	GND	GND	Ground pin.
26	GND	GND	Ground pin.
27	VDD	Power	Power supply, nominally 3.3V.
28	SMB_ADR_tri	Input	SMBus address select bit. This is a tri-level input that decodes 1 of 3 SMBus addresses.
29	DIF_4#	Output	HCSL complementary clock output.
30	DIF_4	Output	HCSL true clock output.
31	VDD	Power	Power supply, nominally 3.3V.
32	GND	GND	Ground pin.
33	DIF_5#	Output	HCSL complementary clock output.
34	DIF_5	Output	HCSL true clock output.
35	vOE5#	Input	Active low input for enabling output 5. This pin has an internal pull-down resistor. 1 = disable output, 0 = enable output.
36	^OE6#	Input	Active low input for enabling output 6. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
37	DIF_6#	Output	HCSL complementary clock output.
38	DIF_6	Output	HCSL true clock output.
39	VDD	Power	Power supply, nominally 3.3V.
40	PD#	Input	Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCOs (if any) and the XTAL oscillator are stopped.
41	DIF_7#	Output	HCSL complementary clock output.
42	DIF_7	Output	HCSL true clock output.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type	Description
43	^OE4#	Input	Active low input for enabling output 4. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
44	^OE7#	Input	Active low input for enabling output 7. This pin has an internal pull-up resistor. 1 = disable output, 0 = enable output.
45	LOCK	Output	3.3V output indicating PLL Lock status. This pin goes high when lock is achieved.
46	IREF	Output	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475Ω is the standard value for 100Ω differential impedance. Other impedances require different values.
47	GNDA	GND	Ground pin for the PLL core.
48	VDDA	Power	Power supply for PLL core.

Power Connections

Pin Number		Description
V _{DD}	GND	
2	3	SRC_IN/SRC_IN#
11, 19, 31, 39	10, 18, 25, 32	DIF(7:0)
27	26	DIGITAL VDD/GND
48	47	Analog VDD/GND for PLL and IREF

NOTE: For best results, also treat pin 2 as analog VDD.

Operating Mode Readback

BYP#_LOBW_HIBW	Mode	Byte0, bit 3	Byte 0, bit 1
Low	Bypass	0	0
Mid	PLL 100M Hi BW	1	0
High	PLL 100M Low BW	0	1

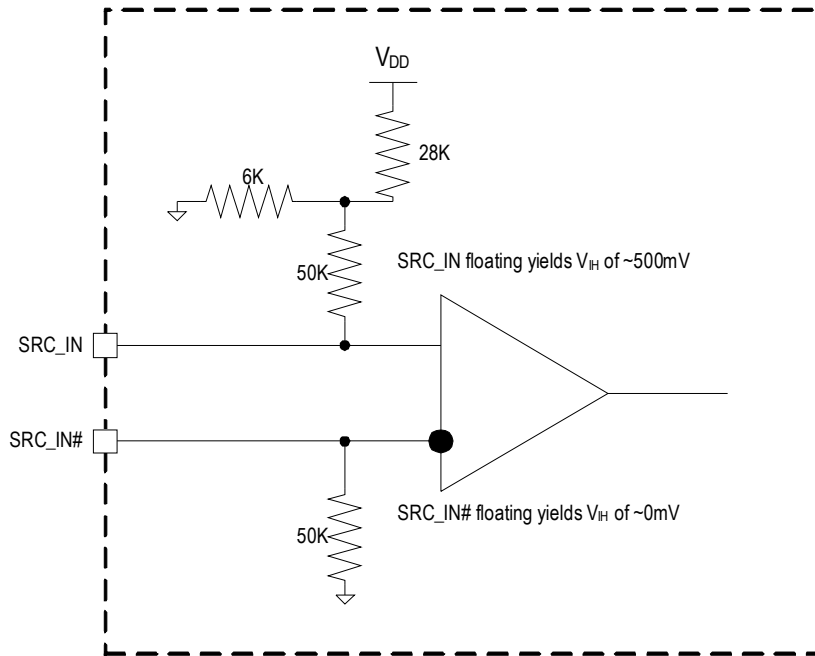
SMBus Address Selection and Readback

SMB_ADR_tri	Address
Low	DA/DB
Mid	DC/DD
High	D8/D9

Tri-level Input Logic Levels

State of Pin	Voltage
Low	< 0.8V
Mid	1.2 < V_{in} < 1.8V
High	V_{in} > 2.0V

Figure 2. Safe Power Sequence (SPS) Clock Input



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the 9DB836. These ratings, which are standard values for Renesas commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
3.3V Core Supply Voltage	$V_{DDA/R}$				4.6	V	1,2
3.3V Core Logic Voltage	V_{DD}				4.6	V	1,2
SMBus Supply Voltage	V_{DDSMB}	SMBus pull-up resistor voltage.			5.5	V	1
Input Low Voltage	V_{IL}		GND-0.5			V	1
Input High Voltage	V_{IH}	Except for SMBus interface.			$V_{DD}+0.5$	V	1
Storage Temperature	T_s		-65		150	°C	1
Junction Temperature	T_j				125	°C	1
Input ESD Protection	ESD prot	Human Body Model.	2000			V	1

¹ Guaranteed by design and characterization, not 100% tested in production.

² Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics

Table 3. Input/Supply/Common Parameters

$T_A = T_{IND}$ unless otherwise indicated. Supply voltage $V_{DD} = 3.3V \pm 5\%$.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Ambient Operating Temperature	T_{IND}	Industrial range.	-40		85	°C	1
Input High Voltage	V_{IH}	Single-ended inputs, except SMBus, low threshold and tri-level inputs.	2		$V_{DD} + 0.3$	V	1
Input Low Voltage	V_{IL}	Single-ended inputs, except SMBus, low threshold and tri-level inputs.	GND - 0.3		0.8	V	1
Input Current	I_{IN}	Single-ended inputs, $V_{IN} = GND$, $V_{IN} = V_{DD}$.	-5	-0.02	5	μA	1
	I_{INP}	Single-ended inputs. $V_{IN} = 0V$; inputs with internal pull-up resistors. $V_{IN} = V_{DD}$; inputs with internal pull-down resistors.	-100		100	μA	1
Input Frequency	F_{ibyp}	$V_{DD} = 3.3V$, Bypass Mode.	5		166	MHz	2
	F_{ipll}	$V_{DD} = 3.3V$, 100MHz PLL Mode.	50	100	110	MHz	2
Pin Inductance	L_{pin}				7	nH	1
Capacitance	C_{IN}	Logic inputs, except DIF_IN.	1.5		5	pF	1
	C_{INDIF_IN}	DIF_IN differential clock inputs.	1.5		2.7	pF	1,4
	C_{OUT}	Output pin capacitance.			6	pF	1
Clk Stabilization	T_{STAB}	From V_{DD} power-up and after input clock stabilization or deassertion of PD# to 1st clock.			1	ms	1,2
Input SS Modulation Frequency for PCIe	f_{MODIN}	Allowable frequency (Triangular modulation).	30	31.5	33	kHz	1
OE# Latency	$t_{LATOE\#}$	DIF start after OE# assertion. DIF stop after OE# deassertion.	1	2	3	cycles	1,3
Tdrive_PD#	t_{DRVPD}	DIF output enable after PD# deassertion.		13	300	μs	1,3
Tfall	t_F	Fall time of control inputs.			5	ns	1,2
Trise	t_R	Rise time of control inputs.			5	ns	1,2

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are > 200mV.

⁴ DIF_IN input.

Table 4. SMBus Parameters

$T_{AMB} = T_{IND}$ unless otherwise indicated. Supply voltage $V_{DD} = 3.3V \pm 5\%$.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
SMBus Input Low Voltage	V_{ILSMB}				0.8	V	1
SMBus Input High Voltage	V_{IHSMB}		2.1		V_{DDSMB}	V	1
SMBus Output Low Voltage	V_{OLSMB}	At I_{PULLUP} .			0.4	V	1
SMBus Sink Current	I_{PULLUP}	At V_{OL} .	4			mA	1
Nominal Bus Voltage	V_{DDSMB}	3V to 5V $\pm 10\%$.	2.7		5.5	V	1
SCLK/SDATA Rise Time	t_{RSMB}	(Maximum $V_{IL} - 0.15V$) to (Minimum $V_{IH} + 0.15V$).			1000	ns	1
SCLK/SDATA Fall Time	t_{FSMB}	(Minimum $V_{IH} + 0.15V$) to (Maximum $V_{IL} - 0.15V$).			300	ns	1
SMBus Operating Frequency	f_{MAXSMB}	Maximum SMBus operating frequency.			400	kHz	1,5

¹ Guaranteed by design and characterization, not 100% tested in production.

² Control input must be monotonic from 20% to 80% of input swing.

³ Time from deassertion until outputs are $> 200mV$.

⁴ DIF_IN input.

⁵ The differential input clock must be running for the SMBus to be active.

Table 5. DIF_IN Clock Input Parameters

$T_{AMB} = T_{IND}$ unless otherwise indicated. Supply voltage $V_{DD} = 3.3V \pm 5\%$.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Input Crossover Voltage	V_{CROSS}	Crossover voltage.	150	375	900	mV	1
Input Swing – DIF_IN	V_{SWING}	Differential value.	300			mV	1
Input Slew Rate – DIF_IN	dv/dt	Measured differentially.	0.6		8	V/ns	1,2
Input Leakage Current	I_{IN}	SRC_IN, $V_{IN} = GND$.			125	μA	
		SRC_IN#, $V_{IN} = V_{DD}$.	-100			μA	
Input Duty Cycle	d_{tin}	Measurement from differential waveform.	45		55	%	1
Input Jitter – Cycle to Cycle	J_{DIFIn}	Differential measurement.	0		125	ps	1

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through $\pm 75mV$ window centered around differential zero.

Table 6. DIF 0.7V Current Mode Differential Outputs

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Slew Rate	T _{RF}	Scope averaging on.	2	2.8	4	V/ns	1,2,3
Slew Rate Matching	ΔT _{RF}	Slew rate matching. Scope averaging on.		8	20	%	1,2,4
Voltage High	V _{HIGH}	Statistical measurement on single-ended signal using oscilloscope math function (scope averaging on).	660	797	850	mV	1
Voltage Low	V _{LOW}		-150	14	150		1
Maximum Voltage	V _{max}	Measurement on single-ended signal using absolute value (scope averaging off).		813	1150		1
Minimum Voltage	V _{min}		-300	-1			1
Crossing Voltage (abs)	V _{cross_abs}	Scope averaging off.	250	378	550		1,5
Crossing Voltage (var)	Δ-V _{cross}	Scope averaging off.		16	140		1,6

¹ Guaranteed by design and characterization, not 100% tested in production. I_{REF} = V_{DD}/(3 x R_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V at Z_o = 50Ω (100Ω differential impedance).

² Measured from differential waveform.

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0 V. This results in a ±150mV window around differential 0V.

⁴ Matching applies to rising edge rate for Clock and falling edge rate for Clock#. It is measured using a ±75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross absolute}) allowed. The intent is to limit V_{cross} induced modulation by setting Δ-V_{cross} to be smaller than V_{cross absolute}.

Table 7. Current Consumption

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
Operating Supply Current	I _{DD3.3OP}	All outputs active at 100MHz, PLL Mode, C _L = full load.		161	206	mA	1
Power Down Current	I _{DD3.3PD}	All differential pairs driven.		52	67	mA	1
	I _{DD3.3PDZ}	All differential pairs tri-stated.		4	6	mA	1

¹ Guaranteed by design and characterization, not 100% tested in production.

Table 8. Output Duty Cycle, Jitter, Skew and PLL Characteristics

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Units	Notes
PLL Bandwidth	B _W	-3dB point in High BW Mode (industrial).	1.5	2.8	4	MHz	1
		-3dB point in High BW Mode (commercial).	2	2.8	4	MHz	1
		-3dB point in Low BW Mode.	0.7	1.1	1.4	MHz	1
PLL Jitter Peaking	t _{JPEAK}	Peak pass band gain.		1.5	2	dB	1
Duty Cycle	t _{DC}	Measured differentially, PLL Mode.	45	49.2	55	%	1
Duty Cycle Distortion	t _{DCD}	Measured differentially, Bypass Mode at 100MHz.	-1	-0.4	1	%	1,4
Skew, Input to Output	t _{pdBYP}	Bypass Mode, V _T = 50% (industrial).	3500	4263	4900	ps	1
		Bypass Mode, V _T = 50% (commercial).	3500	4115	4500	ps	1
	t _{pdPLL}	PLL Mode V _T = 50%.	-250	-45	250	ps	1
Skew, Output to Output	t _{sk3}	V _T = 50% (industrial).		40	60	ps	1
		V _T = 50% (commercial).		40	50	ps	1
Jitter, Cycle to Cycle	t _{jcc-cyc}	PLL Mode.		21	50	ps	1,3
		Additive jitter in Bypass Mode.		3	10	ps	1,3

¹ Guaranteed by design and characterization, not 100% tested in production.

² I_{REF} = V_{DD} / (3 × R_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 × I_{REF} and V_{OH} = 0.7V at Z_o = 50Ω.

³ Measured from differential waveform.

⁴ Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in Bypass mode.

Table 9. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Phase Jitter, PLL Mode	t _{jphPCIeG1-CC}	PCIe Gen1.		25	35	86	ps (p-p)	1,2,3
	t _{jphPCIeG2-CC}	PCIe Gen2 Low Band. 10kHz < f < 1.5MHz		0.74	1.11	3	ps (rms)	1,2
		PCIe Gen2 High Band. 1.5MHz < f < Nyquist (50MHz)		1.95	2.36	3.1	ps (rms)	1,2
	t _{jphPCIeG3-CC}	PCIe Gen3. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.51	0.60	1	ps (rms)	1,2

Table 9. Filtered Phase Jitter Parameters – PCIe Common Clocked (CC) Architectures (Cont.)

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Specification Limit	Units	Notes
Additive Phase Jitter, Bypass Mode	t _{jphPCIeG1-CC}	PCIe Gen1.		5.4	8	Not Applicable	ps (p-p)	1,2,3,4
	t _{jphPCIeG2-CC}	PCIe Gen2 Low Band. 10kHz < f < 1.5MHz		0.004	0.01		ps (rms)	1,2,3,4,6
		PCIe Gen2 High Band. 1.5MHz < f < Nyquist (50MHz)		0.10	0.13		ps (rms)	1,2,3,4,6
	t _{jphPCIeG3-CC}	PCIe Gen3. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.05	0.06		ps (rms)	1,2,3,4,6
	t _{jphPCIeG4-CC}	PCIe Gen4. (PLL BW of 2–4MHz or 2–5MHz, CDR = 10MHz).		0.05	0.06		ps (rms)	1,2,3,4,6

Table 10. Filtered Phase Jitter Parameters – PCIe Independent Reference (IR) Architectures

T_{AMB} = T_{IND} unless otherwise indicated. Supply voltage V_{DD} = 3.3V ±5%.

Parameter	Symbol	Conditions	Minimum	Typical	Maximum	Industry Limits	Units	Notes
Additive Phase Jitter, Bypass mode	t _{jphPCIeG2-SRIS}	PCIe Gen2. (PLL BW of 16MHz, CDR = 5MHz).		0.12	0.16	Not Applicable	ps (rms)	1, 4, 5, 6, 7
	t _{jphPCIeG3-SRIS}	PCIe Gen3. (PLL BW of 2–4MHz, CDR = 10MHz).		0.03	0.04		ps (rms)	1, 4, 5, 6, 7

Notes on PCIe Filtered Phase Jitter tables:

- ¹ Applies to all differential outputs, guaranteed by design and characterization.
- ² Calculated from Intel™-supplied Clock Jitter tool, when driven by Wenzel Associates 100MHz oscillator.
- ³ Sample size of at least 100K cycles. This figure extrapolates to 108ps peak-peak at 1M cycles for a BER of 1⁻¹².
- ⁴ IR is the new name for Separate Reference Independent Spread (SRIS) and Separate Reference no Spread (SRnS) PCIe clock architectures.
- ⁵ According to the PCIe Base Specification Rev4.0 version 1.0, the jitter transfer functions and corresponding jitter limits are not defined for the IR clock architecture. Widely accepted industry limits using widely accepted industry filters are used to populate this table. The PCIe Base Specification Rev5.0 is expected to resolve this.
- ⁶ Additive jitter for RMS values is calculated by solving for b [$b = \sqrt{c^2 - a^2}$] where “a” is rms input jitter and ‘c’ is rms total jitter.

Test Loads and Terminations

Figure 3. HCSL Differential Output Test Load – Source Terminated

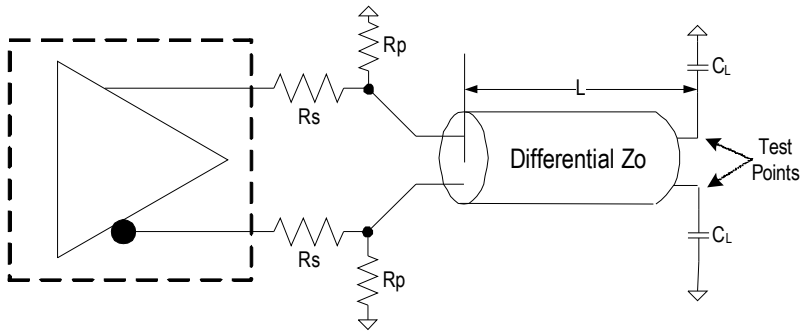


Table 11. Differential Output Termination

DIF Z_O (Ω)	IREF (Ω)	RS (Ω)	RP (Ω)	L (inches)	CL (pF)
100	475	33	49.9	5	2
85	412	27	42.2 or 43.2	5	2

General SMBus Serial Interface Information

How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte N through Byte N+X-1
- Renesas clock will **acknowledge** each byte **one at a time**
- Controller (host) sends a stop bit

Index Block Write Operation		
Controller (Host)		Renesas (Slave/Receiver)
T	starT bit	
Slave Address		
WR	WRite	
Beginning Byte = N		ACK
		ACK
Data Byte Count = X		ACK
Beginning Byte N		ACK
O	X Byte	O
O		O
O		O
Byte N + X - 1		O
		ACK
P	stoP bit	

How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte N+X-1
- Renesas clock sends **Byte 0 through Byte X (if X_(H) was written to Byte 8)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation		
Controller (Host)		Renesas
T	starT bit	
Slave Address		
WR	WRite	
Beginning Byte = N		ACK
		ACK
RT	Repeat starT	
Slave Address		
RD	ReaD	
		ACK
		Data Byte Count=X
ACK		Beginning Byte N
ACK		O
O		O
O		O
O		
		Byte N + X - 1
N	Not acknowledge	
P	stoP bit	

SMBus Table: Frequency Select Register, Read/Write Address (Selectable)

Byte 0	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	PD_Mode	PD# drive mode	RW	Driven	Hi-Z	1
Bit 6	—	OE_Mode	OE#_Disable drive mode	RW	Driven	Hi-Z	1
Bit 5	Reserved						0
Bit 4	Reserved						X
Bit 3	—	MODE1	BYPASS#/PLL1	RW	See Operating Mode Readback table.		Latched
Bit 2	Reserved						1
Bit 1	—	MODE0	BYPASS#/PLL0	RW	See Operating Mode Readback table.		Latched
Bit 0	Reserved						1

SMBus Table: Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	42, 41	DIF_7	Output Enable	RW	Disable	Enable	1
Bit 6	38, 37	DIF_6	Output Enable	RW	Disable	Enable	1
Bit 5	34, 33	DIF_5	Output Enable	RW	Disable	Enable	1
Bit 4	30, 29	DIF_4	Output Enable	RW	Disable	Enable	1
Bit 3	20, 21	DIF_3	Output Enable	RW	Disable	Enable	1
Bit 2	16, 17	DIF_2	Output Enable	RW	Disable	Enable	1
Bit 1	12, 13	DIF_1	Output Enable	RW	Disable	Enable	1
Bit 0	8, 9	DIF_0	Output Enable	RW	Disable	Enable	1

NOTE: The SMBus Output Enable Bit must be '1' and the respective OE pin must be active for the output to run.

SMBus Table: OE Pin Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	42, 41	DIF_7	DIF_7 Stoppable with OE7#	RW	Free-run	Stoppable	1
Bit 6	38, 37	DIF_6	DIF_6 Stoppable with OE6#	RW	Free-run	Stoppable	1
Bit 5	34, 33	DIF_5	DIF_5 Stoppable with OE5#	RW	Free-run	Stoppable	1
Bit 4	30, 29	DIF_4	DIF_4 Stoppable with OE4#	RW	Free-run	Stoppable	1
Bit 3	20, 21	DIF_3	DIF_3 Stoppable with OE3#	RW	Free-run	Stoppable	1
Bit 2	16, 17	DIF_2	DIF_2 Stoppable with OE2#	RW	Free-run	Stoppable	1
Bit 1	12, 13	DIF_1	DIF_1 Stoppable with OE1#	RW	Free-run	Stoppable	1
Bit 0	8, 9	DIF_0	DIF_0 Stoppable with OE0#	RW	Free-run	Stoppable	1

NOTE: To change the default to be "Stoppable", see the 9DB834.

SMBus Table: Reserved Register

Byte 3	Pin #	Name	Control Function	Type	0	1	Default
Bit 7			Reserved				X
Bit 6			Reserved				X
Bit 5			Reserved				X
Bit 4			Reserved				X
Bit 3			Reserved				X
Bit 2			Reserved				X
Bit 1			Reserved				X
Bit 0			Reserved				X

SMBus Table: Vendor & Revision ID Register

Byte 4	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	RID3	REVISION ID	R	—	—	0
Bit 6	—	RID2		R	—	—	0
Bit 5	—	RID1		R	—	—	0
Bit 4	—	RID0		R	—	—	0
Bit 3	—	VID3	VENDOR ID	R	—	—	0
Bit 2	—	VID2		R	—	—	0
Bit 1	—	VID1		R	—	—	0
Bit 0	—	VID0		R	—	—	1

SMBus Table: Device ID Register

Byte 5	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	DID7	Device ID 7 (MSB)	RW	Device ID is 86 Hex for 9DB836		1
Bit 6	—	DID6	Device ID 6	RW			0
Bit 5	—	DID5	Device ID 5	RW			0
Bit 4	—	DID4	Device ID 4	RW			0
Bit 3	—	DID3	Device ID 3	RW			0
Bit 2	—	DID2	Device ID 2	RW			1
Bit 1	—	DID1	Device ID 1	RW			1
Bit 0	—	DID0	Device ID 0	RW			0

SMBus Table: Byte Count Register

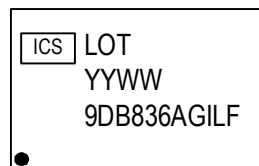
Byte 6	Pin #	Name	Control Function	Type	0	1	Default
Bit 7	—	BC7	Writing to this register configures how many bytes will be read back.	RW	—	—	0
Bit 6	—	BC6		RW	—	—	0
Bit 5	—	BC5		RW	—	—	0
Bit 4	—	BC4		RW	—	—	0
Bit 3	—	BC3		RW	—	—	0
Bit 2	—	BC2		RW	—	—	1
Bit 1	—	BC1		RW	—	—	1
Bit 0	—	BC0		RW	—	—	1

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/pag48-package-outline-drawing-610-mm-body-050mm-pitch-tssop

Marking Diagram



- “LOT” denotes the lot number.
- “YYWW” is the last two digits of the year and the work week number when the part was assembled.
- Line 3: Part number.

Ordering Information

Orderable Part Number	Package	Carrier Type	Temperature
9DB836AGILF	6.10mm body, 0.50mm pitch 48-TSSOP	Tubes	-40° to +85°C
9DB836AGILFT	6.10mm body, 0.50mm pitch 48-TSSOP	Tape and Reel	-40° to +85°C

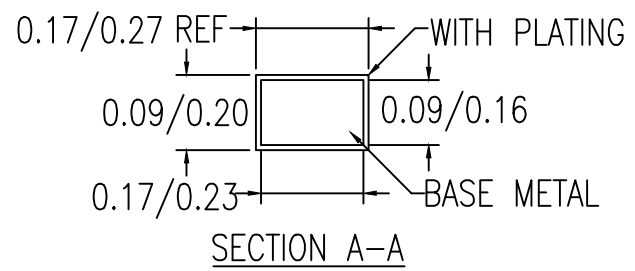
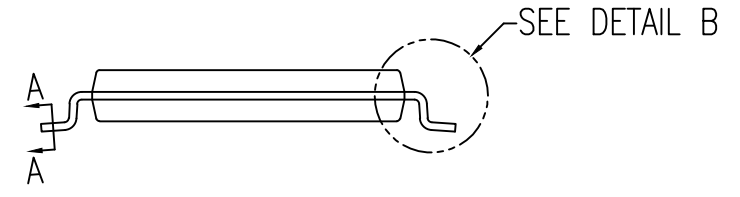
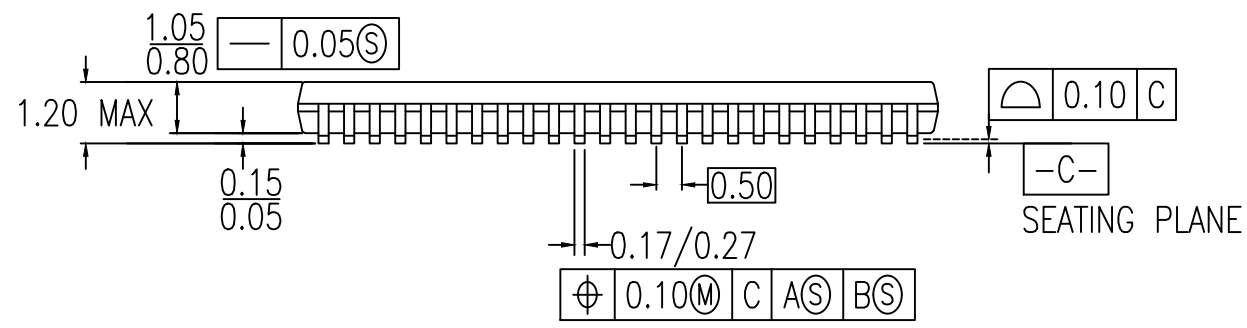
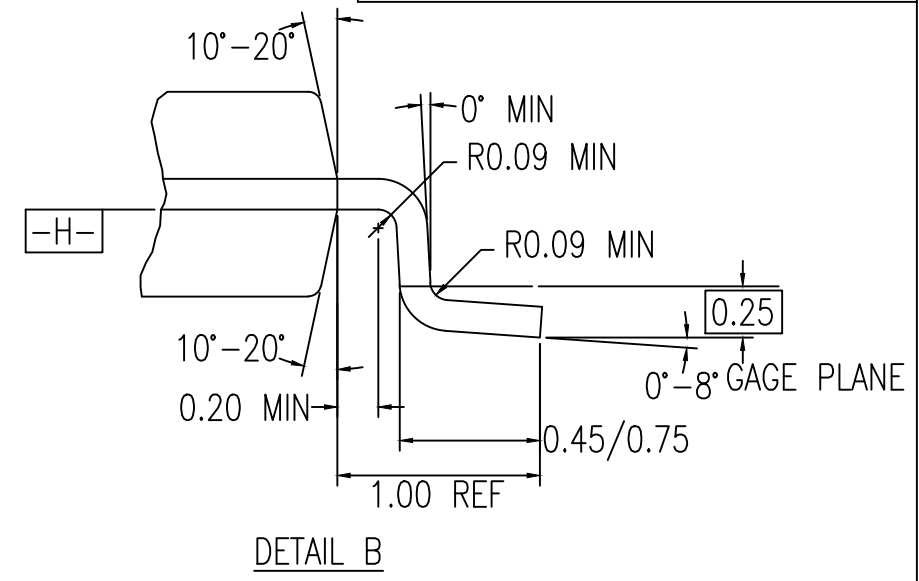
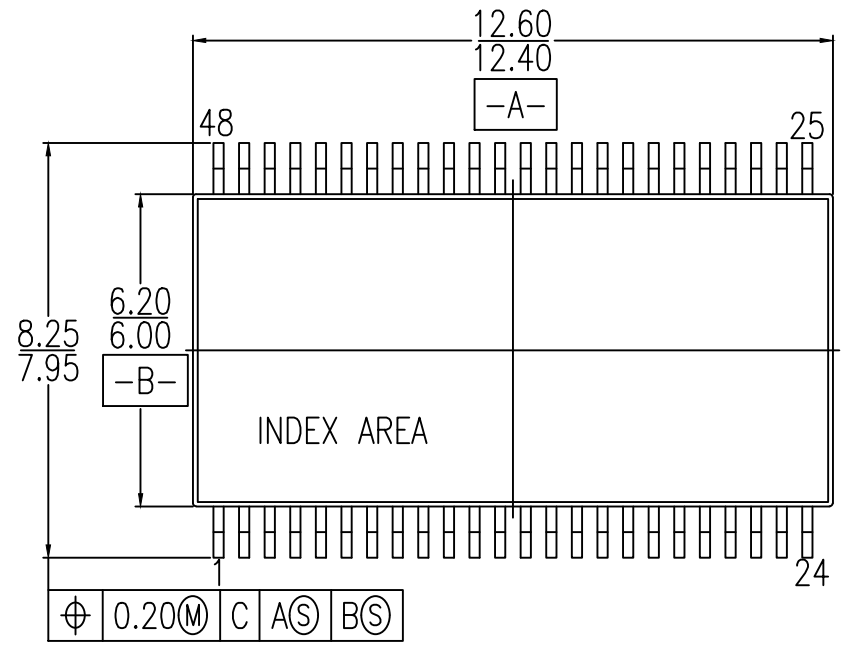
“LF” suffix to the part numbers are the Pb-Free configuration and are RoHS compliant.

“A” is the device revision designator.

Revision History

Revision Date	Description of Change
November 20, 2020	Reformat to Renesas.
October 12, 2018	Initial release.

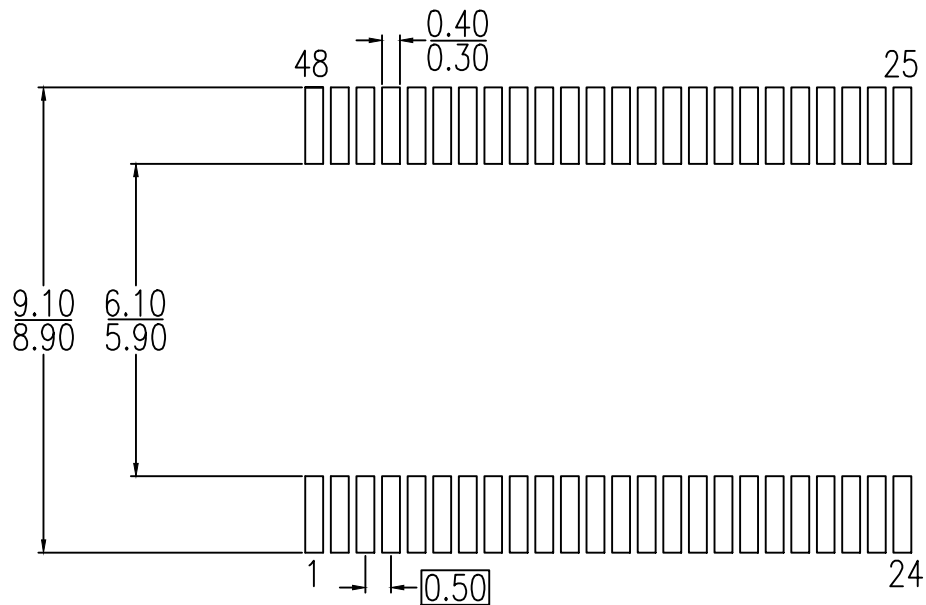
DATE CREATED		REVISIONS		
REV	DESCRIPTION	APPROVED		
7/16/18	00	Revised from PSC-4039_06		R.C
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE				



NOTES:
 1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
 2. ALL DIMENSION ARE IN MM.


TOLERANCES UNLESS SPECIFIED DECIMAL XX± XXX± XXXX±	ANGULAR ±	 www.IDT.com	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572
	TITLE PAG48 Package Outline Drawing 6.10 mm Body, 0.50mm Pitch TSSOP		
SIZE C	DRAWING No. PSC-4765	REV 00	
DO NOT SCALE DRAWING			SHEET 1 OF 2

DATE CREATED		REVISIONS		
DATE	REV	DESCRIPTION	APPROVED	
7/16/18	00	Revised from PSC-4039_06	R.C	
NOTE: REFER TO DCP FOR OFFICIAL RELEASE DATE				



RECOMMENDED LAND PATTERN DIMENSIONS

- NOTES:
 1. ALL DIMENSIONS ARE IN MILLIMETERS

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XXX±		
XXXX±		
TITLE PAC48 Package Outline Drawing 6.10 mm Body, 0.50mm Pitch TSSOP		
SIZE	DRAWING No.	REV
C	PSC-4765	00
DO NOT SCALE DRAWING		SHEET 2 OF 2

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