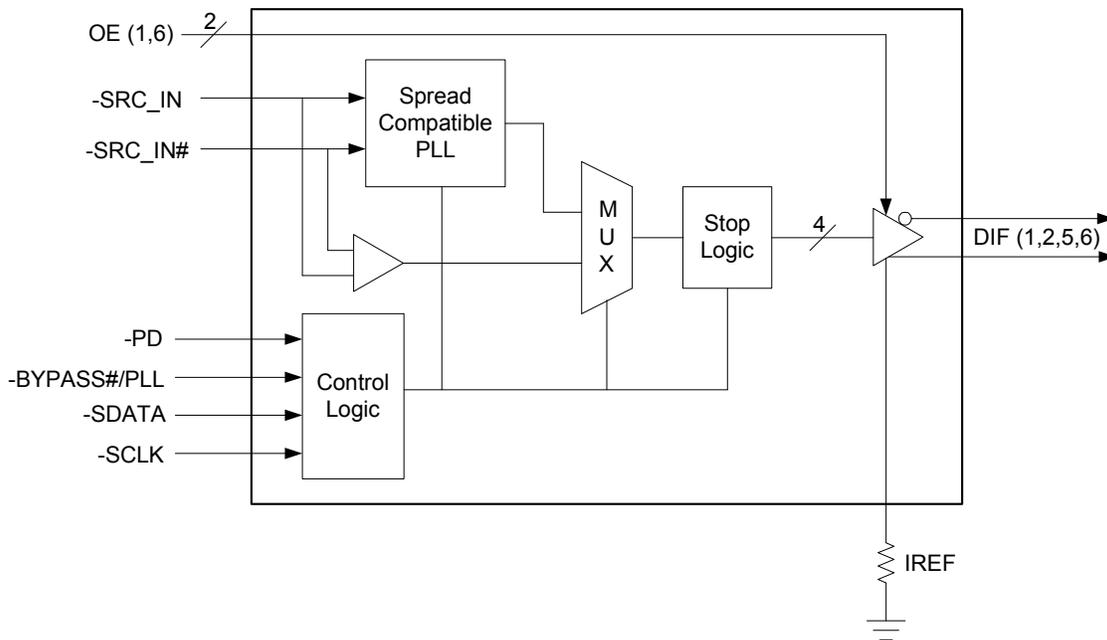# Four Output Differential Buffer for PCI Express

## Description

The 9DB401C is a DB400 Version 2.0 Yellow Cover part with PCI Express support. It can be used in PC or embedded systems to provide outputs that have low cycle-to-cycle jitter (50ps), low output-to-output skew (100ps), and are PCI Express gen 1 compliant. The 9DB401C supports a 1 to 4 output configuration, taking a spread or non spread differential HCSL input from a CK410(B) main clock such as 954101 and 932S401, or any other differential HCSL pair. 9DB401C can generate HCSL or LVDS outputs from 50 to 200MHz in PLL mode or 0 to 400Mhz in bypass mode. There are two de-jittering modes available selectable through the HIGH_BW# input pin, high bandwidth mode provides de-jittering for spread inputs and low bandwidth mode provides extra de-jittering for non-spread inputs. The SRC_STOP#, PD#, and OE real-time input pins provide completely programmable power management control.

## Output Features

- 4 - 0.7V HCSL or LVDS differential output pairs
- Supports zero delay buffer mode and fanout mode
- Bandwidth programming available

## Features/Benefits

- Spread spectrum modulation tolerant, 0 to -0.5% down spread and +/- 0.25% center spread
- Supports undriven differential outputs in PD# and SRC_STOP# modes for power management.

## Key Specifications

- Outputs cycle-cycle jitter: < 50ps
- Outputs skew: < 50ps
- Extended frequency range in bypass mode:
  Revision B: up to 333.33MHz
  Revision C: up to 400MHz
- Real-time PLL lock detect output pin
- 28-pin SSOP/TSSOP package
- Available in RoHS compliant packaging

## Functional Block Diagram



Note: Polarities shown for OE_INV = 0.

## Pin Configuration



**OE_INV = 0**

**OE_INV = 1**

**28-pin SSOP & TSSOP**

## Polarity Inversion Pin List Table

| | OE_INV | |
|---|---|---|
| Pins | 0 | 1 |
| 8 | OE_1 | OE1# |
| 15 | PD# | PD |
| 16 | DIF_STOP# | DIF_STOP |
| 21 | OE_6 | OE6# |

## Power Groups

| Pin Number | | Description |
|---|---|---|
| **VDD** | **GND** | |
| 1 | 4 | SRC_IN/SRC_IN# |
| 5,11,18, 24 | 4 | DIF(1,2,5,6) |
| N/A | 27 | IREF |
| 28 | 27 | Analog VDD & GND for PLL core |

## Pin Description for OE_INV = 0

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | VDD | PWR | Power supply, nominal 3.3V |
| 2 | SRC_IN | IN | 0.7 V Differential SRC TRUE input |
| 3 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input |
| 4 | GND | PWR | Ground pin. |
| 5 | VDD | PWR | Power supply, nominal 3.3V |
| 6 | DIF_1 | OUT | 0.7V differential true clock output |
| 7 | DIF_1# | OUT | 0.7V differential complement clock output |
| 8 | OE_1 | IN | Active high input for enabling output 1.<br>0 = tri-state outputs, 1= enable outputs |
| 9 | DIF_2 | OUT | 0.7V differential true clock output |
| 10 | DIF_2# | OUT | 0.7V differential complement clock output |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode<br>0 = Bypass mode, 1= PLL  mode |
| 13 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 14 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 15 | PD# | IN | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal are stopped. |
| 16 | SRC_STOP# | IN | Active low input to stop SRC outputs. |
| 17 | HIGH_BW# | IN | 3.3V input for selecting PLL Band Width<br>0 = High, 1= Low |
| 18 | VDD | PWR | Power supply, nominal 3.3V |
| 19 | DIF_5# | OUT | 0.7V differential complement clock output |
| 20 | DIF_5 | OUT | 0.7V differential true clock output |
| 21 | OE_6 | IN | Active high input for enabling output 6.<br>0 = tri-state outputs, 1= enable outputs |
| 22 | DIF_6# | OUT | 0.7V differential complement clock output |
| 23 | DIF_6 | OUT | 0.7V differential true clock output |
| 24 | VDD | PWR | Power supply, nominal 3.3V |
| 25 | OE_INV | IN | This latched input selects the polarity of the OE pins.<br>0 = OE pins active high, 1 = OE pins active low (OE#) |
| 26 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs.  This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 27 | GNDA | PWR | Ground pin for the PLL core. |
| 28 | VDDA | PWR | 3.3V power for the PLL core. |

## Pin Description for OE_INV = 1

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| 1 | VDD | PWR | Power supply, nominal 3.3V |
| 2 | SRC_IN | IN | 0.7 V Differential SRC TRUE input |
| 3 | SRC_IN# | IN | 0.7 V Differential SRC COMPLEMENTARY input |
| 4 | GND | PWR | Ground pin. |
| 5 | VDD | PWR | Power supply, nominal 3.3V |
| 6 | DIF_1 | OUT | 0.7V differential true clock output |
| 7 | DIF_1# | OUT | 0.7V differential complement clock output |
| 8 | OE1# | IN | Active low input for enabling DIF pair 1. 1 = tri-state outputs,  0 = enable outputs |
| 9 | DIF_2 | OUT | 0.7V differential true clock output |
| 10 | DIF_2# | OUT | 0.7V differential complement clock output |
| 11 | VDD | PWR | Power supply, nominal 3.3V |
| 12 | BYPASS#/PLL | IN | Input to select Bypass(fan-out) or PLL (ZDB) mode 0 = Bypass mode, 1= PLL  mode |
| 13 | SCLK | IN | Clock pin of SMBus circuitry, 5V tolerant. |
| 14 | SDATA | I/O | Data pin for SMBus circuitry, 5V tolerant. |
| 15 | PD | IN | Asynchronous active high input pin used to power down the device. The internal clocks are disabled and the VCO is stopped. |
| 16 | SRC_STOP | IN | Active high input to stop SRC outputs. |
| 17 | HIGH_BW# | IN | 3.3V input for selecting PLL Band Width 0 = High, 1= Low |
| 18 | VDD | PWR | Power supply, nominal 3.3V |
| 19 | DIF_5# | OUT | 0.7V differential complement clock output |
| 20 | DIF_5 | OUT | 0.7V differential true clock output |
| 21 | OE6# | IN | Active low input for enabling DIF pair 6. 1 = tri-state outputs,  0 = enable outputs |
| 22 | DIF_6# | OUT | 0.7V differential complement clock output |
| 23 | DIF_6 | OUT | 0.7V differential true clock output |
| 24 | VDD | PWR | Power supply, nominal 3.3V |
| 25 | OE_INV | IN | This latched input selects the polarity of the OE pins. 0 = OE pins active high, 1 = OE pins active low (OE#) |
| 26 | IREF | OUT | This pin establishes the reference current for the differential current-mode output pairs.  This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value. |
| 27 | GNDA | PWR | Ground pin for the PLL core. |
| 28 | VDDA | PWR | 3.3V power for the PLL core. |

## Absolute Max

| Symbol | Parameter | Min | Max | Units |
|--------|-----------|-----|-----|-------|
| VDD_A | 3.3V Core Supply Voltage | | 4.6 | V |
| VDD_In | 3.3V Logic Supply Voltage | | 4.6 | V |
| $V_{IL}$ | Input Low Voltage | GND-0.5 | | V |
| $V_{IH}$ | Input High Voltage | | $V_{DD}$+0.5V | V |
| Ts | Storage Temperature | -65 | 150 | °C |
| Tambient | Ambient Operating Temp | 0 | 70 | °C |
| Tcase | Case Temperature | | 115 | °C |
| ESD prot | Input ESD protection human body model | 2000 | | V |

## Electrical Characteristics - Input/Supply/Common Output Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-----------|--------|-----------|-----|-----|-----|-------|-------|
| Input High Voltage | $V_{IH}$ | 3.3 V +/-5% | 2 | | $V_{DD}$ + 0.3 | V | |
| Input Low Voltage | $V_{IL}$ | 3.3 V +/-5% | GND - 0.3 | | 0.8 | V | |
| Input High Current | $I_{IH}$ | $V_{IN}$ = $V_{DD}$ | -5 | | 5 | uA | |
| Input Low Current | $I_{IL1}$ | $V_{IN}$ = 0 V; Inputs with no pull-up resistors | -5 | | | uA | |
| | $I_{IL2}$ | $V_{IN}$ = 0 V; Inputs with pull-up resistors | -200 | | | uA | |
| Operating Supply Current | $I_{DD3.3PLL}$ | Full Active, $C_L$ = Full load; | | 175 | 200 | mA | |
| | $I_{DD3.3ByPass}$ | | | 160 | 175 | mA | |
| Powerdown Current | $I_{DD3.3PD}$ | all diff pairs driven | | | 40 | mA | |
| | | all differential pairs tri-stated | | | 4 | mA | |
| Input Frequency | $F_{iPLL}$ | PLL Mode | 50 | | 200 | MHz | |
| Input Frequency | $F_{iBypass}$ | Bypass Mode (Revision B/REV ID = 1H) | 0 | | 333.33 | MHz | |
| Input Frequency | $F_{iBypass}$ | Bypass Mode (Revision C/REV ID = 2H) | 0 | | 400 | MHz | |
| Pin Inductance[1] | $L_{pin}$ | | | | 7 | nH | 1 |
| Input Capacitance[1] | $C_{IN}$ | Logic Inputs | 1.5 | | 4 | pF | 1 |
| | $C_{OUT}$ | Output pin capacitance | | | 4 | pF | 1 |
| PLL Bandwidth | BW | PLL Bandwidth when PLL_BW=0 | 2.4 | 3 | 3.4 | MHz | 1 |
| | | PLL Bandwidth when PLL_BW=1 | 0.7 | 1 | 1.4 | MHz | 1 |
| Clk Stabilization[1,2] | $T_{STAB}$ | From $V_{DD}$ Power-Up and after input clock stabilization or de-assertion of PD# to 1st clock | | 0.5 | 1 | ms | 1,2 |
| Modulation Frequency | fMOD | Triangular Modulation | 30 | | 33 | kHz | 1 |
| Tdrive_SRC_STOP# | | DIF output enable after SRC_Stop# de-assertion | | 10 | 15 | ns | 1,3 |
| Tdrive_PD# | | DIF output enable after PD# de-assertion | | | 300 | us | 1,3 |
| Tfall | | Fall time of PD# and SRC_STOP# | | | 5 | ns | 1 |
| Trise | | Rise time of PD# and SRC_STOP# | | | 5 | ns | 2 |

[1]Guaranteed by design and characterization, not 100% tested in production.

[2]See timing diagrams for timing requirements.

[3]Time from deassertion until outputs are >200 mV

## Electrical Characteristics - Clock Input Parameters

$T_A$ = 0 - 70°C; Supply Voltage $V_{DD}$ = 3.3 V +/-5%

| PARAMETER | SYMBOL | CONDITIONS | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| Differential Input High Voltage | $V_{IHDIF}$ | Differential inputs (single-ended measurement) | 600 | 1150 | mV | 1 |
| Differential Input Low Voltage | $V_{ILDIF}$ | Differential inputs (single-ended measurement) | $V_{SS}$ - 300 | 300 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 0.4 | 8 | V/ns | 2 |
| Input Leakage Current | $I_{IN}$ | $V_{IN} = V_{DD}$, $V_{IN} = GND$ | -5 | 5 | uA | 1 |
| Input Duty Cycle | $d_{tin}$ | Measurement from differential wavefrom | 45 | 55 | % | 1 |
| Input SRC Jitter - Cycle to Cycle | $SRCJ_{C2CIn}$ | Differential Measurement | | 125 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] Slew rate measured through Vswing centered around differential zero

## Electrical Characteristics - DIF 0.7V Current Mode Differential Pair

$T_A$ = 0 - 70°C; $V_{DD}$ = 3.3 V +/-5%; $C_L$ =2pF, $R_S$=33.2Ω, $R_P$=49.9Ω, $I_{REF}$ = 475Ω

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|
| Current Source Output Impedance | Zo[1] | $V_O = V_x$ | 3000 | | | Ω | 1 |
| Voltage High | VHigh | Statistical measurement on single ended signal using oscilloscope math function. | 660 | | 850 | mV | 1,3 |
| Voltage Low | VLow | | -150 | | 150 | mV | 1,3 |
| Max Voltage | Vovs | Measurement on single ended signal using absolute value. | | | 1150 | mV | 1 |
| Min Voltage | Vuds | | -300 | | | mV | 1 |
| Crossing Voltage (abs) | Vcross(abs) | | 250 | | 550 | mV | 1 |
| Crossing Voltage (var) | d-Vcross | Variation of crossing over all edges | | | 140 | mV | 1 |
| Long Accuracy | ppm | see Tperiod min-max values | | | 0 | ppm | 1,2 |
| Rise Time | $t_r$ | $V_{OL}$ = 0.175V, $V_{OH}$ = 0.525V | 175 | | 700 | ps | 1 |
| Fall Time | $t_f$ | $V_{OH}$ = 0.525V $V_{OL}$ = 0.175V | 175 | | 700 | ps | 1 |
| Rise Time Variation | $d-t_r$ | | | | 125 | ps | 1 |
| Fall Time Variation | $d-t_f$ | | | | 125 | ps | 1 |
| Duty Cycle | $d_{t3}$ | Measurement from differential wavefrom | 45 | | 55 | % | 1 |
| Skew | $t_{sk3}$ | $V_T$ = 50% | | | 50 | ps | 1 |
| Jitter, Cycle to cycle | $t_{jcyc-cyc}$ | PLL mode, Measurement from differential wavefrom | | | 50 | ps | 1 |
| | | BYPASS mode as additive jitter | | | 50 | ps | 1 |

[1] Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that the input clock complies with CK409/CK410 accuracy requirements

[3] $I_{REF} = V_{DD}/(3xR_R)$. For $R_R$ = 475Ω (1%), $I_{REF}$ = 2.32mA. $I_{OH}$ = 6 x $I_{REF}$ and $V_{OH}$ = 0.7V @ $Z_O$=50Ω.

| SRC Reference Clock | | | |
|---|---|---|---|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|---|---|---|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

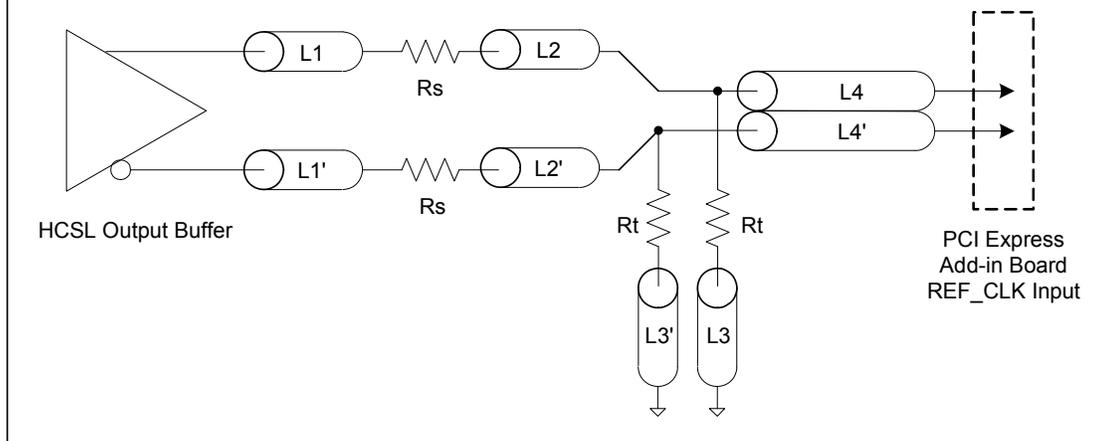| Differential Routing to PCI Express Connector | | | |
|---|---|---|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

Figure 1: Down Device Routing
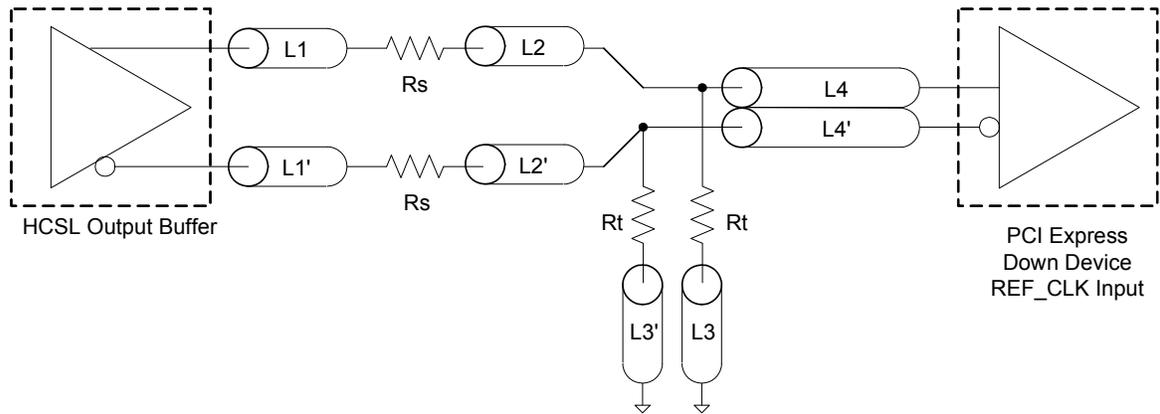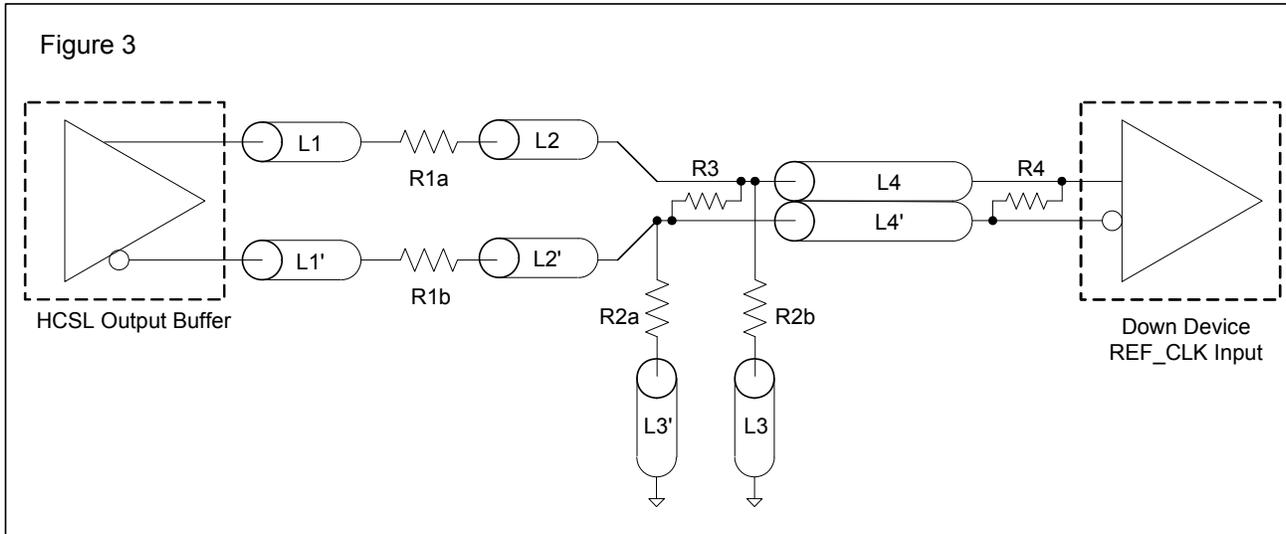


Figure 2: PCI Express Connector Routing

| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|---|---|---|---|---|---|---|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1

R2a = R2b = R2

Figure 3



| Cable Connected AC Coupled Application (figure 4) | | |
|---|---|---|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 µF | |
| Vcm | 0.350 volts | |

Figure 4
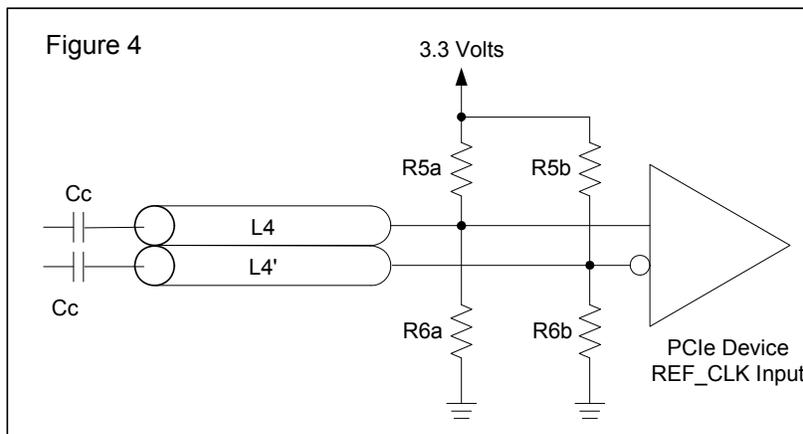
# General SMBus serial interface information for the 9DB401C

## How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address DC $_{(h)}$
- IDT clock will *acknowledge*
- Controller (host) sends the begining byte location = N
- IDT clock will *acknowledge*
- Controller (host) sends the data byte count = X
- IDT clock will *acknowledge*
- Controller (host) starts sending *Byte N through Byte N + X -1*
- IDT clock will *acknowledge* each byte *one at a time*
- Controller (host) sends a Stop bit

## How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address DC $_{(h)}$
- IDT clock will *acknowledge*
- Controller (host) sends the begining byte location = N
- IDT clock will *acknowledge*
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address DD $_{(h)}$
- IDT clock will *acknowledge*
- IDT clock will send the data byte count = X
- IDT clock sends *Byte N + X -1*
- IDT clock sends *Byte 0 through byte X (if X $_{(h)}$ was written to byte 8)*.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

### Index Block Write Operation

| Controller (Host) | | IDT (Slave/Receiver) | |
|---|---|---|---|
| T | starT bit | | |
| Slave Address DC $_{(h)}$ | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| Data Byte Count = X | | | |
| | | ACK | |
| Beginning Byte N | | | |
| | | ACK | |
| ◇ | X Byte | | |
| ◇ | | ◇ | |
| ◇ | | ◇ | |
| | | ◇ | |
| Byte N + X - 1 | | | |
| | | ACK | |
| P | stoP bit | | |

### Index Block Read Operation

| Controller (Host) | | IDT (Slave/Receiver) | |
|---|---|---|---|
| T | starT bit | | |
| Slave Address DC $_{(h)}$ | | | |
| WR | WRite | | |
| | | ACK | |
| Beginning Byte = N | | | |
| | | ACK | |
| RT | Repeat starT | | |
| Slave Address DD $_{(h)}$ | | | |
| RD | ReaD | | |
| | | ACK | |
| | | | |
| | | Data Byte Count = X | |
| ACK | | | |
| | | Beginning Byte N | |
| ACK | | X Byte | |
| | | | ◇ |
| ◇ | | | ◇ |
| ◇ | | | ◇ |
| ◇ | | | |
| | | Byte N + X - 1 | |
| N | Not acknowledge | | |
| P | stoP bit | | |

**SMBus Table: Frequency Select Register, READ/WRITE ADDRESS (DC/DD)**

| Byte 0 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | PD_Mode | PD# drive mode | RW | driven | Hi-Z | 0 |
| Bit 6 | - | STOP_Mode | SRC_Stop# drive mode | RW | driven | Hi-Z | 0 |
| Bit 5 | - | PD_SRC_INV | Power Down and SRC Invert | RW | Normal | Invert | 0 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 2 | - | PLL_BW# | Select PLL BW | RW | High BW | Low BW | 1 |
| Bit 1 | - | BYPASS# | BYPASS#/PLL | RW | fan-out | ZDB | 1 |
| Bit 0 | - | SRC_DIV# | SRC Divide by 2 Select | RW | x/2 | 1x | 1 |

**SMBus Table: Output Control Register**

| Byte 1 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 6 | 22,23 | DIF_6 | Output Control | RW | Disable | Enable | 1 |
| Bit 5 | 19,20 | DIF_5 | Output Control | RW | Disable | Enable | 1 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 2 | 9,10 | DIF_2 | Output Control | RW | Disable | Enable | 1 |
| Bit 1 | 6,7 | DIF_1 | Output Control | RW | Disable | Enable | 1 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | | X |

**SMBus Table: Output Control Register**

| Byte 2 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 6 | 22,23 | DIF_6 | Output Control | RW | Free-run | Stoppable | 0 |
| Bit 5 | 19,20 | DIF_5 | Output Control | RW | Free-run | Stoppable | 0 |
| Bit 4 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 3 | - | Reserved | Reserved | RW | Reserved | | X |
| Bit 2 | 9,10 | DIF_2 | Output Control | RW | Free-run | Stoppable | 0 |
| Bit 1 | 6,7 | DIF_1 | Output Control | RW | Free-run | Stoppable | 0 |
| Bit 0 | - | Reserved | Reserved | RW | Reserved | | X |

**SMBus Table: Output Control Register**

| Byte 3 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | | | Reserved | RW | Reserved | | X |
| Bit 6 | | | Reserved | RW | Reserved | | X |
| Bit 5 | | | Reserved | RW | Reserved | | X |
| Bit 4 | | | Reserved | RW | Reserved | | X |
| Bit 3 | | | Reserved | RW | Reserved | | X |
| Bit 2 | | | Reserved | RW | Reserved | | X |
| Bit 1 | | | Reserved | RW | Reserved | | X |
| Bit 0 | | | Reserved | RW | Reserved | | X |

**SMBus Table: Vendor & Revision ID Register**

| Byte 4 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | RID3 | | R | - | - | X |
| Bit 6 | - | RID2 | REVISION ID | R | - | - | X |
| Bit 5 | - | RID1 | | R | - | - | X |
| Bit 4 | - | RID0 | | R | - | - | X |
| Bit 3 | - | VID3 | | R | - | - | 0 |
| Bit 2 | - | VID2 | VENDOR ID | R | - | - | 0 |
| Bit 1 | - | VID1 | | R | - | - | 0 |
| Bit 0 | - | VID0 | | R | - | - | 1 |

**SMBus Table: DEVICE ID**

| Byte 5 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | Device ID 7 (MSB) | | RW | Reserved | | 0 |
| Bit 6 | - | Device ID 6 | | RW | Reserved | | 1 |
| Bit 5 | - | Device ID 5 | | RW | Reserved | | 0 |
| Bit 4 | - | Device ID 4 | | RW | Reserved | | 0 |
| Bit 3 | - | Device ID 3 | | RW | Reserved | | 0 |
| Bit 2 | - | Device ID 2 | | RW | Reserved | | 0 |
| Bit 1 | - | Device ID 1 | | RW | Reserved | | 0 |
| Bit 0 | - | Device ID 0 | | RW | Reserved | | 1 |

**SMBus Table: Byte Count Register**

| Byte 6 | Pin # | Name | Control Function | Type | 0 | 1 | PWD |
|--------|-------|------|------------------|------|---|---|-----|
| Bit 7 | - | BC7 | | RW | - | - | 0 |
| Bit 6 | - | BC6 | | RW | - | - | 0 |
| Bit 5 | - | BC5 | | RW | - | - | 0 |
| Bit 4 | - | BC4 | Writing to this register configures how many bytes will be read back. | RW | - | - | 0 |
| Bit 3 | - | BC3 | | RW | - | - | 0 |
| Bit 2 | - | BC2 | | RW | - | - | 1 |
| Bit 1 | - | BC1 | | RW | - | - | 1 |
| Bit 0 | - | BC0 | | RW | - | - | 1 |

## PD#

The PD# pin cleanly shuts off all clocks and places the device into a power saving mode. PD# must be asserted before shutting off the input clock or power to insure an orderly shutdown. PD is asynchronous active-low input for both powering down the device and powering up the device. When PD# is asserted, all clocks will be driven high, or tri-stated (depending on the PD# drive mode and Output control bits) before the PLL is shut down.

## PD# Assertion

When PD# is sampled low by two consecutive rising edges of DIF#, all DIF outputs must be held High, or tri-stated (depending on the PD# drive mode and Output control bits) on the next High-Low transition of the DIF# outputs. When the PD# drive mode bit is set to '0', all clock outputs will be held with DIF driven High with 2 x $I_{REF}$ and DIF# tri-stated. If the PD# drive mode bit is set to '1', both DIF and DIF# are tri-stated.
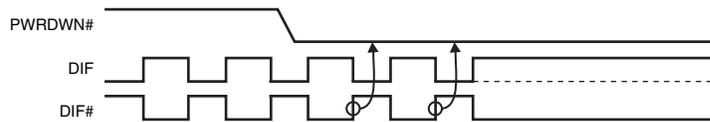


## PD# De-assertion

Power-up latency is less than 1 ms. This is the time from de-assertion of the PD# pin, or VDD reaching 3.3V, or the time from valid SRC_IN clocks until the time that stable clocks are output from the device (PLL Locked). If the PD# drive mode bit is set to '1', all the DIF outputs must driven to a voltage of >200 mV within 300 ms of PD# de-assertion.
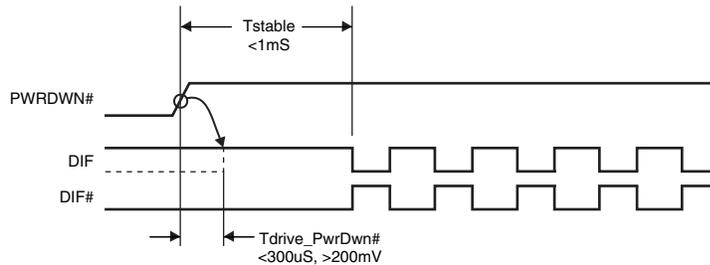
Note: Polarities in timing diagrams are shown OE_INV = 0. They are similar to OE_INV = 1.

## SRC_STOP#

The SRC_STOP# signal is an active-low asynchronous input that cleanly stops and starts the DIF outputs.  A valid clock must be present on SRC_IN for this input to work properly.  The SRC_STOP# signal is de-bounced and must remain stable for two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

## SRC_STOP# - Assertion (transition from '1' to '0')

Asserting SRC_STOP# causes all DIF outputs to stop after their next transition (if the control register settings allow the output to stop).   When the SRC_STOP# drive bit is '0', the final state of all stopped DIF outputs is DIF = High and DIF# = Low.  There is no change in output drive current. DIF is driven with $6xI_{REF.}$ DIF# is not driven, but pulled low by the termination.  When the SRC_STOP# drive bit is '1', the final state of all DIF output pins is Low.  Both DIF and DIF# are not driven.

All stopped differential outputs resume normal operation in a glitch-free manner.  The de-assertion latency to active outputs is 2-6 DIF clock periods, with all DIF outputs resuming simultaneously.  If the SRC_STOP# drive control bit is '1' (tri-state), all stopped DIF outputs must be driven High (>200 mV) within 10 ns of de-assertion.

## SRC_STOP_1 (SRC_Stop = Driven, PD = Driven)
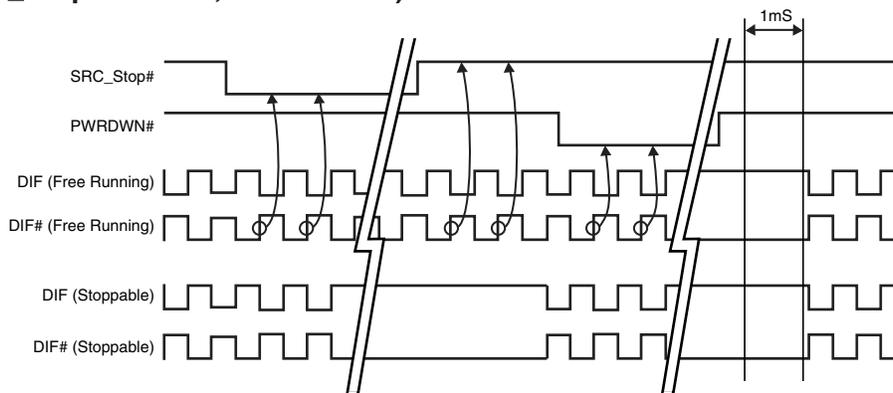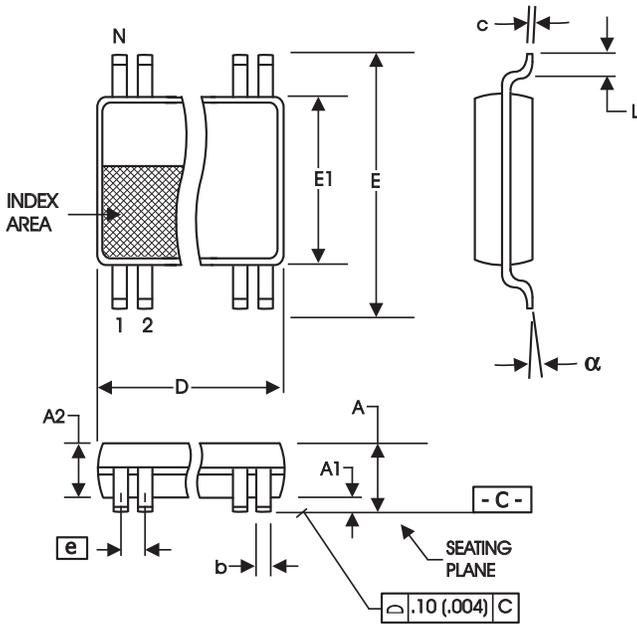


## SRC_STOP_2 (SRC_Stop =Tristate, PD = Driven)
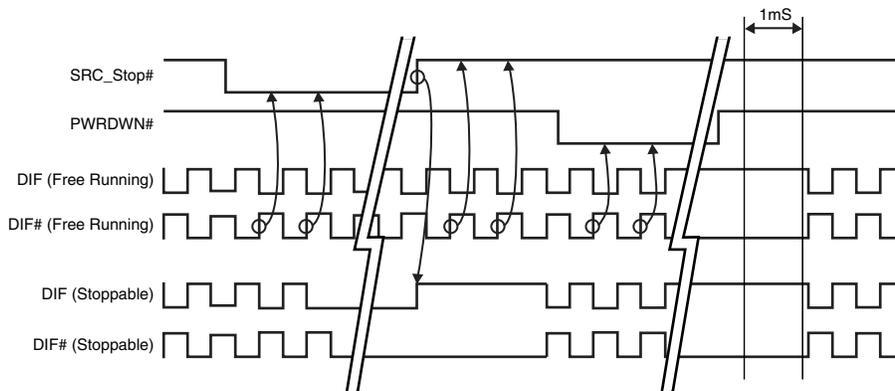
## SRC_STOP_3 (SRC_Stop = Driven, PD = Tristate)

1mS

SRC_Stop#

PWRDWN#

DIF (Free Running)

DIF# (Free Running)

DIF (Stoppable)

DIF# (Stoppable)
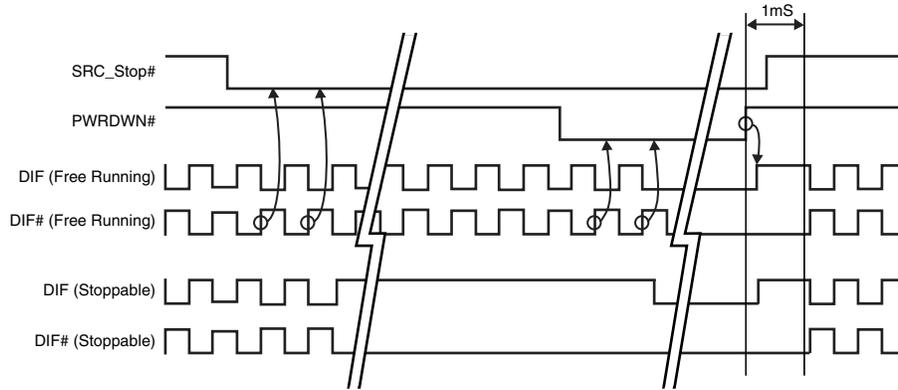
## SRC_STOP_4 (SRC_Stop = Tristate, PD = Tristate)

1mS

SRC_Stop#

PWRDWN#

DIF (Free Running)

DIF# (Free Running)

DIF (Stoppable)

DIF# (Stoppable)
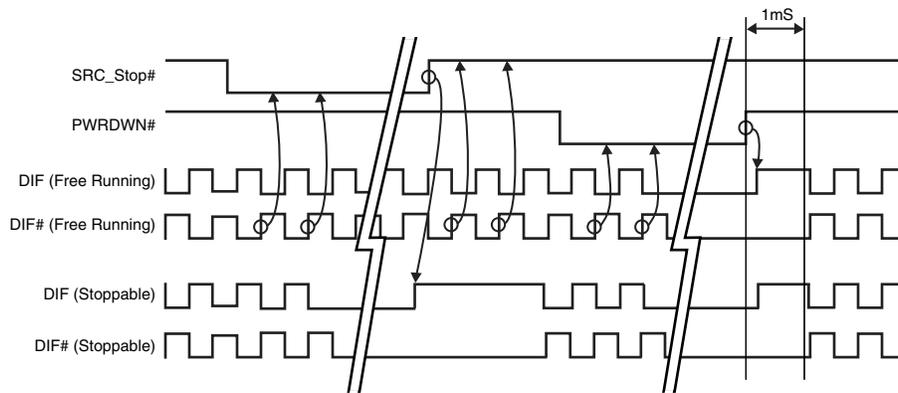
### 209 mil SSOP

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 2.00 | -- | .079 |
| A1 | 0.05 | -- | .002 | -- |
| A2 | 1.65 | 1.85 | .065 | .073 |
| b | 0.22 | 0.38 | .009 | .015 |
| c | 0.09 | 0.25 | .0035 | .010 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 7.40 | 8.20 | .291 | .323 |
| E1 | 5.00 | 5.60 | .197 | .220 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.55 | 0.95 | .022 | .037 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| α | 0° | 8° | 0° | 8° |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 28 | 9.90 | 10.50 | .390 | .413 |

Reference Doc.: JEDEC Publication 95, MO-150

10-0033
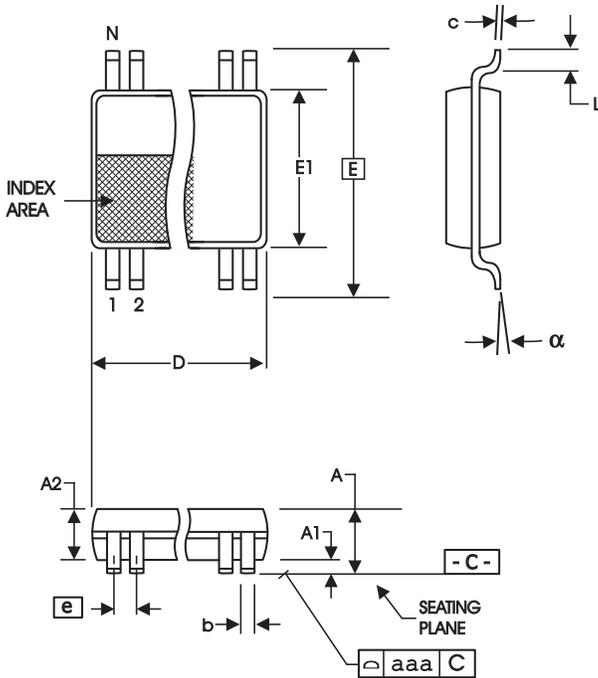
**4.40 mm. Body, 0.65 mm. Pitch TSSOP**

**(173 mil)**     **(25.6 mil)**

| SYMBOL | In Millimeters COMMON DIMENSIONS | | In Inches COMMON DIMENSIONS | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | -- | 1.20 | -- | .047 |
| A1 | 0.05 | 0.15 | .002 | .006 |
| A2 | 0.80 | 1.05 | .032 | .041 |
| b | 0.19 | 0.30 | .007 | .012 |
| c | 0.09 | 0.20 | .0035 | .008 |
| D | SEE VARIATIONS | | SEE VARIATIONS | |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | .169 | .177 |
| e | 0.65 BASIC | | 0.0256 BASIC | |
| L | 0.45 | 0.75 | .018 | .030 |
| N | SEE VARIATIONS | | SEE VARIATIONS | |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | .004 |

VARIATIONS

| N | D mm. | | D (inch) | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 28 | 9.60 | 9.80 | .378 | .386 |

Reference Doc.: JEDEC Publication 95, MO-153

10-0035

## Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---|---|---|---|
| 9DB401CGLF | Tubes | 28-pin TSSOP | 0 to +70°C |
| 9DB401CGLFT | Tape and Reel | 28-pin TSSOP | 0 to +70°C |
| 9DB401CFLF | Tubes | 28-pin SSOP | 0 to +70°C |
| 9DB401CFLFT | Tape and Reel | 28-pin SSOP | 0 to +70°C |

**"LF" denotes Pb Configuration, RoHS compliant.**
**"C" is the device revision designator (will not correlate to the datasheet revision)**

## Revision History

| Rev. | Issue Date | Description | Page # |
|------|-----------|-------------|--------|
| 0.1 | 4/21/2005 | Changed Ordering Information from"LN" to "LF". | 14,15 |
| A | 8/15/2005 | 1. Updated LF Ordering Information to RoHS Compliant.<br>2. Release to web. | 14-15 |
| B | 9/7/2006 | Updated Electrical Characteristics. | Various |
| C | 5/22/2007 | Updated Polarity Inversion Table. | 2 |
| D | 2/28/2008 | Added Input Clock Specs | 6 |
| E | 3/18/2008 | Fixed typo in clock Input Parameters | 6 |
| F | 9/5/2008 | 1. Updated Electrical Characteristics to add propagation delay and phase noise information.<br>2. Added SMBus electrical characteristics<br>3. Added foot note about DIF input running in order for the SMBus interface to work<br>4. Added foot note to Byte 1 about functionality of OE bits and OE pins.<br>5. Updated Block Diagram to correctly indicate the OE pins. | Various |
| G | 11/18/2010 | Updated Block Diagram | 1 |
| H | 1/27/2011 | Updated Termination Figure 4 | 8 |

## IMPORTANT NOTICE AND DISCLAIMER

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