Frequency Generator & Integrated Buffers for Celeron & PII/III™

Recommended Application:

Mobile applications

Output Features:

- 3 CPU (2.5V) (100MHz)
- 7 SDRAM (3.3V) (1 free running SDCLK) (100MHz)
- 7 PCI (3.3 V) @ 33.3MHz, (1 free running)
- 2 IOAPIC (2.5V) @ 33.3 MHz
- 2 (3.3V) @ 48 MHz
  - 1 USB clock (3.3V) (48MHz non-SSC)
  - 1 DOT clock (3.3V) (48MHz non-SSC)
- 1 VCH clock (3.3V) 48 MHz non-SSC, or 66 MHz CPU-SSC
- 3 3V66 (3.3V) (66MHz)
- 1 REF (3.3V) @ 14.318 MHz

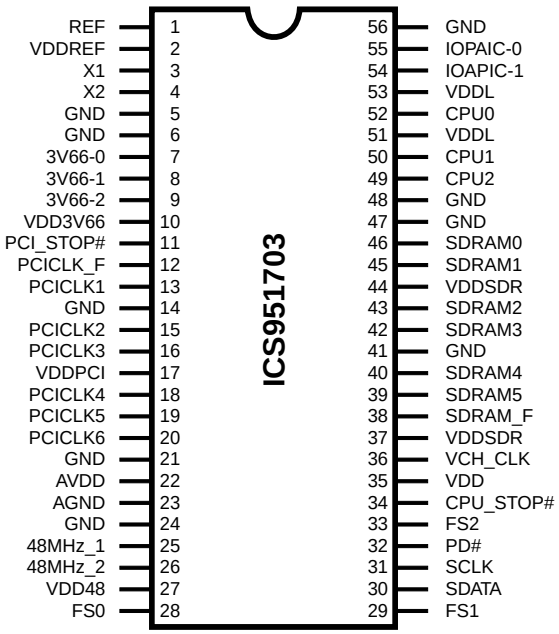
Features:

- Supports spread spectrum modulation, 0 to -0.5% down spread.
- Support power management: PCI_STOP#, CPU_STOP# and power down Mode
- I^2C interface for clock output control

Skew Specifications:

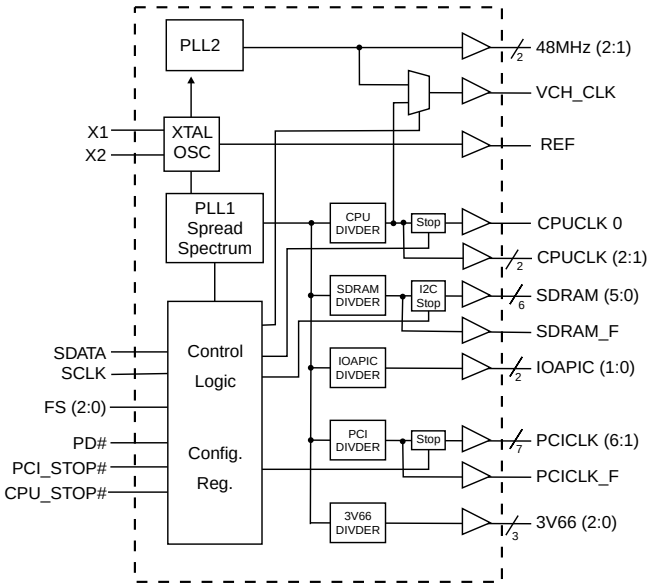
- CPU-CPU <150psec
- PCI-PCI <500psec
- SDRAM-SDRAM <250psec
- CPU-SDRAM <350psec
- CPU-PCI 1-4nsec
- CPU-3V66 1-4nsec

Pin Configuration



56-Pin 300-mil SSOP and TSSOP

Block Diagram



Functionality

FS2	FS1	FS0	Function
0	X	0	Tristate
0	X	1	Test
1	0	1	Active CPU = 100MHz SDRAM = 100MHz

Power Groups

VDD48= 48MHz, PLL2
AVDD = Analog VDD for CPU PLL
VDDREF = REF, Xtal Osc.

General Description

The **ICS9250-31** is a single chip clock solution for mobile applications, providing all necessary clock signals for such a system.

Spread spectrum may be enabled through I^2C programming. Spread spectrum typically reduces EMI by 8dB to 10 dB. This simplifies EMI qualification without resorting to board design iterations or costly shielding. The ICS9250-31 employs a proprietary closed loop design, which tightly controls the percentage of spreading over process and temperature variations.

Pin Configuration

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	REF	OUT	3.3V, 14.318MHz reference clock output.
3	X1	IN	Crystal input.
4	X2	OUT	Crystal output.
5, 6, 14, 21, 23, 24, 41, 47, 48, 56	GND	PWR	Ground
9, 8, 7	3V66 (2:0)	OUT	3.3V Fixed 66MHz clock outputs for HUB
2, 10, 17, 22, 27, 35, 37, 44	VDD	PWR	3.3V power supply
11	PCI_STOP#	IN	Stops all PCICLKs besides the PCICLK_F clocks at logic 0 level, when input low
12	PCICLK_F	OUT	Free running 3.3V PCI clock output not affected by PCI_STOP#
20, 19, 18, 16, 15, 13	PCICLK (6:1)	OUT	3.3V PCI clock outputs
25	48MHz_1	OUT	3.3V Fixed 48MHz clock outputs for USB
26	48MHz_2	OUT	3.3V fixed 48MHz clock output. Stronger output for graphics/video interface (DOT) (minimum 1V/ns edge rate)
33, 29, 28	FS (2:0)	IN	Function Select pins. Determines CPU frequency, all output functionality. Please refer to Functionality table on page 3.
30	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
31	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
32	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
34	CPU_STOP#	IN	Stops CPUCLK[0] at logic 0 level, when input low. CPUCLK(2:1) are not affected.
36	VCH_CLK	OUT	3.3V selectable 48MHz non-SSC or 66.67MHz SSC clock output.
39, 40, 42, 43, 45, 46	SDRAM (5:0)	OUT	3.3V output running 100MHz. All SDRAM outputs can be turned off through I^2C
38	SDRAM_F	OUT	3.3V free running 100MHz SDRAM, cannot be turned off through I^2C
49,50,52	CPUCLK (2:0)	OUT	2.5V Host bus clock output 100MHz depending on FS (2:0) pins.
51, 53	VDDL	PWR	2.5V power supply for CPU & IOAPIC
54, 55	IOAPIC (1:0)	OUT	2.5V clock outputs running at 33.3MHz.

Maximum Allowed Current

Condition	Max 2.5V supply consumption Max discrete cap loads, Vddq2 = 2.625V All static inputs = Vddq3 or GND	Max 3.3V supply consumption Max discrete cap loads, Vddq2 = 3.465V All static inputs = Vddq3 or GND
Powerdown Mode (PWRDWN# = 0)	≤1mA	≤1mA
Full Active 66MHz FS[1:0] = 00	60mA	170mA
Full Active 100MHz FS[1:0] = 01	75mA	170mA
Full Active 133MHz FS[1:0] = 10	90mA	170mA
CPU to SDRAM @ 133MHz FS[1:0] = 11	90mA	185mA

Clock Enable Configuration

PD#	CPUCLK	SDRAM	IOAPIC	66MHz	PCICLK	VCH	REF, 48MHz	Osc	VCOs
0	LOW	LOW	LOW	LOW	LOW	LOW	LOW	OFF	OFF
1	ON	ON	ON	ON	ON	ON	ON	ON	ON

Functionality Table

FS2	FS1	FS0	CPU MHz	SDRAM MHz	3V66 MHz	PCI MHz	48MHz	REF MHz	IOAPIC MHz
0	X	0	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate	Tristate
0	X	1	TCLK/2	TCLK/2	TCLK/3	TCLK/6	TCLK/2	TCLK	TCLK/6
1	0	1	100	100	66	33	48	14.318	33

Byte 0: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	36	VCH_CLK	1	(Active/Inactive)*
Bit 6	49	CPU2	1	(Active/Inactive)
Bit 5	50	CPU1	1	(Active/Inactive)
Bit 4	52	CPU0	1	(Active/Inactive)
Bit 3	<>	Spread Spectrum (1=enabled)	1	(Active/Inactive)
Bit 2	26	48MHz_2	1	(Active/Inactive)
Bit 1	25	48MHz_1	1	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Notes:
Reserved bits must be wirtten as "0".
***Readback of the bit is always "0".**

Byte 1: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	Reserved	0	(Active/Inactive)
Bit 6	-	Reserved	0	(Active/Inactive)
Bit 5	39	SDRAM5	1	(Active/Inactive)
Bit 4	40	SDRAM4	1	(Active/Inactive)
Bit 3	42	SDRAM3	1	(Active/Inactive)
Bit 2	43	SDRAM2	1	(Active/Inactive)
Bit 1	45	SDRAM1	1	(Active/Inactive)
Bit 0	46	SDRAM0	1	(Active/Inactive)

Byte 2: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	9	3V66-2	1	(Active/Inactive)
Bit 6	8	3V66-1	1	(Active/Inactive)
Bit 5	7	3V66-0	1	(Active/Inactive)
Bit 4	-	Reserved	0	(Active/Inactive)
Bit 3	-	Reserved	0	(Active/Inactive)
Bit 2	-	Reserved	0	(Active/Inactive)
Bit 1	-	Reserved	0	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default
3. Undefined bit can be wirtten with either a "1" or "0".

Byte 3: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	-	Reserved	0	(Active/Inactive)
Bit 6	20	PCICLK6	1	(Active/Inactive)
Bit 5	19	PCICLK5	1	(Active/Inactive)
Bit 4	18	PCICLK4	1	(Active/Inactive)
Bit 3	16	PCICLK3	1	(Active/Inactive)
Bit 2	15	PCICLK2	1	(Active/Inactive)
Bit 1	13	PCICLK1	1	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Byte 4: Control Register
(1 = enable, 0 = disable)

Bit	Pin#	Name	PWD	Description
Bit 7	36	VCH_CLK	0	0 = 48MHz non-SSC 1 = 66MHz SSC
Bit 6	-	Reserved	0	(Active/Inactive)
Bit 5	-	Reserved	0	(Active/Inactive)
Bit 4	-	Reserved	0	(Active/Inactive)
Bit 3	-	Reserved	0	(Active/Inactive)
Bit 2	-	Reserved	0	(Active/Inactive)
Bit 1	-	Reserved	0	(Active/Inactive)
Bit 0	-	Reserved	0	(Active/Inactive)

Notes:

1. Inactive means outputs are held LOW and are disabled from switching. These outputs are designed to be configured at power-on and are not expected to be configured during the normal modes of operation.
2. PWD = Power on Default

Absolute Maximum Ratings

Core Supply Voltage ..... 4.6 V
I/O Supply Voltage 3.6V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C
Case Temperature ..... 115°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Group Timing Relationship Table[1]

Group	CPU 100MHz SDRAM 100MHz	
	Offset	Tolerance
CPU to SDRAM	0.0ns	350ps
CPU to 3V66	1-4ns	
3V66 to PCI	0.0ns	500ps
CPU to PCI	1-4ns	

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70C; Supply Voltage V_{DD} = 3.3 V +/-5%, VDDL = 2.5 V +/-5%(unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD}+0.3	V
Input Low Voltage	V_{IL}		V_{SS}-0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}	-5		5	µA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			µA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			µA
Operating Supply Current for 3.3V	$I_{DD3.3OP}$	CPU=SD=100MHz		230	250	mA
Power down Current for 3.3V	$I_{DD3.3PD}$			0.085	1	mA
Operating Supply Current for 2.5V	$I_{DD2.5OP}$	CPU=SD=100MHz		32	50	mA
Power down Current for 2.5V	$I_{DD2.5PD}$			1	10	µA
Input Frequency	F_i	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	L_{pin}				7	nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition time[1]	T_{trans}	To 1st crossing of target frequency			3	ms
Settling time[1]	T_s	From 1st crossing to 1% target frequency			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target frequency			3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPU

T_A = 0 - 70C; VDDL=2.5V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	27	45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	27	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 2.375 V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$ = 1.2 V, $V_{OL@MAX}$ = 0.3 V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	0.94	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.07	1.6	ps
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	50.6	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		74	150	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V		180	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	22	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	22	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.3	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.4	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	47.5	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		117	175	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		160	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - IOAPIC

T_A = 0 - 70C; VDDL=2.5V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	27	45	Ω
Output Impedance	R_{DSN2B}[1]	$V_O = V_{DD}*(0.5)$	13.5	27	45	Ω
Output High Voltage	V_{OH2B}	I_{OH} = -1 mA	2			V
Output Low Voltage	V_{OL2B}	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH2B}	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 2.375 V	-27		-27	mA
Output Low Current	I_{OL2B}	$V_{OL@MIN}$ = 1.2 V, $V_{OL@MAX}$ = 0.3 V	27		30	mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.1	1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.15	1.6	ps
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	45	49.5	55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V		10	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.25 V		80	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - SDRAM

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	10	15	24	Ω
Output Impedance	R_{DNP1}[1]	$V_O = V_{DD}*(0.5)$	10	15	24	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 2.0 V, $V_{OH@MAX}$ = 3.135 V	-54		-46	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.0 V, $V_{OL@MAX}$ = 0.4 V	54		53	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4	1.1	1.6	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4	1.3	1.6	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		50	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		150	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - PCI

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	22	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	22	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.35	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.3	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50.5	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		150	500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		110	500	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF, 48MHz

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20	33	60	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	20	33	60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-29		-23	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	29		27	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4V	0.5	1.8	4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.75	4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	51.5	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			N/A	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		600	1000	ps

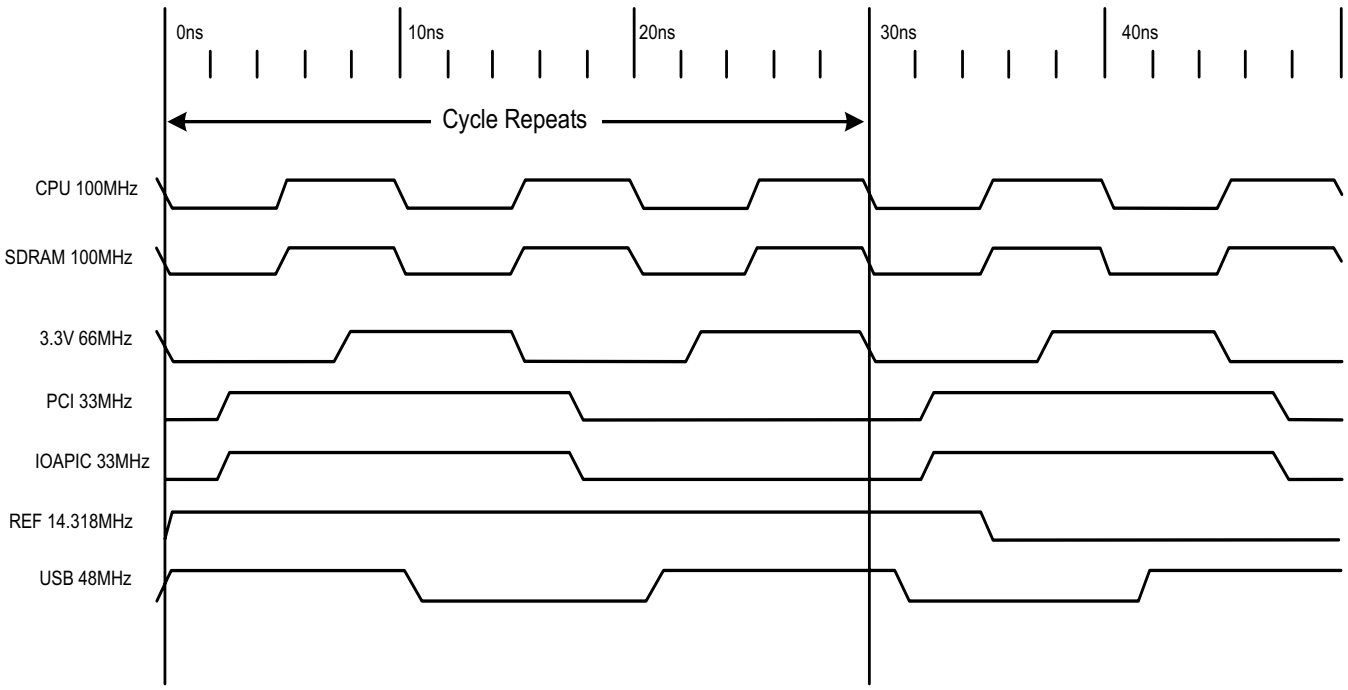
[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - VCH

T_A = 0 - 70C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

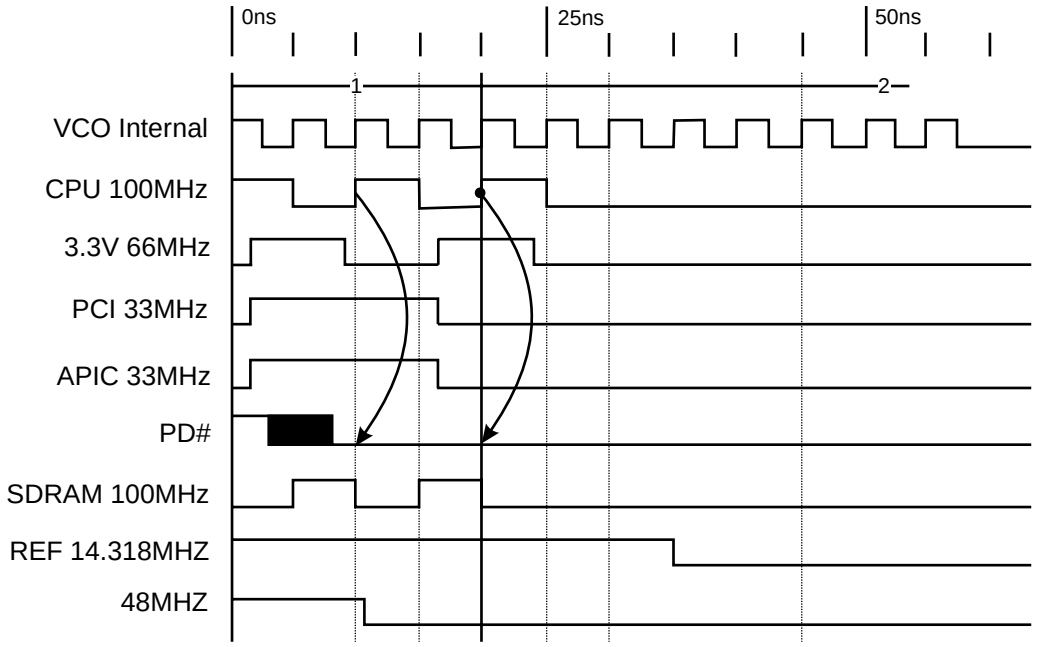
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12	22	55	Ω
Output Impedance	R_{DSN1}[1]	$V_O = V_{DD}*(0.5)$	12	22	55	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.55	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, $V_{OH@MAX}$ = 3.135 V	-33		-33	mA
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V, $V_{OL@MAX}$ = 0.4 V	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.8	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50.6	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V			N/A	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		220	250	ps

[1]Guaranteed by design, not 100% tested in production.



Group Offset Waveforms

Power Down Waveform



Note

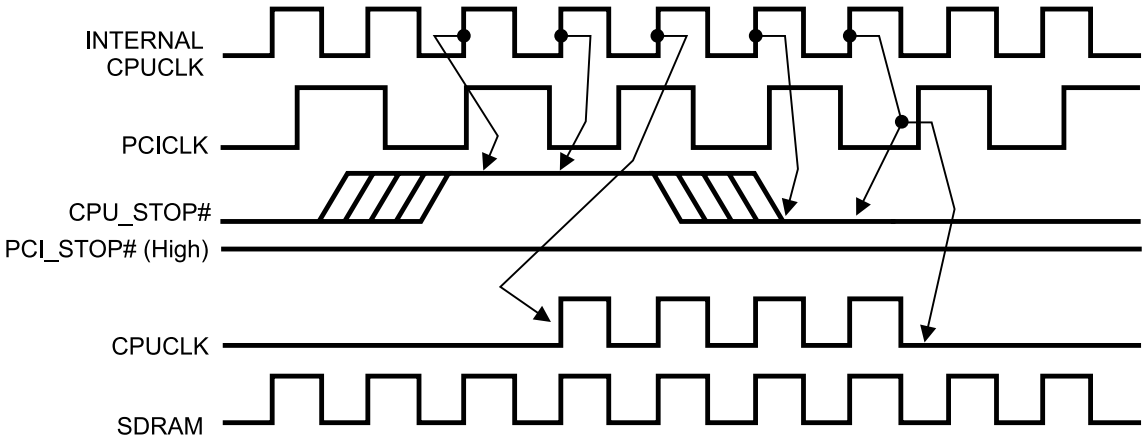
1. After PD# is sampled active (Low) for 2 consective rising edges of CPUCLKs, all the output clocks are driven Low on their next High to Low tranistiion.

2. Power-up latency <3ms.

3. Waveform shown for 100MHz

CPU_STOP# Timing Diagram

CPU_STOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPU clocks for low power operation. CPU_STOP# is synchronized by the **ICS951703**. The minimum that the CPU clock is enabled (CPU_STOP# high pulse) is 100 CPU clocks. All other clocks will continue to run while the CPU clocks are disabled. The CPU clocks will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPU clock on latency is less than 4 CPU clocks and CPU clock off latency is less than 4 CPU clocks.

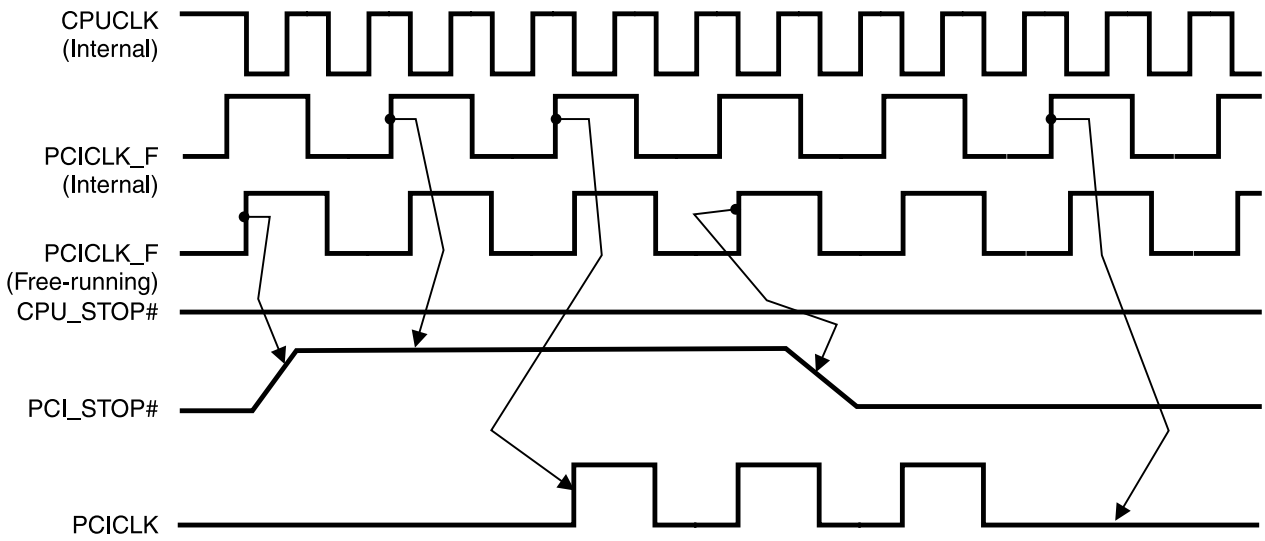


Notes:

1. All timing is referenced to the internal CPU clock.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPU clocks inside the ICS951703.
3. All other clocks continue to run undisturbed. (including SDRAM outputs).

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS951703**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS951703** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS951703 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS951703.
3. All other clocks continue to run undisturbed.
4. CPU_STOP# is shown in a high (true) state.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.
For more information, contact ICS for an I²C programming application note.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 5
- ICS clock will ***acknowledge*** each byte ***one at a time***.
- Controller (host) sends a Stop bit

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Stop Bit	

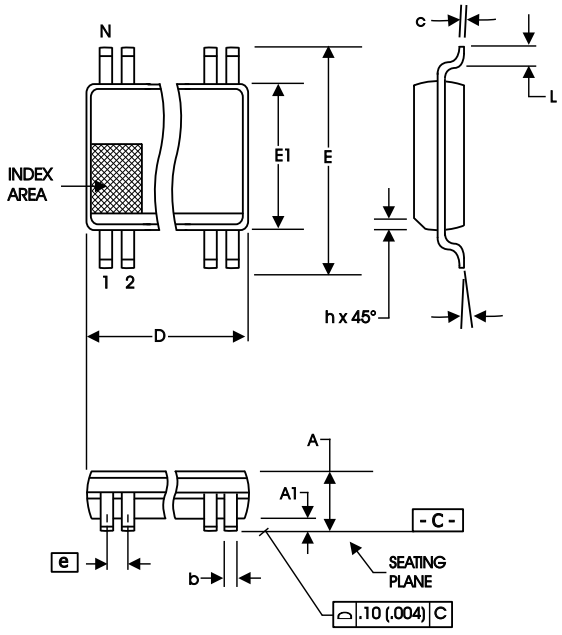
How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 5***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

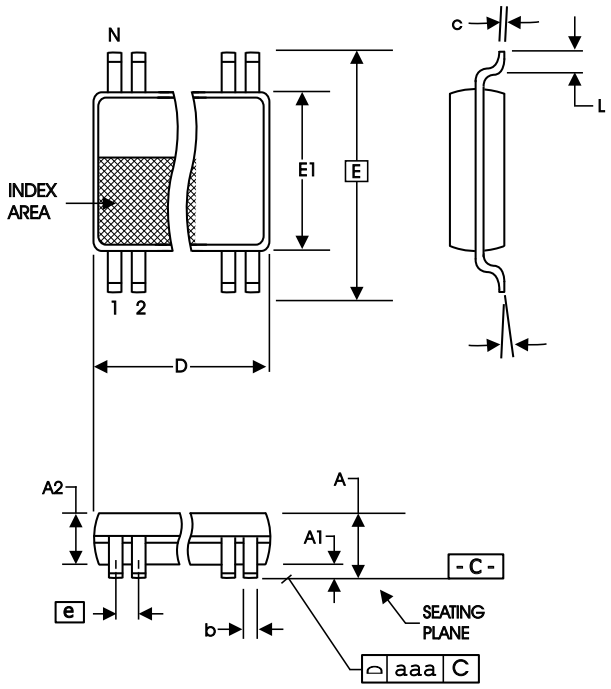
Ordering Information

ICS951703yF-T

Example:

ICS XXXXXX y F - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

'ARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

Ordering Information

ICS951703yG-T

Example:

ICS XXXXXX y G - PPP - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  G=TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

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