Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

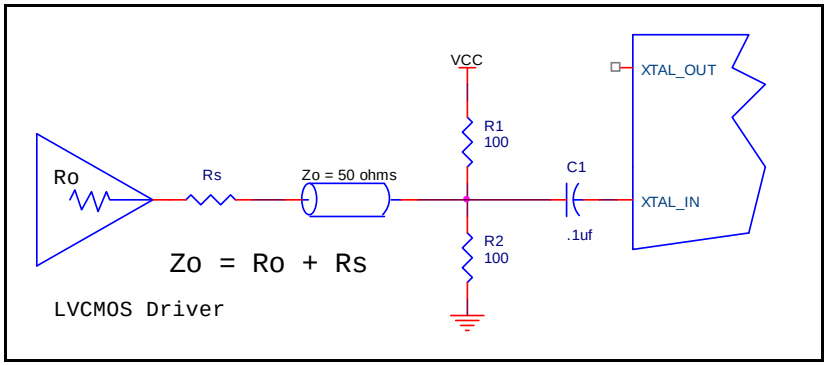


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

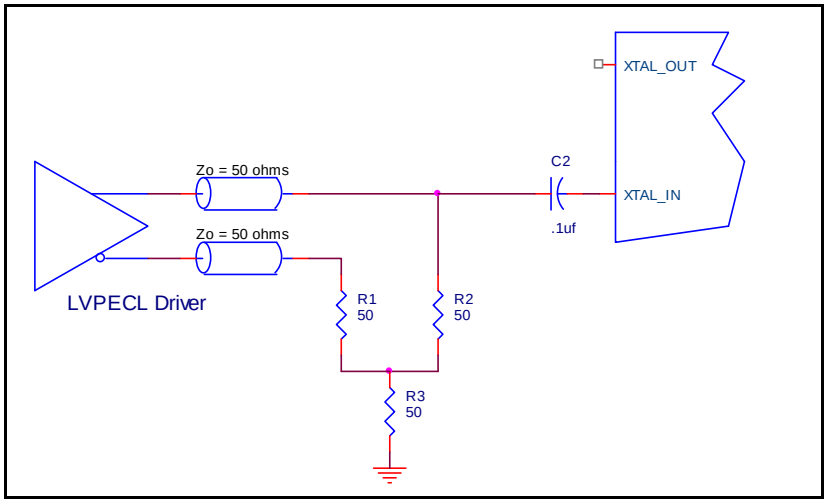


Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

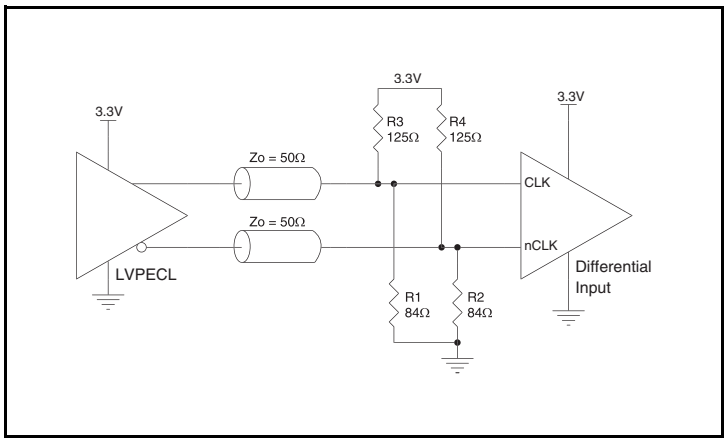


Figure 3A. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

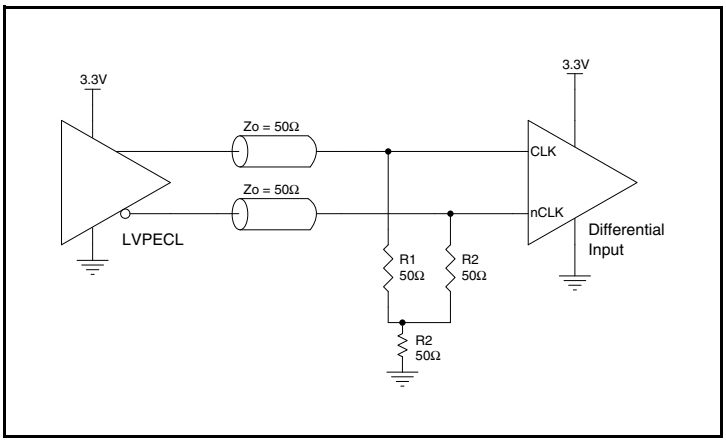


Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

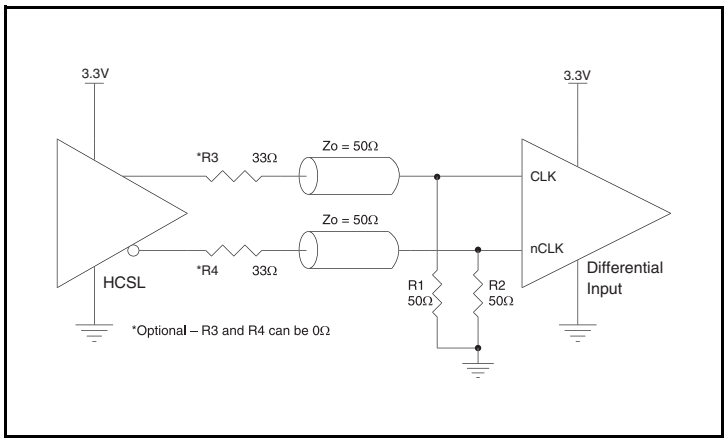


Figure 3C. CLK/nCLK Input Driven by a 3.3V HCSL Driver

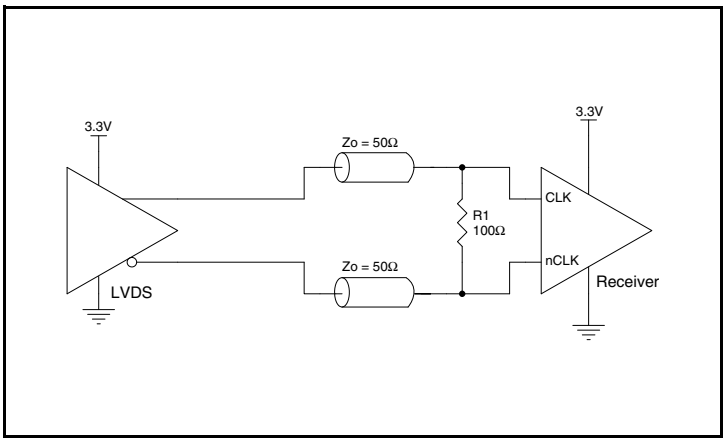


Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver

2.5V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4D* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

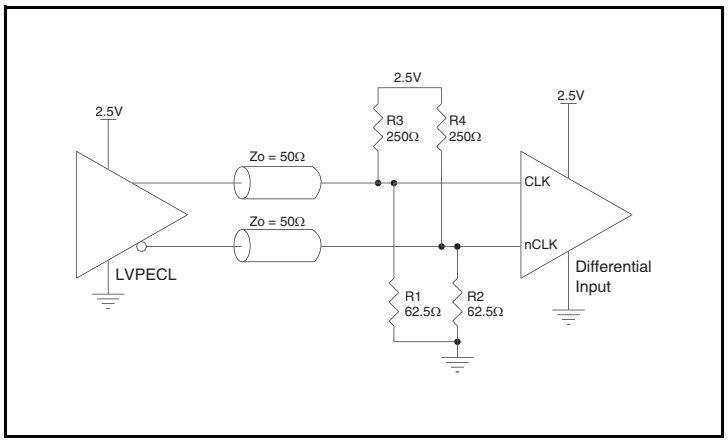


Figure 4A. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

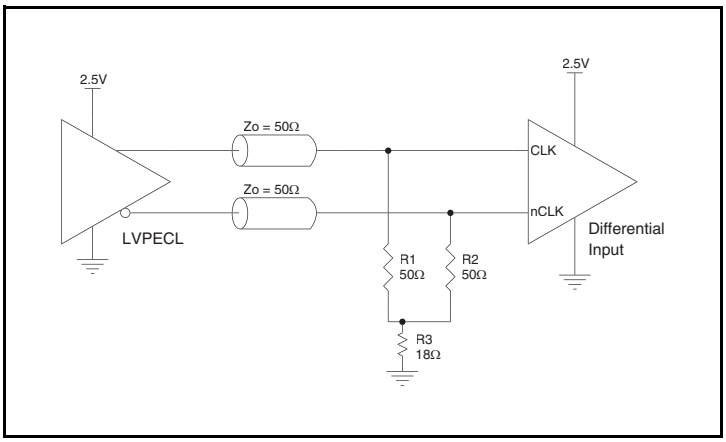


Figure 4B. CLK/nCLK Input Driven by a 2.5V LVPECL Driver

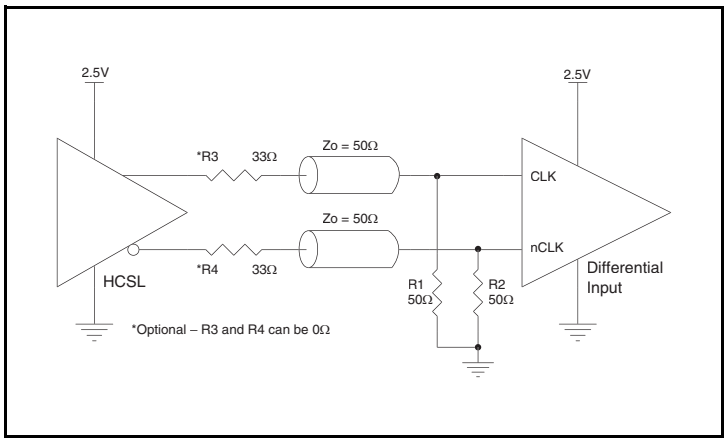


Figure 4C. CLK/nCLK Input Driven by a 2.5V HCSL Driver

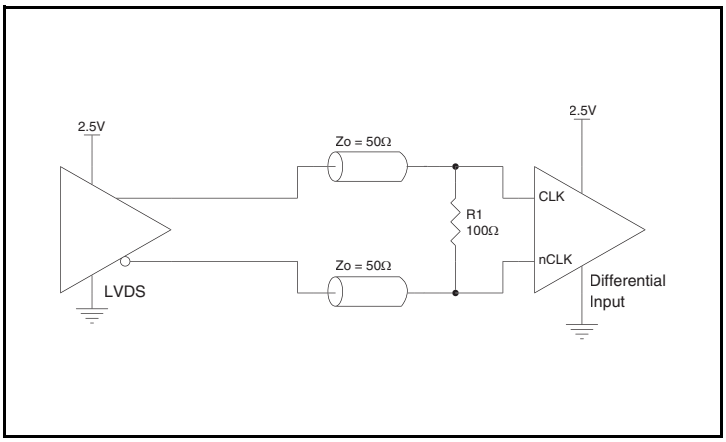


Figure 4D. CLK/nCLK Input Driven by a 2.5V LVDS Driver

LVDS Driver Termination

For a general LVDS interface, the recommended value for the termination impedance (Z_T) is between 90W and 132W. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100W parallel resistor at the receiver and a 100W differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface mounted and must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in *Figure 5A* can be used with either type of output structure. *Figure 5B*, which can also be used with both output types, is an optional termination with center tap capacitance to help filter common mode noise. The capacitor value should be approximately 50pF. If using a non-standard termination, it is recommended to contact IDT and confirm if the output structure is current source or voltage source type. In addition, since these outputs are LVDS compatible, the input receiver's amplitude and common-mode input range should be verified for compatibility with the output.

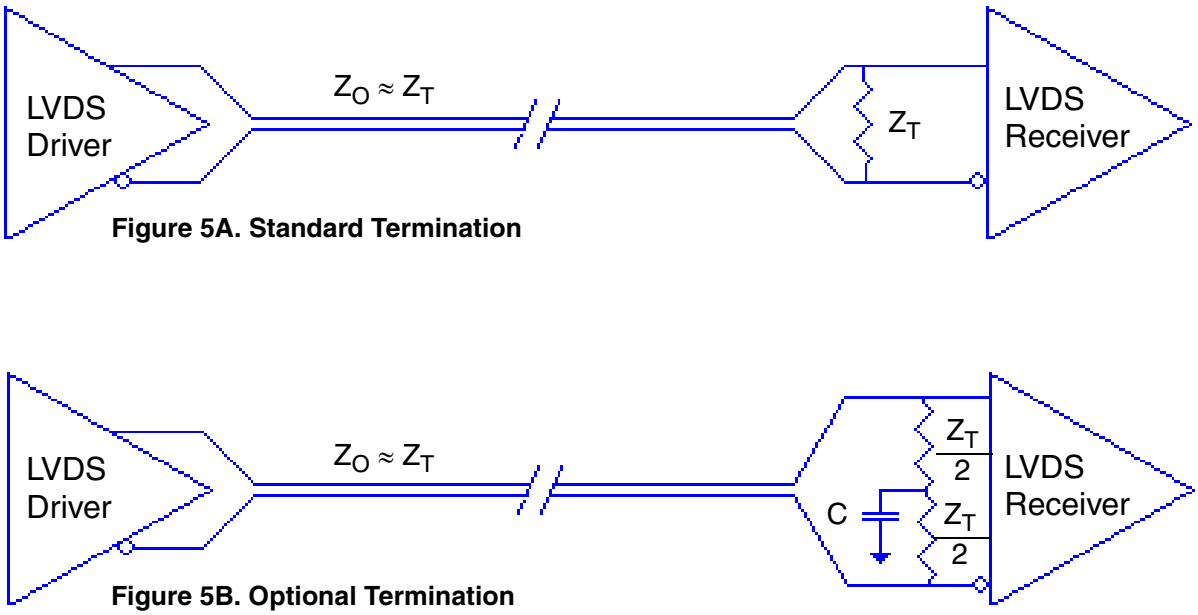


Figure 5A. Standard Termination

Figure 5B. Optional Termination

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50W transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 6A and 6B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

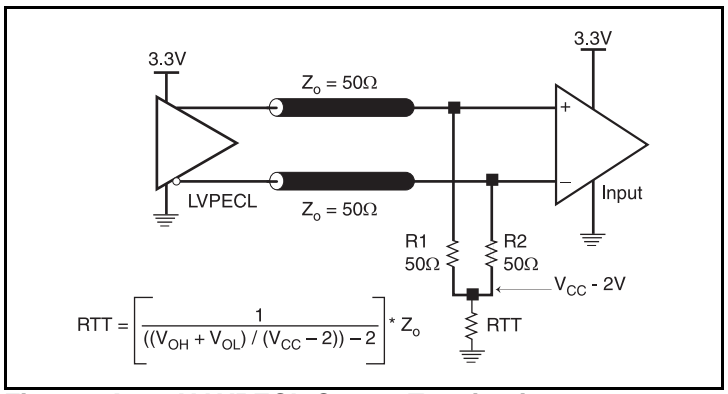


Figure 6A. 3.3V LVPECL Output Termination

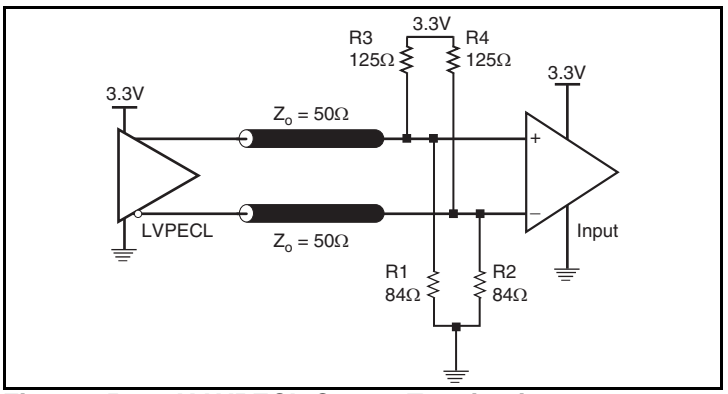


Figure 6B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 7A and *Figure 9B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50W to V_{CCO} – 2V. For V_{CCO} = 2.5V, the V_{CCO} – 2V is very close to ground level. The R3 in Figure 7B can be eliminated and the termination is shown in *Figure 7C.*

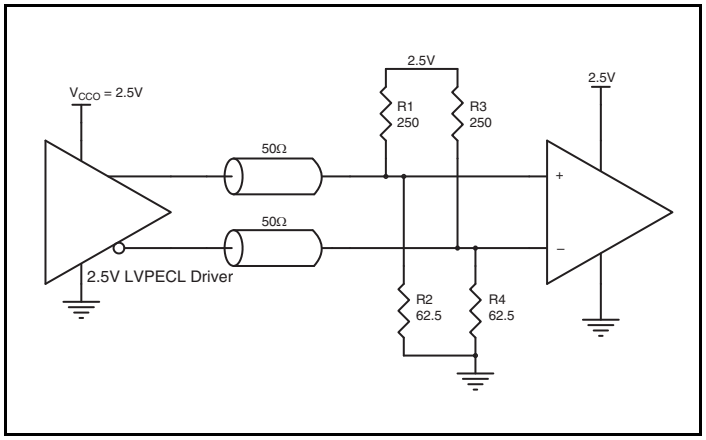


Figure 7A. 2.5V LVPECL Driver Termination Example

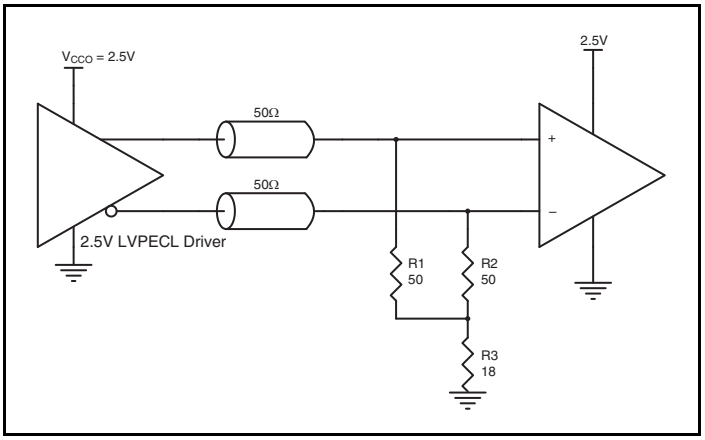


Figure 7B. 2.5V LVPECL Driver Termination Example

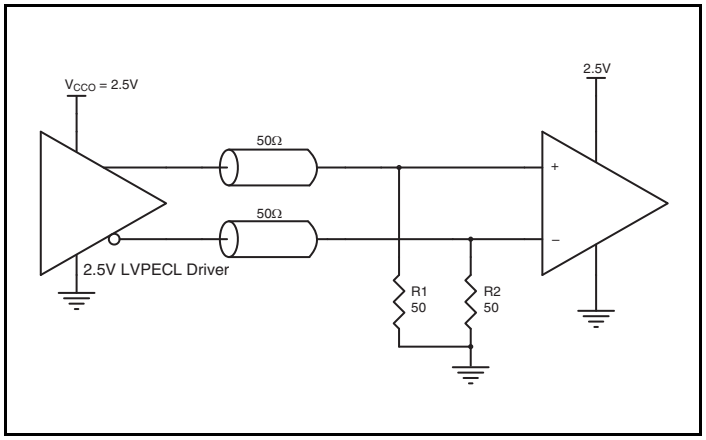


Figure 7C. 2.5V LVPECL Driver Termination Example

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 8.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

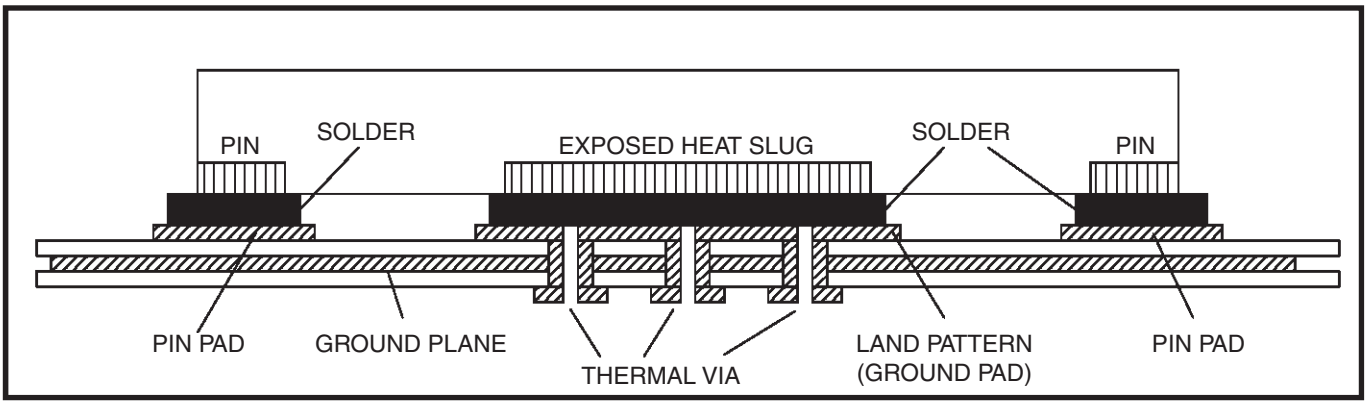


Figure 8. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Layout

Figure 9 (next page) shows an example of IDT8T49N006I application schematic. The schematic focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

In this example, the device is operated at $V_{CC} = V_{CCO} = V_{CCA} = 3.3V$. The CLK, nCLK inputs are provided by a 3.3V LVPECL driver and depicted with a Y-termination rather than the standard four resistor V_{CC} - 2V Thevinin termination for reasons of minimum termination power and layout simplicity. Three examples of LVPECL terminations are shown for the outputs to demonstrate mixing of LVPECL termination design options.

As with any high speed analog circuitry, the power supply pins are vulnerable to noise. To achieve optimum jitter performance, power supply isolation is required. The IDT8T49N006I provides separate power supplies to isolate from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1uF capacitor in each power pin filter should be placed on the device side of the PCB and the other components can be placed on the opposite side. Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices.

The V_{CC} and V_{CCO} filters start to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

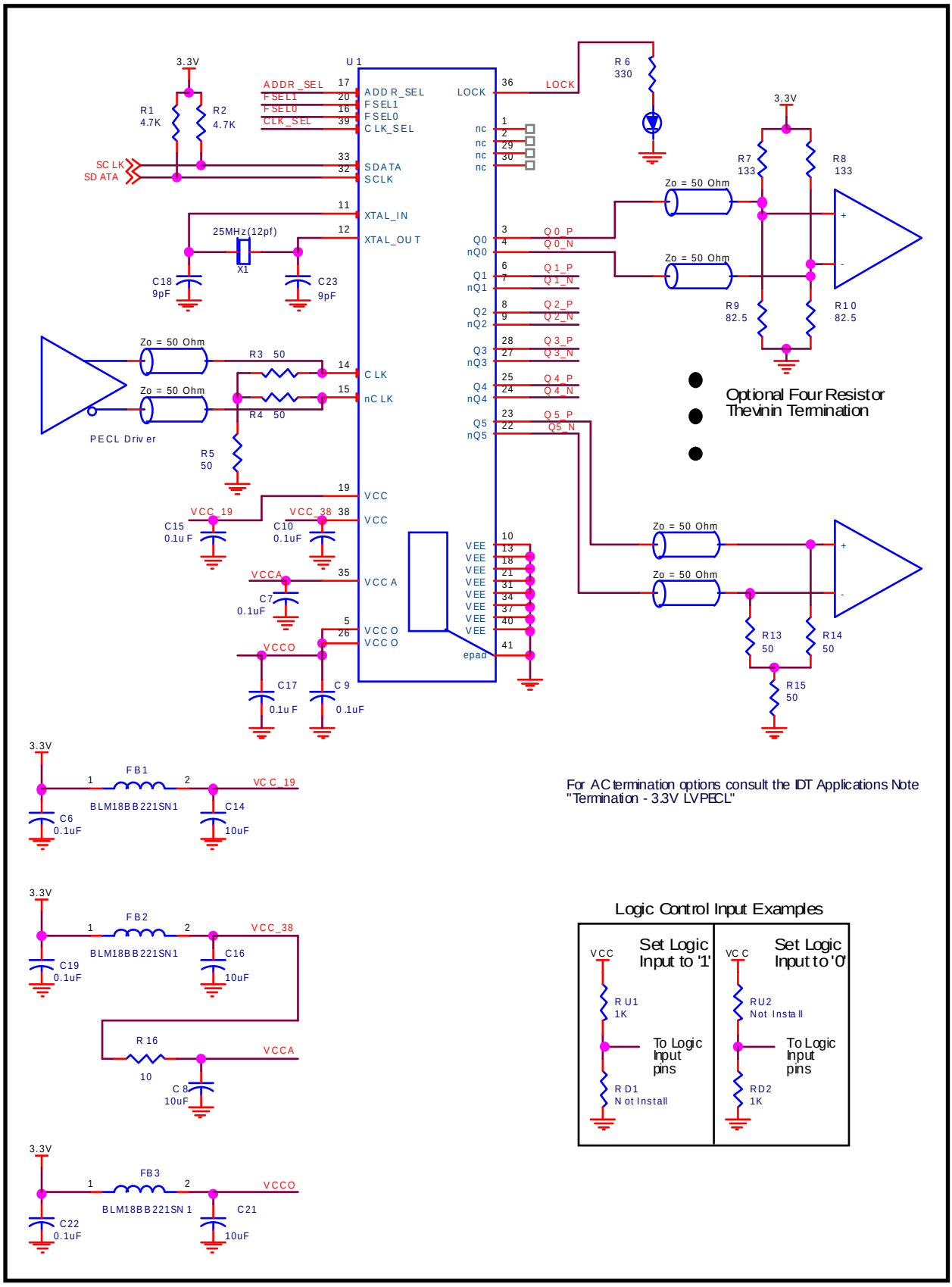


Figure 9. IDT8T49N006I Application Schematic

PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

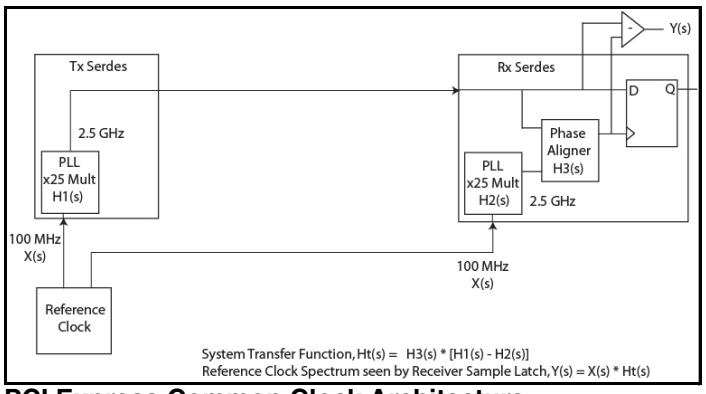
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

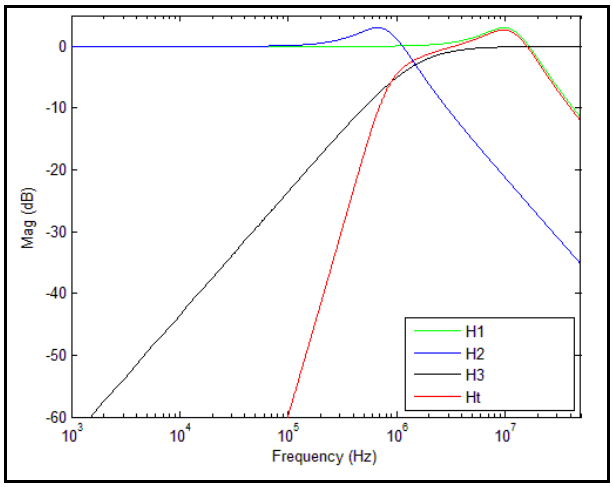
$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].



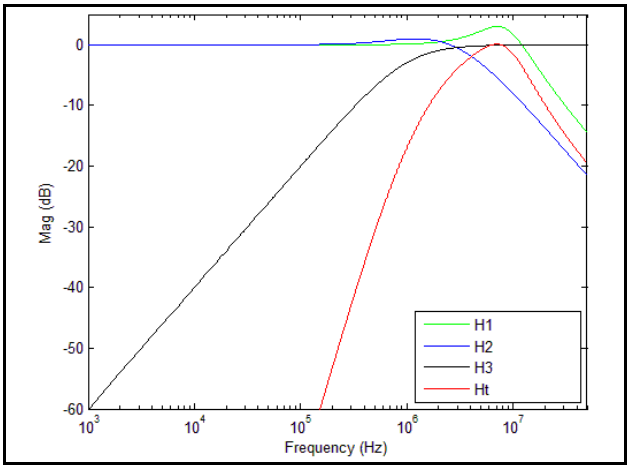
PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

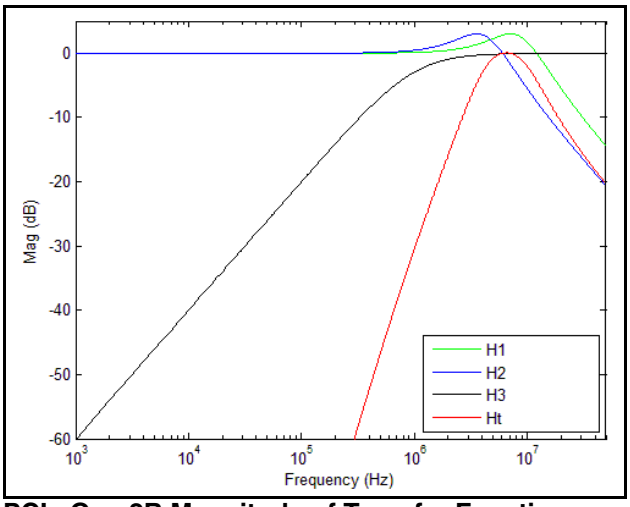


PCIe Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

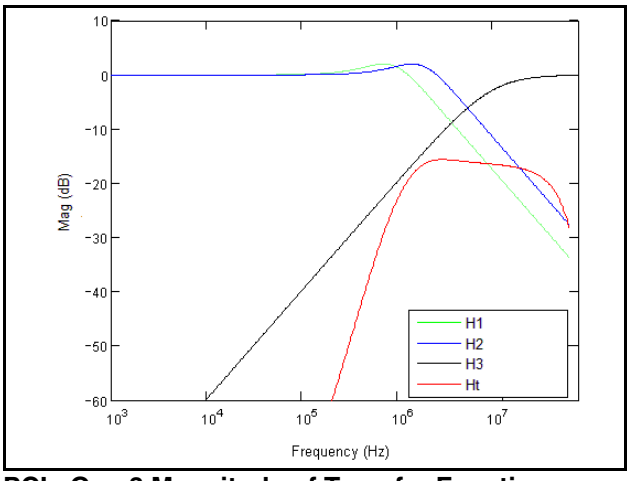


PCIe Gen 2A Magnitude of Transfer Function



PCIe Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



PCIe Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

LVPECL Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N006I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N006I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 208mA = **720.72mW**
- Power $(outputs)_{MAX}$ = **31.55mW/Loaded Output pair**
  If all outputs are loaded, the total power is 6 * 31.55mW = **189.3mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 720.72W + 189.3mW = **910.02W**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = q_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

q_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance q_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.910W * 32.4°C/W = 114.5°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance q_{JA} for 40-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**3**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the LVPECL output pair.

LVPECL output driver circuit and termination are shown in *Figure 10.*

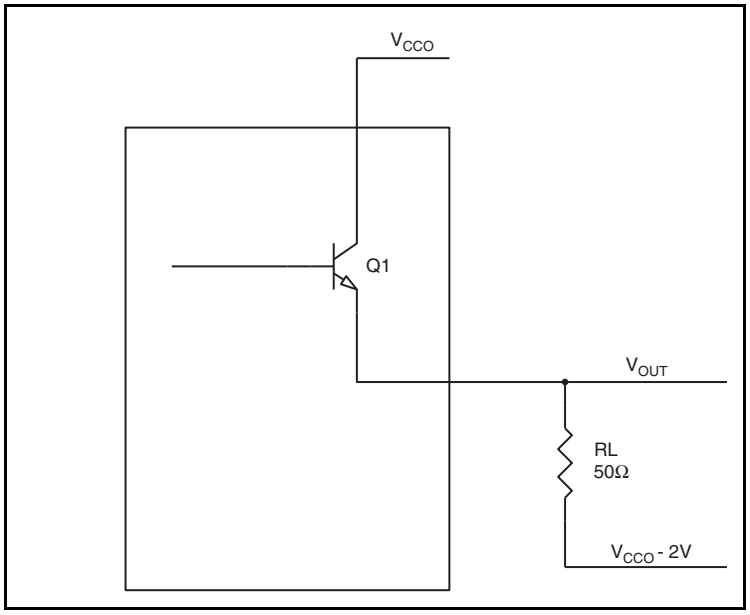


Figure 10. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50W load, and a termination voltage of $V_{CC\ O}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.75V}$
  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.75V}$
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.6V}$
  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.6V}$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.75V)/50W] * 0.75V =$ **18.75mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.6V)/50W] * 1.6V =$ **12.80mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **31.55mW**

LVDS Power Considerations

This section provides information on power dissipation and junction temperature for the IDT8T49N006I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the IDT8T49N006I is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V +5% = 3.465V, which gives worst case results.

- Power (core)$_{MAX}$ = V_{CC_MAX} * (I_{CC_MAX} + I_{CCA_MAX}) = 3.465V * (125mA + 32mA) = **544.05mW**
- Power (outputs)$_{MAX}$ = V_{CCO_MAX} * I_{CCO_MAX} = 3.465V * 124mA = **433.125mW**

Total Power$_{\_MAX}$ = 544.05mW + 433.125mW = **977.175mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = q_{JA} * Pd_total + T_A

Tj = Junction Temperature

q_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance q_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 32.4°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.977W * 32.4°C/W = 116.7°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 8. Thermal Resistance q_{JA} for 40-Lead VFQFN, Forced Convection

θ_{JA} by Velocity			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

Reliability Information

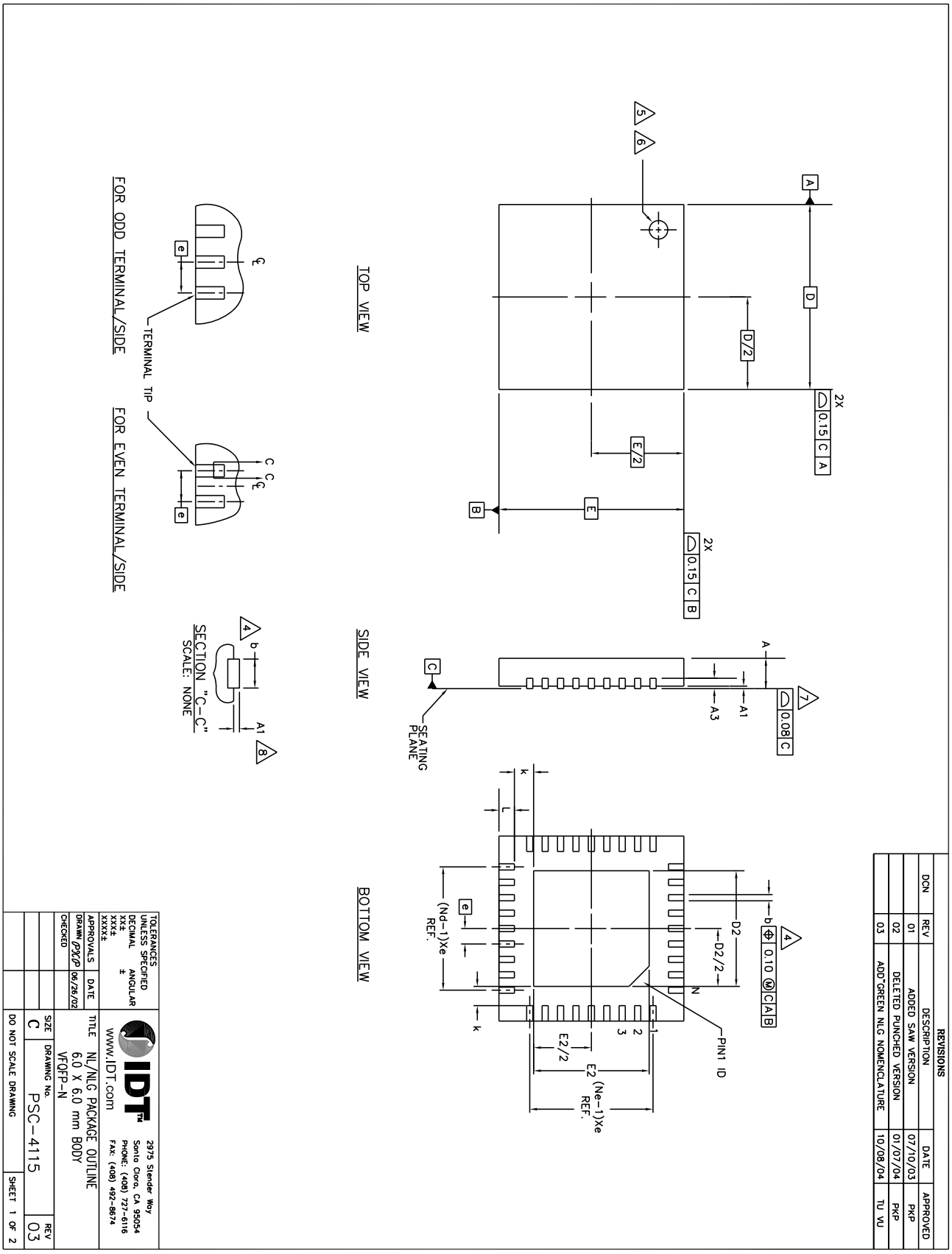
Table 9. q_{JA} vs. Air Flow Table for a 40-Lead VFQFN

θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	32.4°C/W	25.7°C/W	23.4°C/W

Transistor Count

The transistor count for IDT8T49N006I is: 26,856

40-Lead VFQFN Package Outline and Package Dimensions



REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	01	ADDED SAW VERSION	07/10/03	PKP
	02	DELETED PUNCHED VERSION	01/07/04	PKP
	03	ADD"GREEN" NLG NOMENCLTURE	10/08/04	TU VU

SYMBOL	JEDEC VARIATION VJJC-3			NOTE	SYMBOL	JEDEC VARIATION VJJD-5			NOTE
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
e		0.65 BSC			e		0.50 BSC		
N		28		2	N		40		3
Nd		7		2	Nd		10		3
Ne		7		2	Ne		10		3
b	0.25	0.30	0.35	4	b	0.18	0.25	0.30	4
D2		–		10	D2		–		10
E2		–		10	E2		–		10

SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.02	0.05	7
A3		0.20 REF.		
D		6.00 BSC		
E		6.00 BSC		
k	0.20	–	–	
L	0.35	0.40	0.45	

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.30mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. APPLIED TO EXPOSED PAD AND TERMINALS. EXCLUDE EMBEDDED PART OF EXPOSED PAD FROM MEASURING.
8. APPLIED ONLY FOR TERMINALS.
9. THIS OUTLINES CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO-220, VARIATION VJJC-3 & VJJD-5 WITH THE EXCEPTION OF D2 & E2.
10. DIMENSIONS D2 & E2 VARY DEPENDING ON DEVICE, SUPPLIER, ETC.

40-Lead VFQFN, D2/E2 EPAD Dimensions: 4.65mm x 4.65mm

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ± XXX± XXXX±	IDT™ www.IDT.com 2975 Stender Way Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674
APPROVALS DATE DRAWN PSC 06/26/02 CHECKED	TITLE NL/NLG PACKAGE OUTLINE 6.0 X 6.0 mm BODY VFQFP-N
	SIZE C · DRAWING No. PSC-4115 · REV 03
	DO NOT SCALE DRAWING · SHEET 2 OF 2

Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8T49N006A-dddNLGI	IDT8T49N006A-dddNLGI	“Lead-Free” 40-Lead VFQFN	Tray	-40°C to 85°C
8T49N006A-dddNLGI8	IDT8T49N006A-dddNLGI	“Lead-Free” 40-Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: For the specific -ddd order codes, refer to the document *Programmable FemtoClock® NG Product Ordering Guide*.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T10	37	Ordering Information Table - changed Shipping Packaging from 2500 Tape & Reel to 5000 Tape & Reel.	4/23/12
A	T1	3	Pin Description Table - corrected pin numbering for pins “nc” and “Q[3:5], nQ[3:5]”.	6/28/12
A	T10	11, 39 39	Changed name of the *IDT8T49N00xI Programmable FemtoClock® NG Product Ordering Information* document to *Programmable FemtoClock® Ordering Product Information* Deleted quantity from Tape & Reel, Deleted Lead Free note.	8/21/2013
A	 T10	1 11 39	Changed title to Programmable FemtoClock® NG LVPECL/LVDS Clock Generator with 6-Outputs. Changed text from ‘*Programmable FemtoClock® Ordering Product Information’* to ‘*Programmable FemtoClock® NG Product Ordering Guide’.* Changed Note from ‘*Programmable FemtoClock® Ordering Product Information’* to ‘*Programmable FemtoClock® NG Product Ordering Guide’.*	9/26/13
A	T5	15	Changed the min load capacitance from 12pF to 10pF	10/22/13
A			Corrected orderable part number in the datasheet header.	2/18/14