RENESAS LVDS Clock Oscillator

Product Discontinuance Notice – Last Time Buy Expires on (10/24/2013)

DATA SHEET

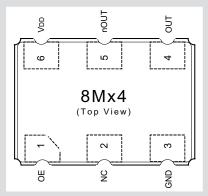
IDT Replacement Part Number: 8N4S270EC-1088CDI, 8N4S270EC-1088CDI8

Fox Replacement Part Number: 771-156.25-74

ICS8MG4-156.250

LOW JITTER, HIGH FREQUENCY XTAL OSCILLATOR

- Stable, ultra low jitter, LVDS clock generation
- For Gigabit Ethernet, Fibre Channel, PCI-Express™, other applications
- · Clock output frequency: 156.25MHz
- · One differential LVDS clock output
- Output Enable (OE) pin (high impedance when low)
- Small 6-pin 5mm x 7mm x 1.5mm SMT ceramic package
- · Low profile package allows back-side PCB mounting
- · Pb-free RoHS compliant (by default; no additional code required)
- 3.3V device power supply options
- Commercial (0 to +70 °C) temperature
- Frequency stability of ±50ppm (including initial accuracy, operating temperature variation, supply voltage variation, load variation, reflow drift, and aging for 10 years)
- Low phase jitter 1ps rms (typical) @ 3.3V (12kHz to 20MHz)



6-pin CERHERMETIC 5mm x 7mm x 1.5mm SMT

ELECTRICAL SPECIFICATIONS

Unless stated otherwise, $V_{DD} = 3.3V \pm 5\%$, $T_A = 0^{\circ}C$ to +70°C (commercial)

ltem		Symb-	Specifications						
		ol	Min.	Тур.	Max.	Units	Test Conditions		
DC Characteristi	cs								
Power Supply (V _{DD} , GND pins)	Power Supply Voltage	V _{DD}	3.135	3.3	3.465	V	3.3V operation		
	Power Supply Current	I _{DD}			114	mA	OE = V _{DD,} 3.3V operation		
	Current w/Output Disabled	I _{OED}			0.5	mA	OE = GND		
	Input Capacitance	C _{IN}		4		pF			
Output Enable	Input High Voltage	V _{IH}	0.7 * V _{DD}			V			
(OE pin) LVCMOS/LVTTL	Input Low Voltage	V _{IL}			0.3 * V _{DD}	V			
	Input High Current	I _{IH}			5	μA	$V_{DD} = V_{IN} = 3.465V$		
	Input Low Current	I _{IL}	-150			μA	$V_{DD} = 3.465V, V_{IN} = 0V$		
	Internal Pullup Resistor	R _{PULLUP}		51		kΩ			
Clock Output	Differential Output Voltage	V _{OD}	250		500	mV			
Level (OUT, nOUT)	V _{oD} Magnitude Change	ΔV_{od}			50	mV	100Ω termination between OUT and nOUT.		
LVDS	Offset Voltage	V _{os}	0.96		1.41	V	See Parameter Measurement Information.		
	V _{os} Magnitude Change	Δ V _{os}			150	mV			
AC Characteristi	cs		-						
Output	Output Frequency Range			156.25		MHz	All conditions		
(OUT, nOUT)	Frequency Stability Error	$\Delta \text{ f/f}_{\text{o}}$			±50	ppm p-p	Includes frequency set, V _{DD} , TA and load variation, reflow drift, 10 yr. aging		
	Output Duty Cycle	odc	48		52	%	See Output Duty Cycle Diagram		
	Output Rise/Fall Time	t _R /t _F	200		700	ps	20% to 80% and Rise/Fall Time Diagram in Parameter Measurement Information		
	Oscillator Start-up Time	t _{osc}			10	ms	Time at Min. V _{DD} (3.135V) to be 0s		
	RMS Phase Jitter, Random ¹	tjit (Ø)		1.0		ps rms	3.3V operation		
	Jitter	t _{DS} ²			1.5	ps	Deterministic		
		t _{RS} ²			12	ps	Random, σ of random jitter		
		t _{acc} ²			8	ps	3.3V operation Accumulated Jitter, n = 2 cycles to 50,000 cycles		

NOTE 1: Measured using an Aeroflex PN9500 with a 12kHz to 20MHz integration range. NOTE 2: Measured using a Wavecrest SIA-3000.



PIN DESCRIPTIONS

Number	Name	Туре		Description
1	OE	Input	Pullup	Output enable pin. High Impedance when LOW. LVCMOS/LVTTL interface levels.
2	nc	Unused		No connect.
3	GND	Power		Power supply ground.
4, 5	OUT, nOUT	Output		Differential clock outputs. LVDS interface levels.
6	V _{DD}	Power		Power supply pin.

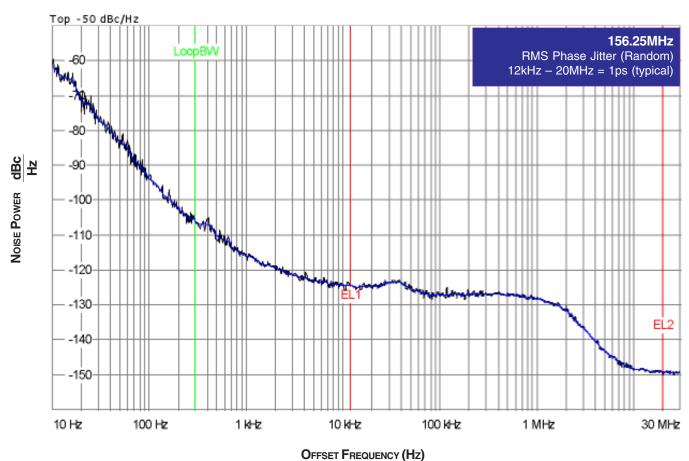
For typical value of internal Pullup resistor, see DC Characteristics.

ABSOLUTE MAXIMUM RATINGS

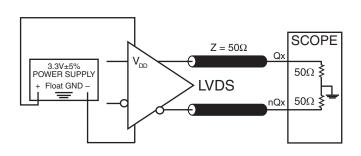
Item	Symbol	Condition	Unit	
Input Voltage	V _i	-0.5 to V _{DD} +0.5	V	
Output Voltage	Vo	-0.5 to V _{DD} +0.5	V	
Positive Supply Voltage	V _{DD}	4.6	V	
Package Thermal Impedence		43	°C/W (0lfpm)	
Storage Temperature	T _s	-40 to +100	°C	

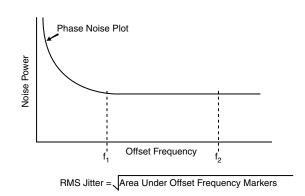
Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Typical Phase Noise at 156.25MHz @ 3.3V



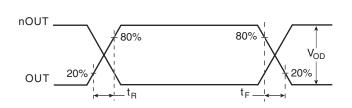
PARAMETER MEASUREMENT INFORMATION

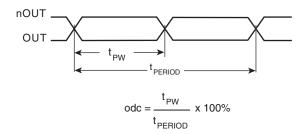




3.3V OUTPUT LOAD ACTEST CIRCUIT

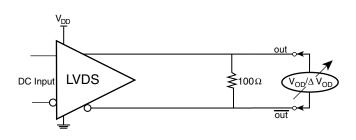
RMS PHASE JITTER



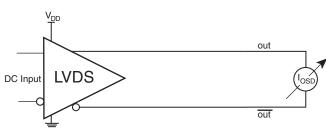


OUTPUT RISE/FALL TIME

OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD

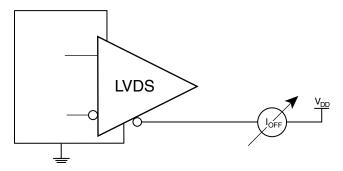


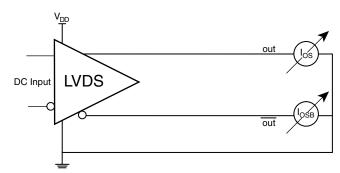
DIFFERENTIAL OUTPUT VOLTAGE SETUP



DIFFERENTIAL OUTPUT SHORT CIRCUIT SETUP

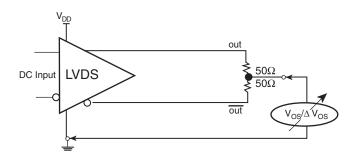
PARAMETER MEASUREMENT INFORMATION, CONTINUED





Power Off Leakage Setup

OUTPUT SHORT CIRCUIT CURRENT SETUP



OFFSET VOLTAGE SETUP

APPLICATION INFORMATION

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in Figure 1. In a 100 Ω differential transmission line environment, LVDS drivers require a matched load termination of 100 Ω across near

the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

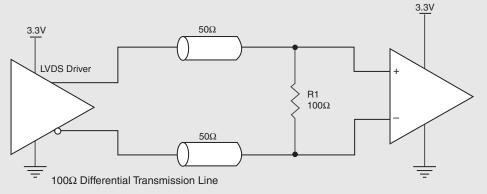
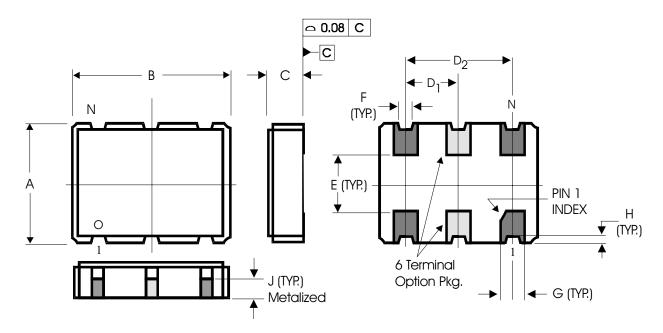


FIGURE 1. TYPICAL LVDS DRIVER TERMINATION

PACKAGE OUTLINE - J SUFFIX FOR 6 LEAD SMT CERHERMETIC, 5mm x 7mm x 1.5mm

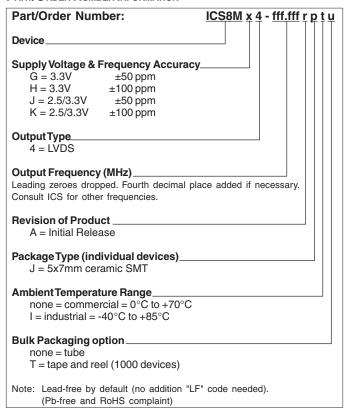


DIMENSIONS IN MILLIMETERS						
SYMBOL	Nominal	Tolerance				
Α	5	±0.15				
В	7	±0.15				
С	1.5	±0.15				
D ₁	2.54	±0.13				
$D_{\!\scriptscriptstyle 2}$	5.08	±0.13				
E	2.6	±0.13				
F	0.6	±0.13				
G	1.4	±0.13				
н	0.15 Ref.	-				
J	0.65 Ref.	-				

ORDERING INFORMATION - 0°C TO + 70°C (COMMERCIAL)

Part/Order Number*	Marking*	Package	Shipping Packaging	Temperature
8MG4-156.250AJ	ICS8MG4 156.250	6 lead CERHERMETIC	Tube	0°C to 70°C
8MG4-156.250AJT	ICS8MG4 156.250	6 lead CERHERMETIC	1000 Tape & Reel	0°C to 70°C

PART/ORDER NUMBER INFORMATION



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.