

Description

The 89TSF5xx is a complete switch fabric, consisting of two chips:
89TSF552 (queuing engine, 10 Gbps).
89TSF500 (crossbar and scheduler).

The 89TSF552 typically resides on a line card and the 89TSF500 usually resides on a separate switch card. An 89TSF552 connects with the 89TSF500 through high-speed serial links.

The 89TSF5xx switch fabric has a modular and scalable architecture that gives system designers maximum flexibility and performance. This architecture allows a switch to be implemented either on a single shelf using an electrical backplane or on multiple shelves connected by optical transceivers, thus helping system vendors overcome physical space constraints.

The 89TSF552 supports line card speeds up to OC-192 (full duplex). It incorporates a 16-bit CSIX-over-LVDS interface to line card devices, allowing the 89TSF5xx to operate seamlessly with the IDT 89TTM552 traffic manager, or other compatible traffic managers and network processors.

In the ingress direction, the 89TSF552 manages a set of virtual output queues (VOQs), negotiates the routing path through the switch fabric, and transmits data to an 89TSF500. In the egress direction, the 89TSF552 receives data from an 89TSF500 and transmits the traffic, through a CSIX-over-LVDS interface, either to IDT's 89TTM552 traffic manager or to another device (such as a network processor) on the line card.

89TSF5xx Features

- ◆ Up to 32 switch ports, with 24 Gbps available per switch port.
- ◆ Variable length CSIX payload (up to 132 bytes) that supports any type of traffic.
- ◆ Virtual output queues (VOQs) in the ingress direction that eliminate head-of-line blocking. The 256 unicast VOQs provide:
 - A maximum of 32 ports with 8 CoS, or
 - A maximum of 16 ports with 4 subports and 4 CoS.
- ◆ Spatial multicast support with up to 4K global multicast labels. Each multicast label can specify from 1 to 32 ports.
- ◆ Efficient backpressure mechanism that eliminates cell loss caused by congestion.
- ◆ In-service scalable architecture.
- ◆ "Stackable" architecture. Total aggregate bandwidth is linearly proportional to the number of 89TSF500s. Port rate

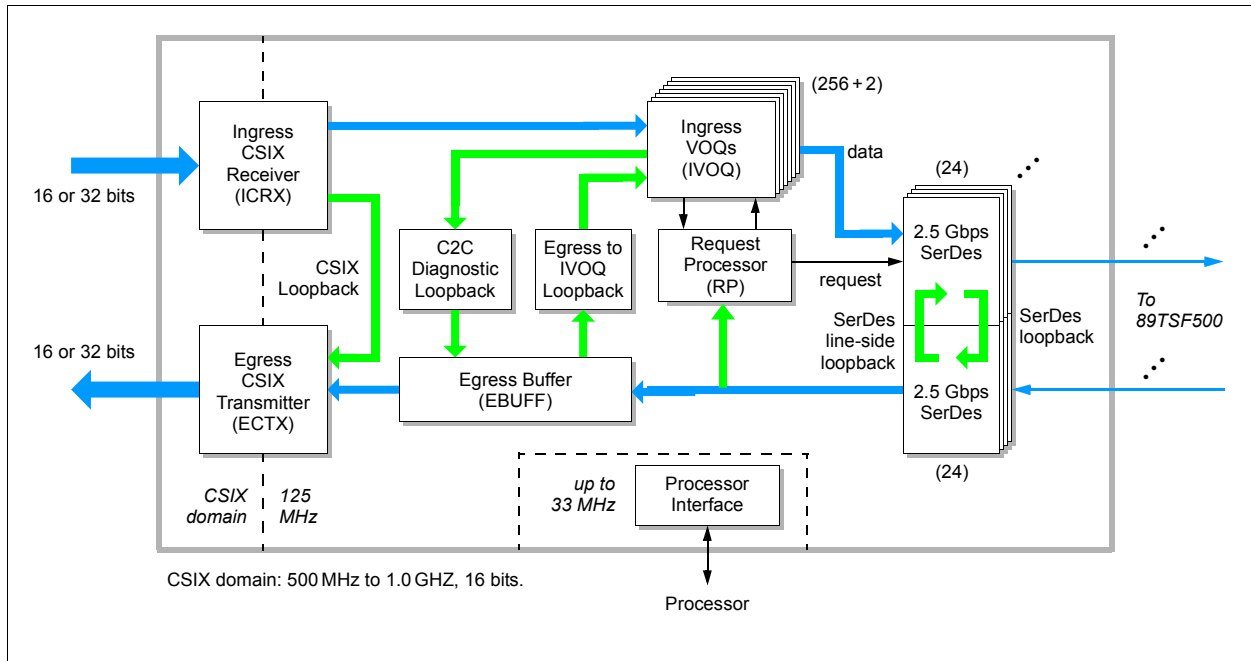
is configurable up to OC-192.

- ◆ Always non-blocking architecture across destination, traffic type (cell, packet), and class of service (CoS).
- ◆ Supports up to 4 egress subports per switch port.
- ◆ Carrier class reliability features:
 - Flexible architecture that allows the 89TSF switch fabric to be employed in a single switch shelf or in multiple switch shelves.
 - Automatic link diagnostics that detect faulty link connections.
 - Both n+m (load-sharing mode) and 1:1 protection (active/standby mode) on serial links.
 - Patented error correction scheme to reduce the system bit error rate by 10⁵.
 - Line cord redundancy via Redundant Destination Mapping (RDM) and Queue-Mapped Redundancy (QMR).
 - Dynamic 89TSF500 rerouting that avoids congested or faulty 89TSF500s.
 - Zero cell loss during controlled switchover to standby 89TSF500s.
- ◆ Advanced diagnostic features including multiple loopback paths.
- ◆ Unicast and multicast traffic with up to 8 classes of service.
- ◆ Industry-standard CSIX-over-LVDS interface.
- ◆ Backward compatibility with IDT's ZSF200 switch fabric.

89TSF552 Features

- ◆ 24 embedded SerDes links per device at 2.5 Gbps per link.
- ◆ Virtual output queues (VOQs) that buffer data according to destination, traffic type and class of Service (CoS).
- ◆ Guaranteed cell ordering.
- ◆ External processor interface for status and register configuration.
- ◆ Support for n+m (load-sharing) and 1:1 (active/standby) redundancy modes.

89TSF552 Functional Block Diagram



89TSF552 Pin Description

Note: Information in this section is subject to change. Contact your IDT FAE before making design decisions.

In this data sheet, direction is indicated as follows: I for In, O for Out, B for Bidirectional, and P for power.

Signal Name	I/O Type	Dir.	Freq.	Remarks
SYS_CLK (pin A21)	3.3V LVTTTL	I	125 MHz	N/A
PLL_SYS_LCK (pin B19)	3.3V LVTTTL	O	—	N/A
PLL_RST (pin C22)	3.3V LVTTTL	I	—	N/A
PLL_DIV_RST_N (pin D22)	3.3V LVTTTL	I	—	33K Ω internal pullup
PLL_SYS_VSSA (pin J20)	AVSS	P	—	33K Ω internal pullup
PLL_SYS_VDDA (pin K20)	3.3V AVDD	P	—	Supply
PLL_SYS_VDD (pin H21)	1.8V VDD	P	—	Supply
PLL_SYS_VSS (pin J21)	VSS	P	—	Supply

Table 1 89TSF552 PLL Control and Power Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
SD[2:0]_REFCLKN (pins A25, Y39, AW26)	Serdes diff clock	I	250MHz	Reference clocks for both Rx and Tx. The reference clock (SD[n]_REFCLKN and SD[n]_REFCLKP) must be synchronous to twice the system clock (SYS_CLK) input. If an entire SerDes group is not used, the reference clock pins for that group should be pulled down to VSS using a 300Ω to 1kΩ resistor.
SD[2:0]_REFCLKP (pins A26, AA39, AW25)	Serdes diff clock	I	250MHz	
SD[2:0]_REF_RES (pins D26, AA36, AT25)	Serdes Bidi	O	—	Reference resistor pins used to generate bias currents for both Rx and Tx. To ensure proper biasing, connect each of these to VSS through a 3.09 kΩ 1% resistor. If an entire SerDes group is not used, the reference resistor pins for that group should be connected to VDD_SD (1.8V).
VDD_SD[2:0]_PLL (pins J23, Y31, AL24)	VAA18	P	—	SerDes common VDD = 1.8V. These are PLL analog power inputs and should be well filtered.
VSS_SD[2:0]_PLL (pins K22, W31, AL23)	VSS	P	—	SerDes PLL ground
VDD_REFCLK[2:0] (pins J24, AA31, AK22)	VAA33	P	—	SerDes common VDD = 3.3V
RXN[23:0]	Serdes diff input	I	—	SerDes Rx differential pairs. A link should be left open (n.c.) if it is not used
RXP[23:0]	Serdes diff input	I	—	
TXN[23:0]	Serdes diff output	O	—	SerDes Tx differential pairs. A link should be left open (n.c.) if it is not used
TXP[23:0]	Serdes diff output	O	—	
VDD_SD	VAA18	P	—	SerDes VDD (1.8V)
VDD_TX	VAA25	P	—	SerDes VDD (2.5V)
VSS	VSS	P	—	Serdes ground included in Table 8 (89TSF552 Misc. Pins)

Table 2 89TSF552 SerDes Pins

Signal Name	Type	Dir.	Freq.	Remarks
ZBUS_AVALID_N (pin AR11)	3.3V LVTTTL	I	33MHz	33K Ω internal pullup
ZBUS_CLK (pin AW7)	3.3V LVTTTL	I	33MHz	N/A
ZBUS_AD[15:0]	3.3V LVTTTL	B	33MHz	33K Ω internal pullup
ZBUS_DEVID[4:0]	3.3V LVTTTL	I	—	33K Ω internal pullup
ZBUS_DVALID_N (pin AV10)	3.3V LVTTTL	B	33MHz	33K Ω internal pullup
ZBUS_INT_N[2:0] (pins AW11, AV11, AU11)	3.3V LVTTTL	O	—	33K Ω internal pullup
ZBUS_PRTY (pin AV9)	3.3V LVTTTL	B	33MHz	33K Ω internal pullup

Table 3 89TSF552 ZBus Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
TCK (pin E19)	3.3V LVTTTL	I	—	33K internal pullup
TDI (pin F19)	3.3V LVTTTL	I	—	33K internal pullup
TDO (pin C18)	3.3V LVTTTL	O	—	33K internal pullup
TMS (pin D19)	3.3V LVTTTL	I	—	33K internal pullup
TRST_N (pin C19)	3.3V LVTTTL	I	—	33K internal pullup

Table 4 89TSF552 Test and Debugging Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
ZTICK (pin AU12)	3.3V LVTTTL	I	—	External reference ZTick input to which the internal ZTick logic will synchronize. If ZTICK_MODE is 0, ZTICK can be left open.
ZTICK_MODE (pin AP16)	3.3V LVTTTL	I	—	External ZTick select. (Enable external ZTick sync.) 1 = internal ZTick to be synchronized to ext. reference ZTick 0 = internal ZTick is async to any ext. ZTick. Pin(s) must be stable at least 16 ns before the deassertion of the RESET_N input. Any change in pin(s) after 16 ns before the deassertion of the RESET_N input must be concurrent with, or followed by, an assertion of the RESET_N input.

Table 5 89TSF552 ZTick Management Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
CRX_REFCLK (pin AH1)	3.3V LVTTTL	I	75-125MHz	CSIX Rx reference clock. This reference clock controls the bit rate on the CRX control bus outputs.
PLL_CRX_RST (pin AH5)	3.3V LVTTTL	I	—	
PLL_CRX_LCK (pin AH6)	3.3V LVTTTL	O	—	
PLL_CRX_VDD (pin AD9)	1.8V AVDD	P	—	Digital power (1.8V)
PLL_CRX_VDDA (pin AC9)	3.3V AVDD	P	—	Analog power (3.3V)
PLL_CRX_VSS (pin AD10)	VSS	P	—	Digital ground
PLL_CRX_VSSA (pin AC10)	AVSS	P	—	Analog ground
CTX_REFCLK (pin F1)	3.3V LVTTTL	I	75-125MHz	CSIX Tx reference clock. This reference clock controls the bit rate on the CTX data bus outputs.
PLL_CTX_RST (pin G3)	3.3V LVTTTL	I	—	
PLL_CTX_LCK (pin G4)	3.3V LVTTTL	O	—	
PLL_CTX_VDD (pin U9)	1.8V AVDD	P	—	Digital power (1.8V)
PLL_CTX_VDDA (pin T9)	3.3V AVDD	P	—	Analog power (3.3V)
PLL_CTX_VSS (pin U10)	VSS	P	—	Digital ground
PLL_CTX_VSSA (pin T10)	AVSS	P	—	Analog ground

Table 6 89TSF552 CSIX PLL Pins

Signal Name	I/O Type	Dir.	Freq.	Remarks
CRX_CLKN (AB1), CRX_CLKP (AB2)	LVDS	I	500MHz - 1GHz	CSIX Rx data bus
CRX_DATN[15:0], CRX_DATP[15:0]	LVDS	I	500MHz - 1GHz	
CRX_PRTYN (V3), CRX_PRTYP (V4)	LVDS	I	500MHz - 1GHz	
CRX_SOFN (AE5), CRX_SOFP (AE6)	LVDS	I	500MHz - 1GHz	
CRX_CTRL_CLKN (AG2), CRX_CTRL_CLKP (AG3)	LVDS	O	500MHz - 1GHz	CSIX Rx control bus
CRX_CTRL_DATN[3:0], CRX_CTRL_DATP[3:0]	LVDS	O	500MHz - 1GHz	
CRX_CTRL_PRTYN (AF1), CRX_CTRL_PRTYP (AF2)	LVDS	O	500MHz - 1GHz	
CRX_CTRL_SOFN (AJ2), CRX_CTRL_SOFP (AJ3)	LVDS	O	500MHz - 1GHz	
CTX_CLKN (P2), CTX_CLKP (P1)	LVDS	O	500MHz - 1GHz	CSIX Tx data bus
CTX_DATN[15:0], CTX_DATP[15:0]	LVDS	O	500MHz - 1GHz	
CTX_PRTYN (V6), CTX_PRTYP (V5)	LVDS	O	500MHz - 1GHz	
CTX_SOFN (K4), CTX_SOFP (K3)	LVDS	O	500MHz - 1GHz	
CTX_CTRL_CLKN (H2), CTX_CTRL_CLKP (H1)	LVDS	I	500MHz - 1GHz	CSIX Tx control bus
CTX_CTRL_DATN[3:0], CTX_CTRL_DATP[3:0]	LVDS	I	500MHz - 1GHz	
CTX_CTRL_PRTYN (L6), CTX_CTRL_PRTYP (L5)	LVDS	I	500MHz - 1GHz	
CTX_CTRL_SOFN (H6), CTX_CTRL_SOFP (H5)	LVDS	I	500MHz - 1GHz	

Table 7 89TSF552 CSIX Pins (LVDS)

Signal Name	I/O Type	Dir.	Freq.	Remarks
RESET_N (pin AR12)	3.3V LVTTTL	I	—	Resets the entire chip. Must be asserted for at least 16 125MHz clock cycles after the PLL power-up initialization sequence is complete. Both assertion and deassertion are asynchronous to all clocks.
CHN_DET_MODE (pin AP21)	3.3V LVTTTL	I	—	Channel determination method 2 enable: 0 → system of mixed family devices, ZSF200 and 89TSF5xx. 1 → system has only 89TSF5xx devices.
SD8_MODE (pin AR22)	3.3V LVTTTL	I	—	SerDes 8-link mode: 0 → 24 SerDes links are enabled 1 → 8 SerDes links are enabled (links 8 through 15 are active)
TURBO_CLK (pin AW13)	3.3V LVTTTL	I	87.5MHz	Turbo interface
TURBO_SOF (pin AV13)	3.3V LVTTTL	I		
TURBO_DAT[2:0] (pins AU13, AV13, AT13)	3.3V LVTTTL	I		
VDD	VDD18	P	—	Core VDD, 1.8V
VDD_IO	VDD33	P	—	I/O VDD, 3.3V
VDDP33	VDDP33	P	—	VDDP for LVDS input buffers, 3.3V
VDD25	VDD25	P	—	VDDO for LVDS outputs, 2.5V
VDD12	VDD12	P	—	VREF for LVDS outputs, 1.25V
VSS	VSS	P	—	Ground

Table 8 89TSF552 Misc. Pins

89TSF552 Electrical and Timing Characteristics

Some data are TBD and will be published as they become available.

The specifications are subject to change without notice.

89TSF552 Absolute Maximum Ratings

The absolute maximum ratings are the maximum conditions that the device can withstand without sustaining permanent damage. Exceeding any of these conditions could result in permanent damage to the device. Normal operation should not be expected at these conditions. In addition, exposure to absolute maximum rated conditions (or near absolute maximum rated conditions) for extended periods may affect device reliability.

Operation of the device is not guaranteed at the absolute maximum ratings, but rather at the operating conditions outlined in “89TSF552 DC Characteristics” on page 8 and “89TSF552 AC Characteristics” on page 9.

Symbol	Parameter	Min	Max	Units	Conditions
T _{JMAX}	Junction temperature under bias	—	105	°C	
T _{STORAGE}	Storage temperature	—	150	°C	
	Storage temperature range	-40	85	°C	Long term storage
T _{SOLDER}	Soldering temperature	—	215	°C	
T _{REWORK}	Rework temperature	—	204	°C	
T _{GP_SOLDER}	Soldering temperature for green package	—	245	°C	
T _{GP_REWORK}	Rework temperature for green package	—	245	°C	
V _{IO}	I/O terminal voltage	-0.6	VDD+0.6	V	longer than 1 ns
		-1.0	VDD+1.0	V	pulse ≤ 1 ns

Table 9 89TSF552 Absolute Maximum Ratings

89TSF552 Operating Ranges

Symbol	Parameter	Min	Typical	Max	Units	Conditions
T _J	Operating junction temperature range	0	—	85	°C	
V _{VDD}	Core digital 1.8V power supply	1.71	1.8	1.89	V	±5%
V _{PLL_SYS_VDD}	PLL digital 1.8V power supply	1.71	1.8	1.89	V	±5%
V _{PLL_SYS_VDDA}	PLL analog 3.3V power supply	3.135	3.3	3.465	V	±5%
V _{PLL_CRX_VDDA}	CRX PLL analog 3.3V power supply	3.135	3.3	3.465	V	±5%
V _{PLL_CTX_VDDA}	CTX PLL analog 3.3V power supply	3.135	3.3	3.465	V	±5%
V _{VDD_IO}	LVTTTL 3.3V I/O power supply	3.135	3.3	3.465	V	±5%
V _{VDDP33}	3.3V LVDS supply	3.135	3.3	3.465	V	±5%
V _{VDD25}	2.5V LVDS supply	2.375	2.5	2.625	V	±5%
V _{VDD12}	1.25V LVDS reference voltage	1.188	1.25	1.313	V	±5%
V _{VDD_SD}	SerDes core 1.8V power supply	1.71	1.8	1.89	V	±5%
V _{VDD_SD_PLL}	SerDes PLL 1.8V power supply	1.71	1.8	1.89	V	±5%
V _{VDD_TX}	SerDes transmit 2.5V power supply	2.375	2.5	2.625	V	±5%
V _{VDD_REFCLK}	SerDes reference clock 3.3V power supply	3.135	3.3	3.465	V	±5%
—	SerDes power supply voltage noise (all power supplies)	—	—	TBD	mV	Peak-to-peak (50 kHz to 100 MHz)
Power Dissipation		—	15.23	18.40	W	Max. values use the maximum voltages and current listed in this table and typical values use the typical voltages and current.

Table 10 89TSF552 Operating Ranges

89TSF552 DC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 10.

Symbol	Parameter	Min	Typical	Max	Units	Conditions
I_{VDD}	Input current for core digital 1.8V core 1.8V power supply	—	4139	4821	mA	
$I_{PLL_SYS_VDD}$	Input current for PLL digital 1.8V power supply	—	1.79	2.11	mA	
$I_{PLL_SYS_VDDA}$	Input current for PLL analog 3.3V power supply	—	0.62	0.71	mA	
$I_{PLL_CRX_VDDA}$	Input current for CRX PLL analog 3.3V power supply	—	0.62	0.71	mA	
$I_{PLL_CTX_VDDA}$	Input current for CTX PLL analog 3.3V power supply	—	0.62	0.71	mA	
I_{VDD_IO}	Input current for LVTTL 3.3V I/O power supply	—	170	195	mA	
I_{VDDP33}	Input current for 3.3V LVDS power supply	—	10	11	mA	
I_{VDD25}	Input current for 2.5V LVDS power supply	—	254	279	mA	
I_{VDD12}	Input current for 1.25V LVDS reference voltage	—	39 ¹	44.9 ¹	mA	
I_{VDD_SD}	Input current for SerDes core 1.8V power supply	—	2270	2695	mA	
$I_{VDD_SD_PLL}$	Input current for SerDes PLL 1.8V power supply	—	210	270	mA	
I_{VDD_TX}	Input current for SerDes transmitters 2.5V power supply	—	813	825	mA	
I_{VDD_REFCLK}	Input current for SerDes reference clock buffer 3.3V power supply	—	1	3.3	mA	
I_{IL33}	Input leakage low current for 3.3V I/O	-5	—	5	μ A	
I_{IH33}	Input leakage high current for 3.3V I/O	-5	—	5	μ A	
I_{IL33PU}	Input leakage low current for 3.3V I/O with internal pullup	-80	—	5	μ A	
I_{IH33PU}	Input leakage high current for 3.3V I/O with internal pullup	-5	—	5	μ A	
I_{IL33PD}	Input leakage low current for 3.3V I/O with internal pulldown	-5	—	5	μ A	
I_{IH33PD}	Input leakage high current for 3.3V I/O with internal pulldown	+5	—	200	μ A	

Table 11 89TSF552 DC Characteristics (except LVDS) (Part 1 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Conditions
V_{IL33}	Input low voltage for 3.3V I/O	-0.3	—	0.8	V	
V_{IH33}	Input high voltage for 3.3V I/O	2.0	—	$V_{DD_{LVTTL33}}+0.5$	V	
V_{OL33}	Output low voltage for 3.3V I/O		—	0.5	V	I = 12 mA for 12 mA drivers and 16 mA for 16 mA drivers
V_{OH33}	Output high voltage for 3.3V I/O	2.4	—	—	V	I = 12 mA for 12 mA drivers and 16 mA for 16 mA drivers

Table 11 89TSF552 DC Characteristics (except LVDS) (Part 2 of 2)

¹ 1.25V LVDS reference should be capable of sourcing and sinking this current.

Symbol	Parameter	Min	Typical	Max	Units	Conditions
V_I	Input voltage range, V_{IA} or V_{IB}	0	—	2400	mV	$ V_{GPD} < 925 \text{ mV}^1$
V_{IDTH}	Input differential threshold	-100	—	+100	mV	$ V_{GPD} < 925 \text{ mV}$
V_{HYST}	Input differential hysteresis	25	—	—	mV	
R_{IN}	Receiver differential input impedance	80	98	120	Ω	
V_{OH}	Output voltage high, V_{OA} or V_{OB}	—	—	1475	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
V_{OL}	Output voltage low, V_{OA} or V_{OB}	925	—	—	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
$ V_{OD} $	Output differential voltage	250	—	400	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
V_{OS}	Output offset voltage	1125	—	1275	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
$ DV_{OD} $	Change in $ V_{OD} $ between '0' and '1'	—	—	25	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
DV_{OS}	Change in V_{OS} between '0' and '1'	—	—	25	mV	$R_{LOAD} = 100 \Omega \pm 1\%$
I_{SA}, I_{SB}	Output current	—	—	40	mA	Driver shorted to ground
I_{SAB}	Output current	—	—	12	mA	Drivers shorted together

Table 12 89TSF552 LVDS DC Parameters

¹ V_{GPD} is the ground potential difference between the transmitter and the receiver

89TSF552 AC Characteristics

Unless otherwise stated, the following parameters are provided given the conditions outlined in Table 10.

Symbol	Parameter	Min	Typical	Max	Units
f_{SYS}	System clock frequency (125 MHz \pm 0.1 MHz)	124.9	125	125.1	MHz
T_{JSYS}	Jitter requirements (peak to peak) for system clock. Peak to peak jitter requirements apply to entire range of allowed system clock frequencies.	—	—	100	ps
D_{SYS}	Percentage duty cycle for system clock	45	50	55	%
T_{RSYSCI}	System clock input rise time (10% to 90%)	—	—	TBD	ns
T_{FSYSCI}	System clock input fall time (90% to 10%)	—	—	TBD	ns

Table 13 89TSF552 System Clock Timing

Symbol	Parameter	Min	Typical	Max	Units
f_{ZB}	ZBus clock frequency	30	$f_{SYS} / 4$	33.1	MHz
D_{ZB}	Percentage duty cycle for ZBus clock	45	50	55	%
T_{RZBCI}	ZBus clock input rise time (10% to 90%)	—	—	TBD	ns
T_{FZBCI}	ZBus clock input fall time (90% to 10%)	—	—	TBD	ns

Table 14 89TSF552 ZBus Clock Timing

Symbol	Parameter	Min	Typical	Max	Units
T_{KQVZB}	ZBus clock rising edge to output valid	—	—	12.0	ns
T_{KQXZB}	ZBus clock rising edge to output invalid	1.0	—	—	ns
T_{KQLZB}	ZBus clock rising edge to output low Z	1.0	—	12.0	ns
T_{KQHZB}	ZBus clock rising edge to output high Z	1.0	—	12.0	ns
T_{SZB}	Input setup time from ZBus clock rising edge	5.0	—	—	ns
T_{HZB}	Input hold time from ZBus clock rising edge	1.0	—	—	ns
T_{RZBI}	Input rise time (10% to 90%)	—	—	TBD	ns
T_{FZBI}	Input fall time (90% to 10%)	—	—	TBD	ns

Table 15 89TSF552 ZBus Interface Timing

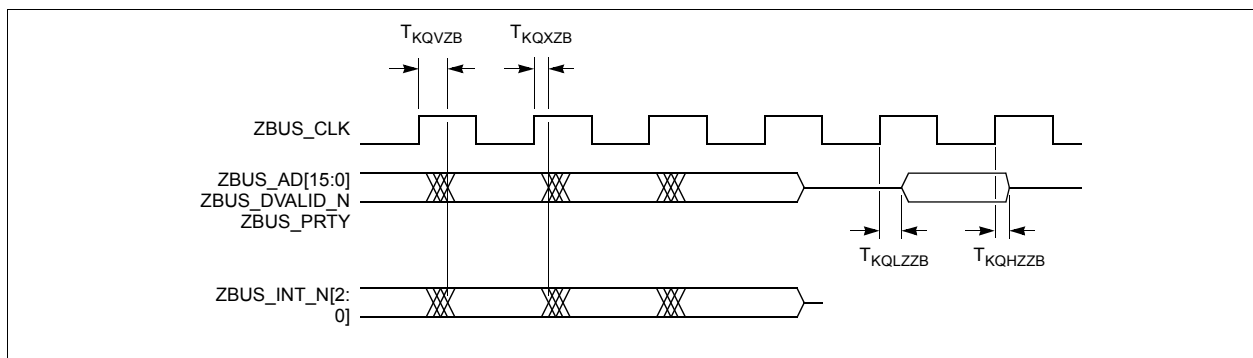


Figure 1 89TSF552 ZBus Interface Output Timing

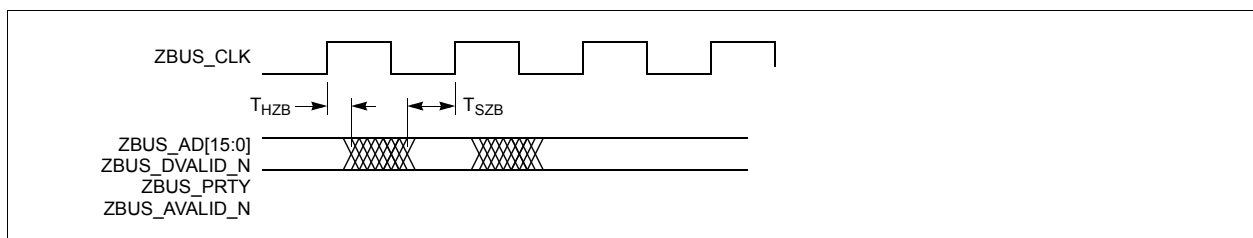


Figure 2 89TSF552 ZBus Interface Input Timing

Symbol	Parameter	Min	Typical	Max	Units
f_{TUR}	Turbo clock frequency	TBD	—	87.5 ¹	MHz
D_{TUR}	Percentage duty cycle for Turbo clock	45	50	55	%
T_{RTURCI}	Turbo clock input rise time (10% to 90%)	—	—	TBD	ns
T_{FTURCI}	Turbo clock input fall time (90% to 10%)	—	—	TBD	ns

Figure 3 89TSF552 Turbo Clock Timing

¹: For help with applications requiring a faster turbo interface, please contact your IDT representative.

Symbol	Parameter	Min	Typical	Max	Units
T_{STUR}	Input setup time to system clock rising edge	1.5	—	—	ns
T_{HTUR}	Input hold time from system clock rising edge	0	—	—	ns
T_{RTURI}	Input rise time (10% to 90%)	—	—	TBD	ns
T_{FTURI}	Input fall time (90% to 10%)	—	—	TBD	ns

Table 16 89TSF552 Turbo Bus Timing

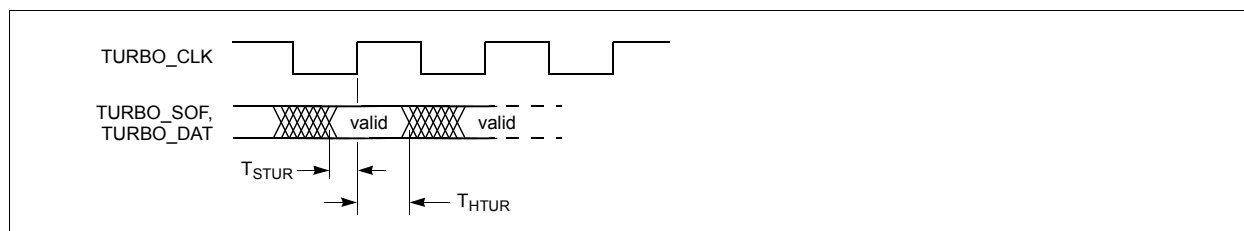


Figure 4 89TSF552 Turbo Bus Timing

Symbol	Parameter	Min	Typical	Max	Units
T_{SZT}	Input setup time from system clock (SYS_CLK pin) rising edge	3.0	—	—	ns
T_{HZE}	Input hold time from system clock rising edge	1.0	—	—	ns
T_{RZTI}	Input rise time (10% to 90%)	—	—	TBD	ns
T_{FZTI}	Input fall time (90% to 10%)	—	—	TBD	ns

Table 17 89TSF552 ZTick Interface Timing

Symbol	Parameter	Min	Typical	Max	Units	Conditions
f_{TX}	Frequency for transmit clock reference	75	—	125	MHz	
T_{JTX}	Jitter requirement for transmit clock reference		—	50 ¹	ps	pk-pk
D_{DTX}	Percentage duty for transmit clock reference	40	—	60	%	
f_{RX}	Frequency for receive clock reference	75	—	125	MHz	
T_{JRX}	Jitter requirement for receive clock reference		—	50 ¹	ps	pk-pk
D_{RX}	Percentage duty for receive clock reference	40	—	60	%	

Table 18 89TSF552 LVDS CSIX Reference Clock Characteristics

¹ Tight input jitter specifications are required to meet low frequency jitter specifications on the clock output. If low frequency output jitter performance is not required, this spec can be relaxed.

Symbol	Parameter	Min	Typical	Max	Units	Conditions
f_{DSCX}	Clock signal frequency	250	—	500	MHz	
D_{DSCX}	Clock signal duty percentage	45	—	55	%	500 MHz
J_{DSCX}	Clock signal jitter	—	—	0.10	UI	500 MHz ¹
T_{FDSCXO}	V_{OD} fall time, 80% to 20%	—	—	0.30	UI	T = 1 ns $R_{LOAD} = 100 \Omega \pm 1\%$
T_{RDSCXO}	V_{OD} rise time, 20% to 80%	—	—	0.30	UI	T = 1 ns $R_{LOAD} = 100 \Omega \pm 1\%$
$T_{SKEW1DSCX}$	$ t_{pHLA} - t_{pLHB} $ or $ t_{pHLB} - t_{pLHA} $ Differential skew	—	—	50	ps	Any differential pair on package
$T_{SKEW2DSCX}$	$ t_{pdiff[m]} - t_{pdiff[n]} $ Channel-to-channel skew	—	—	200	ps	Any 2 signals on package

Table 19 89TSF552 LVDS CSIX Interface Characteristics

¹ jitter is measured peak-to-peak from $f_{clock}/1000$ to f_{clock} . Low frequency jitter is determined by the jitter of the clock reference.

Symbol	Parameter	Min	Typical	Max	Units	Conditions
	Common mode range	1.5	2	3	V	
V_{PP} (differential)	"Eye" opening	300	400	—	mV	Common mode should be $V_{DD_REFCLK} - 1/2$ "eye" opening
f_{SDREF}	SerDes reference clock frequency	$2 \times f_{SYS}$			MHz	The expected frequency is 250 MHz (2×125 MHz).
D_{SDREF}	Percentage duty cycle for SerDes reference clock	40	—	60	%	
J_{SDREF}	Random jitter for SerDes reference clock	—	—	5	ps	RMS

Table 20 89TSF552 SerDes Reference Clock Characteristics (Part 1 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Conditions
f_{SDREF}	Frequency offset between source and target SerDes reference clocks	-100	—	+100	ppm	
T_{RSDREFCI}	SerDes reference clock input rise time (10% to 90%)	—	—	TBD	ns	T_{RZBCI}
T_{FSDREFCI}	SerDes reference clock input fall time (90% to 10%)	—	—	TBD	ns	T_{FZBCI}

Table 20 89TSF552 SerDes Reference Clock Characteristics (Part 2 of 2)

Symbol	Parameter	Min	Typical	Max	Units	Notes
J_{DR}	Deterministic jitter at receiver	—	—	0.37	UI	
J_{TR}	Total jitter at receiver	—	—	0.52	UI	at 10^{-12} BER
Z_{RTERM}	Single-ended termination of differential inputs	45	—	55	Ω	
LDR	Rx return loss	TBD	—	—	dB	100 MHz to 1.875 GHz
—	Rx common mode return loss	TBD	—	—	dB	100 MHz to 1.875 GHz
V_{RSense}	Input sensitivity	200	—	—	mV	Differential peak-peak
V_{MAX}	Maximum input voltage	—	—	2000	mV	Differential peak-peak
T_{reye}	"Eye" opening	190	—	—	ps	
I_{roff}	Off current	-50	—	50	mA	Maximum current into a pin with power off

Table 21 89TSF552 SerDes Interface Receiver Characteristics

Symbol	Parameter	Min	Typical ¹	Max	Units	Notes
V_{DIFF1}	Differential output (without pre-emphasis) (amplitude setting 1)	430	680	—	mV	Refer to Table 23.
V_{DIFF2}	Differential output (without pre-emphasis) (amplitude setting 2)	660	1100	—	mV	Refer to Table 24.
V_{DIFF3}	Differential output (without pre-emphasis) (amplitude setting 3)	700	1200	—	mV	Refer to Table 25.
t_{drf}	Driver rise/fall time					
	Amplitude Setting 1	—	—	240	ps	Measured at 20–80%
	Amplitude Setting 3	—	—	270	ps	Measured at 20–80%
Z_{D}	Differential output impedance	—	100	—	Ω	100 MHz to 1.875 GHz
Z_{SE}	Single-ended output impedance	—	50	—	Ω	100 MHz to 1.875 GHz
Z_{MSE}	Single-ended output impedance matching	3	—	8	%	100 MHz to 1.875 GHz
J_{D}	Deterministic jitter	—	—	0.14	UI	Without pre-emphasis
J_{T}	Total jitter	—	—	0.38	UI	At ± 7 sigma

Table 22 89TSF552 SerDes Interface Transmitter Characteristics

¹ The typical amplitude values are obtained when $V_{\text{DD_TX}}=2.5\text{V}$, and $V_{\text{DD_SD}}=1.8\text{V}$

Register Field Value ¹	Normalized Increase in Amplitude ²	Deviation in Amplitude from Nominal (%)
0	0.00	0.0%
1	0.31	15.5%
2	0.46	23%
3	0.77	38.5%
4	0.61	30.5%
5	0.91	45.5%
6	1.05	52.5%
7	1.29	64.5%

Table 23 SERDES Tx Typical Pre-Emphasis Levels for Tx Amplitude Setting 1 (625mV typical)

¹ Differential voltage values are configurable via settings in the SerDes Group Link Configuration Registers. Refer to the 89TSF5xx User Manual for additional information.

² Amount "a" in Figure 5.

Register Field Value ¹	Normalized Increase in Amplitude ²	Deviation in Amplitude from Nominal (%)
0	0.00	0.0%
1	0.17	8.5%
2	0.26	13%
3	0.44	22%
4	0.35	17.5%
5	0.52	26%
6	0.60	30%
7	0.73	36.5%

Table 24 SERDES Tx Typical Pre-Emphasis Levels for Tx Amplitude Setting 2 (1100mV typical)

¹ Differential voltage values are configurable via settings in the SerDes Group Link Configuration Registers. Refer to the 89TSF5xx User Manual for additional information.

² Amount "a" in Figure 5.

Register Field Value ¹	Normalized Increase in Amplitude ²	Deviation in Amplitude from Nominal (%)
0	0.00	0.0%
1	0.16	8.0%
2	0.24	12%
3	0.40	20%
4	0.31	15.5%
5	0.47	23.5%
6	0.54	27%
7	0.65	32.5%

Table 25 SERDES Tx Typical Pre-Emphasis Levels for Tx Amplitude Setting 3 (1200mV typical)

¹ Differential voltage values are configurable via settings in the SerDes Group Link Configuration Registers. Refer to the 89TSF5xx User Manual for additional information.

² Amount "a" in Figure 5.

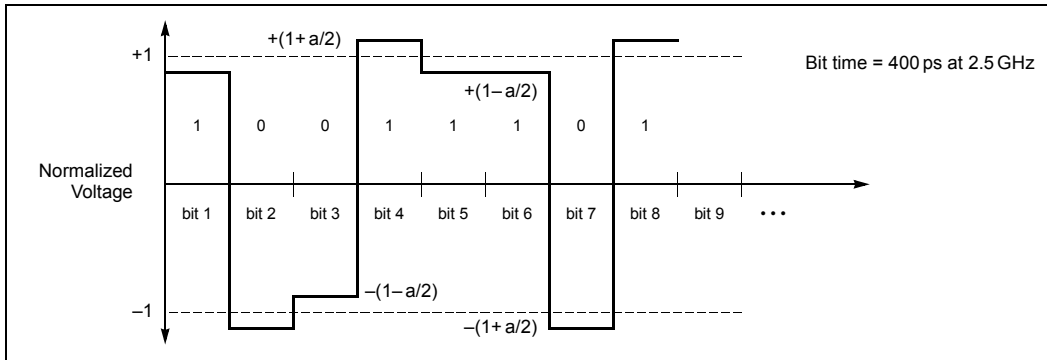


Figure 5 Output with Pre-Emphasis

89TSF552 AC Test Conditions

Input Rise/Fall Time	1 V / ns (20% / 80%)
Output timing measurement reference level (V _{REF}) for 3.3V interfaces	1.65V
Output load	As shown in Figure 6

Table 26 89TSF552 AC Test Conditions

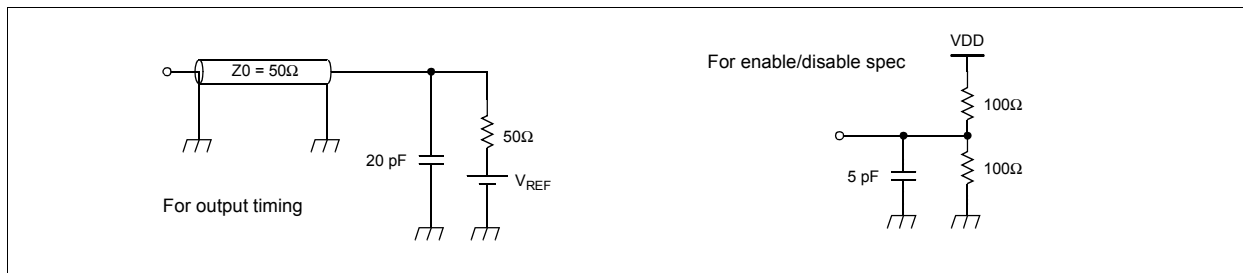


Figure 6 89TSF552 AC Test Load

89TSF552 Thermal Considerations

This section describes the temperature and heat sink calculations for flip-chip BGA devices.

Symbol	Parameter	Value	Units	Conditions
θ_{JA}	Thermal resistance, junction to ambient (no heat sink)	9.0	°C / W	Still air
		5.5	°C / W	200 FPM
		4.5	°C / W	500 FPM
θ_{JB}	Estimated thermal resistance, junction to board	2.2	°C / W	
θ_{JC}	Thermal resistance, junction to case	0.19	°C / W	

Table 27 89TSF552 Thermal Characteristics

The thermal circuit is shown below.

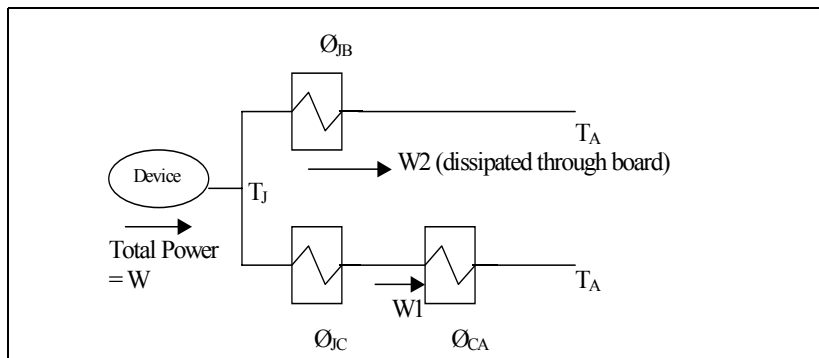


Figure 7 89TSF552 Thermal Circuit

For flip-chip BGA devices, there are two paths for heat dissipation: one through the package balls to the board and other through the package case to air. The device specifications provide θ_{JB} and θ_{JC} numbers. The θ_{CA} number comes from the heat sink manufacturer and depends on type of heat sink (area, height, fin type, etc.) and the airflow across the heat sink. The device specifications also provide the maximum operating junction temperature (T_J) that will not degrade the device reliability. The system designer should ensure that the device maximum junction temperature is not exceeded under any operating condition. One method of accomplishing this is to calculate the maximum ambient temperature (T_A) that can be tolerated based on the above device parameters. The formula is shown below.

$$T_A = T_J - W \times \frac{\theta_{JB} \times (\theta_{JC} + \theta_{CA})}{\theta_{JB} + \theta_{JC} + \theta_{CA}}$$

The following graph depicts the ambient temperature (T_A) versus θ_{CA} .

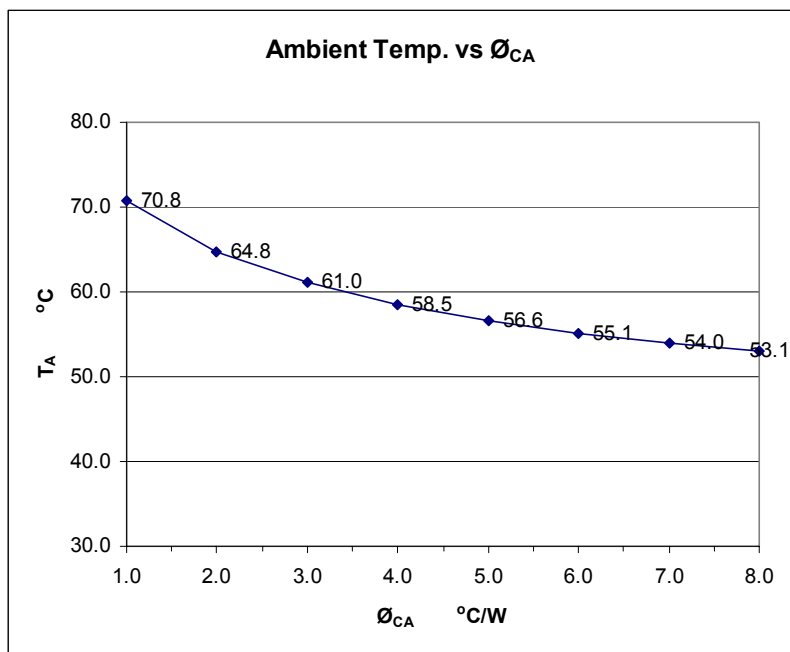


Figure 8 89TSF552 Ambient Temperature Curve

For system designers, specification of the maximum device junction temperature (operating) is critical, since it allows them to select a heat sink that meets the maximum ambient temperature requirements of their system.

The other parameter that is device package-specific is θ_{JA} , without a heat sink, and is specified for various air-flow conditions. This is the intrinsic thermal resistance of the package (junction to case + case to ambient) and is mainly specified as a reference parameter. (This is when a heat sink is not present and the top surface of the package is essentially acting as the heat sink). However, in devices that have high power dissipation, heat sink usage is highly desirable. Consequently, system designers may have limited use for this parameter.

89TSF552 Power, Reset, and Initialization Sequencing Requirements

Power Supply Power-Up Sequence

There is a power supply power-up sequence requirement that addresses potential latching issues with some I/O buffers. All 3.3V I/O power must ramp up before all other power supply pins:

- 3.3V I/O (VDD_{IO} , $VDDP33$, $VDD_{REFCLKn}$)
- all other power supply pins

Further, IDT recommends that the designer use current limiting resistors on the bidirectional ZBus pins to limit potential high transient current from short-circuit current or bus contention during the power-up period. Such events can occur because of an unknown state of output enable of the bidirectional buffers. After core power ramps up (with RESET_N asserted), the bidirectional I/O lines enter normal operating mode.

Power Supply Power-Down Sequence

Because the power supply power-off state clears any latching condition, the power-down sequence is not dictated by latching.

However, potential high transient current from short-circuit current or bus contention can also occur during the power-down period. We recommend appropriate sequencing. All 3.3V I/O power should ramp down before the 1.8V core (VDD) power:

- 3.3V I/O (VDD_{IO})
- 1.8V core (VDD)

However, if appropriate current limiting techniques (e.g., series resistors) are employed and the 2.5V and 1.5V power supplies ramp down soon after the 1.8V core power supply (within about 50 ms), the system designer can safely ignore this recommendation.

PLL Power-Up Initialization

PLL inputs into the 89TSF552, from an external device such as the ZBus bridge in IDT's reference system, require a special initialization sequence. Figure 9 shows the initialization sequence.

PLL initialization is necessary only at power-up. If the PLLs fail to lock, repeatedly assert PLL_RST until they do.

Note: The 89TSF552 must be reset after PLL initialization. Hold RESET_N low for at least 16 clocks (SYS_CLK) after PLL initialization completes.

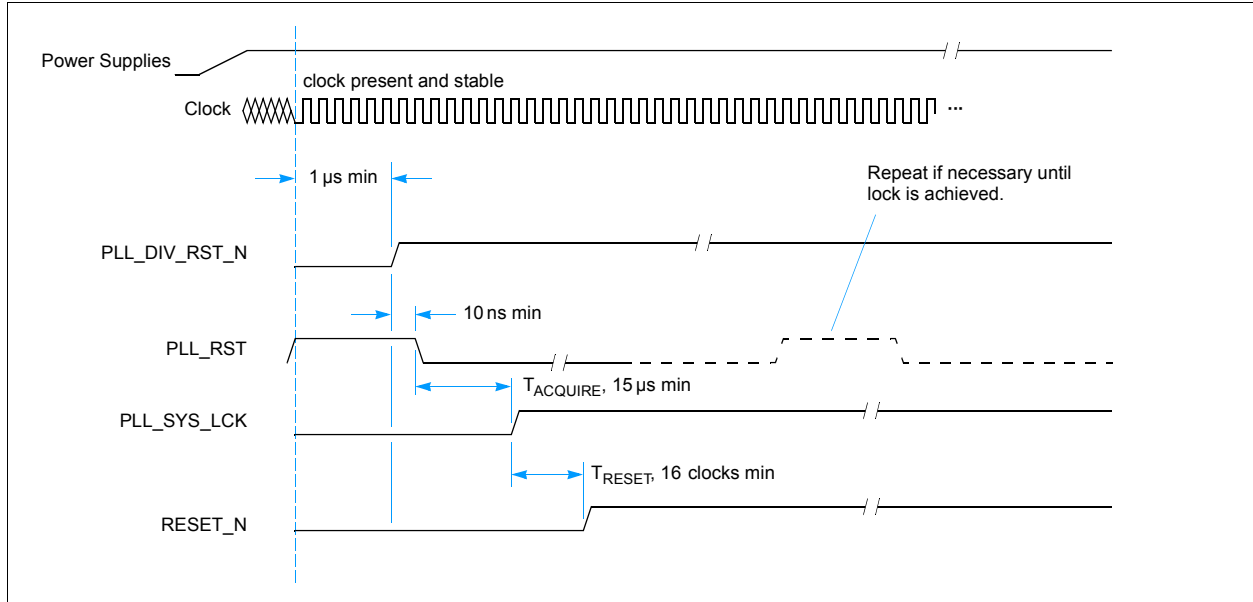


Figure 9 PLL Power-Up Initialization for the 89TSF552

Device Reset

It is possible to reset the entire 89TSF552 device except for the PLL. To reset the device without being required to re-initialize the PLL, assert the RESET_N pin (low) for at least 16 clocks (SYS_CLK) and then deassert it.

Pin List I/O Description

The 89TSF552 Pin List on page 19 uses the following I/O notations:

I	Input
O	Output
B	Bidirectional
P	Power
DNC	Do not connect
RPD	Reserved, pulldwn. Pin must be connected to VSS through a 300 - 1K Ω resistor.
RPU	Reserved, pullup. Pin is connected to VDD_IO (3.3V) through a 1K - 10K Ω resistor.

89TSF552 Pin List

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
A2	DNC	DNC	do not connect	B6	DNC	DNC	do not connect
A3	RPD	I	RPD	B7	DNC	DNC	do not connect
A4	VDD_IO	P	VDD33	B8	DNC	DNC	do not connect
A5	DNC	DNC	do not connect	B9	DNC	DNC	do not connect
A6	VSS	P	VSS	B10	DNC	DNC	do not connect
A7	DNC	DNC	do not connect	B11	DNC	DNC	do not connect
A8	VDD_IO	P	VDD33	B12	DNC	DNC	do not connect
A9	DNC	DNC	do not connect	B13	DNC	DNC	do not connect
A10	VSS	P	VSS	B14	DNC	DNC	do not connect
A11	DNC	DNC	do not connect	B15	DNC	DNC	do not connect
A12	DNC	DNC	do not connect	B16	DNC	DNC	do not connect
A13	DNC	DNC	do not connect	B17	DNC	DNC	do not connect
A14	VSS	P	VSS	B18	VDD_IO	P	VDD33
A15	DNC	DNC	do not connect	B19	PLL_SYS_LCK	O	3.3V LVTTTL
A16	VDD_IO	P	VDD33	B20	VSS	P	VSS
A17	DNC	DNC	do not connect	B21	VSS	P	VSS
A18	VSS	P	VSS	B22	VSS	P	VSS
A19	DNC	DNC	do not connect	B23	RPD	I	RPD
A20	VSS	P	VSS	B24	VSS	P	VSS
A21	SYS_CLK	I	3.3V LVTTTL	B25	VSS	P	VSS
A22	VSS	P	VSS	B26	VSS	P	VSS
A23	RPD	I	RPD	B27	VSS	P	VSS
A24	VSS	P	VSS	B28	VSS	P	VSS
A25	SD2_REFCLKN	I	Serdes diff clock	B29	VSS	P	VSS
A26	SD2_REFCLKP	I	Serdes diff clock	B30	VSS	P	VSS
A27	VSS	P	VSS	B31	VSS	P	VSS
A28	RXN[23]	I	Serdes diff input	B32	VSS	P	VSS
A29	RXP[23]	I	Serdes diff input	B33	VSS	P	VSS
A30	RXN[22]	I	Serdes diff input	B34	VSS	P	VSS
A31	RXP[22]	I	Serdes diff input	B35	VSS	P	VSS
A32	RXN[21]	I	Serdes diff input	B36	VSS	P	VSS
A33	RXP[21]	I	Serdes diff input	B37	VSS	P	VSS
A34	RXN[20]	I	Serdes diff input	B38	VSS	P	VSS
A35	RXP[20]	I	Serdes diff input	B39	VSS	P	VSS
A36	VSS	P	VSS	C1	VDD_IO	P	VDD33
A37	VSS	P	VSS	C2	DNC	DNC	do not connect
A38	VSS	P	VSS	C3	DNC	DNC	do not connect
B1	VSS	P	VSS	C4	DNC	DNC	do not connect
B2	DNC	DNC	do not connect	C5	DNC	DNC	do not connect
B3	DNC	DNC	do not connect	C6	DNC	DNC	do not connect
B4	DNC	DNC	do not connect	C7	DNC	DNC	do not connect
B5	DNC	DNC	do not connect	C8	DNC	DNC	do not connect
				C9	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
C10	DNC	DNC	do not connect	D14	DNC	DNC	do not connect
C11	DNC	DNC	do not connect	D15	DNC	DNC	do not connect
C12	DNC	DNC	do not connect	D16	VSS	P	VSS
C13	DNC	DNC	do not connect	D17	DNC	DNC	do not connect
C14	DNC	DNC	do not connect	D18	VDD_IO	P	VDD33
C15	DNC	DNC	do not connect	D19	TMS	I	3.3V LVTTTL
C16	DNC	DNC	do not connect	D20	VSS	P	VSS
C17	DNC	DNC	do not connect	D21	DNC	DNC	do not connect
C18	TDO	I	3.3V LVTTTL	D22	PLL_DIV_RST_N	I	3.3V LVTTTL
C19	TRST_N	I	3.3V LVTTTL	D23	RPD	I	RPD
C20	RPU	I	RPU	D24	VSS	P	VSS
C21	DNC	DNC	do not connect	D25	DNC	DNC	do not connect
C22	PLL_RST	I	3.3V LVTTTL	D26	SD2_REF_RES	B	Serdes Bidi
C23	RPD	I	RPD	D27	VSS	P	VSS
C24	VSS	P	VSS	D28	VSS	P	VSS
C25	DNC	DNC	do not connect	D29	VSS	P	VSS
C26	RPD	I	RPD	D30	VSS	P	VSS
C27	VSS	P	VSS	D31	VSS	P	VSS
C28	TXN[23]	O	Serdes diff output	D32	VSS	P	VSS
C29	TXP[23]	O	Serdes diff output	D33	VSS	P	VSS
C30	TXN[22]	O	Serdes diff output	D34	VSS	P	VSS
C31	TXP[22]	O	Serdes diff output	D35	VSS	P	VSS
C32	TXN[21]	O	Serdes diff output	D36	VSS	P	VSS
C33	TXP[21]	O	Serdes diff output	D37	TXP[19]	O	Serdes diff output
C34	TXN[20]	O	Serdes diff output	D38	VSS	P	VSS
C35	TXP[20]	O	Serdes diff output	D39	RXP[19]	I	Serdes diff input
C36	VSS	P	VSS	E1	VSS	P	VSS
C37	TXN[19]	O	Serdes diff output	E2	DNC	DNC	do not connect
C38	VSS	P	VSS	E3	DNC	DNC	do not connect
C39	RXN[19]	I	Serdes diff input	E4	VDD_IO	P	VDD33
D1	DNC	DNC	do not connect	E5	RPD	I	RPD
D2	DNC	DNC	do not connect	E6	RPD	I	RPD
D3	DNC	DNC	do not connect	E7	VSS	P	VSS
D4	VSS	P	VSS	E8	VDD_IO	P	VDD33
D5	DNC	DNC	do not connect	E9	DNC	DNC	do not connect
D6	VDD_IO	P	VDD33	E10	DNC	DNC	do not connect
D7	DNC	DNC	do not connect	E11	DNC	DNC	do not connect
D8	DNC	DNC	do not connect	E12	DNC	DNC	do not connect
D9	VSS	P	VSS	E13	DNC	DNC	do not connect
D10	VDD_IO	P	VDD33	E14	DNC	DNC	do not connect
D11	DNC	DNC	do not connect	E15	DNC	DNC	do not connect
D12	VSS	P	VSS	E16	DNC	DNC	do not connect
D13	DNC	DNC	do not connect	E17	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
E18	RPD	I	RPD	F22	DNC	DNC	do not connect
E19	TCK	I	3.3V LVTTTL	F23	DNC	DNC	do not connect
E20	RPU	I	RPU	F24	DNC	DNC	do not connect
E21	DNC	DNC	do not connect	F25	DNC	DNC	do not connect
E22	DNC	DNC	do not connect	F26	DNC	DNC	do not connect
E23	DNC	DNC	do not connect	F27	DNC	DNC	do not connect
E24	DNC	DNC	do not connect	F28	DNC	DNC	do not connect
E25	DNC	DNC	do not connect	F29	DNC	DNC	do not connect
E26	VSS	P	VSS	F30	DNC	DNC	do not connect
E27	DNC	DNC	do not connect	F31	DNC	DNC	do not connect
E28	DNC	DNC	do not connect	F32	DNC	DNC	do not connect
E29	DNC	DNC	do not connect	F33	DNC	DNC	do not connect
E30	DNC	DNC	do not connect	F34	DNC	DNC	do not connect
E31	DNC	DNC	do not connect	F35	DNC	DNC	do not connect
E32	DNC	DNC	do not connect	F36	VSS	P	VSS
E33	DNC	DNC	do not connect	F37	TXP[18]	O	Serdes diff output
E34	DNC	DNC	do not connect	F38	VSS	P	VSS
E35	DNC	DNC	do not connect	F39	RXP[18]	I	Serdes diff input
E36	VSS	P	VSS	G1	VDD25	P	VDD25
E37	TXN[18]	O	Serdes diff output	G2	VSS	P	VSS
E38	VSS	P	VSS	G3	PLL_CTX_RST	I	3.3V LVTTTL
E39	RXN[18]	I	Serdes diff input	G4	PLL_CTX_LCK	O	3.3V LVTTTL
F1	CTX_REFCLK	I	3.3V LVTTTL	G5	VSS	P	VSS
F2	VSS	P	VSS	G6	RPD	I	RPD
F3	DNC	DNC	do not connect	G7	DNC	DNC	do not connect
F4	DNC	DNC	do not connect	G8	DNC	DNC	do not connect
F5	RPD	I	RPD	G9	DNC	DNC	do not connect
F6	RPD	I	RPD	G10	DNC	DNC	do not connect
F7	RPD	I	RPD	G11	DNC	DNC	do not connect
F8	DNC	DNC	do not connect	G12	DNC	DNC	do not connect
F9	DNC	DNC	do not connect	G13	DNC	DNC	do not connect
F10	DNC	DNC	do not connect	G14	DNC	DNC	do not connect
F11	DNC	DNC	do not connect	G15	DNC	DNC	do not connect
F12	DNC	DNC	do not connect	G16	DNC	DNC	do not connect
F13	DNC	DNC	do not connect	G17	DNC	DNC	do not connect
F14	DNC	DNC	do not connect	G18	DNC	DNC	do not connect
F15	DNC	DNC	do not connect	G19	DNC	DNC	do not connect
F16	DNC	DNC	do not connect	G20	DNC	DNC	do not connect
F17	DNC	DNC	do not connect	G21	DNC	DNC	do not connect
F18	DNC	DNC	do not connect	G22	DNC	DNC	do not connect
F19	TDI	I	3.3V LVTTTL	G23	DNC	DNC	do not connect
F20	DNC	DNC	do not connect	G24	DNC	DNC	do not connect
F21	DNC	DNC	do not connect	G25	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
G26	DNC	DNC	do not connect	H30	DNC	DNC	do not connect
G27	DNC	DNC	do not connect	H31	DNC	DNC	do not connect
G28	DNC	DNC	do not connect	H32	DNC	DNC	do not connect
G29	DNC	DNC	do not connect	H33	DNC	DNC	do not connect
G30	DNC	DNC	do not connect	H34	DNC	DNC	do not connect
G31	DNC	DNC	do not connect	H35	DNC	DNC	do not connect
G32	DNC	DNC	do not connect	H36	VSS	P	VSS
G33	DNC	DNC	do not connect	H37	TXP[17]	O	Serdes diff output
G34	DNC	DNC	do not connect	H38	VSS	P	VSS
G35	DNC	DNC	do not connect	H39	RXP[17]	I	Serdes diff input
G36	VSS	P	VSS	J1	VSS	P	VSS
G37	TXN[17]	O	Serdes diff output	J2	CTX_CTRL_DATP[0]	I	LVDS
G38	VSS	P	VSS	J3	CTX_CTRL_DATN[0]	I	LVDS
G39	RXN[17]	I	Serdes diff input	J4	VDD25	P	VDD25
H1	CTX_CTRL_CLKP	I	LVDS	J5	CTX_CTRL_DATP[3]	I	LVDS
H2	CTX_CTRL_CLKN	I	LVDS	J6	CTX_CTRL_DATN[3]	I	LVDS
H3	CTX_CTRL_DATP[2]	I	LVDS	J7	VDD25	P	VDD25
H4	CTX_CTRL_DATN[2]	I	LVDS	J8	DNC	DNC	do not connect
H5	CTX_CTRL_SOFP	I	LVDS	J9	DNC	DNC	do not connect
H6	CTX_CTRL_SOFN	I	LVDS	J10	DNC	DNC	do not connect
H7	DNC	DNC	do not connect	J11	DNC	DNC	do not connect
H8	DNC	DNC	do not connect	J12	DNC	DNC	do not connect
H9	DNC	DNC	do not connect	J13	DNC	DNC	do not connect
H10	DNC	DNC	do not connect	J14	DNC	DNC	do not connect
H11	DNC	DNC	do not connect	J15	DNC	DNC	do not connect
H12	DNC	DNC	do not connect	J16	DNC	DNC	do not connect
H13	DNC	DNC	do not connect	J17	DNC	DNC	do not connect
H14	DNC	DNC	do not connect	J18	DNC	DNC	do not connect
H15	DNC	DNC	do not connect	J19	DNC	DNC	do not connect
H16	DNC	DNC	do not connect	J20	PLL_SYS_VSSA	P	AVSS
H17	DNC	DNC	do not connect	J21	PLL_SYS_VSS	P	VSS
H18	DNC	DNC	do not connect	J22	DNC	DNC	do not connect
H19	DNC	DNC	do not connect	J23	VDD_SD2_PLL	P	VAA18
H20	DNC	DNC	do not connect	J24	VDD_REFCLK2	P	VAA33
H21	PLL_SYS_VDD	P	1.8V VDD	J25	DNC	DNC	do not connect
H22	DNC	DNC	do not connect	J26	DNC	DNC	do not connect
H23	DNC	DNC	do not connect	J27	VSS	P	VSS
H24	DNC	DNC	do not connect	J28	DNC	DNC	do not connect
H25	DNC	DNC	do not connect	J29	DNC	DNC	do not connect
H26	DNC	DNC	do not connect	J30	DNC	DNC	do not connect
H27	DNC	DNC	do not connect	J31	DNC	DNC	do not connect
H28	DNC	DNC	do not connect	J32	DNC	DNC	do not connect
H29	DNC	DNC	do not connect	J33	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
J34	DNC	DNC	do not connect	K38	VSS	P	VSS
J35	DNC	DNC	do not connect	K39	RXP[16]	I	Serdes diff input
J36	VSS	P	VSS	L1	VDD25	P	VDD25
J37	TXN[16]	O	Serdes diff output	L2	CTX_DATP[13]	O	LVDS
J38	VSS	P	VSS	L3	CTX_DATN[13]	O	LVDS
J39	RXN[16]	I	Serdes diff input	L4	VSS	P	VSS
K1	CTX_DATP[15]	O	LVDS	L5	CTX_CTRL_PRTYP	I	LVDS
K2	CTX_DATN[15]	O	LVDS	L6	CTX_CTRL_PRTYN	I	LVDS
K3	CTX_SOFN	O	LVDS	L7	VSS	P	VSS
K4	CTX_SOFN	O	LVDS	L8	DNC	DNC	do not connect
K5	CTX_CTRL_DATP[1]	I	LVDS	L9	DNC	DNC	do not connect
K6	CTX_CTRL_DATN[1]	I	LVDS	L10	DNC	DNC	do not connect
K7	VDD25	P	VDD25	L11	VSS	P	VSS
K8	DNC	DNC	do not connect	L12	VSS	P	VSS
K9	DNC	DNC	do not connect	L13	VSS	P	VSS
K10	DNC	DNC	do not connect	L14	VSS	P	VSS
K11	DNC	DNC	do not connect	L15	VSS	P	VSS
K12	DNC	DNC	do not connect	L16	VSS	P	VSS
K13	DNC	DNC	do not connect	L17	VSS	P	VSS
K14	DNC	DNC	do not connect	L18	VSS	P	VSS
K15	DNC	DNC	do not connect	L19	VSS	P	VSS
K16	DNC	DNC	do not connect	L20	VSS	P	VSS
K17	DNC	DNC	do not connect	L21	VSS	P	VSS
K18	DNC	DNC	do not connect	L22	DNC	DNC	do not connect
K19	DNC	DNC	do not connect	L23	VSS	P	VSS
K20	PLL_SYS_VDDA	P	3.3V AVDD	L24	VSS	P	VSS
K21	DNC	DNC	do not connect	L25	VSS	P	VSS
K22	VSS_SD2_PLL	P	VSS	L26	VSS	P	VSS
K23	VSS	P	VSS	L27	VSS	P	VSS
K24	VSS	P	VSS	L28	VSS	P	VSS
K25	VSS	P	VSS	L29	VSS	P	VSS
K26	VSS	P	VSS	L30	VSS	P	VSS
K27	VSS	P	VSS	L31	DNC	DNC	do not connect
K28	VSS	P	VSS	L32	DNC	DNC	do not connect
K29	VSS	P	VSS	L33	DNC	DNC	do not connect
K30	VSS	P	VSS	L34	DNC	DNC	do not connect
K31	DNC	DNC	do not connect	L35	DNC	DNC	do not connect
K32	DNC	DNC	do not connect	L36	VSS	P	VSS
K33	DNC	DNC	do not connect	L37	TXN[15]	O	Serdes diff output
K34	DNC	DNC	do not connect	L38	VSS	P	VSS
K35	DNC	DNC	do not connect	L39	RXN[15]	I	Serdes diff input
K36	VSS	P	VSS	M1	CTX_DATP[10]	O	LVDS
K37	TXP[16]	O	Serdes diff output	M2	CTX_DATN[10]	O	LVDS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
M3	CTX_DATP[12]	O	LVDS	N7	VDD25	P	VDD25
M4	CTX_DATN[12]	O	LVDS	N8	DNC	DNC	do not connect
M5	CTX_DATP[14]	O	LVDS	N9	DNC	DNC	do not connect
M6	CTX_DATN[14]	O	LVDS	N10	DNC	DNC	do not connect
M7	VSS	P	VSS	N11	VSS	P	VSS
M8	DNC	DNC	do not connect	N12	VSS	P	VSS
M9	DNC	DNC	do not connect	N13	VDD_IO	P	VDD33
M10	DNC	DNC	do not connect	N14	VDD_IO	P	VDD33
M11	VSS	P	VSS	N15	VDD_IO	P	VDD33
M12	VSS	P	VSS	N16	VDD_IO	P	VDD33
M13	VSS	P	VSS	N17	VDD_IO	P	VDD33
M14	VSS	P	VSS	N18	VDD_IO	P	VDD33
M15	VSS	P	VSS	N19	VDD_IO	P	VDD33
M16	VSS	P	VSS	N20	VDD_IO	P	VDD33
M17	VSS	P	VSS	N21	VDD_IO	P	VDD33
M18	VSS	P	VSS	N22	DNC	DNC	do not connect
M19	VSS	P	VSS	N23	VDD_SD	P	VAA18
M20	VSS	P	VSS	N24	VDD_SD	P	VAA18
M21	VSS	P	VSS	N25	VDD_SD	P	VAA18
M22	DNC	DNC	do not connect	N26	VDD_SD	P	VAA18
M23	VDD_TX	P	VAA25	N27	VDD_SD	P	VAA18
M24	VDD_TX	P	VAA25	N28	VDD_TX	P	VAA25
M25	VDD_TX	P	VAA25	N29	VSS	P	VSS
M26	VDD_TX	P	VAA25	N30	VSS	P	VSS
M27	VDD_TX	P	VAA25	N31	DNC	DNC	do not connect
M28	VDD_TX	P	VAA25	N32	DNC	DNC	do not connect
M29	VSS	P	VSS	N33	DNC	DNC	do not connect
M30	VSS	P	VSS	N34	DNC	DNC	do not connect
M31	DNC	DNC	do not connect	N35	DNC	DNC	do not connect
M32	DNC	DNC	do not connect	N36	VSS	P	VSS
M33	DNC	DNC	do not connect	N37	TXN[14]	O	Serdes diff output
M34	DNC	DNC	do not connect	N38	VSS	P	VSS
M35	DNC	DNC	do not connect	N39	RXN[14]	I	Serdes diff input
M36	VSS	P	VSS	P1	CTX_CLKP	O	LVDS
M37	TXP[15]	O	Serdes diff output	P2	CTX_CLKN	O	LVDS
M38	VSS	P	VSS	P3	CTX_DATP[7]	O	LVDS
M39	RXP[15]	I	Serdes diff input	P4	CTX_DATN[7]	O	LVDS
N1	VSS	P	VSS	P5	CTX_DATP[9]	O	LVDS
N2	CTX_DATP[8]	O	LVDS	P6	CTX_DATN[9]	O	LVDS
N3	CTX_DATN[8]	O	LVDS	P7	VDD25	P	VDD25
N4	VDD25	P	VDD25	P8	DNC	DNC	do not connect
N5	CTX_DATP[11]	O	LVDS	P9	DNC	DNC	do not connect
N6	CTX_DATN[11]	O	LVDS	P10	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
P11	VSS	P	VSS	R15	VDD	P	VDD18
P12	VSS	P	VSS	R16	VDD	P	VDD18
P13	VDD_IO	P	VDD33	R17	VSS	P	VSS
P14	VSS	P	VSS	R18	VSS	P	VSS
P15	VDD	P	VDD18	R19	VDD	P	VDD18
P16	VDD	P	VDD18	R20	VDD	P	VDD18
P17	VSS	P	VSS	R21	VSS	P	VSS
P18	VSS	P	VSS	R22	VSS	P	VSS
P19	VDD	P	VDD18	R23	VSS	P	VSS
P20	VDD	P	VDD18	R24	VSS	P	VSS
P21	VSS	P	VSS	R25	VSS	P	VSS
P22	VSS	P	VSS	R26	VSS	P	VSS
P23	VSS	P	VSS	R27	VDD_SD	P	VAA18
P24	VSS	P	VSS	R28	VDD_TX	P	VAA25
P25	VSS	P	VSS	R29	VSS	P	VSS
P26	VSS	P	VSS	R30	VSS	P	VSS
P27	VDD_SD	P	VAA18	R31	DNC	DNC	do not connect
P28	VDD_TX	P	VAA25	R32	DNC	DNC	do not connect
P29	VSS	P	VSS	R33	DNC	DNC	do not connect
P30	VSS	P	VSS	R34	DNC	DNC	do not connect
P31	DNC	DNC	do not connect	R35	DNC	DNC	do not connect
P32	DNC	DNC	do not connect	R36	VSS	P	VSS
P33	DNC	DNC	do not connect	R37	TXN[13]	O	Serdes diff output
P34	DNC	DNC	do not connect	R38	VSS	P	VSS
P35	DNC	DNC	do not connect	R39	RXN[13]	I	Serdes diff input
P36	VSS	P	VSS	T1	CTX_DATP[2]	O	LVDS
P37	TXP[14]	O	Serdes diff output	T2	CTX_DATN[2]	O	LVDS
P38	VSS	P	VSS	T3	CTX_DATP[3]	O	LVDS
P39	RXP[14]	I	Serdes diff input	T4	CTX_DATN[3]	O	LVDS
R1	VDD25	P	VDD25	T5	CTX_DATP[5]	O	LVDS
R2	CTX_DATP[6]	O	LVDS	T6	CTX_DATN[5]	O	LVDS
R3	CTX_DATN[6]	O	LVDS	T7	VSS	P	VSS
R4	VSS	P	VSS	T8	DNC	DNC	do not connect
R5	CTX_DATP[4]	O	LVDS	T9	PLL_CTX_VDDA	P	3.3V AVDD
R6	CTX_DATN[4]	O	LVDS	T10	PLL_CTX_VSSA	P	AVSS
R7	VSS	P	VSS	T11	VSS	P	VSS
R8	DNC	DNC	do not connect	T12	VSS	P	VSS
R9	DNC	DNC	do not connect	T13	VDDP33	P	VDDP33
R10	DNC	DNC	do not connect	T14	VSS	P	VSS
R11	VSS	P	VSS	T15	VDD	P	VDD18
R12	VSS	P	VSS	T16	VDD	P	VDD18
R13	VDDP33	P	VDDP33	T17	VSS	P	VSS
R14	VSS	P	VSS	T18	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
T19	VDD	P	VDD18	U23	VDD	P	VDD18
T20	VDD	P	VDD18	U24	VDD	P	VDD18
T21	VSS	P	VSS	U25	VSS	P	VSS
T22	VSS	P	VSS	U26	VSS	P	VSS
T23	VDD	P	VDD18	U27	VDD_SD	P	VAA18
T24	VDD	P	VDD18	U28	VDD_TX	P	VAA25
T25	VSS	P	VSS	U29	VSS	P	VSS
T26	VSS	P	VSS	U30	VSS	P	VSS
T27	VDD_SD	P	VAA18	U31	DNC	DNC	do not connect
T28	VDD_TX	P	VAA25	U32	DNC	DNC	do not connect
T29	VSS	P	VSS	U33	DNC	DNC	do not connect
T30	VSS	P	VSS	U34	DNC	DNC	do not connect
T31	DNC	DNC	do not connect	U35	DNC	DNC	do not connect
T32	DNC	DNC	do not connect	U36	VSS	P	VSS
T33	DNC	DNC	do not connect	U37	TXN[12]	O	Serdes diff output
T34	DNC	DNC	do not connect	U38	VSS	P	VSS
T35	DNC	DNC	do not connect	U39	RXN[12]	I	Serdes diff input
T36	VSS	P	VSS	V1	CRX_DATN[0]	I	LVDS
T37	TXP[13]	O	Serdes diff output	V2	CRX_DATP[0]	I	LVDS
T38	VSS	P	VSS	V3	CRX_PRTYN	I	LVDS
T39	RXP[13]	I	Serdes diff input	V4	CRX_PRTYP	I	LVDS
U1	VSS	P	VSS	V5	CTX_PRTYP	O	LVDS
U2	CTX_DATP[0]	O	LVDS	V6	CTX_PRTYN	O	LVDS
U3	CTX_DATN[0]	O	LVDS	V7	VDD25	P	VDD25
U4	VDD25	P	VDD25	V8	DNC	DNC	do not connect
U5	CTX_DATP[1]	O	LVDS	V9	DNC	DNC	do not connect
U6	CTX_DATN[1]	O	LVDS	V10	DNC	DNC	do not connect
U7	VDD25	P	VDD25	V11	VSS	P	VSS
U8	DNC	DNC	do not connect	V12	VSS	P	VSS
U9	PLL_CTX_VDD	P	1.8V AVDD	V13	VDD25	P	VDD25
U10	PLL_CTX_VSS	P	VSS	V14	VSS	P	VSS
U11	VSS	P	VSS	V15	VDD	P	VDD18
U12	VSS	P	VSS	V16	VDD	P	VDD18
U13	VDD25	P	VDD25	V17	VSS	P	VSS
U14	VSS	P	VSS	V18	VSS	P	VSS
U15	VDD	P	VDD18	V19	VDD	P	VDD18
U16	VDD	P	VDD18	V20	VDD	P	VDD18
U17	VSS	P	VSS	V21	VSS	P	VSS
U18	VSS	P	VSS	V22	VSS	P	VSS
U19	VDD	P	VDD18	V23	VDD	P	VDD18
U20	VDD	P	VDD18	V24	VDD	P	VDD18
U21	VSS	P	VSS	V25	VSS	P	VSS
U22	VSS	P	VSS	V26	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
V27	VDD_SD	P	VAA18	W31	VSS_SD1_PLL	P	VSS
V28	VDD_TX	P	VAA25	W32	DNC	DNC	do not connect
V29	VSS	P	VSS	W33	DNC	DNC	do not connect
V30	VSS	P	VSS	W34	DNC	DNC	do not connect
V31	DNC	DNC	do not connect	W35	DNC	DNC	do not connect
V32	DNC	DNC	do not connect	W36	VSS	P	VSS
V33	DNC	DNC	do not connect	W37	VSS	P	VSS
V34	DNC	DNC	do not connect	W38	VSS	P	VSS
V35	DNC	DNC	do not connect	W39	VSS	P	VSS
V36	VSS	P	VSS	Y1	CRX_DATN[5]	I	LVDS
V37	TXP[12]	O	Serdes diff output	Y2	CRX_DATP[5]	I	LVDS
V38	VSS	P	VSS	Y3	CRX_DATN[4]	I	LVDS
V39	RXP[12]	I	Serdes diff input	Y4	CRX_DATP[4]	I	LVDS
W1	VDD25	P	VDD25	Y5	CRX_DATN[3]	I	LVDS
W2	CRX_DATN[2]	I	LVDS	Y6	CRX_DATP[3]	I	LVDS
W3	CRX_DATP[2]	I	LVDS	Y7	VSS	P	VSS
W4	VSS	P	VSS	Y8	DNC	DNC	do not connect
W5	CRX_DATN[1]	I	LVDS	Y9	DNC	DNC	do not connect
W6	CRX_DATP[1]	I	LVDS	Y10	DNC	DNC	do not connect
W7	VSS	P	VSS	Y11	VSS	P	VSS
W8	DNC	DNC	do not connect	Y12	VSS	P	VSS
W9	DNC	DNC	do not connect	Y13	VDDP33	P	VDDP33
W10	VDD12	P	VDD12	Y14	VSS	P	VSS
W11	VSS	P	VSS	Y15	VDD	P	VDD18
W12	VSS	P	VSS	Y16	VDD	P	VDD18
W13	VDD25	P	VDD25	Y17	VSS	P	VSS
W14	VSS	P	VSS	Y18	VSS	P	VSS
W15	VDD	P	VDD18	Y19	VDD	P	VDD18
W16	VDD	P	VDD18	Y20	VDD	P	VDD18
W17	VSS	P	VSS	Y21	VSS	P	VSS
W18	VSS	P	VSS	Y22	VSS	P	VSS
W19	VDD	P	VDD18	Y23	VDD	P	VDD18
W20	VDD	P	VDD18	Y24	VDD	P	VDD18
W21	VSS	P	VSS	Y25	VSS	P	VSS
W22	VSS	P	VSS	Y26	VSS	P	VSS
W23	VDD	P	VDD18	Y27	VDD_SD	P	VAA18
W24	VDD	P	VDD18	Y28	VDD_TX	P	VAA25
W25	VSS	P	VSS	Y29	VSS	P	VSS
W26	VSS	P	VSS	Y30	VSS	P	VSS
W27	VDD_SD	P	VAA18	Y31	VDD_SD1_PLL	P	VAA18
W28	VDD_TX	P	VAA25	Y32	DNC	DNC	do not connect
W29	VSS	P	VSS	Y33	DNC	DNC	do not connect
W30	VSS	P	VSS	Y34	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
Y35	DNC	DNC	do not connect	AA39	SD1_REFCLKP	I	Serdes diff clock
Y36	DNC	DNC	do not connect	AB1	CRX_CLKN	I	LVDS
Y37	DNC	DNC	do not connect	AB2	CRX_CLKP	I	LVDS
Y38	VSS	P	VSS	AB3	CRX_DATN[8]	I	LVDS
Y39	SD1_REFCLKN	I	Serdes diff clock	AB4	CRX_DATP[8]	I	LVDS
AA1	VSS	P	VSS	AB5	CRX_DATN[9]	I	LVDS
AA2	CRX_DATN[7]	I	LVDS	AB6	CRX_DATP[9]	I	LVDS
AA3	CRX_DATP[7]	I	LVDS	AB7	VDD25	P	VDD25
AA4	VDD25	P	VDD25	AB8	DNC	DNC	do not connect
AA5	CRX_DATN[6]	I	LVDS	AB9	DNC	DNC	do not connect
AA6	CRX_DATP[6]	I	LVDS	AB10	DNC	DNC	do not connect
AA7	VDD25	P	VDD25	AB11	VSS	P	VSS
AA8	DNC	DNC	do not connect	AB12	VSS	P	VSS
AA9	DNC	DNC	do not connect	AB13	VDDP33	P	VDDP33
AA10	VDD12	P	VDD12	AB14	VSS	P	VSS
AA11	VSS	P	VSS	AB15	VDD	P	VDD18
AA12	VSS	P	VSS	AB16	VDD	P	VDD18
AA13	VDDP33	P	VDDP33	AB17	VSS	P	VSS
AA14	VSS	P	VSS	AB18	VSS	P	VSS
AA15	VDD	P	VDD18	AB19	VDD	P	VDD18
AA16	VDD	P	VDD18	AB20	VDD	P	VDD18
AA17	VSS	P	VSS	AB21	VSS	P	VSS
AA18	VSS	P	VSS	AB22	VSS	P	VSS
AA19	VDD	P	VDD18	AB23	VDD	P	VDD18
AA20	VDD	P	VDD18	AB24	VDD	P	VDD18
AA21	VSS	P	VSS	AB25	VSS	P	VSS
AA22	VSS	P	VSS	AB26	VSS	P	VSS
AA23	VDD	P	VDD18	AB27	VDD_SD	P	VAA18
AA24	VDD	P	VDD18	AB28	VDD_TX	P	VAA25
AA25	VSS	P	VSS	AB29	VSS	P	VSS
AA26	VSS	P	VSS	AB30	VSS	P	VSS
AA27	VDD_SD	P	VAA18	AB31	DNC	DNC	do not connect
AA28	VDD_TX	P	VAA25	AB32	DNC	DNC	do not connect
AA29	VSS	P	VSS	AB33	DNC	DNC	do not connect
AA30	VSS	P	VSS	AB34	DNC	DNC	do not connect
AA31	VDD_REFCLK1	P	VAA33	AB35	DNC	DNC	do not connect
AA32	DNC	DNC	do not connect	AB36	VSS	P	VSS
AA33	DNC	DNC	do not connect	AB37	VSS	P	VSS
AA34	VSS	P	VSS	AB38	VSS	P	VSS
AA35	VSS	P	VSS	AB39	VSS	P	VSS
AA36	SD1_REF_RES	B	Serdes Bidi	AC1	VDD25	P	VDD25
AA37	RPD	I	RPD	AC2	CRX_DATN[10]	I	LVDS
AA38	VSS	P	VSS	AC3	CRX_DATP[10]	I	LVDS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AC4	VSS	P	VSS	AD8	DNC	DNC	do not connect
AC5	CRX_DATN[11]	I	LVDS	AD9	PLL_CRX_VDD	P	1.8V AVDD
AC6	CRX_DATP[11]	I	LVDS	AD10	PLL_CRX_VSS	P	VSS
AC7	VSS	P	VSS	AD11	VSS	P	VSS
AC8	DNC	DNC	do not connect	AD12	VSS	P	VSS
AC9	PLL_CRX_VDDA	P	3.3V AVDD	AD13	VDD25	P	VDD25
AC10	PLL_CRX_VSSA	P	AVSS	AD14	VSS	P	VSS
AC11	VSS	P	VSS	AD15	VDD	P	VDD18
AC12	VSS	P	VSS	AD16	VDD	P	VDD18
AC13	VDD25	P	VDD25	AD17	VSS	P	VSS
AC14	VSS	P	VSS	AD18	VSS	P	VSS
AC15	VDD	P	VDD18	AD19	VDD	P	VDD18
AC16	VDD	P	VDD18	AD20	VDD	P	VDD18
AC17	VSS	P	VSS	AD21	VSS	P	VSS
AC18	VSS	P	VSS	AD22	VSS	P	VSS
AC19	VDD	P	VDD18	AD23	VDD	P	VDD18
AC20	VDD	P	VDD18	AD24	VDD	P	VDD18
AC21	VSS	P	VSS	AD25	VSS	P	VSS
AC22	VSS	P	VSS	AD26	VSS	P	VSS
AC23	VDD	P	VDD18	AD27	VDD_SD	P	VAA18
AC24	VDD	P	VDD18	AD28	VDD_TX	P	VAA25
AC25	VSS	P	VSS	AD29	VSS	P	VSS
AC26	VSS	P	VSS	AD30	VSS	P	VSS
AC27	VDD_SD	P	VAA18	AD31	DNC	DNC	do not connect
AC28	VDD_TX	P	VAA25	AD32	DNC	DNC	do not connect
AC29	VSS	P	VSS	AD33	DNC	DNC	do not connect
AC30	VSS	P	VSS	AD34	DNC	DNC	do not connect
AC31	DNC	DNC	do not connect	AD35	DNC	DNC	do not connect
AC32	DNC	DNC	do not connect	AD36	VSS	P	VSS
AC33	DNC	DNC	do not connect	AD37	TXP[11]	O	Serdes diff output
AC34	DNC	DNC	do not connect	AD38	VSS	P	VSS
AC35	DNC	DNC	do not connect	AD39	RXP[11]	I	Serdes diff input
AC36	VSS	P	VSS	AE1	VSS	P	VSS
AC37	TXN[11]	O	Serdes diff output	AE2	CRX_DATN[15]	I	LVDS
AC38	VSS	P	VSS	AE3	CRX_DATP[15]	I	LVDS
AC39	RXN[11]	I	Serdes diff input	AE4	VDD25	P	VDD25
AD1	CRX_DATN[12]	I	LVDS	AE5	CRX_SOFN	I	LVDS
AD2	CRX_DATP[12]	I	LVDS	AE6	CRX_SOFP	I	LVDS
AD3	CRX_DATN[13]	I	LVDS	AE7	VDD25	P	VDD25
AD4	CRX_DATP[13]	I	LVDS	AE8	DNC	DNC	do not connect
AD5	CRX_DATN[14]	I	LVDS	AE9	DNC	DNC	do not connect
AD6	CRX_DATP[14]	I	LVDS	AE10	DNC	DNC	do not connect
AD7	VSS	P	VSS	AE11	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AE12	VSS	P	VSS	AF16	VDD	P	VDD18
AE13	VDD_IO	P	VDD33	AF17	VSS	P	VSS
AE14	VSS	P	VSS	AF18	VSS	P	VSS
AE15	VDD	P	VDD18	AF19	VDD	P	VDD18
AE16	VDD	P	VDD18	AF20	VDD	P	VDD18
AE17	VSS	P	VSS	AF21	VSS	P	VSS
AE18	VSS	P	VSS	AF22	VSS	P	VSS
AE19	VDD	P	VDD18	AF23	VSS	P	VSS
AE20	VDD	P	VDD18	AF24	VSS	P	VSS
AE21	VSS	P	VSS	AF25	VSS	P	VSS
AE22	VSS	P	VSS	AF26	VSS	P	VSS
AE23	VSS	P	VSS	AF27	VDD_SD	P	VAA18
AE24	VSS	P	VSS	AF28	VDD_TX	P	VAA25
AE25	VSS	P	VSS	AF29	VSS	P	VSS
AE26	VSS	P	VSS	AF30	VSS	P	VSS
AE27	VDD_SD	P	VAA18	AF31	DNC	DNC	do not connect
AE28	VDD_TX	P	VAA25	AF32	DNC	DNC	do not connect
AE29	VSS	P	VSS	AF33	DNC	DNC	do not connect
AE30	VSS	P	VSS	AF34	DNC	DNC	do not connect
AE31	DNC	DNC	do not connect	AF35	DNC	DNC	do not connect
AE32	DNC	DNC	do not connect	AF36	VSS	P	VSS
AE33	DNC	DNC	do not connect	AF37	TXP[10]	O	Serdes diff output
AE34	DNC	DNC	do not connect	AF38	VSS	P	VSS
AE35	DNC	DNC	do not connect	AF39	RXP[10]	I	Serdes diff input
AE36	VSS	P	VSS	AG1	VDD25	P	VDD25
AE37	TXN[10]	O	Serdes diff output	AG2	CRX_CTRL_CLKN	O	LVDS
AE38	VSS	P	VSS	AG3	CRX_CTRL_CLKP	O	LVDS
AE39	RXN[10]	I	Serdes diff input	AG4	VSS	P	VSS
AF1	CRX_CTRL_PRTYN	O	LVDS	AG5	CRX_CTRL_DATN[2]	O	LVDS
AF2	CRX_CTRL_PRTYP	O	LVDS	AG6	CRX_CTRL_DATP[2]	O	LVDS
AF3	CRX_CTRL_DATN[0]	O	LVDS	AG7	VSS	P	VSS
AF4	CRX_CTRL_DATP[0]	O	LVDS	AG8	DNC	DNC	do not connect
AF5	CRX_CTRL_DATN[1]	O	LVDS	AG9	DNC	DNC	do not connect
AF6	CRX_CTRL_DATP[1]	O	LVDS	AG10	DNC	DNC	do not connect
AF7	VDD25	P	VDD25	AG11	VSS	P	VSS
AF8	DNC	DNC	do not connect	AG12	VSS	P	VSS
AF9	DNC	DNC	do not connect	AG13	VDD_IO	P	VDD33
AF10	DNC	DNC	do not connect	AG14	VDD_IO	P	VDD33
AF11	VSS	P	VSS	AG15	VDD_IO	P	VDD33
AF12	VSS	P	VSS	AG16	VDD_IO	P	VDD33
AF13	VDD_IO	P	VDD33	AG17	VDD_IO	P	VDD33
AF14	VSS	P	VSS	AG18	VDD_IO	P	VDD33
AF15	VDD	P	VDD18	AG19	VDD_IO	P	VDD33

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AG20	VDD_IO	P	VDD33	AH24	VDD_TX	P	VAA25
AG21	VDD_IO	P	VDD33	AH25	VDD_TX	P	VAA25
AG22	DNC	DNC	do not connect	AH26	VDD_TX	P	VAA25
AG23	VDD_SD	P	VAA18	AH27	VDD_TX	P	VAA25
AG24	VDD_SD	P	VAA18	AH28	VDD_TX	P	VAA25
AG25	VDD_SD	P	VAA18	AH29	VSS	P	VSS
AG26	VDD_SD	P	VAA18	AH30	VSS	P	VSS
AG27	VDD_SD	P	VAA18	AH31	DNC	DNC	do not connect
AG28	VDD_TX	P	VAA25	AH32	DNC	DNC	do not connect
AG29	VSS	P	VSS	AH33	DNC	DNC	do not connect
AG30	VSS	P	VSS	AH34	DNC	DNC	do not connect
AG31	DNC	DNC	do not connect	AH35	DNC	DNC	do not connect
AG32	DNC	DNC	do not connect	AH36	VSS	P	VSS
AG33	DNC	DNC	do not connect	AH37	TXP[09]	O	Serdes diff output
AG34	DNC	DNC	do not connect	AH38	VSS	P	VSS
AG35	DNC	DNC	do not connect	AH39	RXP[09]	I	Serdes diff input
AG36	VSS	P	VSS	AJ1	VSS	P	VSS
AG37	TXN[09]	O	Serdes diff output	AJ2	CRX_CTRL_SOFN	O	LVDS
AG38	VSS	P	VSS	AJ3	CRX_CTRL_SOPF	O	LVDS
AG39	RXN[09]	I	Serdes diff input	AJ4	VDD_IO	P	VDD33
AH1	CRX_REFCLK	I	3.3V LVTTTL	AJ5	RPD	I	RPD
AH2	VSS	P	VSS	AJ6	VSS	P	VSS
AH3	CRX_CTRL_DATN[3]	O	LVDS	AJ7	RPD	I	RPD
AH4	CRX_CTRL_DATP[3]	O	LVDS	AJ8	DNC	DNC	do not connect
AH5	PLL_CRX_RST	I	3.3V LVTTTL	AJ9	DNC	DNC	do not connect
AH6	PLL_CRX_LCK	O	3.3V LVTTTL	AJ10	DNC	DNC	do not connect
AH7	VSS	P	VSS	AJ11	VSS	P	VSS
AH8	DNC	DNC	do not connect	AJ12	VSS	P	VSS
AH9	DNC	DNC	do not connect	AJ13	VSS	P	VSS
AH10	DNC	DNC	do not connect	AJ14	VSS	P	VSS
AH11	VSS	P	VSS	AJ15	VSS	P	VSS
AH12	VSS	P	VSS	AJ16	VSS	P	VSS
AH13	VSS	P	VSS	AJ17	VSS	P	VSS
AH14	VSS	P	VSS	AJ18	VSS	P	VSS
AH15	VSS	P	VSS	AJ19	VSS	P	VSS
AH16	VSS	P	VSS	AJ20	VSS	P	VSS
AH17	VSS	P	VSS	AJ21	VSS	P	VSS
AH18	VSS	P	VSS	AJ22	DNC	DNC	do not connect
AH19	VSS	P	VSS	AJ23	VSS	P	VSS
AH20	VSS	P	VSS	AJ24	VSS	P	VSS
AH21	VSS	P	VSS	AJ25	VSS	P	VSS
AH22	DNC	DNC	do not connect	AJ26	VSS	P	VSS
AH23	VDD_TX	P	VAA25	AJ27	VSS	P	VSS

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AJ28	VSS	P	VSS	AK32	DNC	DNC	do not connect
AJ29	VSS	P	VSS	AK33	DNC	DNC	do not connect
AJ30	VSS	P	VSS	AK34	DNC	DNC	do not connect
AJ31	DNC	DNC	do not connect	AK35	DNC	DNC	do not connect
AJ32	DNC	DNC	do not connect	AK36	VSS	P	VSS
AJ33	DNC	DNC	do not connect	AK37	TXP[08]	O	Serdes diff output
AJ34	DNC	DNC	do not connect	AK38	VSS	P	VSS
AJ35	DNC	DNC	do not connect	AK39	RXP[08]	I	Serdes diff input
AJ36	VSS	P	VSS	AL1	VDD_IO	P	VDD33
AJ37	TXN[08]	O	Serdes diff output	AL2	DNC	DNC	do not connect
AJ38	VSS	P	VSS	AL3	RPD	I	RPD
AJ39	RXN[08]	I	Serdes diff input	AL4	VSS	P	VSS
AK1	DNC	DNC	do not connect	AL5	RPD	I	RPD
AK2	DNC	DNC	do not connect	AL6	VSS	P	VSS
AK3	RPD	I	RPD	AL7	RPD	I	RPD
AK4	RPD	I	RPD	AL8	DNC	DNC	do not connect
AK5	RPD	I	RPD	AL9	DNC	DNC	do not connect
AK6	RPD	I	RPD	AL10	DNC	DNC	do not connect
AK7	RPD	I	RPD	AL11	DNC	DNC	do not connect
AK8	DNC	DNC	do not connect	AL12	DNC	DNC	do not connect
AK9	DNC	DNC	do not connect	AL13	DNC	DNC	do not connect
AK10	DNC	DNC	do not connect	AL14	DNC	DNC	do not connect
AK11	DNC	DNC	do not connect	AL15	DNC	DNC	do not connect
AK12	DNC	DNC	do not connect	AL16	DNC	DNC	do not connect
AK13	DNC	DNC	do not connect	AL17	DNC	DNC	do not connect
AK14	DNC	DNC	do not connect	AL18	DNC	DNC	do not connect
AK15	DNC	DNC	do not connect	AL19	DNC	DNC	do not connect
AK16	DNC	DNC	do not connect	AL20	DNC	DNC	do not connect
AK17	DNC	DNC	do not connect	AL21	DNC	DNC	do not connect
AK18	DNC	DNC	do not connect	AL22	DNC	DNC	do not connect
AK19	VSS	P	VSS	AL23	VSS_SD0_PLL	P	VSS
AK20	DNC	DNC	do not connect	AL24	VDD_SD0_PLL	P	VAA18
AK21	DNC	DNC	do not connect	AL25	DNC	DNC	do not connect
AK22	VDD_REFCLK0	P	VAA33	AL26	DNC	DNC	do not connect
AK23	VSS	P	VSS	AL27	DNC	DNC	do not connect
AK24	VSS	P	VSS	AL28	DNC	DNC	do not connect
AK25	VSS	P	VSS	AL29	DNC	DNC	do not connect
AK26	VSS	P	VSS	AL30	DNC	DNC	do not connect
AK27	VSS	P	VSS	AL31	DNC	DNC	do not connect
AK28	VSS	P	VSS	AL32	DNC	DNC	do not connect
AK29	VSS	P	VSS	AL33	DNC	DNC	do not connect
AK30	VSS	P	VSS	AL34	DNC	DNC	do not connect
AK31	DNC	DNC	do not connect	AL35	DNC	DNC	do not connect

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AL36	VSS	P	VSS	AN1	VSS	P	VSS
AL37	TXN[07]	O	Serdes diff output	AN2	DNC	DNC	do not connect
AL38	VSS	P	VSS	AN3	RPD	I	RPD
AL39	RXN[07]	I	Serdes diff input	AN4	VDD_IO	P	VDD33
AM1	DNC	DNC	do not connect	AN5	RPD	I	RPD
AM2	DNC	DNC	do not connect	AN6	VSS	P	VSS
AM3	RPD	I	RPD	AN7	RPD	I	RPD
AM4	RPD	I	RPD	AN8	VSS	P	VSS
AM5	RPD	I	RPD	AN9	DNC	DNC	do not connect
AM6	RPD	I	RPD	AN10	DNC	DNC	do not connect
AM7	RPD	I	RPD	AN11	DNC	DNC	do not connect
AM8	DNC	DNC	do not connect	AN12	DNC	DNC	do not connect
AM9	DNC	DNC	do not connect	AN13	DNC	DNC	do not connect
AM10	DNC	DNC	do not connect	AN14	DNC	DNC	do not connect
AM11	DNC	DNC	do not connect	AN15	DNC	DNC	do not connect
AM12	DNC	DNC	do not connect	AN16	VSS	P	VSS
AM13	DNC	DNC	do not connect	AN17	DNC	DNC	do not connect
AM14	DNC	DNC	do not connect	AN18	VSS	P	VSS
AM15	DNC	DNC	do not connect	AN19	DNC	DNC	do not connect
AM16	DNC	DNC	do not connect	AN20	VSS	P	VSS
AM17	DNC	DNC	do not connect	AN21	DNC	DNC	do not connect
AM18	DNC	DNC	do not connect	AN22	DNC	DNC	do not connect
AM19	DNC	DNC	do not connect	AN23	DNC	DNC	do not connect
AM20	DNC	DNC	do not connect	AN24	DNC	DNC	do not connect
AM21	DNC	DNC	do not connect	AN25	DNC	DNC	do not connect
AM22	DNC	DNC	do not connect	AN26	DNC	DNC	do not connect
AM23	DNC	DNC	do not connect	AN27	DNC	DNC	do not connect
AM24	DNC	DNC	do not connect	AN28	DNC	DNC	do not connect
AM25	DNC	DNC	do not connect	AN29	DNC	DNC	do not connect
AM26	DNC	DNC	do not connect	AN30	DNC	DNC	do not connect
AM27	DNC	DNC	do not connect	AN31	DNC	DNC	do not connect
AM28	DNC	DNC	do not connect	AN32	DNC	DNC	do not connect
AM29	DNC	DNC	do not connect	AN33	DNC	DNC	do not connect
AM30	DNC	DNC	do not connect	AN34	DNC	DNC	do not connect
AM31	DNC	DNC	do not connect	AN35	DNC	DNC	do not connect
AM32	DNC	DNC	do not connect	AN36	VSS	P	VSS
AM33	DNC	DNC	do not connect	AN37	TXN[06]	O	Serdes diff output
AM34	DNC	DNC	do not connect	AN38	VSS	P	VSS
AM35	DNC	DNC	do not connect	AN39	RXN[06]	I	Serdes diff input
AM36	VSS	P	VSS	AP1	DNC	DNC	do not connect
AM37	TXP[07]	O	Serdes diff output	AP2	DNC	DNC	do not connect
AM38	VSS	P	VSS	AP3	RPD	I	RPD
AM39	RXP[07]	I	Serdes diff input	AP4	RPD	I	RPD

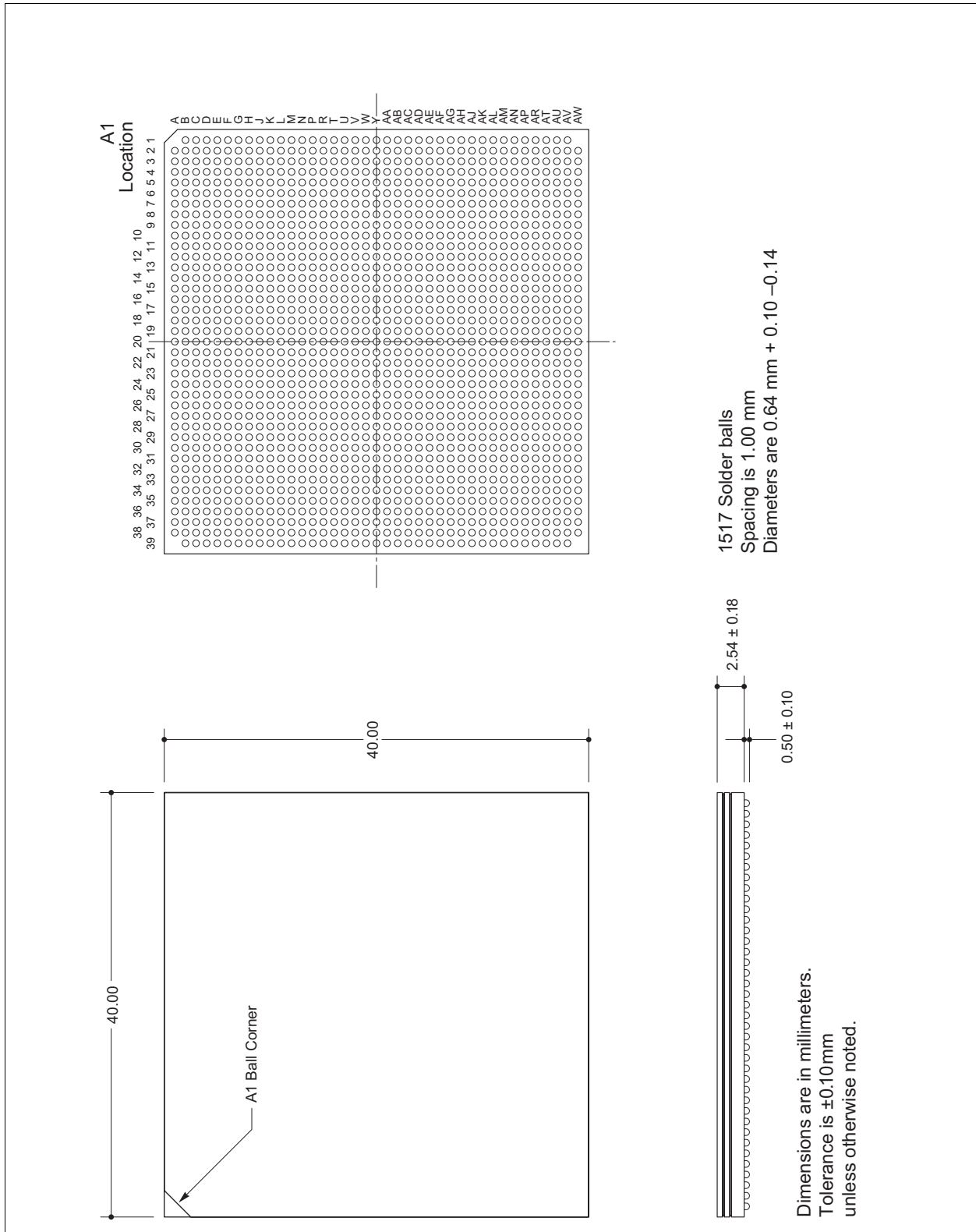
Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AP5	RPD	I	RPD	AR9	ZBUS_DEVID[2]	I	3.3V LVTTTL
AP6	RPD	I	RPD	AR10	ZBUS_DEVID[4]	I	3.3V LVTTTL
AP7	RPD	I	RPD	AR11	ZBUS_AVALID_N	I	3.3V LVTTTL
AP8	RPD	I	RPD	AR12	RESET_N	I	3.3V LVTTTL
AP9	ZBUS_DEVID[1]	I	3.3V LVTTTL	AR13	DNC	DNC	do not connect
AP10	ZBUS_DEVID[3]	I	3.3V LVTTTL	AR14	DNC	DNC	do not connect
AP11	VSS	P	VSS	AR15	DNC	DNC	do not connect
AP12	DNC	DNC	do not connect	AR16	DNC	DNC	do not connect
AP13	DNC	DNC	do not connect	AR17	DNC	DNC	do not connect
AP14	DNC	DNC	do not connect	AR18	DNC	DNC	do not connect
AP15	VSS	P	VSS	AR19	RPD	I	RPD
AP16	ZTICK_MODE	I	3.3V LVTTTL	AR20	DNC	DNC	do not connect
AP17	RPD	I	RPD	AR21	RPU	I	RPU
AP18	RPU	I	RPU	AR22	SD8_MODE	I	3.3V LVTTTL
AP19	RPU	I	RPU	AR23	DNC	DNC	do not connect
AP20	RPU	I	RPU	AR24	DNC	DNC	do not connect
AP21	CHN_DET_MODE	I	3.3V LVTTTL	AR25	VSS	P	VSS
AP22	RPD	I	RPD	AR26	DNC	DNC	do not connect
AP23	DNC	DNC	do not connect	AR27	DNC	DNC	do not connect
AP24	DNC	DNC	do not connect	AR28	DNC	DNC	do not connect
AP25	DNC	DNC	do not connect	AR29	DNC	DNC	do not connect
AP26	DNC	DNC	do not connect	AR30	DNC	DNC	do not connect
AP27	DNC	DNC	do not connect	AR31	DNC	DNC	do not connect
AP28	DNC	DNC	do not connect	AR32	DNC	DNC	do not connect
AP29	DNC	DNC	do not connect	AR33	DNC	DNC	do not connect
AP30	DNC	DNC	do not connect	AR34	DNC	DNC	do not connect
AP31	DNC	DNC	do not connect	AR35	DNC	DNC	do not connect
AP32	DNC	DNC	do not connect	AR36	VSS	P	VSS
AP33	DNC	DNC	do not connect	AR37	TXN[05]	O	Serdes diff output
AP34	DNC	DNC	do not connect	AR38	VSS	P	VSS
AP35	DNC	DNC	do not connect	AR39	RXN[05]	I	Serdes diff input
AP36	VSS	P	VSS	AT1	RPD	I	RPD
AP37	TXP[06]	O	Serdes diff output	AT2	DNC	DNC	do not connect
AP38	VSS	P	VSS	AT3	RPD	I	RPD
AP39	RXP[06]	I	Serdes diff input	AT4	VDD_IO	P	VDD33
AR1	VDD_IO	P	VDD33	AT5	RPD	I	RPD
AR2	DNC	DNC	do not connect	AT6	VSS	P	VSS
AR3	RPD	I	RPD	AT7	ZBUS_AD[03]	B	3.3V LVTTTL
AR4	VSS	P	VSS	AT8	VDD_IO	P	VDD33
AR5	RPD	I	RPD	AT9	ZBUS_AD[09]	B	3.3V LVTTTL
AR6	VSS	P	VSS	AT10	VSS	P	VSS
AR7	RPD	I	RPD	AT11	ZBUS_AD[15]	B	3.3V LVTTTL
AR8	ZBUS_DEVID[0]	I	3.3V LVTTTL	AT12	VDD_IO	P	VDD33

Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AT13	TURBO_DAT[0]	I	3.3V LVTTTL	AU17	DNC	DNC	do not connect
AT14	VSS	P	VSS	AU18	DNC	DNC	do not connect
AT15	DNC	DNC	do not connect	AU19	DNC	DNC	do not connect
AT16	VDD_IO	P	VDD33	AU20	DNC	DNC	do not connect
AT17	DNC	DNC	do not connect	AU21	DNC	DNC	do not connect
AT18	VSS	P	VSS	AU22	DNC	DNC	do not connect
AT19	DNC	DNC	do not connect	AU23	VSS	P	VSS
AT20	VDD_IO	P	VDD33	AU24	VSS	P	VSS
AT21	DNC	DNC	do not connect	AU25	RPD	I	RPD
AT22	VSS	P	VSS	AU26	DNC	DNC	do not connect
AT23	VSS	P	VSS	AU27	VSS	P	VSS
AT24	VSS	P	VSS	AU28	TXP[00]	O	Serdes diff output
AT25	SD0_REF_RES	B	Serdes Bidi	AU29	TXN[00]	O	Serdes diff output
AT26	DNC	DNC	do not connect	AU30	TXP[01]	O	Serdes diff output
AT27	VSS	P	VSS	AU31	TXN[01]	O	Serdes diff output
AT28	VSS	P	VSS	AU32	TXP[02]	O	Serdes diff output
AT29	VSS	P	VSS	AU33	TXN[02]	O	Serdes diff output
AT30	VSS	P	VSS	AU34	TXP[03]	O	Serdes diff output
AT31	VSS	P	VSS	AU35	TXN[03]	O	Serdes diff output
AT32	VSS	P	VSS	AU36	VSS	P	VSS
AT33	VSS	P	VSS	AU37	TXN[04]	O	Serdes diff output
AT34	VSS	P	VSS	AU38	VSS	P	VSS
AT35	VSS	P	VSS	AU39	RXN[04]	I	Serdes diff input
AT36	VSS	P	VSS	AV1	VDD_IO	P	VDD33
AT37	TXP[05]	O	Serdes diff output	AV2	RPD	I	RPD
AT38	VSS	P	VSS	AV3	VSS	P	VSS
AT39	RXP[05]	I	Serdes diff input	AV4	ZBUS_PRTY	B	3.3V LVTTTL
AU1	VSS	P	VSS	AV5	ZBUS_AD[01]	B	3.3V LVTTTL
AU2	RPD	I	RPD	AV6	ZBUS_AD[05]	B	3.3V LVTTTL
AU3	RPD	I	RPD	AV7	ZBUS_AD[07]	B	3.3V LVTTTL
AU4	RPD	I	RPD	AV8	ZBUS_AD[10]	B	3.3V LVTTTL
AU5	RPD	I	RPD	AV9	ZBUS_AD[12]	B	3.3V LVTTTL
AU6	ZBUS_AD[02]	B	3.3V LVTTTL	AV10	ZBUS_DVALID_N	B	3.3V LVTTTL
AU7	ZBUS_AD[06]	B	3.3V LVTTTL	AV11	ZBUS_INT_N[1]	O	3.3V LVTTTL
AU8	ZBUS_AD[08]	B	3.3V LVTTTL	AV12	TURBO_DAT[1]	I	3.3V LVTTTL
AU9	ZBUS_AD[11]	B	3.3V LVTTTL	AV13	TURBO_SOF	I	3.3V LVTTTL
AU10	ZBUS_AD[13]	B	3.3V LVTTTL	AV14	DNC	DNC	do not connect
AU11	ZBUS_INT_N[0]	O	3.3V LVTTTL	AV15	DNC	DNC	do not connect
AU12	ZTICK	I	3.3V LVTTTL	AV16	DNC	DNC	do not connect
AU13	TURBO_DAT[2]	I	3.3V LVTTTL	AV17	DNC	DNC	do not connect
AU14	DNC	DNC	do not connect	AV18	DNC	DNC	do not connect
AU15	DNC	DNC	do not connect	AV19	DNC	DNC	do not connect
AU16	DNC	DNC	do not connect	AV20	DNC	DNC	do not connect

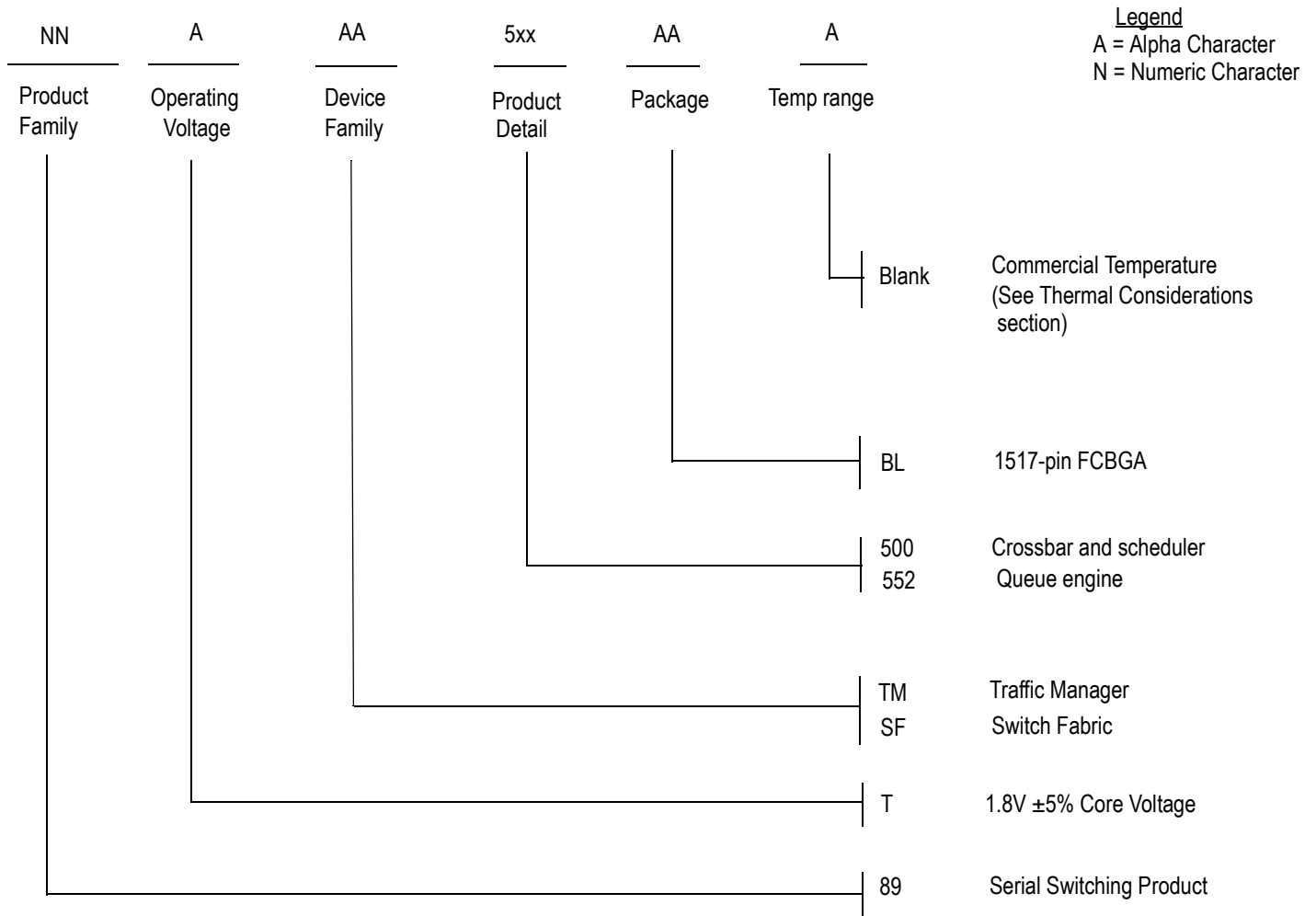
Pin	Signal	I/O	Type	Pin	Signal	I/O	Type
AV21	DNC	DNC	do not connect	AW26	SD0_REFCLKN	I	Serdes diff clock
AV22	DNC	DNC	do not connect	AW27	VSS	P	VSS
AV23	VSS	P	VSS	AW28	RXP[00]	I	Serdes diff input
AV24	VSS	P	VSS	AW29	RXN[00]	I	Serdes diff input
AV25	VSS	P	VSS	AW30	RXP[01]	I	Serdes diff input
AV26	VSS	P	VSS	AW31	RXN[01]	I	Serdes diff input
AV27	VSS	P	VSS	AW32	RXP[02]	I	Serdes diff input
AV28	VSS	P	VSS	AW33	RXN[02]	I	Serdes diff input
AV29	VSS	P	VSS	AW34	RXP[03]	I	Serdes diff input
AV30	VSS	P	VSS	AW35	RXN[03]	I	Serdes diff input
AV31	VSS	P	VSS	AW36	VSS	P	VSS
AV32	VSS	P	VSS	AW37	VSS	P	VSS
AV33	VSS	P	VSS	AW38	VSS	P	VSS
AV34	VSS	P	VSS				
AV35	VSS	P	VSS				
AV36	VSS	P	VSS				
AV37	TXP[04]	O	Serdes diff output				
AV38	VSS	P	VSS				
AV39	RXP[04]	I	Serdes diff input				
AW2	VDD_IO	P	VDD33				
AW3	ZBUS_AD[00]	B	3.3V LVTTTL				
AW4	VSS	P	VSS				
AW5	ZBUS_AD[04]	B	3.3V LVTTTL				
AW6	VDD_IO	P	VDD33				
AW7	ZBUS_CLK	I	3.3V LVTTTL				
AW8	VSS	P	VSS				
AW9	ZBUS_AD[14]	B	3.3V LVTTTL				
AW10	VDD_IO	P	VDD33				
AW11	ZBUS_INT_N[2]	O	3.3V LVTTTL				
AW12	VSS	P	VSS				
AW13	TURBO_CLK	I	3.3V LVTTTL				
AW14	VDD_IO	P	VDD33				
AW15	DNC	DNC	do not connect				
AW16	VSS	P	VSS				
AW17	DNC	DNC	do not connect				
AW18	VDD_IO	P	VDD33				
AW19	DNC	DNC	do not connect				
AW20	VSS	P	VSS				
AW21	DNC	DNC	do not connect				
AW22	VDD_IO	P	VDD33				
AW23	VSS	P	VSS				
AW24	VSS	P	VSS				
AW25	SD0_REFCLKP	I	Serdes diff clock				

89TSF552 Package Diagram

The 89TSF552 package is an Amkor FCBGA, having 1517 pins, with 1 mm pitch; a 39x39 pin array; and a 40x40 mm enclosure. The package geometry is shown below.



Ordering Information



Legend

A = Alpha Character
N = Numeric Character

Valid Combinations

89TSF552BL

1517-pin FCBGA package, Commercial Temperature

Revision History

November 24, 2004: Initial publication by IDT.

June 17, 2005: Made changes to Tables 21 through 25.

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