

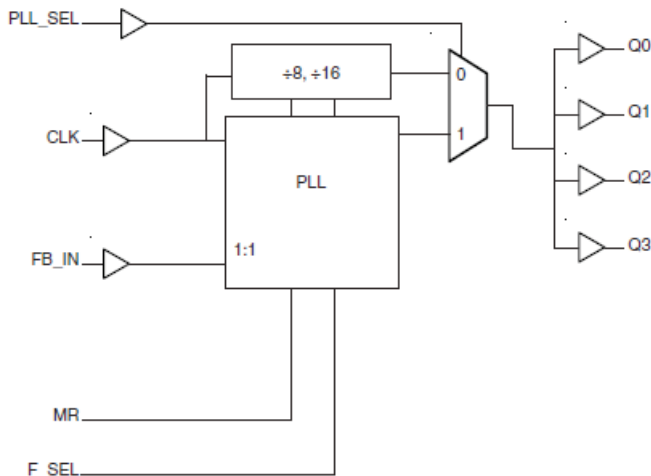
GENERAL DESCRIPTION

The 86004 is a high performance 1:4 LVCMOS/LVTTL Clock Buffer. The 86004 has a fully integrated PLL and can be configured as zero delay buffer and has an input and output frequency range of 15.625MHz to 62.5MHz. The VCO operates at a frequency range of 250MHz to 500MHz. The external feedback allows the device to achieve “zero delay” between the input clock and the output clocks. The PLL_SEL pin can be used to bypass the PLL for system test and debug purposes. In bypass mode, the reference clock is routed around the PLL and into the internal output divider.

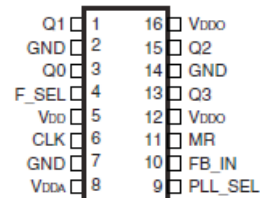
FEATURES

- Four LVCMOS/LVTTL outputs, 7Ω typical output impedance
- Single LVCMOS/LVTTL clock input
- CLK accepts the following input levels: LVCMOS or LVTTL
- Output frequency range: 15.625MHz to 62.5MHz
- Input frequency range: 15.625MHz to 62.5MHz
- VCO range: 250MHz to 500MHz
- External feedback for “zero delay” clock regeneration with configurable frequencies
- Fully integrated PLL
- Cycle-to-cycle jitter: 65ps (maximum)
- Output skew: 65ps (maximum)
- Full 3.3V or 2.5V, or 3.3V core/2.5V output operating supply
- 0°C to 70° ambient operating temperature
- Available in lead-free RoHS compliant package

BLOCK DIAGRAM



PIN ASSIGNMENT



86004

16-Lead TSSOP

4.4mm x 5.0mm x 0.925mm package body

G Package

Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 3, 13, 15	Q1, Q0, Q3, Q2	Output		Clock outputs. 7 typical output impedance. LVCMOS/LVTTL interface levels.
2, 7, 14	GND	Power		Power supply ground.
4	F_SEL	Input	Pulldown	Frequency range select input. See Table 3A and 3B. LVCMOS/LVTTL interface levels.
5	V _{DD}	Power		Core supply pin.
6	CLK	Input	Pulldown	LVCMOS/LVTTL clock input.
8	V _{DDA}	Power		Analog supply pin.
9	PLL_SEL	Input	Pullup	Selects between the PLL and reference clock as input to the dividers. When LOW, selects the reference clock (PLL Bypass). When HIGH, selects PLL (PLL Enabled). LVCMOS/LVTTL interface levels.
10	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with “zero delay”. Connect to one of the outputs. LVCMOS/LVTTL interface levels.
11	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset causing the outputs to go low. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
12, 16	V _{DDO}	Power		Output supply pins.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
R _{PULLUP}	Input Pullup Resistor			51		kΩ
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
C _{PD}	Power Dissipation Capacitance (per output)	V _{DD} , V _{DDA} , V _{DDO} = 3.465V			23	pF
		V _{DD} , V _{DDA} , V _{DDO} = 2.625V			17	pF
R _{OUT}	Output Impedance	3.3V ± 5%	5	7	12	Ω

TABLE 3A. CONTROL INPUT FUNCTION TABLE, PLL_SEL = 1

Input	Input/Output Frequency Range (MHz)		
	F_SEL	Minimum	Maximum
0		31.25	62.5
1		15.625	31.25

TABLE 3B. CONTROL INPUT FUNCTION TABLE, PLL_SEL = 0

Input	Output
F_SEL	
0	Ref ÷8
1	Ref ÷16

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, V_O	-0.5V to $V_{DDO} + 0.5V$
Package Thermal Impedance, θ_{JA}	89°C/W (0 lfm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				98	mA
I_{DDA}	Analog Supply Current				17	mA
I_{DDO}	Output Supply Current				8	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		3.135	3.3	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				98	mA
I_{DDA}	Analog Supply Current				17	mA
I_{DDO}	Output Supply Current				8	mA

TABLE 4C. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		2.375	2.5	V_{DD}	V
V_{DDO}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current				88	mA
I_{DDA}	Analog Supply Current				14	mA
I_{DDO}	Output Supply Current				6	mA

TABLE 4D. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$ OR $2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	CLK, MR, FB_IN, F_SEL $V_{DD} = V_{IN} = 3.465V$			150	μA
		PLL_SEL $V_{DD} = V_{IN} = 3.465V$			5	μA
I_{IL}	Input Low Current	CLK, MR, FB_IN, F_SEL $V_{DD} = 3.465V, V_{IN} = 0V$	-5			μA
		PLL_SEL $V_{DD} = 3.465V, V_{IN} = 0V$	-150			μA
V_{OH}	Output High Voltage; NOTE 1	$V_{DDO} = 3.465V$	2.6			V
		$V_{DDO} = 2.625V$	1.8			V
V_{OL}	Output Low Voltage; NOTE 1	$V_{DDO} = 3.465V$ or $2.625V$			0.5	V

NOTE 1: Outputs terminated with 50Ω to $V_{DDO}/2$. See Parameter Measurement Information Section, *Output Load Test Circuit diagrams*.

TABLE 5A. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
tp_{LH}	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.1		6.1	ns
$t(\emptyset)$	Static Phase Offset; NOTE 2, 4	PLL_SEL = 3.3V	-500		500	ps
$tsk(o)$	Output Skew; NOTE 3, 4	PLL_SEL = 0V			65	ps
$tjit(cc)$	Cycle-to-Cycle Jitter; NOTE 4			50	65	ps
t_L	PLL Lock Time				1	mS
t_R / t_F	Output Rise/Fall Time		0.4		1	ns
odc	Output Duty Cycle		49		51	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5B. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = 3.3V \pm 5\%$, $V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.25		6.25	ns
$t(\emptyset)$	Static Phase Offset; NOTE 2, 4	PLL_SEL = 2.5V	-500		500	ps
$tsk(o)$	Output Skew; NOTE 3, 4	PLL_SEL = 0V			65	ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 4				65	ps
t_L	PLL Lock Time				1	mS
t_R / t_F	Output Rise/Fall Time		0.4		1	ns
odc	Output Duty Cycle		48		52	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

Measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

TABLE 5C. AC CHARACTERISTICS, $V_{DD} = V_{DDA} = V_{DDO} = 2.5V \pm 5\%$, $T_A = 0^\circ\text{C}$ TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency	F_SEL = 0	31.25		62.5	MHz
		F_SEL = 1	15.625		31.25	MHz
$t_{p_{LH}}$	Propagation Delay, Low-to-High; NOTE 1	PLL_SEL = 0V, Bypass Mode	4.5		6.5	ns
$t(\emptyset)$	Static Phase Offset; NOTE 2, 4	PLL_SEL = 2.5V	-500		500	ps
$tsk(o)$	Output Skew; NOTE 3, 4	PLL_SEL = 0V			65	ps
$t_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 4				70	ps
t_L	PLL Lock Time				1	mS
t_R / t_F	Output Rise/Fall Time		0.4		1	ns
odc	Output Duty Cycle		48		52	%

All parameters measured at f_{MAX} unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the output at $V_{DDO}/2$.

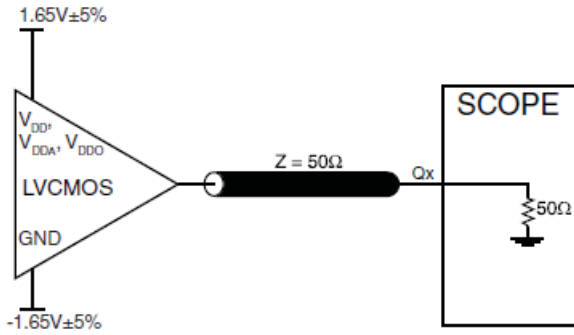
NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

NOTE 3: Defined as skew between outputs at the same supply voltages and with equal load conditions.

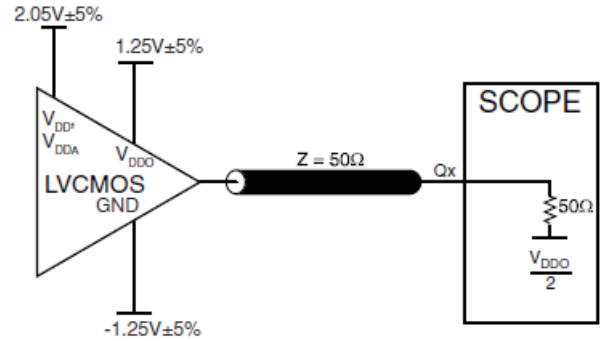
Measured at $V_{DDO}/2$.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

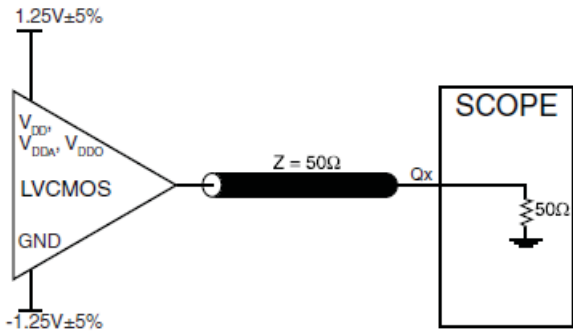
PARAMETER MEASUREMENT INFORMATION



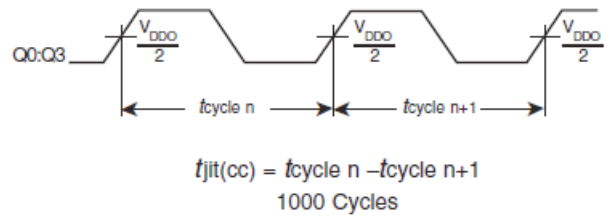
3.3V CORE/3.3V OUTPUT LOAD AC TEST CIRCUIT



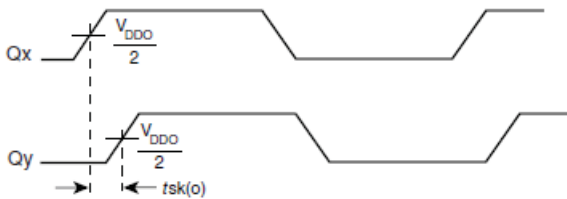
3.3V CORE/2.5V OUTPUT LOAD AC TEST CIRCUIT



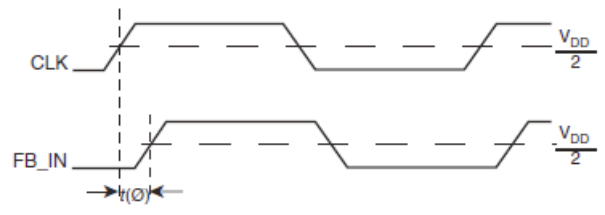
2.5V CORE/ 2.5V OUTPUT LOAD AC TEST CIRCUIT



CYCLE-TO-CYCLE JITTER

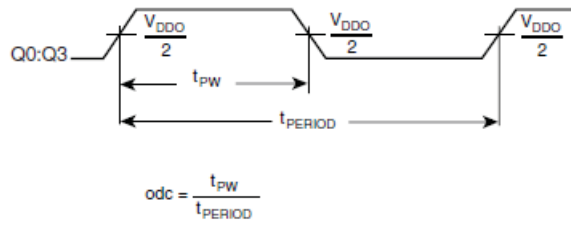


OUTPUT SKEW

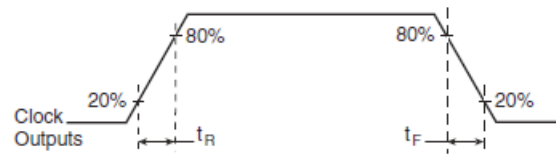


$t(\emptyset)_{\text{mean}}$ = Static Phase Offset
 (where $t(\emptyset)$ is any random sample, and $t(\emptyset)_{\text{mean}}$ is the average of the sampled cycles measured on controlled edges)

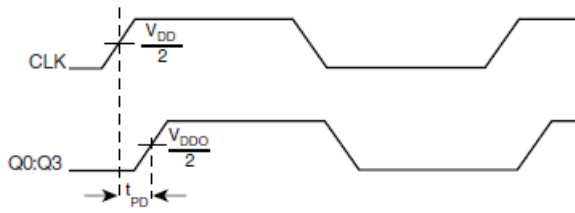
STATIC PHASE OFFSET



OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



OUTPUT RISE/FALL TIME



PROPAGATION DELAY

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The 86004 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , and V_{DDO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a 10Ω resistor along with a $10\mu\text{F}$ and a $.01\mu\text{F}$ bypass capacitor should be connected to each V_{DDA} .

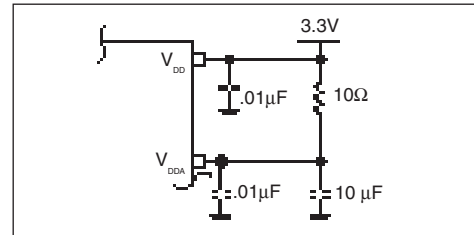


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

LVC MOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

LVC MOS OUTPUT:

All unused LVC MOS output can be left floating. We recommend that there is no trace attached.

SCHEMATIC EXAMPLE

Figure 2 shows a schematic example of using an 86004. It is recommended to have one decouple capacitor per power pin. Each decoupling capacitor should be located as close as possible to the

power pin. The low pass filter R7, C11 and C16 for clean analog supply should also be located as close to the V_{DDA} pin as possible.

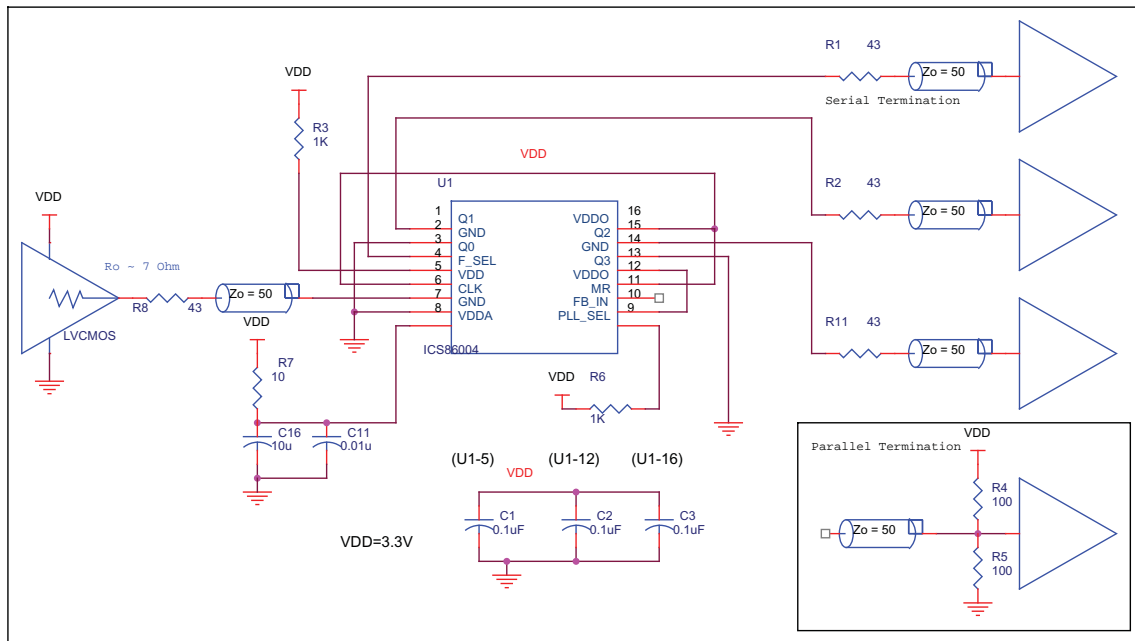


FIGURE 2. 86004 SCHEMATIC EXAMPLE

RELIABILITY INFORMATION

TABLE 5. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	137.1°C/W	118.2°C/W	106.8°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	89.0°C/W	81.8°C/W	78.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT

The transistor count for 86004 is: 2496

PACKAGE OUTLINE - G SUFFIX 16 LEAD TSSOP

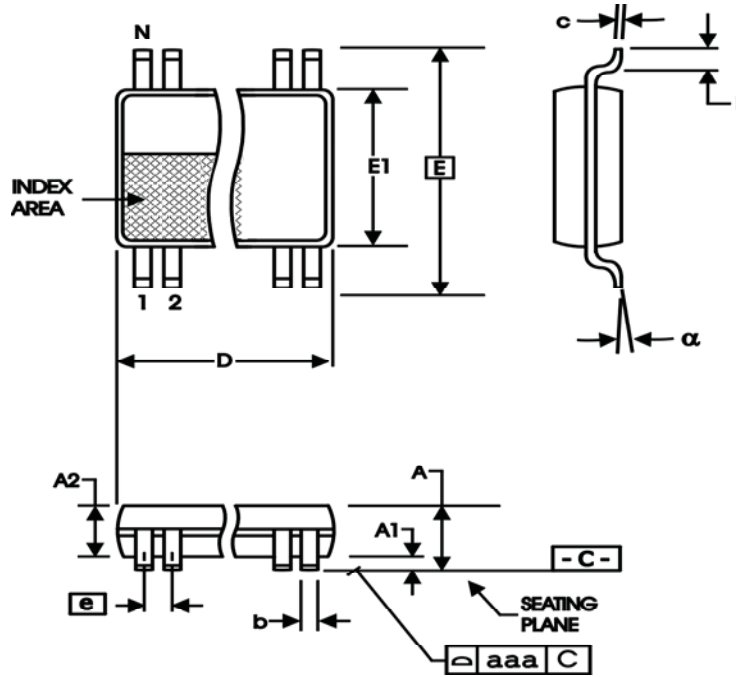


TABLE 6. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
86004BGLF	86004BGL	16 Lead "Lead-Free" TSSOP	Tube	0°C to 70°C
86004BGLFT	86004BGL	16 Lead "Lead-Free" TSSOP	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

Rev	Table	Page	Description of Change	Date
A	T7	1 12	Pin Assignment - corrected package body dimensions from 4.4mm x 3.0 mm x 0.92mm to 4.4mm x5.0 mm x 0.925mm. Ordering Information Table - corrected marking from 86004BG from 86004BG. Added lead-free marking.	3/31/06
B	4A	3	3.3V Power Supply Table - changed V_{DA} max from 3.465V to V_{DD} , changed I_{DDO} from 79mA max. to 8mA max.	6/21/06
	4B	3	3.3V/2.5V Power Supply Table - changed V_{DA} max from 3.465V to V_{DD} , changed I_{DDO} from 79mA max. to 8mA max.	
	4C	3	2.5V Power Supply Table - changed V_{DDA} max from 3.465V to V_{DD} , changed I_{DDO} from 79mA max. to 6mA max.	
B	T7	11	Ordering Information - removed leaded devices. Updated data sheet format.	7/10/15

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.