

## GENERAL DESCRIPTION

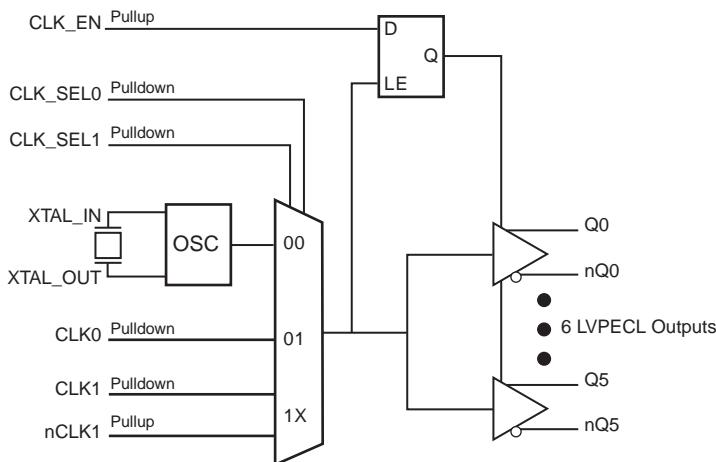
The ICS8536-01 is a low skew, high performance 1-to-6 Selectable Crystal, Single-Ended, or Differential Input-to-3.3V, 2.5V LVPECL Fanout Buffer. The ICS8536-01 has selectable crystal, single ended or differential clock inputs. The single ended clock input accepts LVC MOS or LVTTL input levels and translates them to LVPECL levels. The CLK1, nCLK1 pair can accept most standard differential input levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8536-01 ideal for those applications demanding well defined performance and repeatability.

## FEATURES

- Six 3.3V, 2.5V LVPECL outputs
- Selectable crystal oscillator, differential CLK1, nCLK1 pair or LVC MOS/LVTTL clock input
- CLK1, nCLK1 pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Maximum output frequency: 700MHz
- Crystal frequency range: 12MHz - 40MHz
- Output skew: 55ps (maximum) CLK1, nCLK1 @ 3.3V
- Part-to-part skew: 450ps (maximum)
- Additive phase jitter, RMS: 0.19ps (typical)
- Full 3.3V or 2.5V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

## BLOCK DIAGRAM



## PIN ASSIGNMENT

nQ2	1	24	Q3
Q2	2	23	nQ3
Vcc	3	22	Vcc
nQ1	4	21	Q4
Q1	5	20	nQ4
VEE	6	19	Vcc
nQ0	7	18	Q5
Q0	8	17	nQ5
CLK_SEL0	9	16	CLK_SEL1
XTAL_IN	10	15	nCLK1
XTAL_OUT	11	14	CLK1
CLK_EN	12	13	CLK0

**ICS8536-01**  
**24-Lead TSSOP**  
4.40mm x 7.8mm x 0.925mm  
package body  
**G Package**  
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type	Description
1, 2	nQ2, Q2	Output	Differential output pair. LVPECL interface levels.
3, 19, 22	V <sub>CC</sub>	Power	Power supply pins.
4, 5	nQ1, Q1	Output	Differential output pair. LVPECL interface levels.
6	V <sub>EE</sub>	Power	Negative supply pin.
7, 8	nQ0, Q0	Output	Differential output pair. LVPECL interface levels.
9, 16	CLK_SEL0, CLK_SEL1	Input	Pulldown Clock select pins. LVCMOS/LVTTL interface levels. See Table 3B.
10, 11	XTAL_IN, XTAL_OUT	Input	Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
12	CLK_EN	Input	Pullup Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, the outputs are disabled. LVCMOS / LVTTL interface levels. See Table 3A.
13	CLK0	Input	Pulldown LVCMOS/LVTTL clock input.
14	CLK1	Input	Pulldown Non-inverting differential clock input.
15	nCLK1	Input	Pullup Inverting differential clock input.
17, 18	nQ5, Q5	Output	Differential output pair. LVPECL interface levels.
20, 21	nQ4, Q4	Output	Differential output pair. LVPECL interface levels.
23, 24	nQ3, Q3	Output	Differential output pair. LVPECL interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ

TABLE 3A. CONTROL INPUT FUNCTION TABLE

Inputs				Outputs	
CLK_EN	CLK_SEL1	CLK_SEL0	Selected Source	Q0:Q5	nQ0:nQ5
0	0	0	XTAL	Disabled	Disabled
0	0	1	CLK0	Disabled	Disabled
0	1	X	CLK1, nCLK1	Disabled	Disabled
1	0	0	XTAL	Enabled	Enabled
1	0	1	CLK0	Enabled	Enabled
1	1	X	CLK1, nCLK1	Enabled	Enabled

After CLK\_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in *Figure 1*.

In the active mode, the state of the outputs are a function of the selected clock input as described in Table 3B.

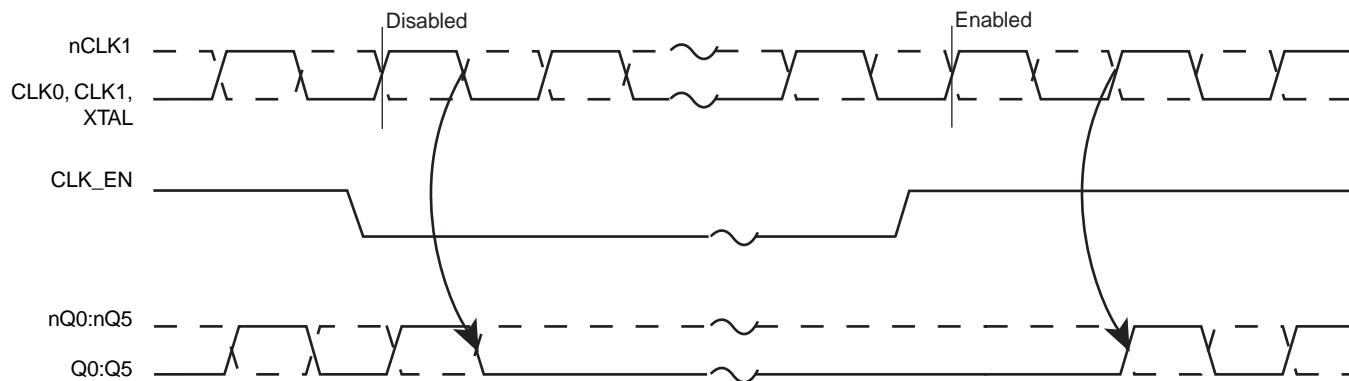


FIGURE 1. CLK\_EN TIMING DIAGRAM

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_I$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_O$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	84.6°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				85	mA

TABLE 4B. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Power Supply Voltage		2.375	2.5	2.625	V
$I_{EE}$	Power Supply Current				85	mA

TABLE 4C. LVCMOS / LVTTL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{CC} = 3.3V$		2		$V_{CC} + 0.3$	V
		$V_{CC} = 2.5V$		1.7		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{CC} = 3.3V$		-0.3		0.8	V
		$V_{CC} = 2.5V$		-0.3		0.7	V
$I_{IH}$	Input High Current	CLK0, CLK_SEL0:1	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			150	$\mu A$
		CLK_EN	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK_SEL0:1	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$
		CLK_EN	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$

**TABLE 4D. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$  OR  $2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	$V_{CC} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
		$V_{CC} = V_{IN} = 3.465V$			150	$\mu A$
$I_{IL}$	Input Low Current	$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$
		$V_{CC} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-5			$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1:  $V_{IL}$  should not be less than -0.3V.NOTE 2: Common mode voltage is defined as  $V_{IH}$ .**TABLE 4E. LVPECL DC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .**TABLE 4F. LVPECL DC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CC} - 1.4$		$V_{CC} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CC} - 2.0$		$V_{CC} - 1.5$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.4		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CC} - 2V$ .**TABLE 5. CRYSTAL CHARACTERISTICS**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation	Fundamental				
Frequency		12		40	MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6A. AC CHARACTERISTICS,  $V_{CC} = 3.3V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	CLK1/nCLK1				700	MHz
		CLK0				300	MHz
$t_{PD}$	Propagation Delay, NOTE1A, 1B	CLK1/nCLK1		1.7		2.5	ns
		CLK0		1.35		2.0	ns
$t_{JIT}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2	CLK1/nCLK1, 155.52MHz, Integration Range: 12kHz - 20MHz			0.19		ps
$t_{SK(o)}$	Output Skew; NOTE 3, 5					55	ps
$t_{SK(pp)}$	Part-to-Part Skew; NOTE 4, 5					450	ps
$t_R / t_F$	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle	CLK1/nCLK1		48		52	%
		CLK0		44		56	%
$MUX_{-ISOLATION}$	MUX Isolation	NOTE 6A	$f = 150MHz$		-76		dB
		NOTE 6B	$f = 250MHz$		-75		dB

All parameters measured at  $f_{OUT} \leq 300MHz$  unless noted otherwise.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

The cycle-to-cycle jitter on the input will equal the jitter on the output. The part does not add jitter.

NOTE 1A: Measured from the differential input crossing point to the differential output crossing point.

NOTE 1B: Measured from  $V_{CC}/2$  input crossing point to the differential output crossing point.

NOTE 2: Driving only one input clock.

NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 5: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 6A: CLK0 (150MHz) sensitivity is measured with CLK\_SEL[1:0] = 00.

NOTE 6B: CLK0 (250MHz) sensitivity is measured with CLK\_SEL[1:0] = 1X.

TABLE 6B. AC CHARACTERISTICS,  $V_{CC} = 2.5V \pm 5\%$ ,  $V_{EE} = 0V$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$ 

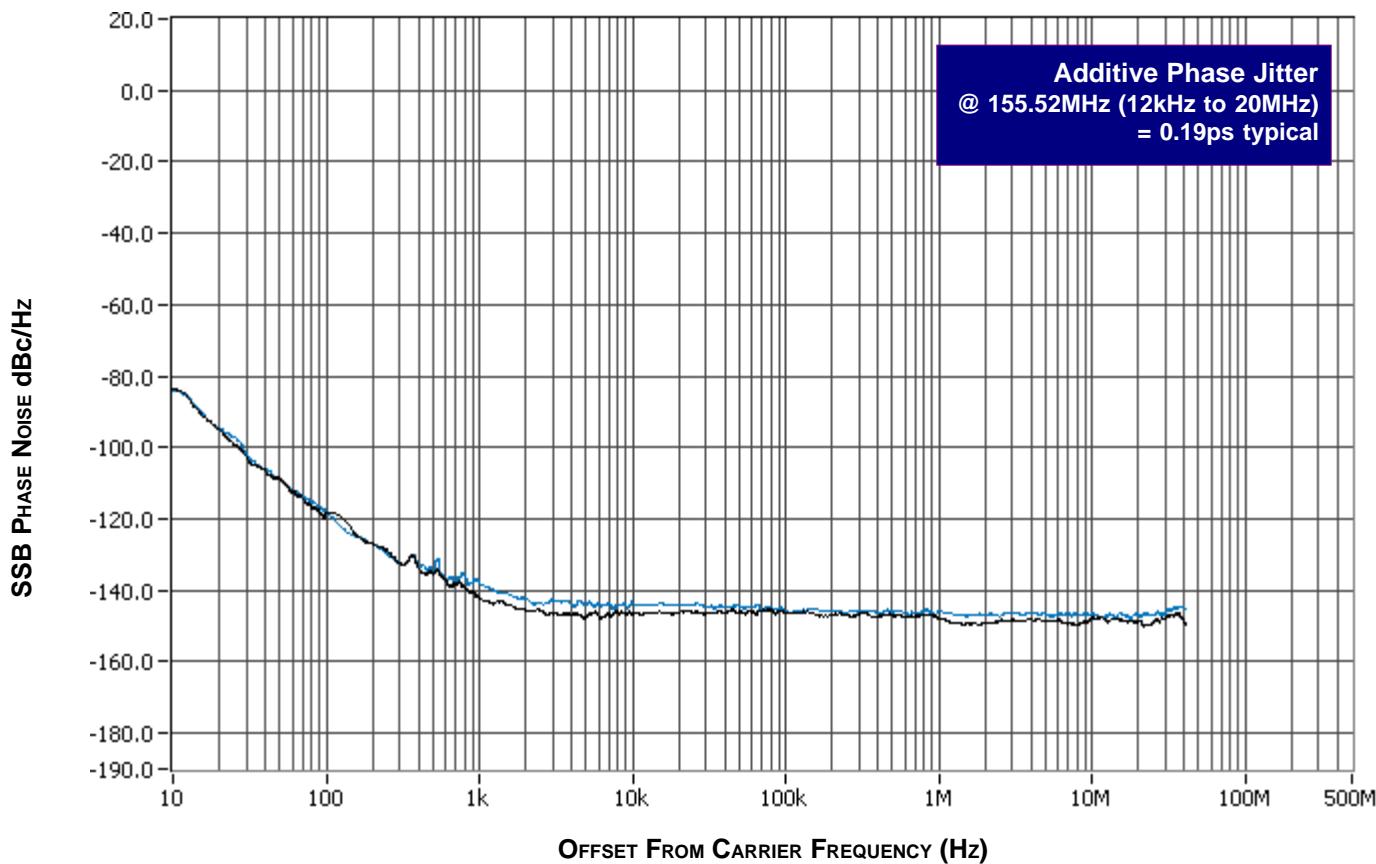
Symbol	Parameter	Test Conditions		Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency	CLK1, nCLK1				700	MHz
		CLK0				300	MHz
$t_{PD}$	Propagation Delay, NOTE1A, 1B	CLK1, nCLK1		1.7		2.65	ns
		CLK0		1.4		2.05	ns
$t_{JIT}$	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section; NOTE 2	CLK1, nCLK1, 155.52MHz, Integration Range: 12kHz - 20MHz			0.19		ps
$t_{SK(o)}$	Output Skew; NOTE 3, 5					55	ps
$t_{SK(pp)}$	Part-to-Part Skew; NOTE 4, 5					450	ps
$t_R / t_F$	Output Rise/Fall Time		20% to 80%	200		700	ps
odc	Output Duty Cycle	CLK1, nCLK1		48		52	%
		CLK0		46		54	%
$MUX_{-ISOLATION}$	MUX Isolation	NOTE 6A	$f = 150MHz$		-76		dB
		NOTE 6B	$f = 250MHz$		-75		dB

For notes, see Table 6A above.

## ADDITIVE PHASE JITTER

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise***. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz

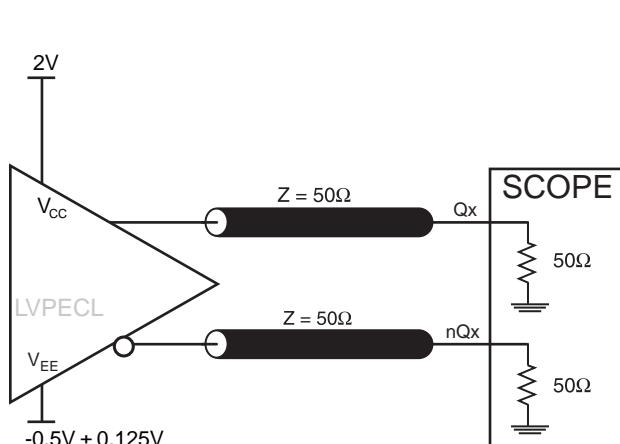
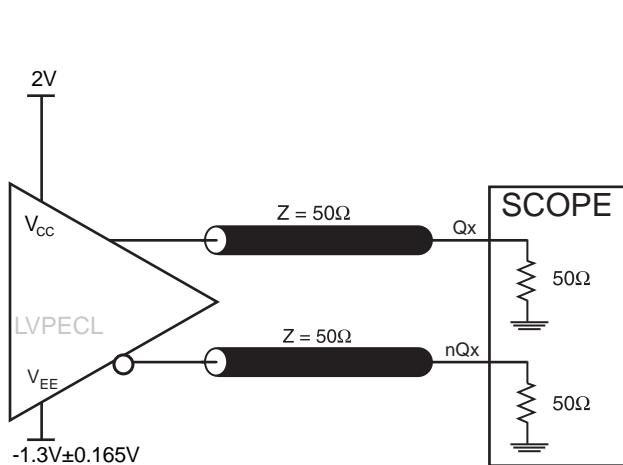
band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



As with most timing specifications, phase noise measurements have issues relating to the limitations of the measurement equipment. The noise floor of the equipment can be higher or

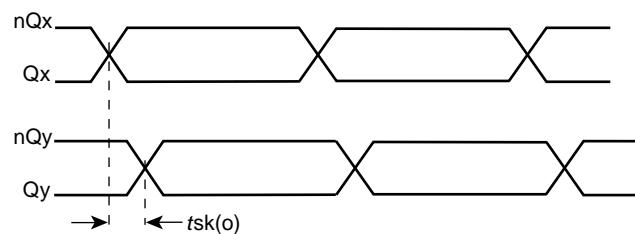
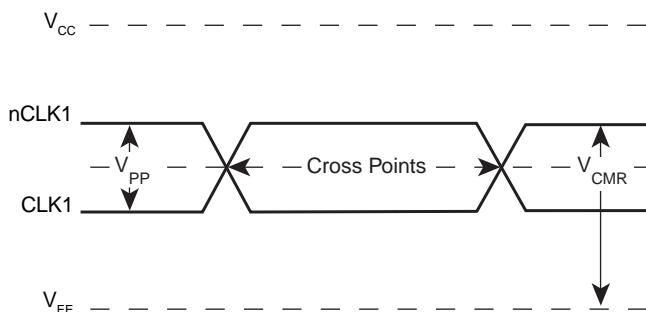
lower than the noise floor of the device. Additive phase noise is dependent on both the noise floor of the input source and measurement equipment.

## PARAMETER MEASUREMENT INFORMATION



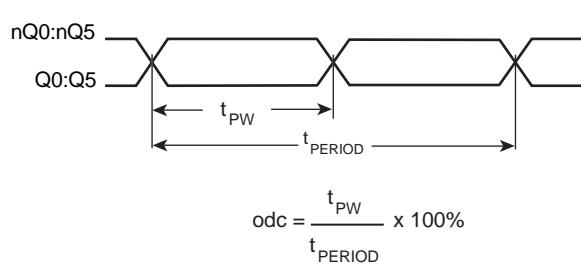
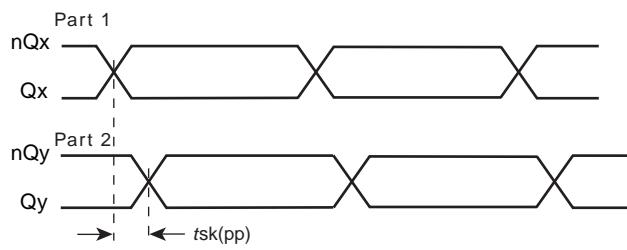
3.3V LVPECL Output Load AC Test Circuit

2.5V LVPECL Output Load AC Test Circuit



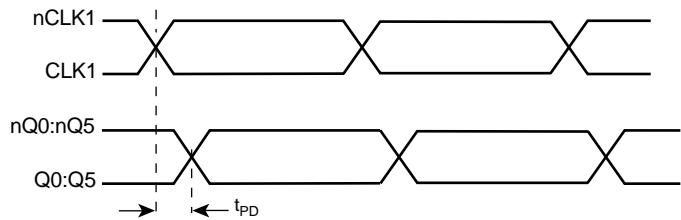
DIFFERENTIAL INPUT LEVELS

OUTPUT SKEW

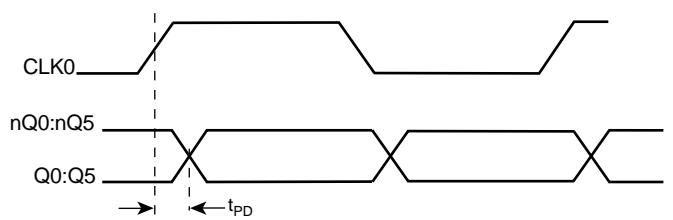


PART-TO-PART SKEW

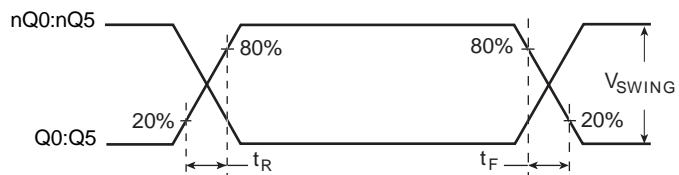
OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



PROPAGATION DELAY (DIFFERENTIAL INPUT)



PROPAGATION DELAY (LVCMOS INPUT)



OUTPUT RISE/FALL TIME

## APPLICATION INFORMATION

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage  $V_1 = V_{cc}/2$  is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is 2.5V and  $V_{cc} = 3.3V$ , R1 and R2 value should be adjusted to set  $V_1$  at 1.25V. The values below are for when both the single-ended swing and  $V_{cc}$  are at the same voltage. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First,  $R_3$  and  $R_4$  in parallel should equal the transmission line impedance. For most

50 applications,  $R_3$  and  $R_4$  can be  $100\Omega$ . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however  $V_{IL}$  cannot be less than -0.3V and  $V_{IH}$  cannot be more than  $V_{cc} + 0.3V$ . Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

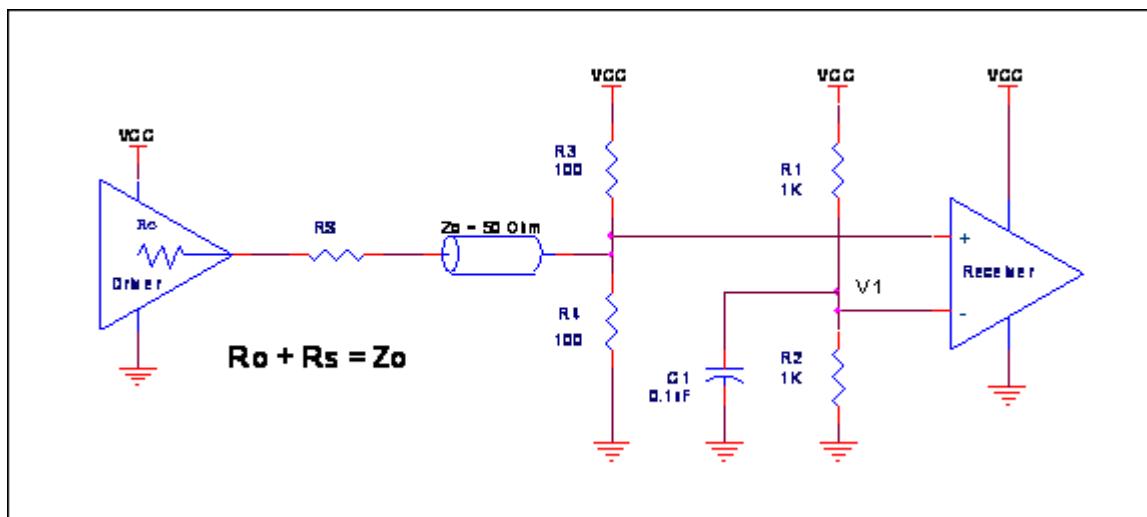


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

### CRYSTAL INPUT INTERFACE

The ICS8536-01 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in Figure 2 below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

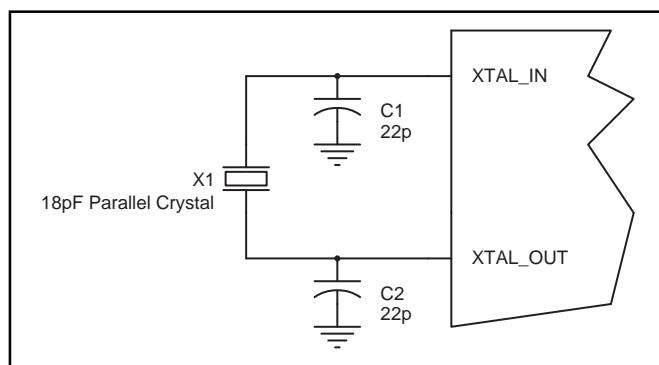


FIGURE 2. CRYSTAL INPUT INTERFACE

## OVERDRIVING THE CRYSTAL INTERFACE

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 3 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the

signal in half. This can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. Figure 3 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

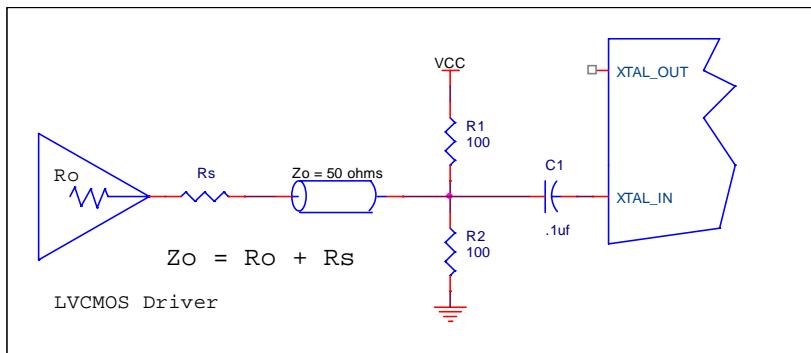


FIGURE 3A. GENERAL DIAGRAM FOR LVCMOS DRIVER TO XTAL INPUT INTERFACE

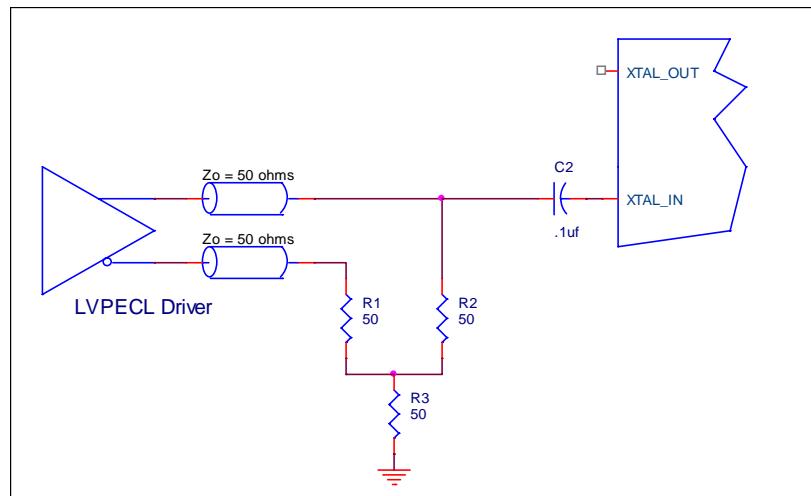
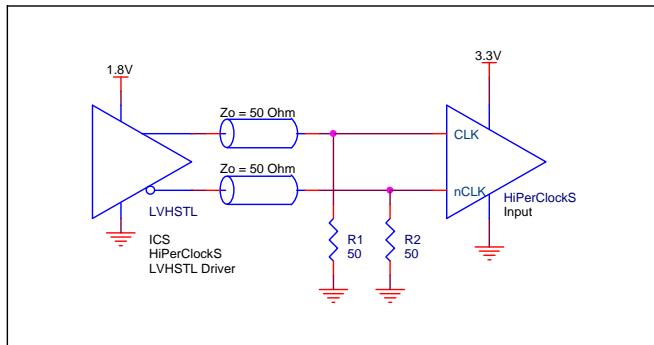


FIGURE 3B. GENERAL DIAGRAM FOR LVPECL DRIVER TO XTAL INPUT INTERFACE

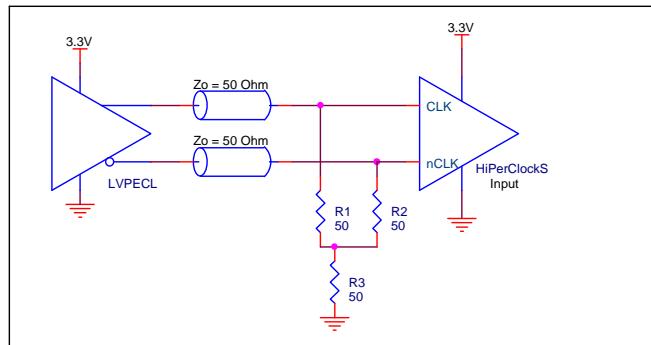
## DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK, nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{swing}$  and  $V_{oh}$  must meet the  $V_{pp}$  and  $V_{cmr}$  input requirements. Figures 4A to 4F show interface examples for the CLK, nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the

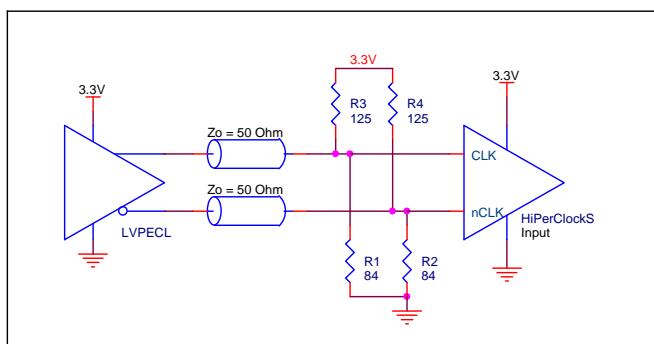
driver component to confirm the driver termination requirements. For example in Figure 4A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



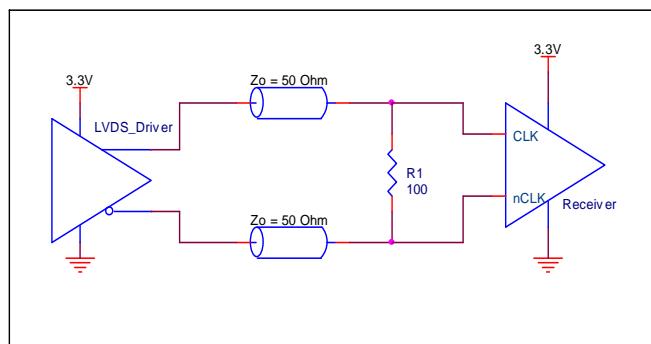
**FIGURE 4A. CLK, nCLK INPUT  
DRIVEN BY AN IDT OPEN Emitter  
LVHSTL DRIVER**



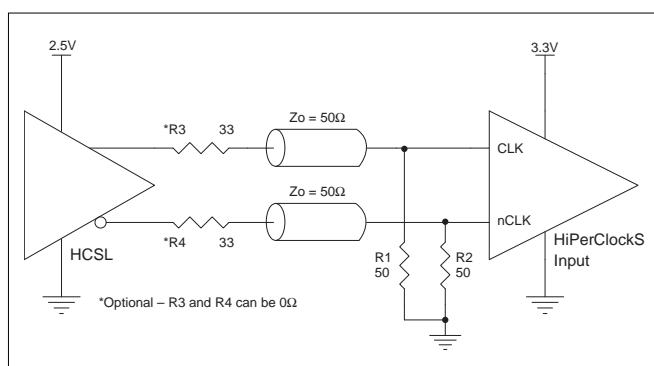
**FIGURE 4B. CLK, nCLK INPUT  
DRIVEN BY A 3.3V LVPECL DRIVER**



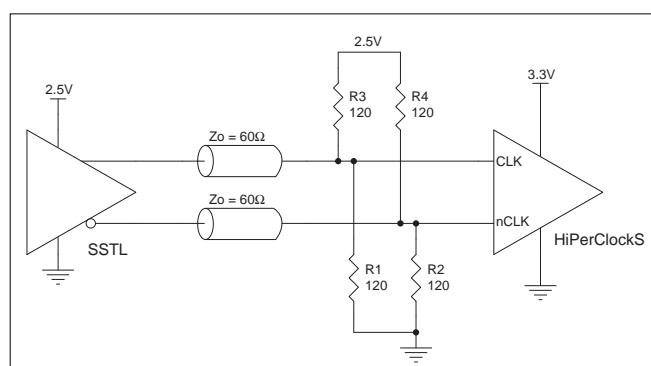
**FIGURE 4C. CLK, nCLK INPUT  
DRIVEN BY A 3.3V LVPECL DRIVER**



**FIGURE 4D. CLK, nCLK INPUT  
DRIVEN BY A 3.3V LVDS DRIVER**



**FIGURE 4E. CLK, nCLK INPUT  
DRIVEN BY A 3.3V HCSL DRIVER**



**FIGURE 4F. CLK, nCLK INPUT  
DRIVEN BY A 2.5V SSTL DRIVER**

## RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

### INPUTS:

#### CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from XTAL\_IN to ground.

#### CLK INPUT

For applications not requiring the use of the clock, it can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from the CLK input to ground.

#### CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a  $1\text{k}\Omega$  resistor can be tied from CLK to ground.

#### LVCMOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A  $1\text{k}\Omega$  resistor can be used.

### OUTPUTS:

#### LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to

drive  $50\Omega$  transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

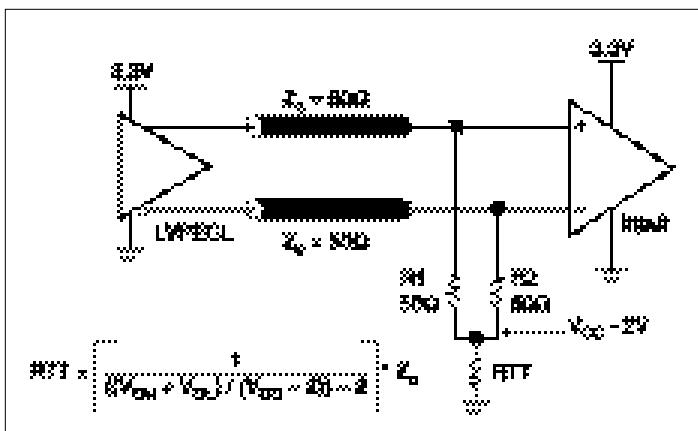


FIGURE 5A. LVPECL OUTPUT TERMINATION

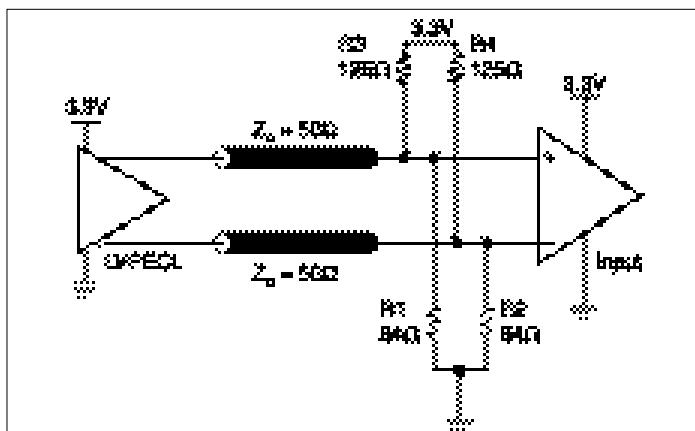


FIGURE 5B. LVPECL OUTPUT TERMINATION

## TERMINATION FOR 2.5V LVPECL OUTPUTS

Figure 6A and Figure 6B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating  $50\Omega$  to  $V_{cc} - 2V$ . For  $V_{cc} = 2.5V$ , the  $V_{cc} - 2V$  is very close to ground

level. The  $R3$  in Figure 6B can be eliminated and the termination is shown in Figure 6C.

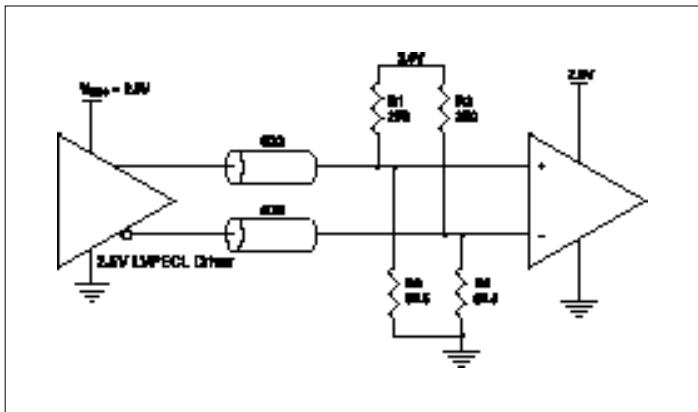


FIGURE 6A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

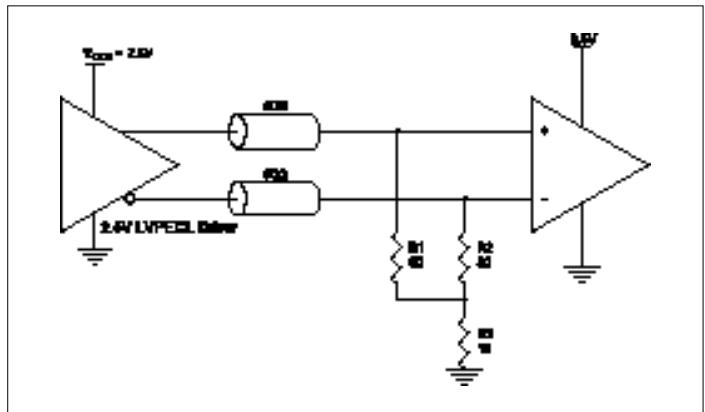


FIGURE 6B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

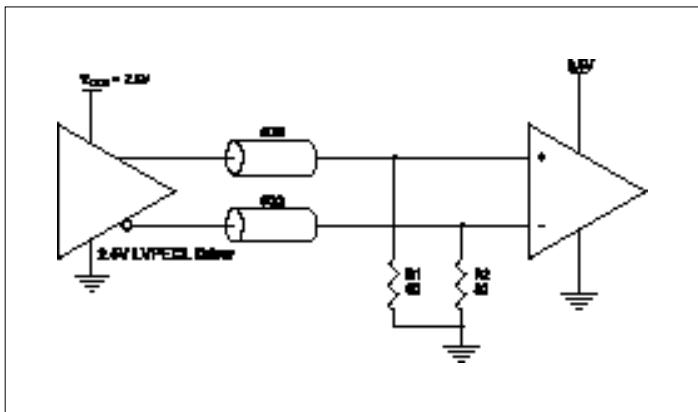


FIGURE 6C. 2.5V LVPECL TERMINATION EXAMPLE

## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8536-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8536-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{cc} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{cc,MAX} * I_{EE,MAX} = 3.465V * 85mA = 294.525\text{mW}$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
If all outputs are loaded, the total power is  $6 * 30\text{mW} = 180\text{mW}$

**Total Power<sub>MAX</sub>** (3.465V, with all outputs switching) =  $294.525\text{mW} + 180\text{mW} = 474.525\text{mW}$

### 2. Junction Temperature.

Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature,  $T_j$ , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is 84.6°C/W per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of 70°C with all outputs switching is:

$70^\circ\text{C} + 0.475\text{W} * 84.6^\circ\text{C/W} = 110.2^\circ\text{C}$ . This is below the limit of 125°C.

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 24-PIN TSSOP, FORCED CONVECTION**

<b><math>\theta_{JA}</math> by Velocity (Meters per Second)</b>			
Multi-Layer PCB, JEDEC Standard Test Boards	<b>0</b> 84.6°C/W	<b>1</b> 80.3°C/W	<b>2.5</b> 78.1°C/W

### 3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 7*.

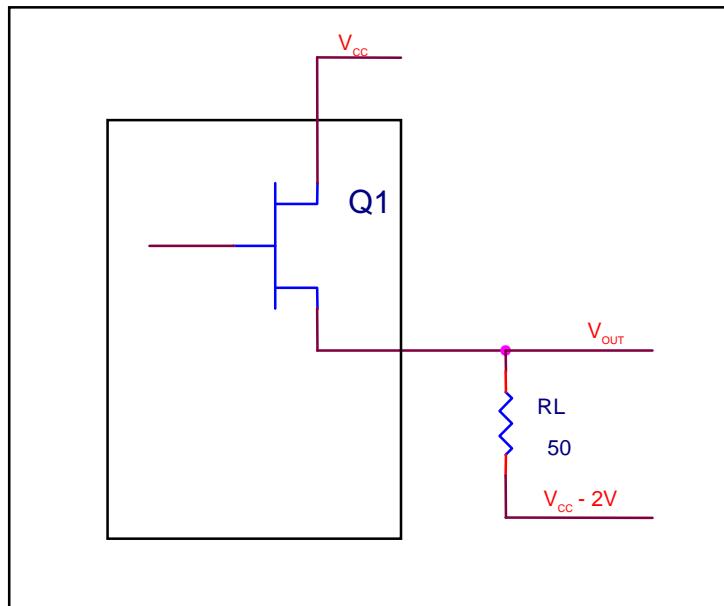


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate power dissipation due to the load, use the following equations which assume a  $50\Omega$  load, and a termination voltage of  $V_{cc} - 2V$ .

- For logic high,  $V_{out} = V_{oh_{max}} = V_{cc_{max}} - 0.9V$   
 $(V_{cc_{max}} - V_{oh_{max}}) = 0.9V$
- For logic low,  $V_{out} = V_{ol_{max}} = V_{cc_{max}} - 1.7V$   
 $(V_{cc_{max}} - V_{ol_{max}}) = 1.7V$

$Pd_H$  is power dissipation when the output drives high.

$Pd_L$  is the power dissipation when the output drives low.

$$Pd_H = [(V_{oh_{max}} - (V_{cc_{max}} - 2V))/R_L] * (V_{cc_{max}} - V_{oh_{max}}) = [(2V - (V_{cc_{max}} - V_{oh_{max}}))/R_L] * (V_{cc_{max}} - V_{oh_{max}}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{ol_{max}} - (V_{cc_{max}} - 2V))/R_L] * (V_{cc_{max}} - V_{ol_{max}}) = [(2V - (V_{cc_{max}} - V_{ol_{max}}))/R_L] * (V_{cc_{max}} - V_{ol_{max}}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

## RELIABILITY INFORMATION

TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 24 LEAD TSSOP

Multi-Layer PCB, JEDEC Standard Test Boards	$\theta_{JA}$ by Velocity (Meters per Second)		
	0	1	2.5
	84.6°C/W	80.3°C/W	78.1°C/W

### TRANSISTOR COUNT

The transistor count for ICS8536-01 is: 513

## PACKAGE OUTLINE - G SUFFIX FOR 24 LEAD TSSOP

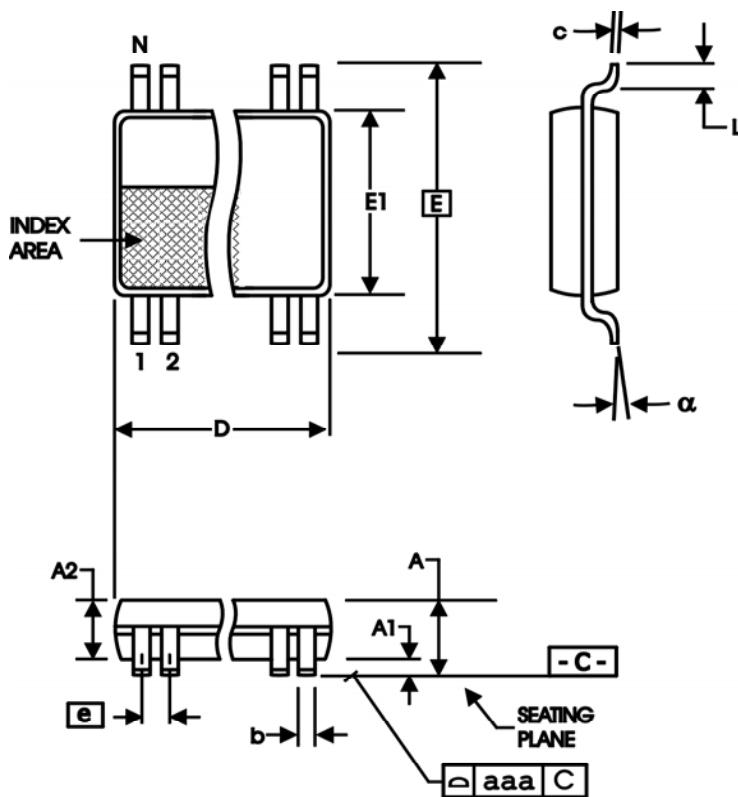


TABLE 9. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	24	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	7.70	7.90
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
alpha	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

**TABLE 10. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS8536AG-01LF	ICS8536AG-01L	24 Lead "Lead-Free" TSSOP	tube	0°C to 70°C
ICS8536AG-01LFT	ICS8536AG-01L	24 Lead "Lead-Free" TSSOP	tape & reel	0°C to 70°C

## Revision History Sheet

Rev	Table	Page	Description of Changes	Date
B	4A, 4B	1	Removed HiPerClock references throughout.	
		4	Updated diagrams to current standard throughout.	
	6A	6	Features List: Removed non lead-free package.	
	6B	6	Vcc: changed Core Supply Voltage to Power Supply Voltage.	
		15, 16	Per PCN #Table Note: changed $f_{MAX}$ to $f_{OUT} \leq 300MHz$ .	
		10	$t_{PD}$ : 2.0ns (Max) to 2.6ns (Max).	8/17/12
		19	Updated text in Power Considerations section.	
		20	Removed non lead-free ordering options and note. Removed quantity from T&R.	
			Deleted disclaimer at bottom of page 19.	
			Updated disclaimer on last page.	



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).