## General Description

The ICS8523I is a low skew, high performance 1-to-4 Differential-to-HSTL Fanout Buffer. The ICS8523I has two selectable clock inputs. The CLK, nCLK pair can accept most standard differential input levels. The PCLK, nPCLK pair can accept LVPECL, CML, or SSTL input levels. The clock enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8523I ideal for those applications demanding well defined performance and repeatability.

Features

- Four differential HSTL compatible outputs
- Selectable differential CLK, nCLK or LVPECL clock inputs
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, HSTL, HCSL, SSTL
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, CML, SSTL
- Maximum output frequency: 650MHz
- Translates any single-ended input signal to HSTL levels with resistor bias on nCLK input
- Additive phase jitter, RMS: 0.082ps (typical), 100MHz f_{OUT}
- Additive phase jitter, RMS: 0.190ps (typical), 120MHz f_{OUT}
- Output skew: 50ps (maximum)
- Part-to-part skew: 250ps (maximum)
- Propagation delay: 1.6ns (maximum)
- 3.3V core, 1.8V output operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free packages

Block Diagram
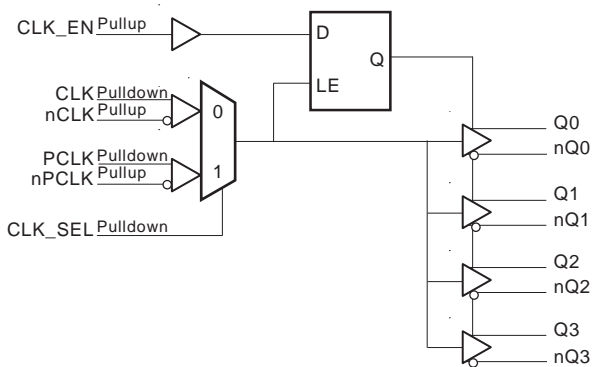
Pin Assignment

ICS8523I
20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1	GND	Power		Power supply ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follow clock input. When LOW, Qx outputs are forced low, nQx outputs are forced high. LVCMOS / LVTTL interface levels.
3	CLK_SEL	Input	Pulldown	Clock select input. When HIGH, selects differential PCLK, nPCLK inputs. When LOW, selects CLK, nCLK inputs. LVCMOS / LVTTL interface levels.
4	CLK	Input	Pulldown	Non-inverting differential clock input.
5	nCLK	Input	Pullup	Inverting differential clock input.
6	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
7	nPCLK	Input	Pullup	Inverting differential LVPECL clock input.
8, 9	nc	Unused		No connect.
10	V_{DD}	Power		Positive supply pin.
11, 12	nQ3, Q3	Output		Differential output pair. HSTL interface levels.
13, 18	V_{DDO}	Power		Output supply pins.
14, 15	nQ2, Q2	Output		Differential output pair. HSTL interface levels.
16, 17	nQ1, Q1	Output		Differential output pair. HSTL interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. HSTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Control Input Function Table

Inputs			Outputs	
CLK_EN	**CLK_SEL**	**Selected Source**	**Q[0:3]**	**nQ[0:3]**
0	0	CLK, nCLK	Disabled; LOW	Disabled; HIGH
0	1	PCLK, nPCLK	Disabled; LOW	Disabled; HIGH
1	0	CLK, nCLK	Enabled	Enabled
1	1	PCLK, nPCLK	Enabled	Enabled

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock edge as shown in Figure 1. In the active mode, the state of the outputs are a function of the CLK, nCLK and PCLK, nPCLK inputs as described in Table 3B.
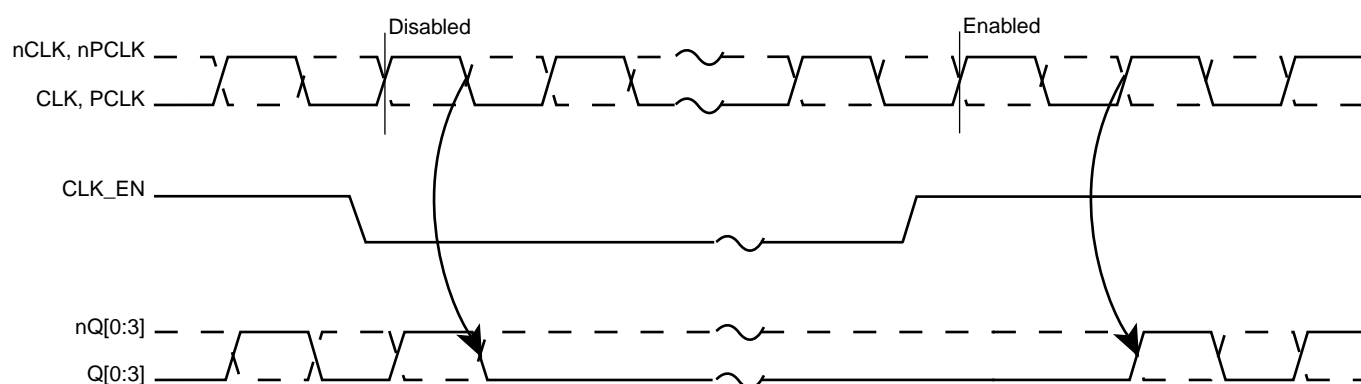

Figure 1. CLK_EN Timing Diagram

Table 3B. Clock Input Function Table

Inputs		Outputs			
CLK or PCLK	**nCLK or nPCLK**	**Q[0:3]**	**nQ[0:3]**	**Input to Output Mode**	**Polarity**
0	0	LOW	HIGH	Differential to Differential	Non-Inverting
1	1	HIGH	LOW	Differential to Differential	Non-Inverting
0	Biased; NOTE 1	LOW	HIGH	Single-Ended to Differential	Non-Inverting
1	Biased; NOTE 1	HIGH	LOW	Single-Ended to Differential	Non-Inverting
Biased; NOTE 1	0	HIGH	LOW	Single-Ended to Differential	Inverting
Biased; NOTE 1	1	LOW	HIGH	Single-Ended to Differential	Inverting

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO} + 0.5V
Package Thermal Impedance, θ_{JA}	73.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
V_{DDO}	Output Supply Voltage		1.6	1.8	2.0	V
I_{DD}	Power Supply Current				55	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK_EN	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK_SEL	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK_EN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK_SEL	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA

Table 4C. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nCLK	V_{DD} = V_{IN} = 3.465V			5	µA
		CLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} − 0.85	V

NOTE 1: V_{IL} should not be less than -0.3V.
NOTE 2: Common mode input voltage is defined as V_{IH}.

Table 4D. LVPECL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	nPCLK	V_{DD} = V_{IN} = 3.465V			5	µA
		PCLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	nPCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
		PCLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
V_{PP}	Peak-to-Peak Voltage			0.3		1.0	V
V_{CMR}	Common Mode Input Voltage; NOTE 1			1.5		V_{DD}	V

NOTE 1: Common mode input voltage is defined as V_{IH}.

Table 4E. HSTL DC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Current; NOTE 1		0.9		1.4	V
V_{OL}	Output Low Current; NOTE 1		0		0.4	V
V_{OX}	Output Crossover Voltage		40% x (V_{OH} − V_{OL}) + V_{OL}		60% x (V_{OH} − V_{OL}) + V_{OL}	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.3	V

NOTE 1: Outputs termination with 50Ω to ground.

AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, V_{DDO} = 1.8V ±0.2V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency				650	MHz
t_{PD}	Propagation Delay; NOTE 1	f ≤ 650MHz	1.0		1.6	ns
f_{jit}	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	f_{OUT} = 100MHz, Integration Range: 12kHz - 20MHz		0.082		ps
		f_{OUT} = 120MHz, Integration Range: 12kHz - 20MHz		0.190		ps
$t_{sk(o)}$	Output Skew; NOTE 2, 3				50	ps
$t_{sk(pp)}$	Part-to-Part Skew; NOTE 3, 4				250	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	250		700	ps
odc	Output Duty Cycle		45		55	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at 500MHz unless noted otherwise.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage, same frequency, same temperature and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise.** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

Additive Phase Jitter @ 100MHz
12kHz to 20MHz = 0.082ps (typical)
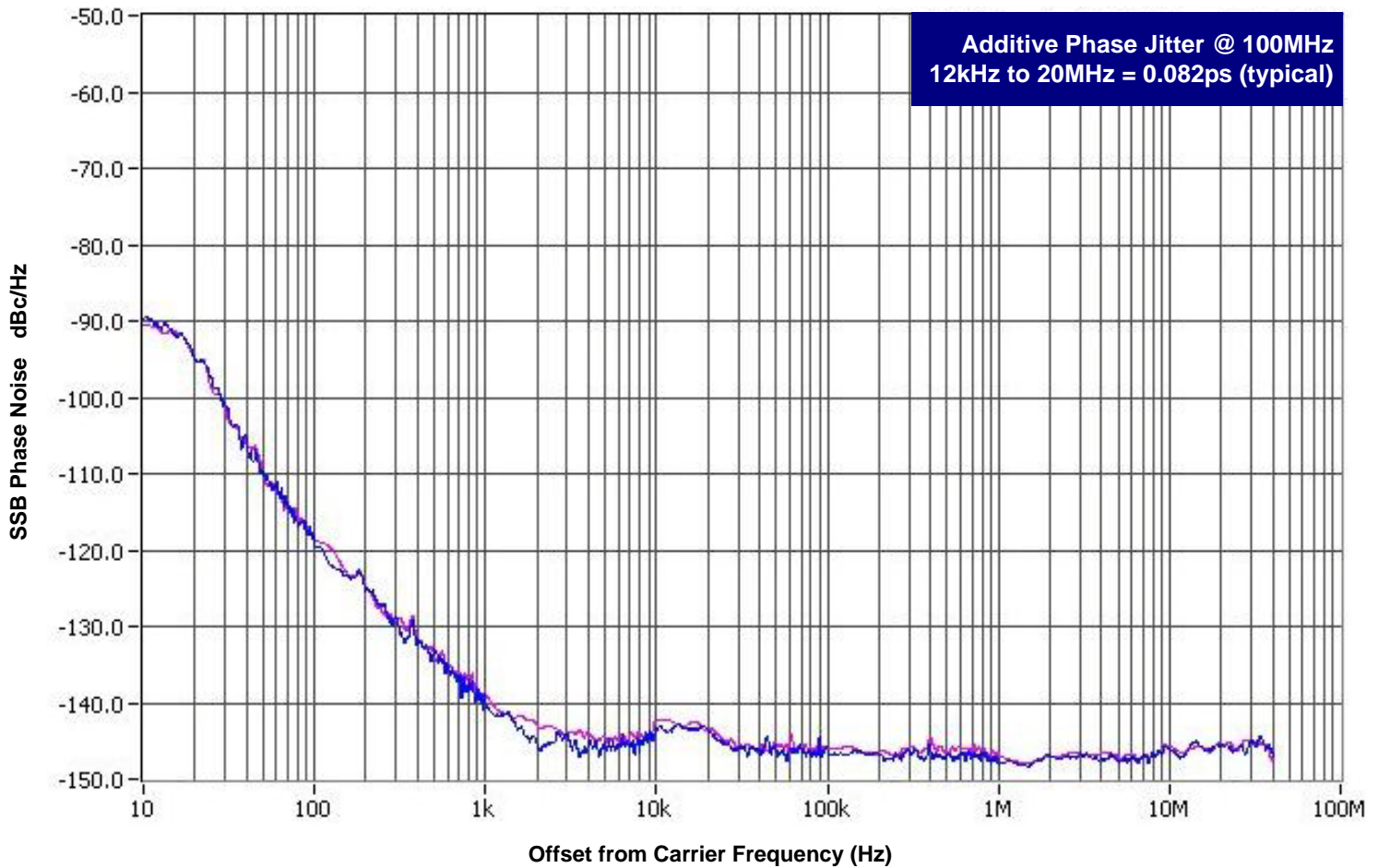
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

The source generator used is, "IFR2042 into a Hewlett Packard 8133A 3GHz Pulse Generator".
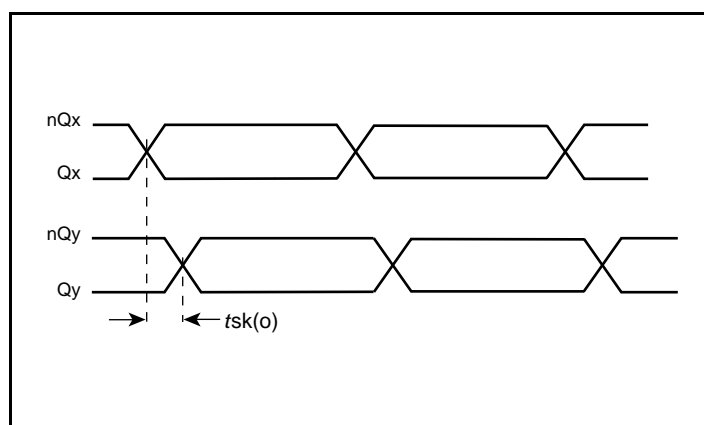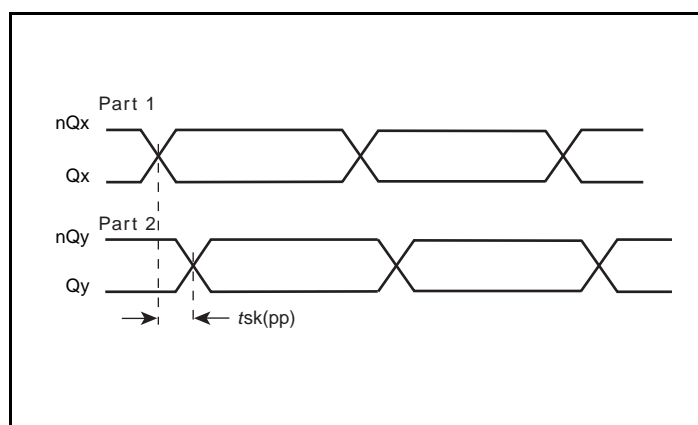
Parameter Measurement Information
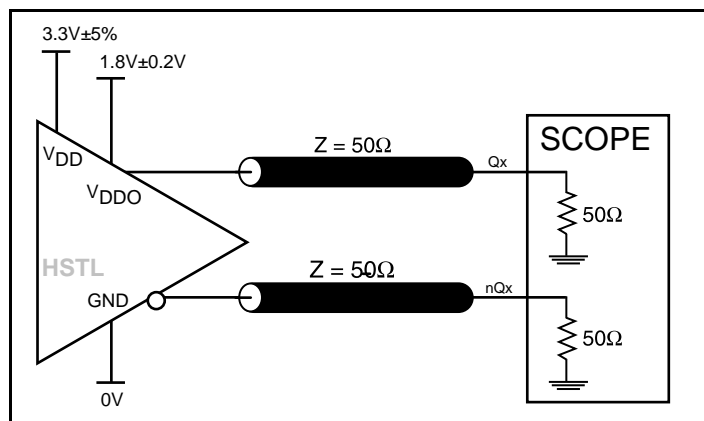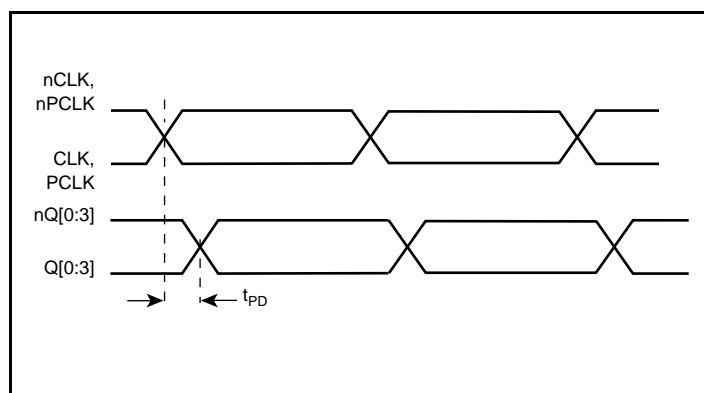

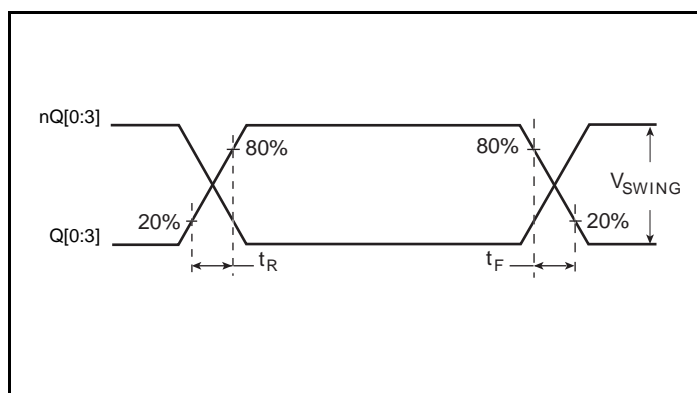**3.3V/1.8V Output Load AC Test Circuit**
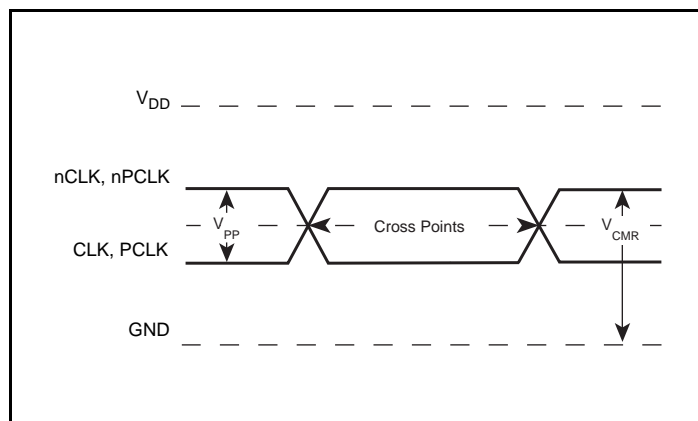
Differential Input Level
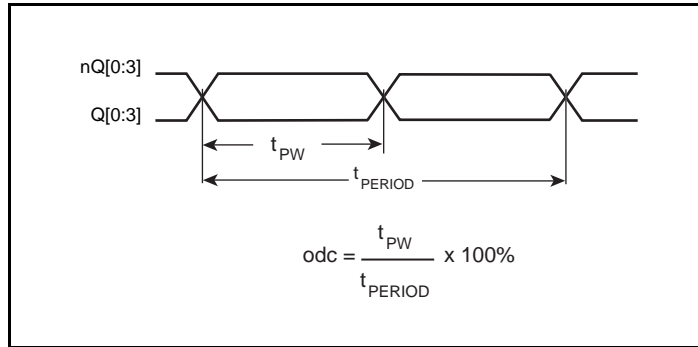

Output Skew

Part-to-Part Skew

Propagation Delay

Output Rise/Fall Time

Parameter Measurement Information, continued

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period

Applications Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and V_{CC} = 3.3V, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single ended swing and V_{CC} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{CC} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.
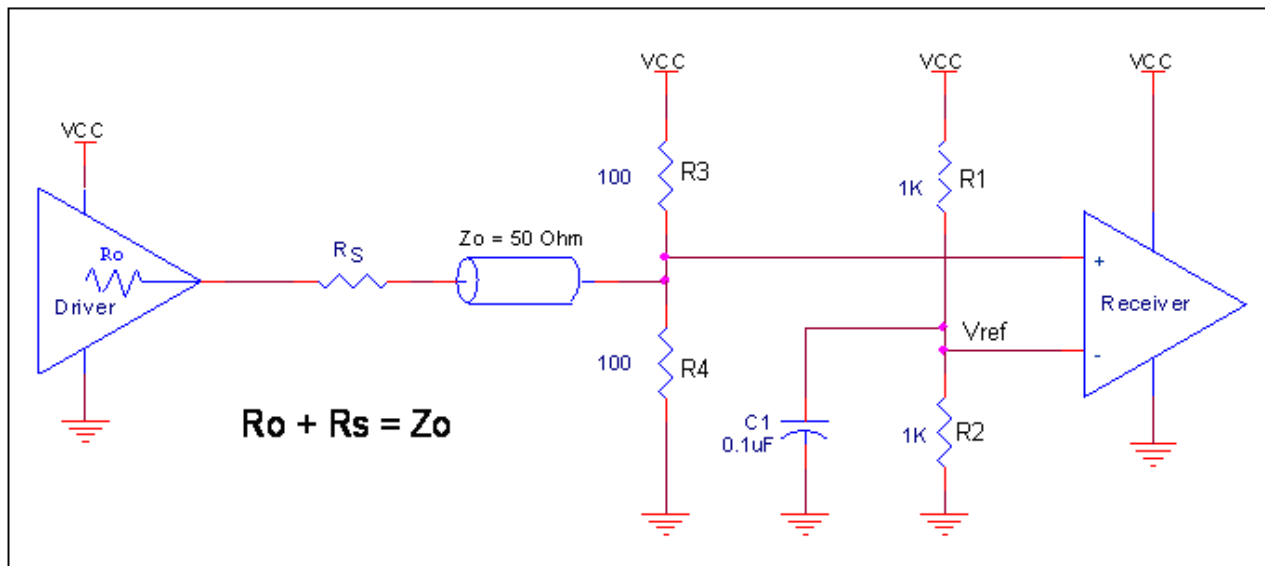

Figure 2. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels

3.3V Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both differential signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 3A to 3F* show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.
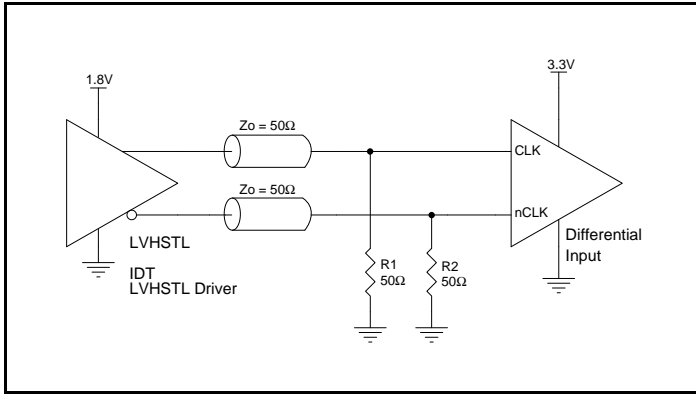
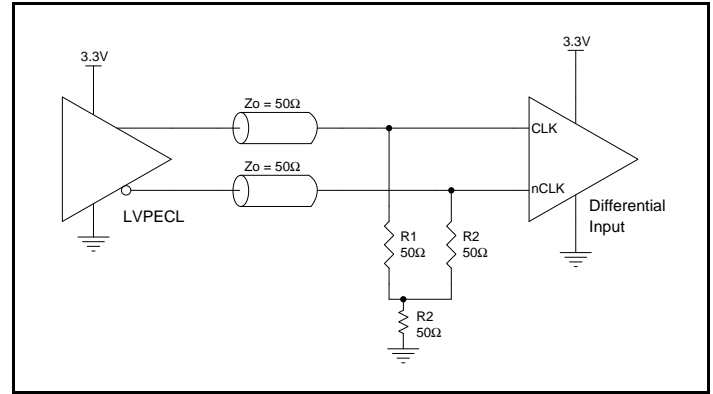**Figure 3A. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver**

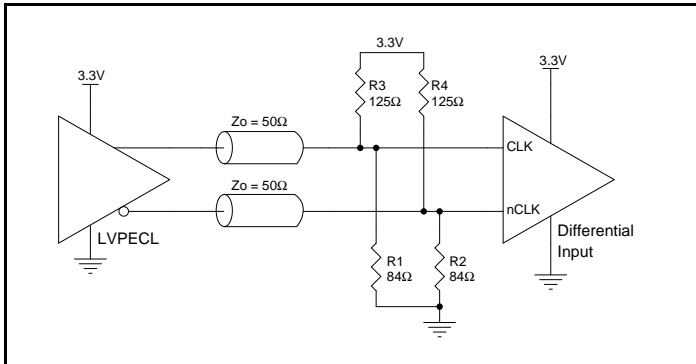**Figure 3B. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

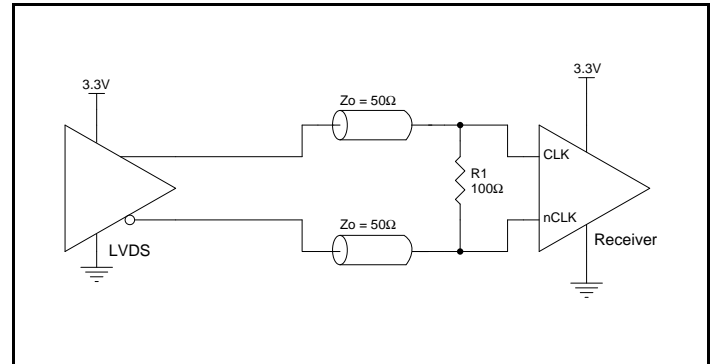**Figure 3C. CLK/nCLK Input Driven by a 3.3V LVPECL Driver**

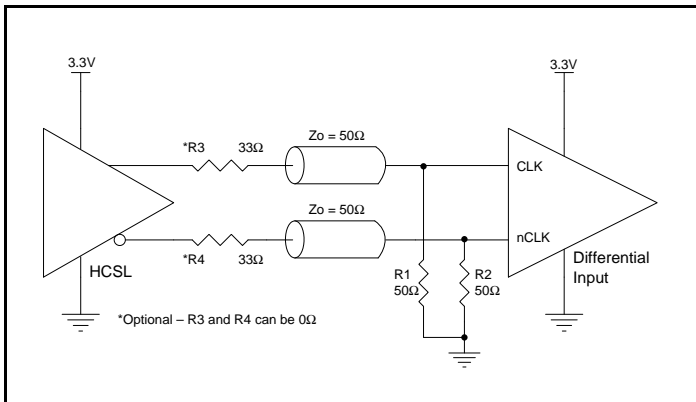**Figure 3D. CLK/nCLK Input Driven by a 3.3V LVDS Driver**

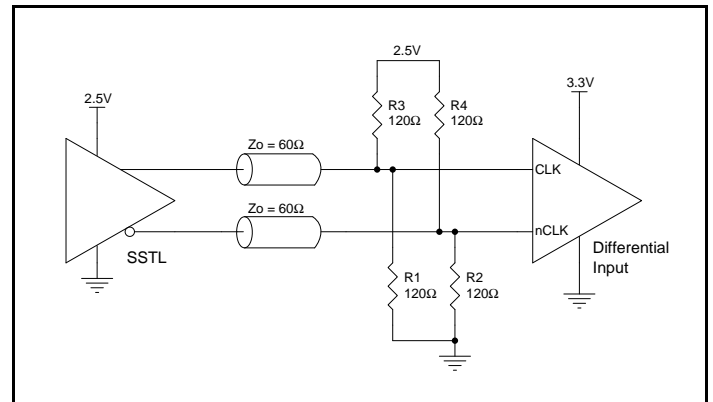**Figure 3E. CLK/nCLK Input Driven by a 3.3V HCSL Driver**

Figure 3F. CLK/nCLK Input Driven by a 2.5V SSTL Driver

3.3V LVPECL Clock Input Interface

The PCLK /nPCLK accepts LVPECL, CML, SSTL and other differential signals. Both signals must meet the V_{PP} and V_{CMR} input requirements. *Figures 4A to 4E* show interface examples for the PCLK/ nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.
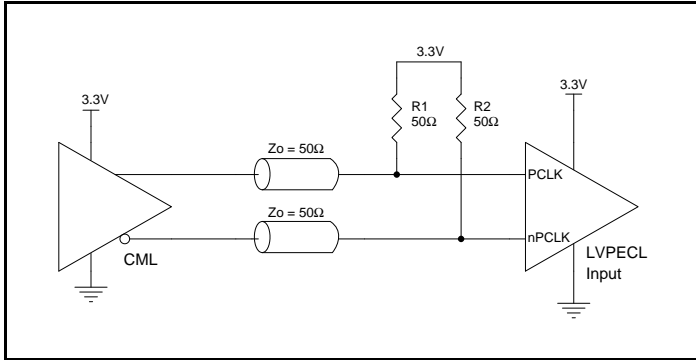

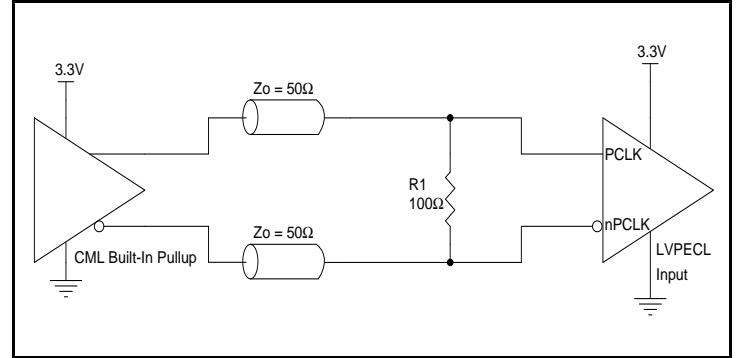**Figure 4A. PCLK/nPCLK Input Driven by a CML Driver**

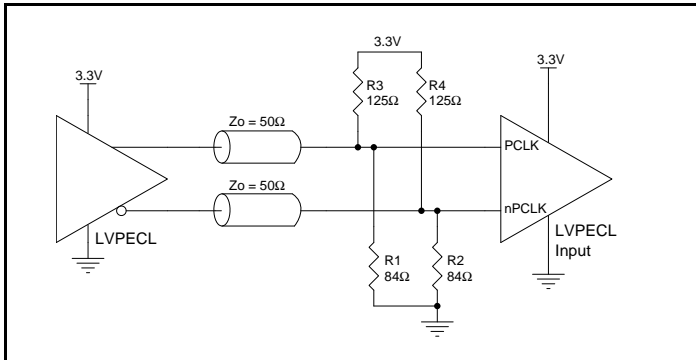**Figure 4B. PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver**

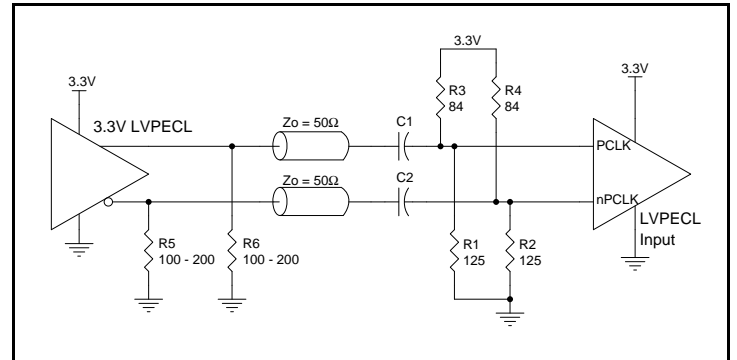**Figure 4C. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver**

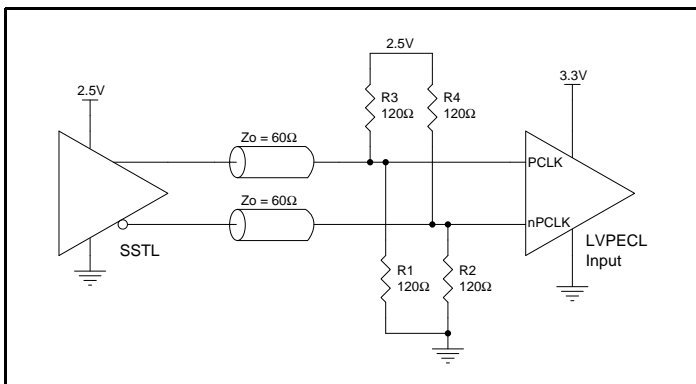**Figure 4D. PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple**

Figure 4E. PCLK/nPCLK Input Driven by an SSTL Driver

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

PCLK/nPCLK Inputs

For applications not requiring the use of a differential input, both the PCLK and nPCLK pins can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from PCLK to ground.

Outputs:
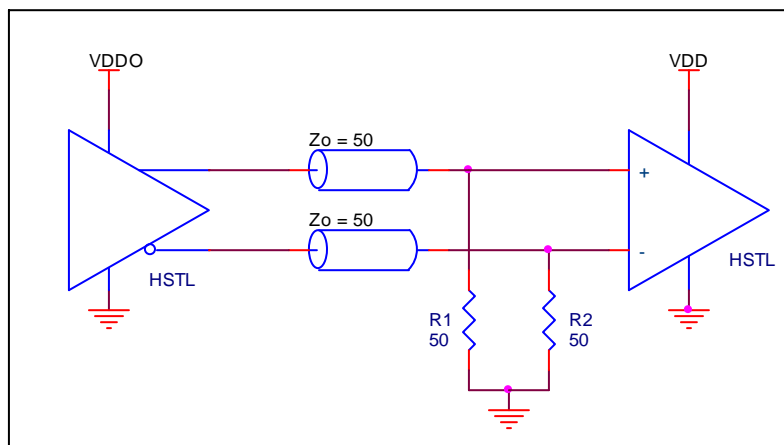
HSTL Outputs

All unused LVHSTL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

HSTL Output Termination

Schematic Example

Figure 5 shows a schematic example of the ICS8523I. In this example, the input is driven by an IDT HSTL driver. The decoupling capacitors should be physically located near the power pin. For ICS8523I, the unused clock outputs can be left floating.
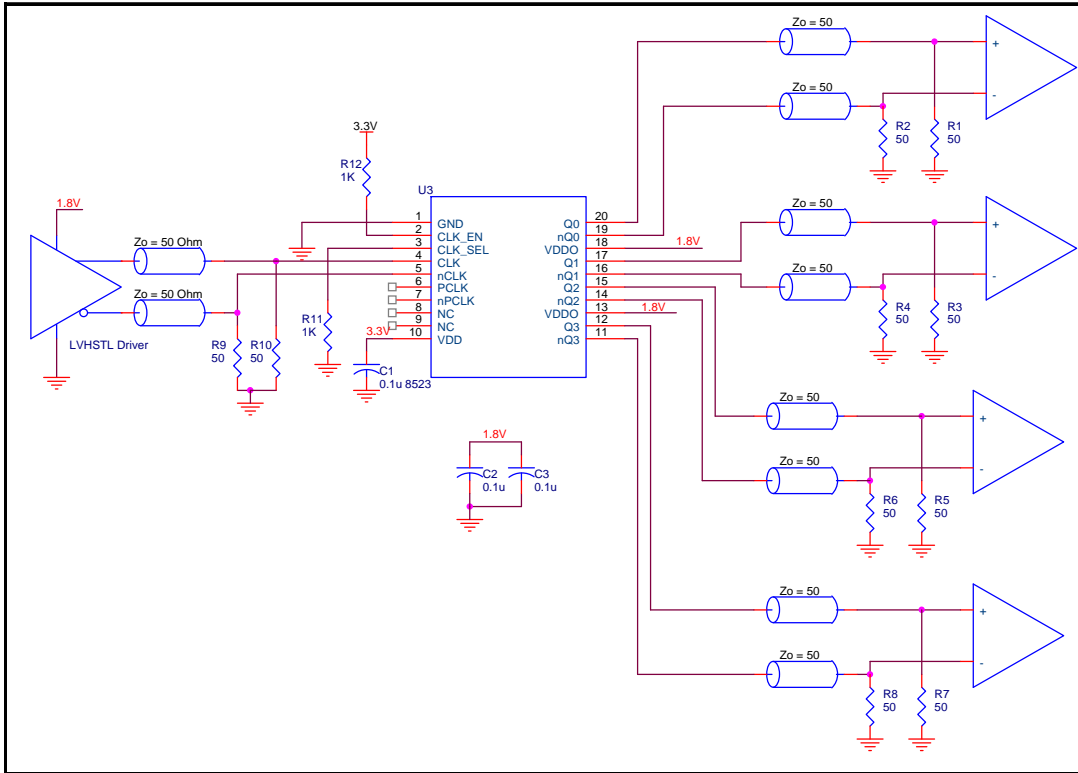

Figure 5. ICS8523I HSTL Buffer Schematic Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8523I.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8523I is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 55mA = **190.6mW**

- Power (outputs)$_{MAX}$ = **32.6mW/Loaded Output pair**
  If all outputs are loaded, the total power is 4 x 32.6mW = **130.4mW**

Total Power$_{\_MAX}$ (3.465V, with all outputs switching) = 190.6mW + 130.4mW = **321mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad, and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 66.6°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.321W * 66.6°C/W = 106.4°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 6. Thermal Resitance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

3. Calculations and Equations.

The purpose of this section is to calculate the power dissipation for the HSTL output pair.

HSTL output driver circuit and termination are shown in *Figure 6.*
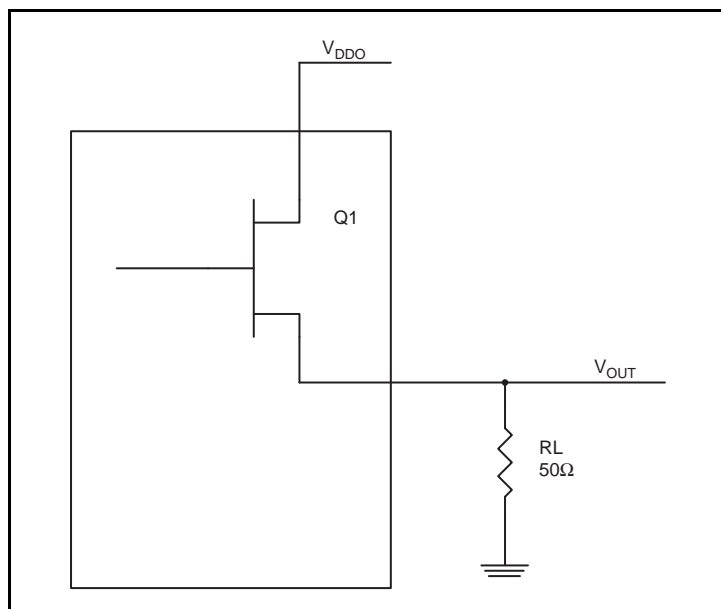
Figure 6. HSTL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load.

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd\_H = (V_{OH\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OH\_MAX})$$
$$Pd\_L = (V_{OL\_MAX}/R_L) * (V_{DDO\_MAX} - V_{OL\_MAX})$$

$$Pd\_H = (0.9V/50\Omega) * (2V - 0.9V) = \textbf{19.8mW}$$
$$Pd\_L = (0.4V/50\Omega) * (2V - 0.4V) = \textbf{12.8mW}$$

Total Power Dissipation per output pair = Pd_H + Pd_L = **32.6mW**

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ$_{JA}$ by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	114.5°C/W	98.0°C/W	88.0°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	73.2°C/W	66.6°C/W	63.5°C/W

Transistor Count

The transistor count for ICS8523I is: 472

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP
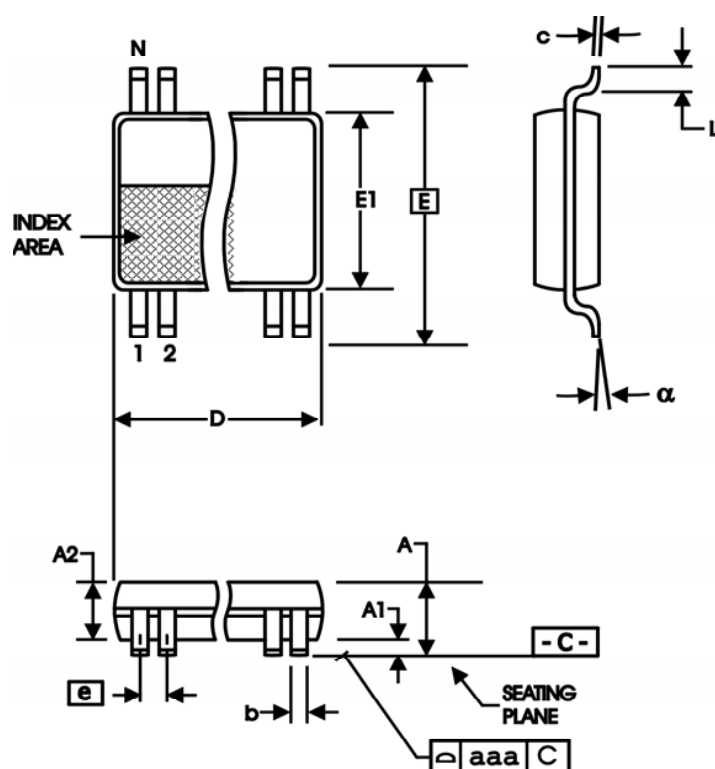
Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8523CGILF	ICS8523CGILF	"Lead-Free" 20 Lead TSSOP	Tube	-40°C to 85°C
8523CGILFT	ICS8523CGILF	"Lead-Free" 20 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
B	T5	5	AC Characteristics table - t_{PD} row, changed Min. from 1.2ns to 1.0ns.	1/11/02
B		1	Revised Features section, Bullet 1,6 - took out 1.8V	5/6/02
B		8 - 10	In the Application Information section, added Schematic Examples.	10/28/02
C	T2 T4D	2 4 5 11 - 12	Pin Characteristics Table - changed C_{IN} 4pF max. to 4pF typical. Absolute Maximum Ratings - changed Output rating. HSTL DC Characteristics Table - changed V_{OH} 1V min. to 0.9V min. Power Considerations - changed Total Power Dissipation to reflect V_{OH} change. Calculations changed due to new Total Power Dissipation. Changed LVHSTL to HSTL throughout data sheet.	6/23/03
C	 T9	1 9 15	Features section - added Lead-Free bullet. Updated LVPECL Clock Input Interface section. Added Lead-Free marking to Ordering Information table.	9/13/04
C	T8	15	Ordering Information Table - in the *Part/Order Number* and *Marking* columns, changed die revision from "B" to "C".	3/2/07
D	T5	6	AC Characteristics Table - changed t_R/t_F minimum from 300ps to 250ps.	3/13/07
E	 T4C T4D T5 T9	1 4 4 5 5 6 8 8 9 10 11 16	Features Section - added Additive Phase Jitter bullets. Pin Assignment has nCLK, nPCLK. Changed $\overline{CLK}$, $\overline{PCLK}$ to nCLK, nPCLK throughout the datasheet. Absolute Maximum Ratings - corrected Outputs Rating. Differential DC Characteristics Table - updated notes. LVPECL DC Characteristics Table - updated notes. AC Characteristics Table - added Buffer Additive Phase Jitter specs. Add thermal note and updated NOTE 4. Added Additive Phase Jitter plot. Corrected Output Duty Cycle/Pulse Width/Period diagram. Updated *Wiring the Differential Input to Accept Single-ended Levels* application note. Updated *3.3V Differential Clock Input Interface* application note. Updated *3.3V LVPECL Clock Input Interface* application note. Added *HSTL Output Termination* diagram. Ordering Information Table - corrected marking.	1/21/11
E	T9	16	Removed leaded orderable parts from Ordering Information table	11/15/12

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