

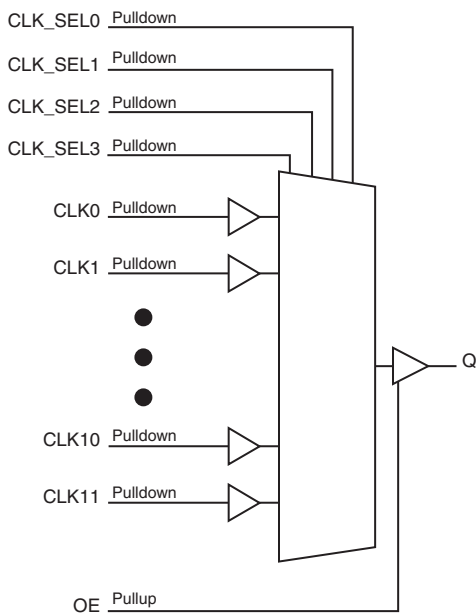
General Description

The 850S1201 is a low skew 12:1 Single-ended Clock Multiplexer. The 850S1201 has 12 selectable single-ended clock inputs and 1 single-ended clock output. The device operates up to 250MHz and is packaged in a 20 TSSOP package.

Features

- 12:1 single-ended multiplexer
- Nominal output impedance: 20Ω (V_{DD} = 3.3V)
- Maximum output frequency: 250MHz
- Propagation delay: 2.7ns (maximum)
- Full 3.3V or 2.5V supply modes
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package

Block Diagram



Pin Assignment

| | | | |
|-----------------|----|----|------|
| CLK8 | 1 | 20 | CLK7 |
| CLK9 | 2 | 19 | CLK6 |
| CLK10 | 3 | 18 | CLK5 |
| CLK11 | 4 | 17 | CLK4 |
| V _{DD} | 5 | 16 | CLK3 |
| CLK_SEL0 | 6 | 15 | CLK2 |
| CLK_SEL1 | 7 | 14 | CLK1 |
| CLK_SEL2 | 8 | 13 | CLK0 |
| CLK_SEL3 | 9 | 12 | GND |
| OE | 10 | 11 | Q |

850S1201
20-Lead TSSOP
6.50mm x 4.40mm x 0.925mm
package body
G Package
Top View

Pin Description and Pin Characteristics

Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---------------------|---|--------|----------|--|
| 1 | CLK8 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 2 | CLK9 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 3 | CLK10 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 4 | CLK11 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 5 | V _{DD} | Power | | Power supply pin. |
| 6, 7, 8, 9 | CLK_SEL0, CLK_SEL1, CLK_SEL2, CLK_SEL3 | Input | Pulldown | Clock select inputs. See Table 3. LVCMOS / LVTTL interface levels. |
| 10 | OE | Input | Pullup | Output enable pin for Q output. LVCMOS/LVTTL interface levels. |
| 11 | Q | Output | | Single-ended clock output. LVCMOS/LVTTL interface levels. |
| 12 | GND | Power | | Power supply ground. |
| 13 | CLK0 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 14 | CLK1 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 15 | CLK2 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 16 | CLK3 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 17 | CLK4 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 18 | CLK5 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 19 | CLK6 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 20 | CLK7 | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------------|-------------------------------|---------------------------|---------|---------|---------|-------|
| C _{IN} | Input Capacitance | | | 2 | | pF |
| C _{PD} | Power Dissipation Capacitance | V _{DD} = 3.465V | | 10 | | pF |
| | | V _{DD} = 2.625V | | 8 | | pF |
| R _{PULLUP} | Input Pullup Resistor | | | 51 | | kΩ |
| R _{PULLDOWN} | Input Pulldown Resistor | | | 51 | | kΩ |
| R _{OUT} | Output Impedance | V _{DD} = 3.3V±5% | | 20 | | Ω |
| | | V _{DD} = 2.5V±5% | | 25 | | Ω |

Function Tables

Table 3. Clock Input Function Table

| Inputs | | | | Input Selected to Q |
|----------|----------|----------|----------|---------------------|
| CLK_SEL3 | CLK_SEL2 | CLK_SEL1 | CLK_SEL0 | |
| 0 | 0 | 0 | 0 | CLK0 |
| 0 | 0 | 0 | 1 | CLK1 |
| 0 | 0 | 1 | 0 | CLK2 |
| 0 | 0 | 1 | 1 | CLK3 |
| 0 | 1 | 0 | 0 | CLK4 |
| 0 | 1 | 0 | 1 | CLK5 |
| 0 | 1 | 1 | 0 | CLK6 |
| 0 | 1 | 1 | 1 | CLK7 |
| 1 | 0 | 0 | 0 | CLK8 |
| 1 | 0 | 0 | 1 | CLK9 |
| 1 | 0 | 1 | 0 | CLK10 |
| 1 | 0 | 1 | 1 | CLK11 |
| 1 | 1 | 0 | 0 | Output goes LOW |
| 1 | 1 | 0 | 1 | Output goes LOW |
| 1 | 1 | 1 | 0 | Output goes LOW |
| 1 | 1 | 1 | 1 | Output goes LOW |

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|--|--------------------------|
| Supply Voltage, V_{DD} | 4.6V |
| Inputs, V_I | -0.5V to $V_{DD} + 0.5V$ |
| Outputs, V_O | -0.5V to $V_{DD} + 0.5V$ |
| Package Thermal Impedance, θ_{JA} | 87.2°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|---------------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} | Power Supply Current | Output Unterminated | | | 49 | mA |

Table 4B. Power Supply DC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-------------------------|---------------------|---------|---------|---------|-------|
| V_{DD} | Positive Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{DD} | Power Supply Current | Output Unterminated | | | 41 | mA |

Table 4C. LVCMOS/LVTTL DC Characteristics, $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------------------|--|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | $V_{DD} = 3.465V$ | 2 | | $V_{DD} + 0.3$ | V |
| | | $V_{DD} = 2.625V$ | 1.7 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | $V_{DD} = 3.465V$ | -0.3 | | 0.8 | V |
| | | $V_{DD} = 2.625V$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | CLK[0:11], CLK_SEL[0:3] $V_{DD} = V_{IN} = 3.465V$ or $2.625V$ | | | 150 | μA |
| | | OE $V_{DD} = V_{IN} = 3.465V$ or $2.625V$ | | | 10 | μA |
| I_{IL} | Input Low Current | CLK[0:11], CLK_SEL[0:3] $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -10 | | | μA |
| | | OE $V_{DD} = 3.465V$ or $2.625V$, $V_{IN} = 0V$ | -150 | | | μA |
| V_{OH} | Output High Voltage; NOTE 1 | $V_{DD} = 3.3V \pm 5\%$, $I_{OH} = -12mA$ | 2.6 | | | V |
| | | $V_{DD} = 2.5V \pm 5\%$, $I_{OH} = -12mA$ | 1.8 | | | V |
| V_{OL} | Output Low Voltage; NOTE 1 | $V_{DD} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$, $I_{OL} = 12mA$ | | | 0.5 | V |

NOTE 1: Output terminated with 50Ω to $V_{DD}/2$. See Parameter Measurement Information section. *Load Test Circuit diagrams.*

AC Electrical Characteristics

Table 5A. AC Characteristics, $V_{DD} = 3.3V \pm 5\%$, $T_A = -40^\circ C$ to $85^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------------|---|---|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 250 | MHz |
| t_{PLH} | Propagation Delay, Low-to-High; NOTE 1 | | 1.4 | | 2.7 | ns |
| τ_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.35 | | ps |
| $t_{sk(i)}$ | Input Skew | | | | 175 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 2, 3 | | | | 600 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 100 | | 500 | ps |
| odc | Output Duty Cycle; NOTE 4 | $f \leq 200MHz$ | 46 | | 54 | % |
| | | $f = 250MHz$ | 40 | | 60 | % |
| $MUX_{ISOLATION}$ | MUX Isolation | 155.52MHz | | 43 | | dB |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

NOTE 3: This parameter is defined according with JEDEC Standard 65.

NOTE 4: Input duty cycle must be 50%.

Table 5B. AC Characteristics, $V_{DD} = 2.5V \pm 5\%$, $T_A = -40^{\circ}C$ to $85^{\circ}C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------------|--|--|---------|---------|---------|-------|
| f_{MAX} | Output Frequency | | | | 250 | MHz |
| t_{pLH} | Propagation Delay, Low-to-High; NOTE 1 | | 1.5 | | 2.7 | ns |
| f_{jit} | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.32 | | ps |
| $t_{sk(i)}$ | Input Skew | | | | 195 | ps |
| $t_{sk(pp)}$ | Part-to-Part Skew; NOTE 2, 3 | | | | 600 | ps |
| t_R / t_F | Output Rise/Fall Time | 20% to 80% | 80 | | 600 | ps |
| odc | Output Duty Cycle; NOTE 4 | $f \leq 200MHz$ | 46 | | 54 | % |
| | | $f = 250MHz$ | 40 | | 60 | % |
| $MUX_{ISOLATION}$ | MUX Isolation | 155.52MHz | | 43 | | dB |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE 1: Measured from $V_{DD}/2$ of the input to $V_{DD}/2$ of the output.

NOTE 2: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

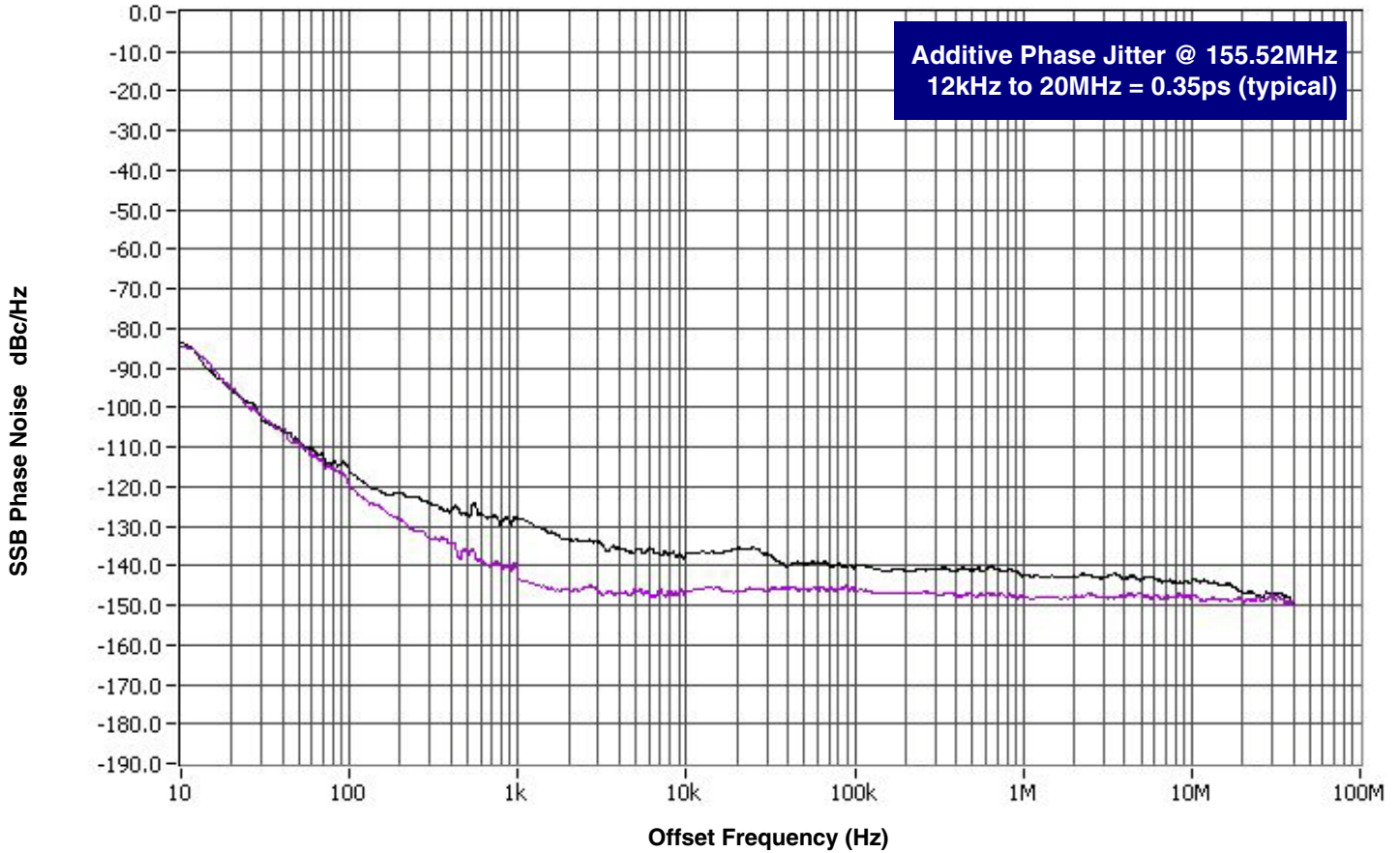
NOTE 3: This parameter is defined according with JEDEC Standard 65.

NOTE 4: Input duty cycle must be 50%.

Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the **dBc Phase Noise**. This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio

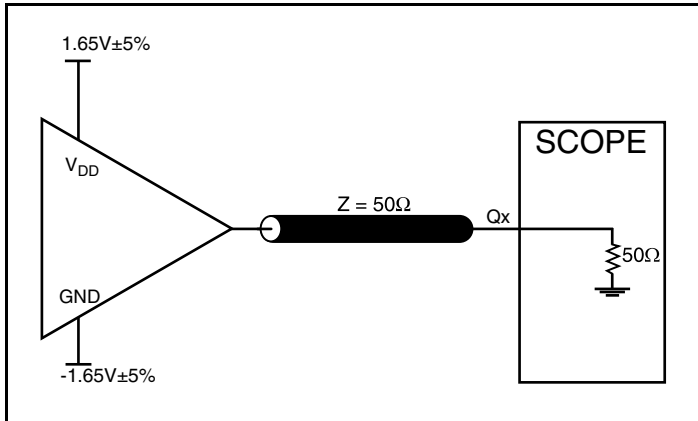
of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a **dBc** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



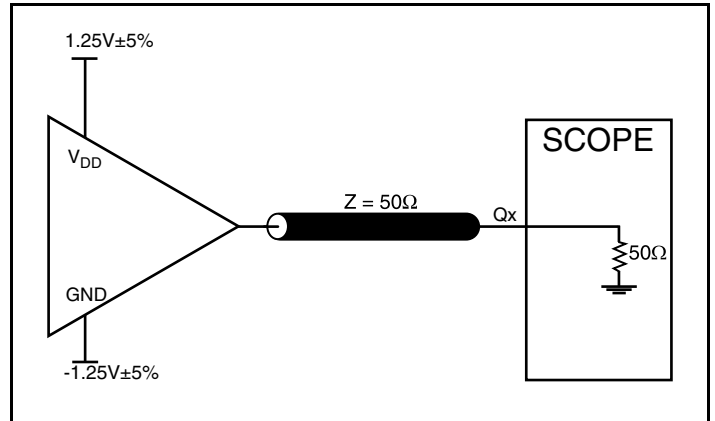
As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This

is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

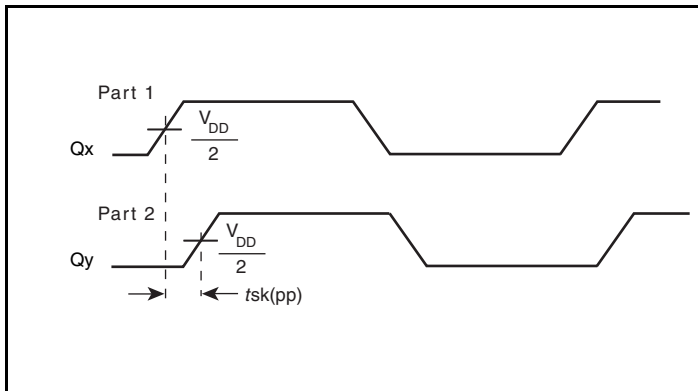
Parameter Measurement Information



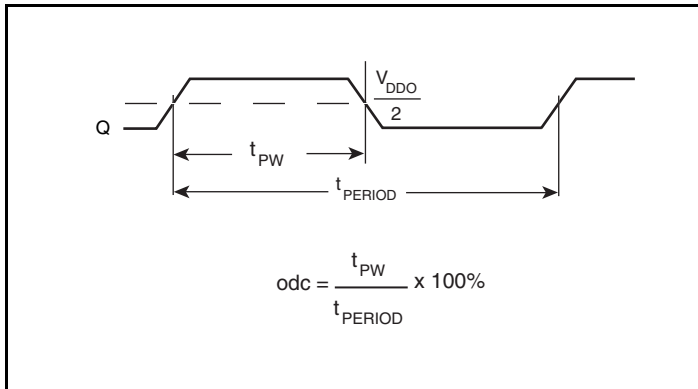
3.3V Output Load AC Test Circuit



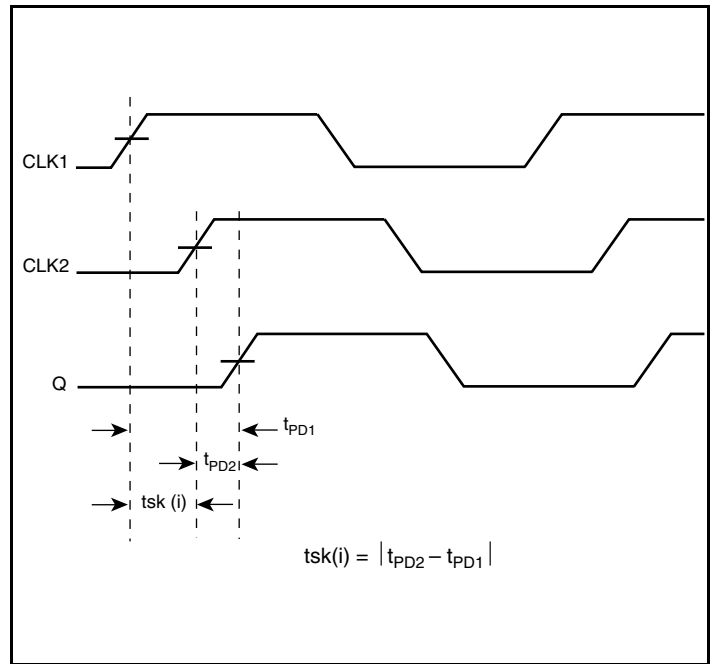
2.5V Output Load AC Test Circuit



Part-to-Part Skew

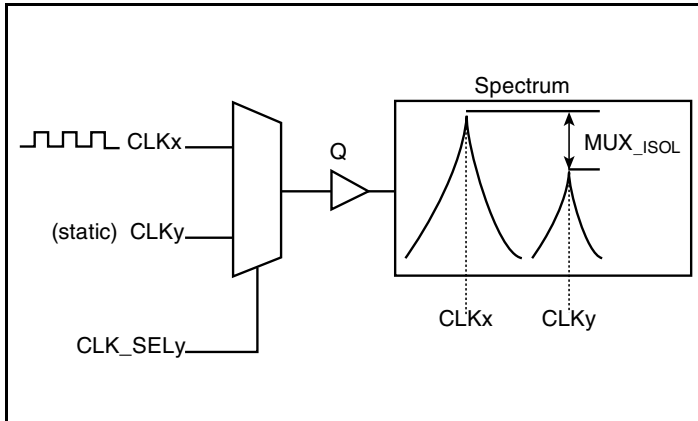


Output Duty Cycle/Pulse Width/Period

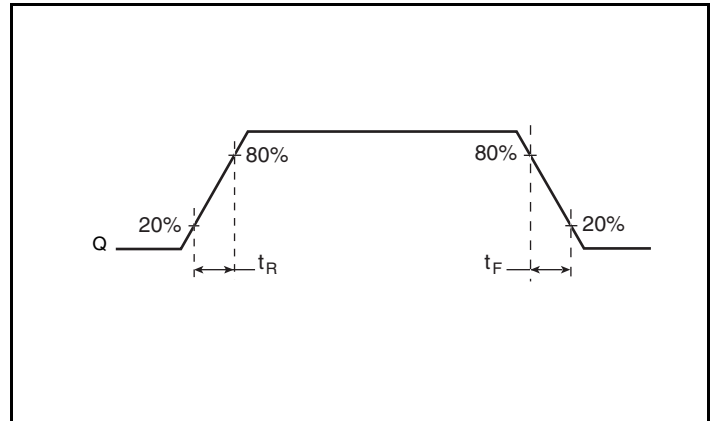


Input Skew

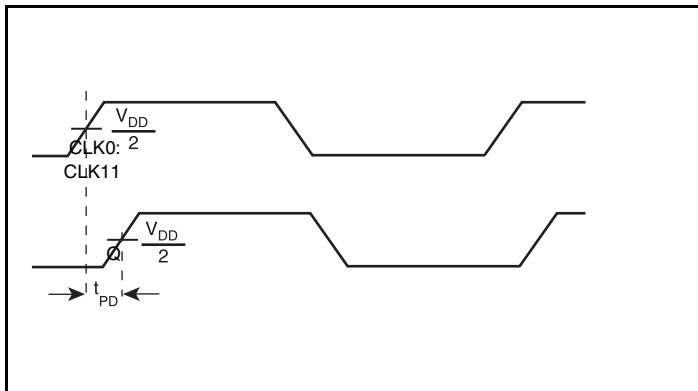
Parameter Measurement Information, continued



MUX Isolation



Output Rise/Fall Time



Propagation Delay

Recommendations for Unused Input Pins

Inputs:

CLK Inputs

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1k Ω resistor can be tied from the CLK input to ground.

LVC MOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1k Ω resistor can be used.

Reliability Information

Table 6. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

| θ_{JA} vs. Air Flow | | | |
|---|----------|------|------|
| Meters per Second | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 87.2°C/W | 82.9 | 80.7 |

Transistor Count

The transistor count for 850S1201 is: 649

Package Outline and Package Dimensions

Package Outline - G Suffix for 20 Lead TSSOP

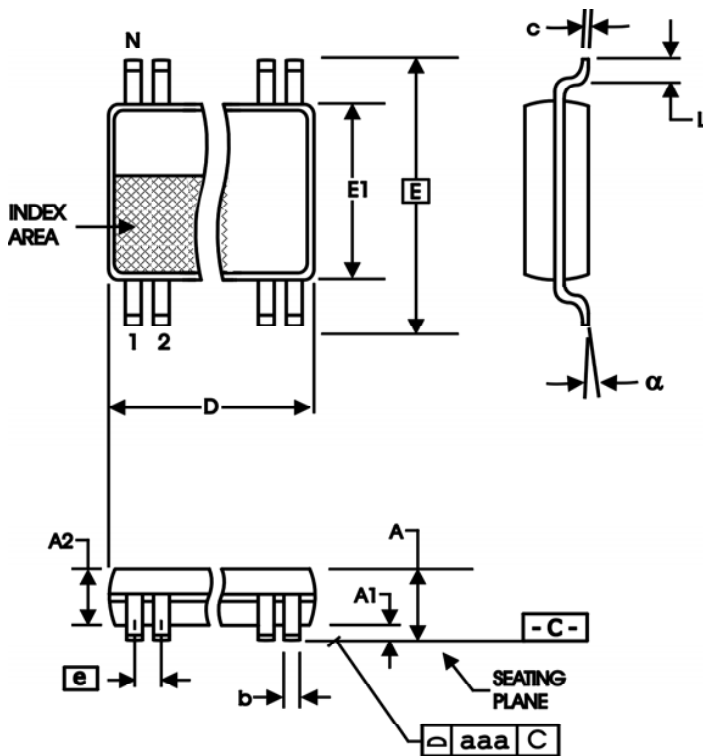


Table 7. Package Dimensions

| All Dimensions in Millimeters | | |
|-------------------------------|------------|---------|
| Symbol | Minimum | Maximum |
| N | 20 | |
| A | | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 6.40 | 6.60 |
| E | 6.40 Basic | |
| E1 | 4.30 | 4.50 |
| e | 0.65 Basic | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 8. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|---------------------------|--------------------|---------------|
| 850S1201BGILF | ICS0S1201BIL | "Lead-Free" 20 Lead TSSOP | Tube | -40°C to 85°C |
| 850S1201BGILFT | ICS0S1201BIL | "Lead-Free" 20 Lead TSSOP | Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|-----|----------------|------------|---|--------|
| A | T5A, T5B T8 | 5, 6 11 | AC Characteristics Table - added thermal note. Ordering Information Table - correct Part/Order Number from 850S1201AGILF/T to 850S1201BGILF/T. | 1/4/10 |
| B | | 1 | General Description - deleted HiperClocks logo. Throughout the datasheet - deleted "ICS" prefix and "I" suffix from the part number. Updated header/footer. | 2/8/16 |
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