

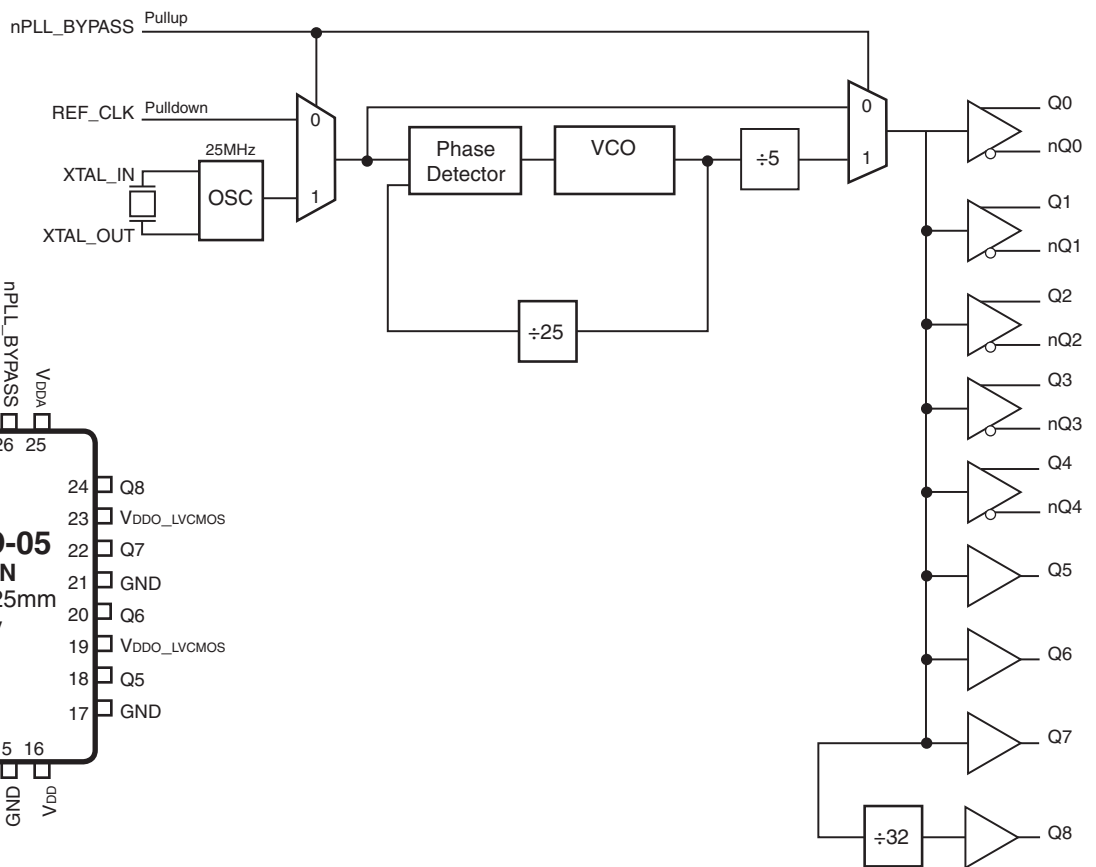
GENERAL DESCRIPTION

The ICS8440259D-05 is a 9 output synthesizer optimized to generate Gigabit and 10 Gigabit Ether-net. Using a 25MHz, 18pF parallel resonant crystal, the device will generate 125MHz and 3.90625MHz clocks with mix-ed LVDS and LVCMOS/LVTTL output levels. The ICS8440259D-05 uses IDT's 3rd generations low phase noise VCO technology and can achieve <1ps typical rms phase jitter, easily meeting Ethernet jitter requirements. The ICS8440259D-05 is packaged in a small, 32-pin VFQFN package that is optimum for applications with space limitations.

FEATURES

- Five differential LVDS outputs at 125MHz
Three LVCMOS/LVTTL single-ended outputs at 125MHz
One LVCMOS/LVTTL single-ended output at 3.90625MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input and PLL bypass from a single select pin
- VCO range: 510MHz - 650MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.41ps (typical)
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package

BLOCK DIAGRAM



PIN ASSIGNMENT

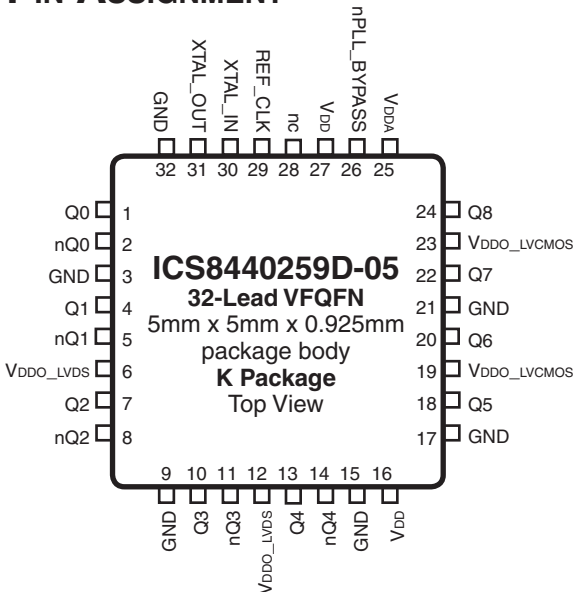


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential clock outputs. LVDS interface levels.
3, 9, 15, 17, 21, 32	GND	Power		Power supply ground.
4, 5	Q1, nQ1	Output		Differential clock outputs. LVDS interface levels.
6, 12	V _{DDO_LVDS}	Power		Output supply pins for Q[0:4]/nQ[0:4] LVDS outputs.
7, 8	Q2, nQ2	Output		Differential clock outputs. LVDS interface levels.
10, 11	Q3, nQ3	Output		Differential clock outputs. LVDS interface levels.
13, 14	Q4, nQ4	Output		Differential clock outputs. LVDS interface levels.
16, 27	V _{DD}	Power		Core supply pins.
18, 20, 22, 24	Q5, Q6, Q7, Q8	Output		Single-ended clock outputs. LVCMOS/LVTTL interface levels.
19, 23	V _{DDO_LVCMOS}	Power		Output supply pins for Q5:Q8 LVCMOS outputs.
25	V _{DDA}	Power		Analog supply pin.
26	nPLL_BYPASS	Input	Pullup	Input select and PLL bypass control pin. See Table 3. LVCMOS/LVTTL interface levels.
28	nc	Unused		No connect.
29	REF_CLK	Input	Pulldown	Single-ended reference clock input. Only selected in nPLL_BYPASS mode. LVCMOS/LVTTL interface levels.
30, 31	XTAL_IN, XTAL_OUT	Input		Crystal oscillator interface. XTAL_OUT is the output. XTAL_IN is the input.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C _{IN}	Input Capacitance			4		pF
C _{PD}	Power Dissipation Capacitance	V _{DD} , V _{DDO_LVCMOS} = 3.465V		15		pF
R _{PULLDOWN}	Input Pulldown Resistor			51		kΩ
R _{OUT}	Output Impedance	Q5:Q8		25		Ω

TABLE 3. PLL BYPASS AND INPUT SELECT FUNCTION TABLE

Inputs		
nPLL_BYPASS	PLL Bypass	Input Selected
0	PLL Bypassed	REF_CLK
1	PLL Enabled	XTAL_IN/XTAL_OUT (default)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to $V_{DD} + 0.5V$
Outputs, I_O (LVCMOS)	-0.5V to $V_{DDO_LVCMOS} + 0.5V$
Outputs, I_O (LVDS)	
Continuous Current	10mA
Surge Current	15mA
Operating Temperature Range, T_A	-40°C to +85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{DD} = V_{DDO_LVCMOS} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		$V_{DD} - 0.40$	3.3	V_{DD}	V
V_{DDO_LVCMOS} V_{DDO_LVDS}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current	Output Not Loaded			120	mA
I_{DDA}	Analog Supply Current	Output Not Loaded			40	mA
I_{DDO_LVCMOS}	LVCMOS Output Supply Current	Output Not Loaded			20	mA
I_{DDO_LVDS}	LVDS Output Supply Current	Output Not Loaded			165	mA

TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{DD} = V_{DDO_LVCMOS} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK			150	μA
		nPLL_BYPASS			5	μA
I_{IL}	Input Low Current	REF_CLK	-5			μA
		nPLL_BYPASS	-150			μA
V_{OH}	Output High Voltage	Q5:Q8	$I = -12mA$	2.6		V
V_{OL}	Output Low Voltage	Q5:Q8	$I = 12mA$		0.5	V

TABLE 4C. LVDS DC CHARACTERISTICS, $V_{DD} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	400	545	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.25	1.35	1.50	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

TABLE 5. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	Ω
Shunt Capacitance				7	pF
Drive Level				1	mW

NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 6. AC CHARACTERISTICS, $V_{DD} = V_{DDO_LVCMOS} = V_{DDO_LVDS} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q0/nQ0:Q4/nQ4		125		MHz
		Q5:Q7		125		MHz
		Q8		3.90625		MHz
$t_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	Q0:4/nQ0:4	125MHz, (1.875MHz - 20MHz)	0.44		ps
		Q5:Q7	125MHz, (1.875MHz - 20MHz)	0.41		ps
t_R / t_F	Output Rise/Fall Time	Q0/nQ0:Q4/nQ4 (NOTE 2)	125MHz, 20% to 80%	0.5	1.20	ns
		Q0/nQ0:Q4/nQ4	125MHz, 20% to 80%	0.4	0.65	ns
		Q5:Q7	125MHz, 20% to 80%	0.35	1.20	ns
		Q8 (NOTE 2)	3.90625MHz, 20% to 80%	1.0	1.65	ns
odc	Output Duty Cycle	Q0/nQ0:Q4/nQ4	125MHz	45	55	%
		Q5:Q7	125MHz	42	58	%
		Q8	3.90625MHz	49	51	%
odc	Output Duty Cycle, BYPASS Mode	Q0/nQ0:Q4/nQ4	125MHz	47	53	%
		Q5:Q7	125MHz	43	57	%
		Q8	3.90625MHz	49	51	%

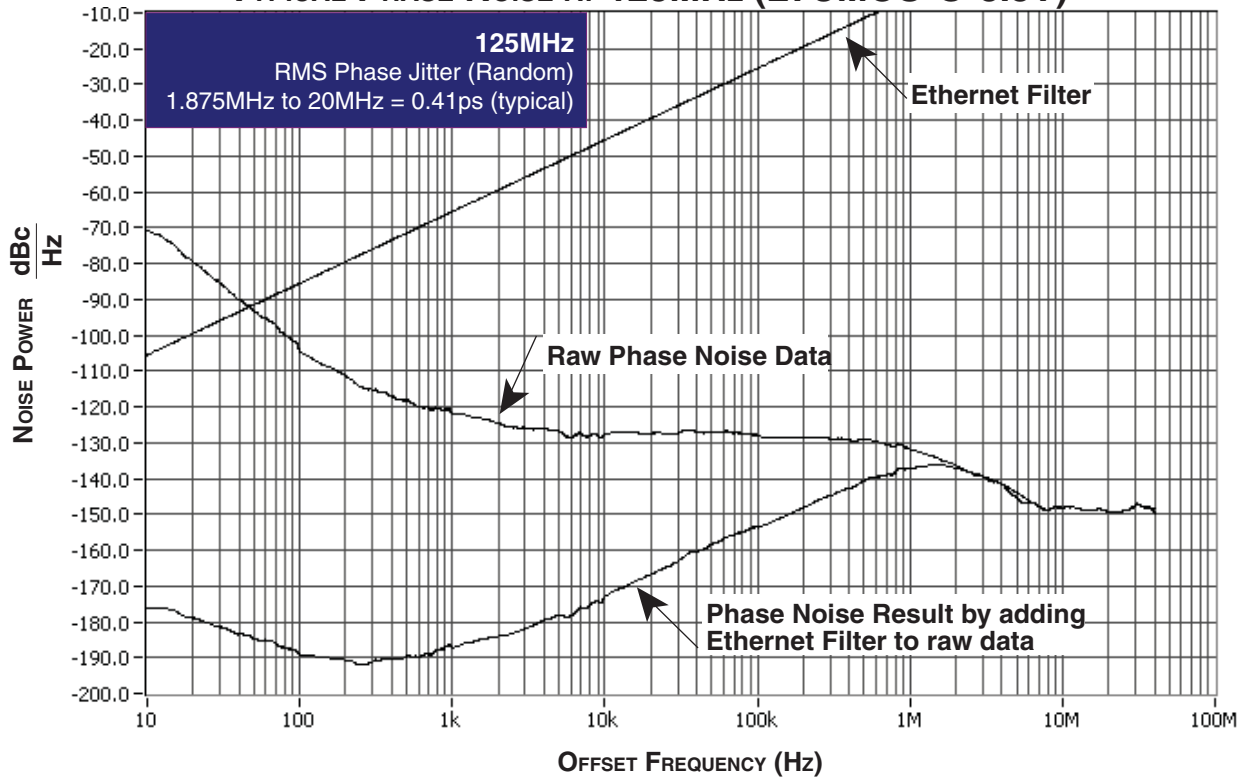
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTE: T_A , Ambient Temperature applied using forced air flow.

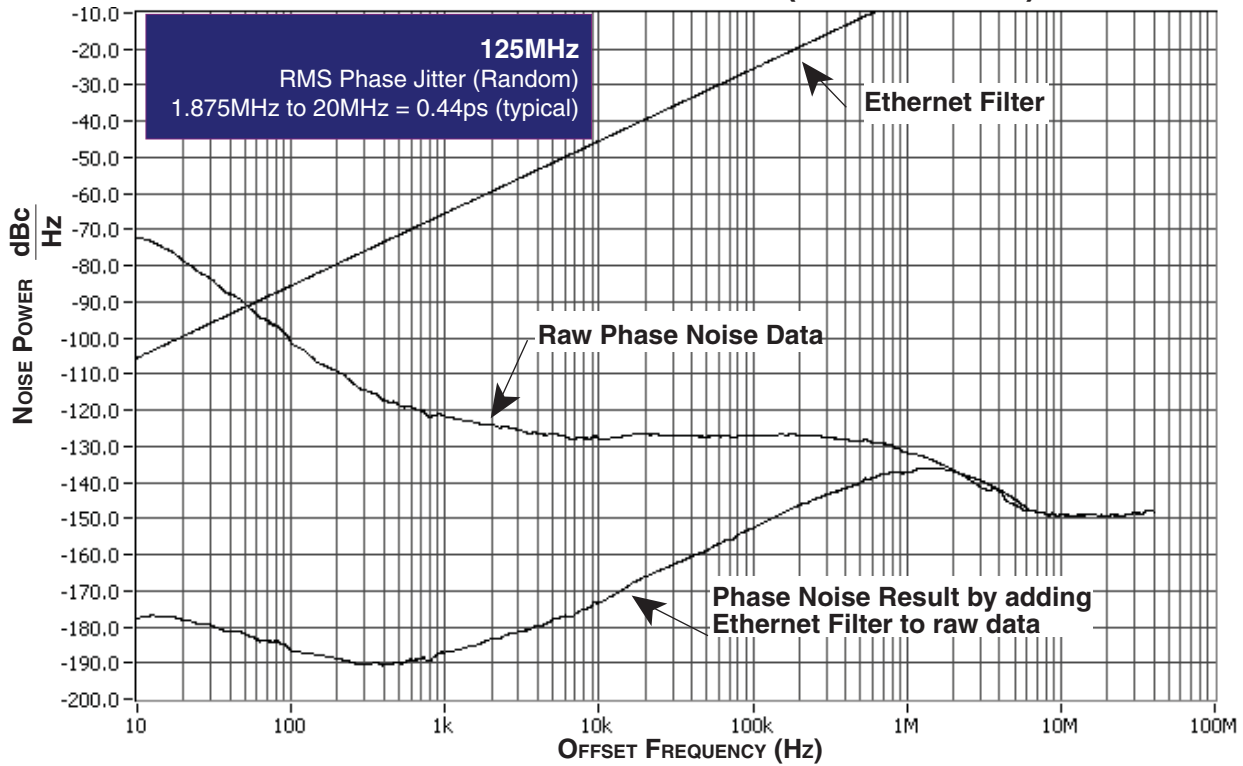
NOTE 1: Please refer to the Phase Noise Plots.

NOTE 2: Output loaded with 15pF.

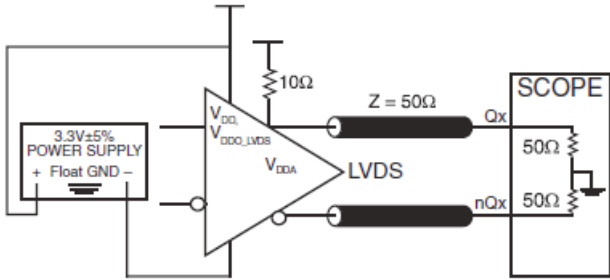
TYPICAL PHASE NOISE AT 125MHz (LVCMOS @ 3.3V)



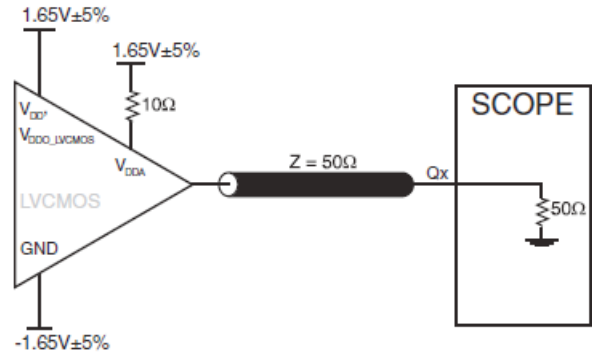
TYPICAL PHASE NOISE AT 125MHz (LVDS @ 3.3V)



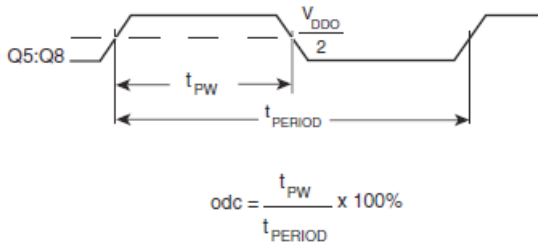
PARAMETER MEASUREMENT INFORMATION



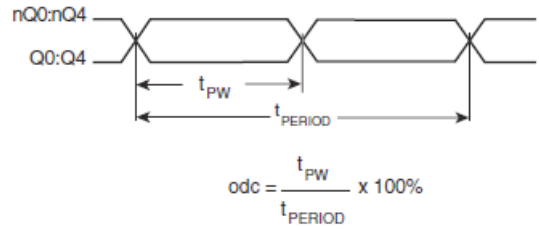
3.3V LVDS OUTPUT LOAD AC TEST CIRCUIT



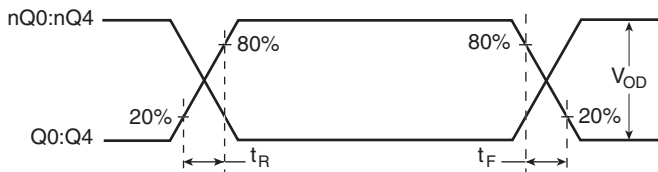
3.3V LVCMOS OUTPUT LOAD AC TEST CIRCUIT



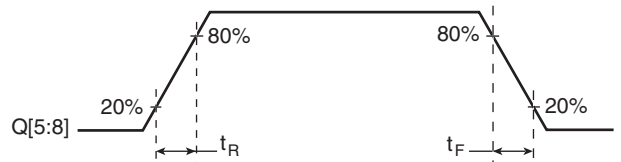
LVCMOS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



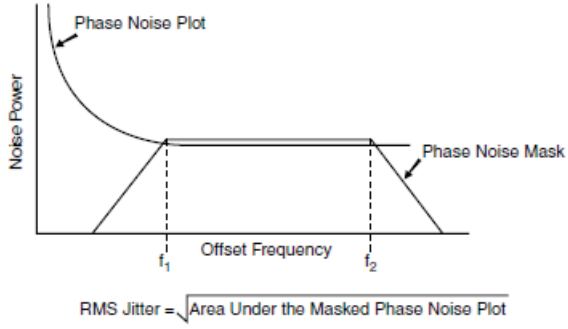
LVDS OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD



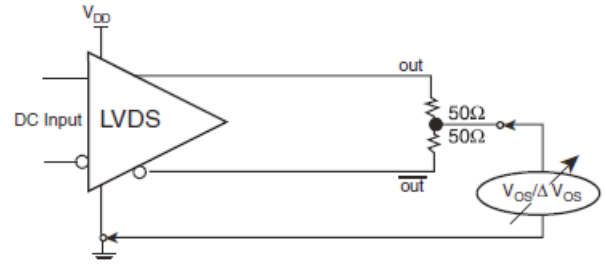
LVDS OUTPUT RISE/FALL TIME



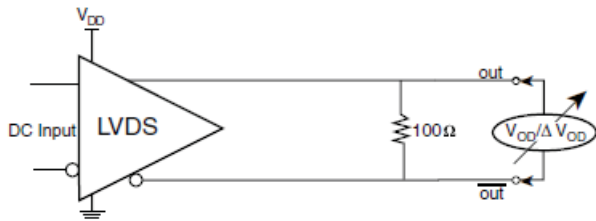
LVCMOS OUTPUT RISE/FALL TIME



RMS PHASE JITTER



OFFSET VOLTAGE SETUP



DIFFERENTIAL OUTPUT VOLTAGE SETUP

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS8440259D-05 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} , V_{DDA} , V_{DDO_LVDS} and V_{DDO_LVCMOS} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{DDA} pin.

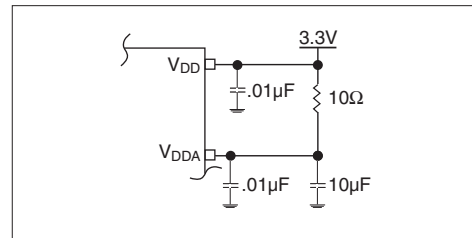


FIGURE 1. POWER SUPPLY FILTERING

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from XTAL_IN to ground.

REF_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a $1\text{k}\Omega$ resistor can be tied from the REF_CLK to ground.

LVC MOS CONTROL PINS

All control pins have internal pull-downs; additional resistance is not required but can be added for additional protection. A $1\text{k}\Omega$ resistor can be used.

OUTPUTS:

LVC MOS OUTPUTS

All unused LVC MOS output can be left floating. There should be no trace attached.

LVDS OUTPUTS

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

CRYSTAL INPUT INTERFACE

The ICS8440259D-05 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below

were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

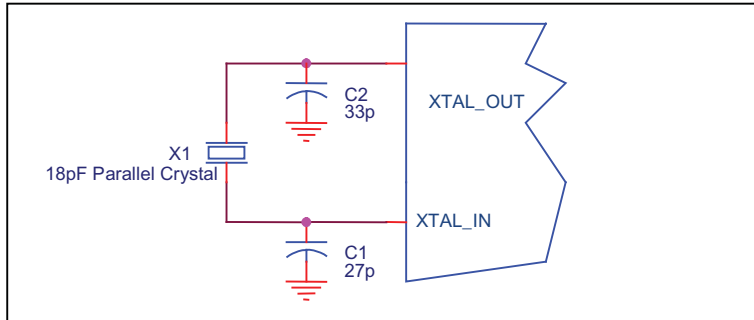


FIGURE 2. CRYSTAL INPUT INTERFACE

LVC MOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and making R_2 50Ω.

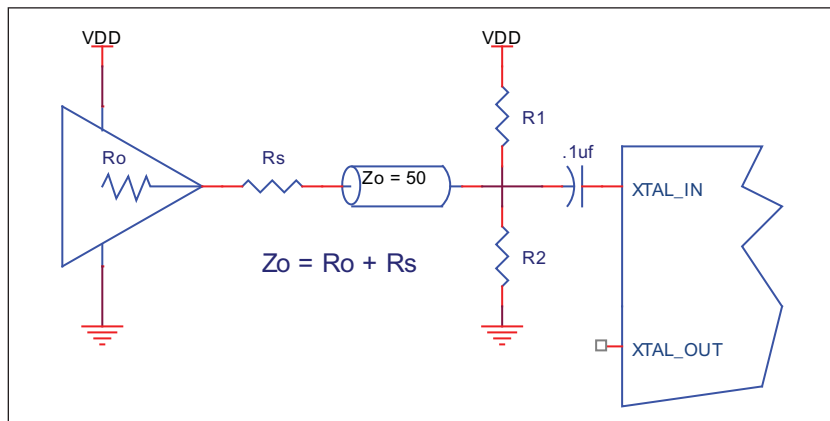


FIGURE 3. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 4*. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a

multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

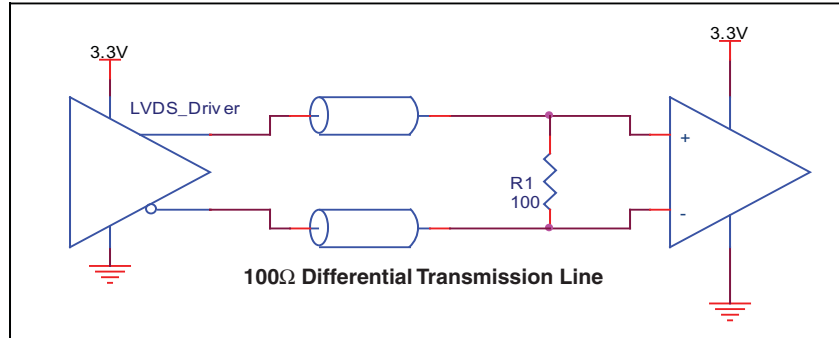


FIGURE 4. TYPICAL LVDS DRIVER TERMINATION

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application

specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

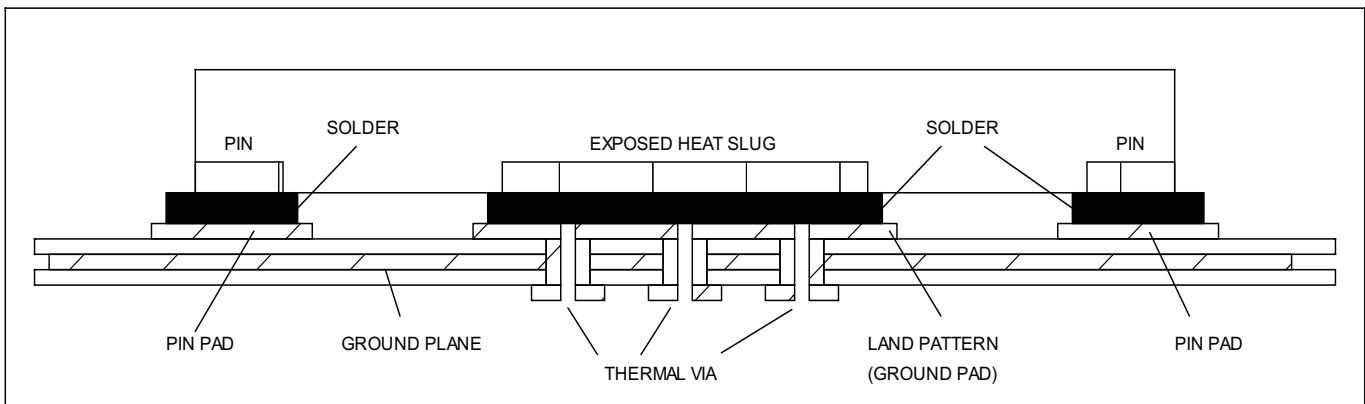


FIGURE 5. P.C.ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8440259D-05. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8440259D-05 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{DD} = 3.3V + 5\% = 3.465V$, which gives worst case results.

Core and LVDS Output Power Dissipation

- Power (core, LVDS) = $V_{DD_MAX} * (I_{DD} + I_{DDO_LVDS} + I_{DDA}) = 3.465V * (120mA + 165mA + 40mA) = \mathbf{1126.13mW}$

LVC MOS Output Power Dissipation

- Power (LVC MOS, no load) = $V_{DD_MAX} * I_{DDO_LVC MOS} = 3.465V * 20mA = \mathbf{69.3mW}$
- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{DDO}/2$
Output Current $I_{OUT} = V_{DDO_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 25\Omega)] = \mathbf{23.1mA}$
- Power Dissipation on the R_{OUT} per LVC MOS output
Power (R_{OUT}) = $R_{OUT} * (I_{OUT})^2 = 25\Omega * (23.1mA)^2 = \mathbf{13.3mW}$ per output
- Total Power Dissipation on the R_{OUT}
Total Power (R_{OUT}) = $13.3mW * 4 = \mathbf{53.2mW}$
- Dynamic Power Dissipation at 125MHz
Power (125MHz) = $C_{PD} * Frequency * (V_{DDO})^2 = 15pF * 125MHz * (3.465V)^2 = \mathbf{22.5mW}$ per output
Total Power (125MHz) = $22.5mW * 3 = \mathbf{67.5mW}$
- Dynamic Power Dissipation at 3.9MHz
Power (3.9MHz) = $C_{PD} * frequency * (V_{DDO})^2 = 15pF * 3.90625MHz * (3.465V)^2 = \mathbf{0.7mW}$ per output

Total Power Dissipation

- Total Power**
= Power (core, LVDS) + Power (LVC MOS, no load) + Total Power (R_{OUT}) + Total Power (125MHz) + Total Power (3.9MHz)
= $1126.13mW + 69.3mW + 53.2mW + 67.5mW + 0.7mW$
= **1391.51mW**

2. Junction Temperature.

Junction temperature, T_j, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7.

Therefore, T_j for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 1.391\text{W} * 37^\circ\text{C/W} = 121.5^\circ\text{C}.$$

This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 7. THERMAL RESISTANCE θ_{JA} FOR 32-LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. Air Flow (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

RELIABILITY INFORMATION

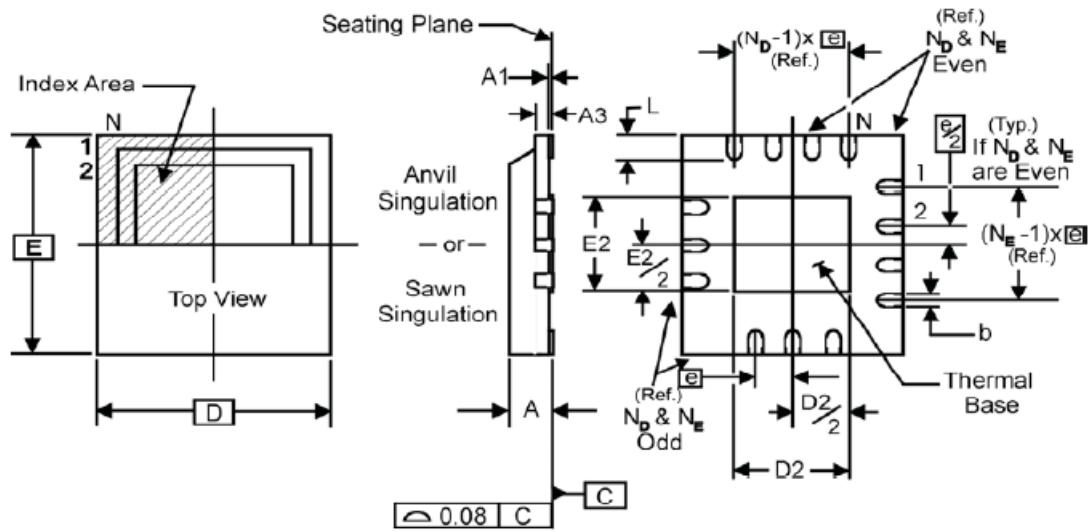
TABLE 8. θ_{JA} vs. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. Air Flow (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TRANSISTOR COUNT

The transistor count for ICS8440259D-05 is: 2975

PACKAGE OUTLINE - K SUFFIX FOR 32 LEAD VFQFN



NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page.

TABLE 9. PACKAGE DIMENSIONS

JEDEC VARIATION		
ALL DIMENSIONS IN MILLIMETERS (VHHD -2/ -4)		
SYMBOL	Minimum	Maximum
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_D	8	
N_E	8	
D, E	5.0 BASIC	
D2, E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 10. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8440259DK-05LF	ICS0259D05L	32 Lead "Lead-Free" VFQFN	Tray	0°C to 70°C
8440259DK-05LFT	ICS0259D05L	32 Lead "Lead-Free" VFQFN	Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History

9/3/14 Updated datasheet format
 Pg 1 Removed Block Diagram VCO limits
 Removed references to leaded devices
 Pg 15 Ordering Information - removed leaded devices

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.