General Description

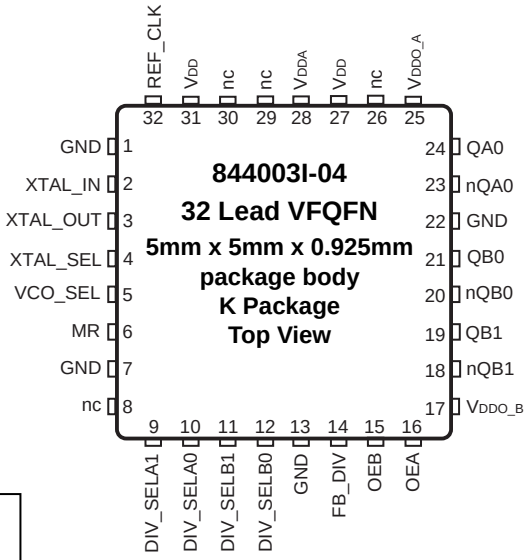
The 844003I-04 is a 3 differential output LVDS Synthesizer designed to generate Ethernet reference clock frequencies. Using a 19.44MHz, 20MHz or 25MHz, 18pF parallel resonant crystal, the following frequencies can be generated based on the settings of four frequency select pins (DIV_SELA[1:0], DIV_SELB[1:0]): 625MHz, 622.08MHz, 312.5MHz, 250MHz, 156.25MHz, 125MHz and 100MHz. The 844003I-04 has two output banks, Bank A with one differential LVDS output pair and Bank B with two differential LVDS output pairs.

The two banks have their own dedicated frequency select pins and can be independently set for the frequencies mentioned above. The 844003I-04 uses IDT's 3RD generation low phase noise VCO technology and can achieve 1ps or lower typical rms phase jitter, easily meeting Ethernet jitter requirements. The 844003I-04 is packaged in a 32-pin VFQFN package.

Features

- Three LVDS outputs on two banks, Bank A with one LVDS pair and Bank B with 2 LVDS output pairs
- Using a 19.44MHz, 20MHz, or 25MHz crystal, the two output banks can be independently set for 625MHz, 622.08MHz, 312.5MHz, 250MHz, 156.25MHz, 125MHz or 100MHz
- Selectable crystal oscillator interface or LVCMOS/LVTTL single-ended input
- VCO range: 490MHz to 680MHz
- RMS phase jitter at 125MHz (1.875MHz – 20MHz): 0.50ps (typical)
- Full 3.3V output supply mode
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- For functional replacement part use 8T49N241

Pin Assignment



Block Diagram

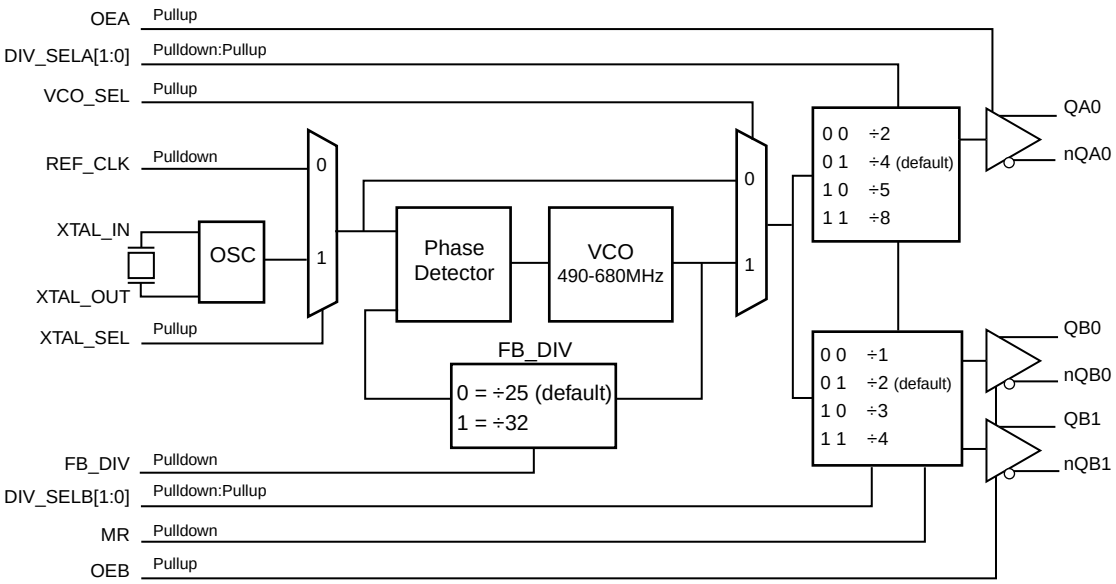


Table 1. Pin Descriptions

Number	Name	Type		Description
1, 7, 13, 22	GND	Power		Power supply ground.
2, 3	XTAL_IN XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. XTAL_IN is also the overdrive pin if you want to overdrive the crystal circuit with a single-ended reference clock.
4	XTAL_SEL	Input	Pullup	Crystal select pin. Selects between the single-ended REF_CLK or crystal interface. Has an internal pullup resistor so the crystal interface is selected by default. LVCMOS/LVTTL interface levels.
5	VCO_SEL	Input	Pullup	VCO select pin. When Low, the PLL is bypassed and the crystal reference or REF_CLK (depending on XTAL_SEL setting) are passed directly to the output dividers. Has an internal pullup resistor so the PLL is not bypassed by default. LVCMOS/LVTTL interface levels.
6	MR	Input	Pulldown	Active HIGH Master Reset. When logic HIGH, the internal dividers are reset, (except for ÷1 state, when the device is configured as a buffer), causing the true outputs QXx to go low and the inverted outputs nQXx to go high. When logic LOW, the internal dividers and the outputs are enabled. MR has an internal pulldown resistor so the power-up default state of outputs and dividers are enabled. LVCMOS/LVTTL interface levels.
8, 26, 29, 30	nc	Unused		No connect.
9	DIV_SELA1	Input	Pulldown	Division select pin for Bank A. Default = LOW. LVCMOS/LVTTL interface levels.
10	DIV_SELA0	Input	Pullup	Division select pin for Bank A. Default = HIGH. LVCMOS/LVTTL interface levels.
11	DIV_SELB1	Input	Pulldown	Division select pin for Bank B. Default = LOW. LVCMOS/LVTTL interface levels.
12	DIV_SELB0	Input	Pullup	Division select pin for Bank B. Default = HIGH. LVCMOS/LVTTL interface levels.
14	FB_DIV	Input	Pulldown	Feedback divide select. When Low (default), the feedback divider is set for ÷25. When HIGH, the feedback divider is set for ÷32. LVCMOS/LVTTL interface levels.
15	OEB	Input	Pullup	Output enable Bank B. Active High output enable. When logic HIGH, the output pair on Bank B is enabled. When logic LOW, the output pair is in a high-impedance state. Has an internal pullup resistor so the default power-up state of the outputs is enabled. LVCMOS/LVTTL interface levels.
16	OEA	Input	Pullup	Output enable Bank A. Active High output enable. When logic HIGH, the output pair on Bank A is enabled. When logic LOW, the output pair is in a high-impedance state. Has an internal pullup resistor so the default power-up state of the outputs is enabled. LVCMOS/LVTTL interface levels.
17	V_{DDO_B}	Power		Output power supply pin for Bank B outputs.
18, 19	nQB1, QB1	Output		Differential Bank B output pair. LVDS interface levels.
20, 21	nQB0, QB0	Output		Differential Bank B output pair. LVDS interface levels.
23, 24	nQA0, QA0	Output		Differential Bank A output pair. LVDS interface levels.
25	V_{DDO_A}	Power		Output supply pin for Bank A outputs.
27, 31	V_{DD}	Power		Core supply pins.
28	V_{DDA}	Power		Analog supply pin.
32	REF_CLK	Input	Pulldown	Single-ended reference clock input. Has an internal pulldown resistor to pull to low state by default. Can leave floating if using the crystal interface. LVCMOS/LVTTL interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3A. Output Bank A Configuration Select Function Table

Inputs		Outputs
DIV_SELA1	**DIV_SELA0**	**QA0, nQA0**
0	0	÷2
0	1	÷4 (default)
1	0	÷5
1	1	÷8

Table 3B. Output Bank B Configuration Select Function Table

Inputs		Outputs
DIV_SELB1	**DIV_SELB0**	**QB[0:1], nQB[0:1]**
0	0	÷1
0	1	÷2 (default)
1	0	÷3
1	1	÷4

Table 3C. OEA Select Function Table

Input	Outputs
OEA	**QA0, nQA0**
0	High-Impedance
1	Active (default)

Table 3D. OEB Select Function Table

Input	Outputs
OEB	**QB[0:1], nQB[0:1]**
0	High-Impedance
1	Active (default)

Table 3E. Feedback Divider Configuration Select Function Table

Input	
FB_DIV	**Feedback Divide**
0	÷25 (default)
1	÷32

Table 3F. Bank A Frequency Table

Inputs				Feedback Divider	Bank A Output Divider	M/N Multiplication Factor	QA0, nQA0 Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELA1	DIV_SELA0				
25	0	0	0	25	2	12.5	312.5
20	0	0	0	25	2	12.5	250
25	0	0	1	25	4	6.25	156.25
24	0	0	1	25	4	6.25	150
20	0	0	1	25	4	6.25	125
25	0	1	0	25	5	5	125
25	0	1	1	25	8	3.125	78.125
24	0	1	1	25	8	3.125	75
20	0	1	1	25	8	3.125	62.5
19.44	1	0	0	32	2	16	311.04
15.625	1	0	0	32	2	16	250
19.44	1	0	1	32	4	8	155.52
18.75	1	0	1	32	4	8	150
15.625	1	0	1	32	4	8	125
15.625	1	1	0	32	5	6.4	100
19.44	1	1	1	32	8	4	77.76
18.75	1	1	1	32	8	4	75
15.625	1	1	1	32	8	4	62.5

Table 3G. Bank B Frequency Table

Inputs				Feedback Divider	Bank B Output Divider	M/N Multiplication Factor	QBx/ nQBx Output Frequency (MHz)
Crystal Frequency (MHz)	FB_DIV	DIV_SELB1	DIV_SELB0				
25	0	0	0	25	1	25	625
25	0	0	1	25	2	12.5	312.5
20	0	0	1	25	2	12.5	250
22.5	0	1	0	25	3	8.333	187.5
25	0	1	1	25	4	6.25	156.25
24	0	1	1	25	4	6.25	150
20	0	1	1	25	4	6.25	125
19.44	1	0	0	32	1	32	622.08
19.44	1	0	1	32	2	16	311.04
15.625	1	0	1	32	2	16	250
18.75	1	1	0	32	3	10.667	200
19.44	1	1	1	32	4	8	155.52
18.75	1	1	1	32	4	8	150
15.625	1	1	1	32	4	8	125

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to V_{DD} -0.5V to V_{DD} + 0.5V
Outputs, I_O Continuous Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		2.97	3.3	3.63	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.20	3.3	V_{DD}	V
V_{DDO_A}, V_{DDO_B}	Output Supply Voltage		2.97	3.3	3.63	V
I_{DD}	Power Supply Current				140	mA
I_{DDA}	Analog Supply Current				20	mA
$I_{DDO\_A} + I_{DDO\_B}$	Output Supply Current				70	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	REF_CLK, MR, FB_DIV, DIV_SELA1, DIV_SELB1	$V_{DD} = V_{IN} = 3.63V$			150	µA
		OEA, OEB, VCO_SEL, XTAL_SEL, DIV_SELB0, DIV_SELA0	$V_{DD} = V_{IN} = 3.63V$			5	µA
I_{IL}	Input Low Current	REF_CLK, MR, FB_DIV, DIV_SELA1, DIV_SELB1	$V_{DD} = 3.465V$, $V_{IN} = 0V$	-5			µA
		OEA, OEB, VCO_SEL, XTAL_SEL, DIV_SELB0, DIV_SELA0		-150			µA

Table 4C. LVDS DC Characteristics, $V_{DD} = V_{DDO\_A} = V_{DDO\_B} = 3.3V \pm 10\%$, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		300	400	500	mV
ΔV_{OD}	V_{OD} Magnitude Change				50	mV
V_{OS}	Offset Voltage		1.25	1.35	1.55	V
ΔV_{OS}	V_{OS} Magnitude Change				50	mV

Table 5. Crystal Characteristics

Parameter		Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental			
Frequency	FB_DIV = ÷25		19.6	26.5625	27.2	MHz
	FB_DIV = ÷32		15.313		21.25	MHz
Equivalent Series Resistance (ESR)					50	Ω
Shunt Capacitance					7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

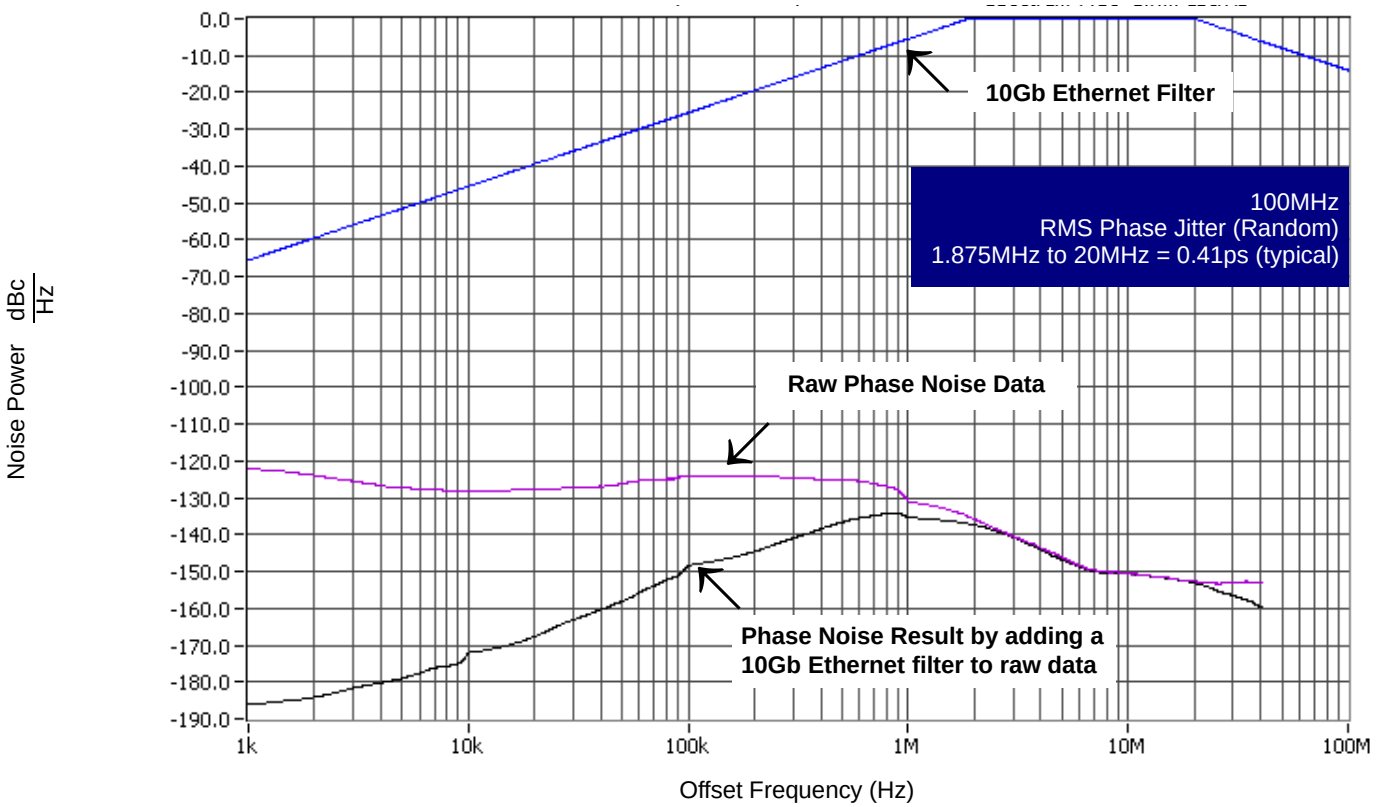
AC Electrical Characteristics

Table 6. AC Characteristics, V_{DD} = V_{DDO} = 3.3V ± 5%, T_A = -40°C to 85°C

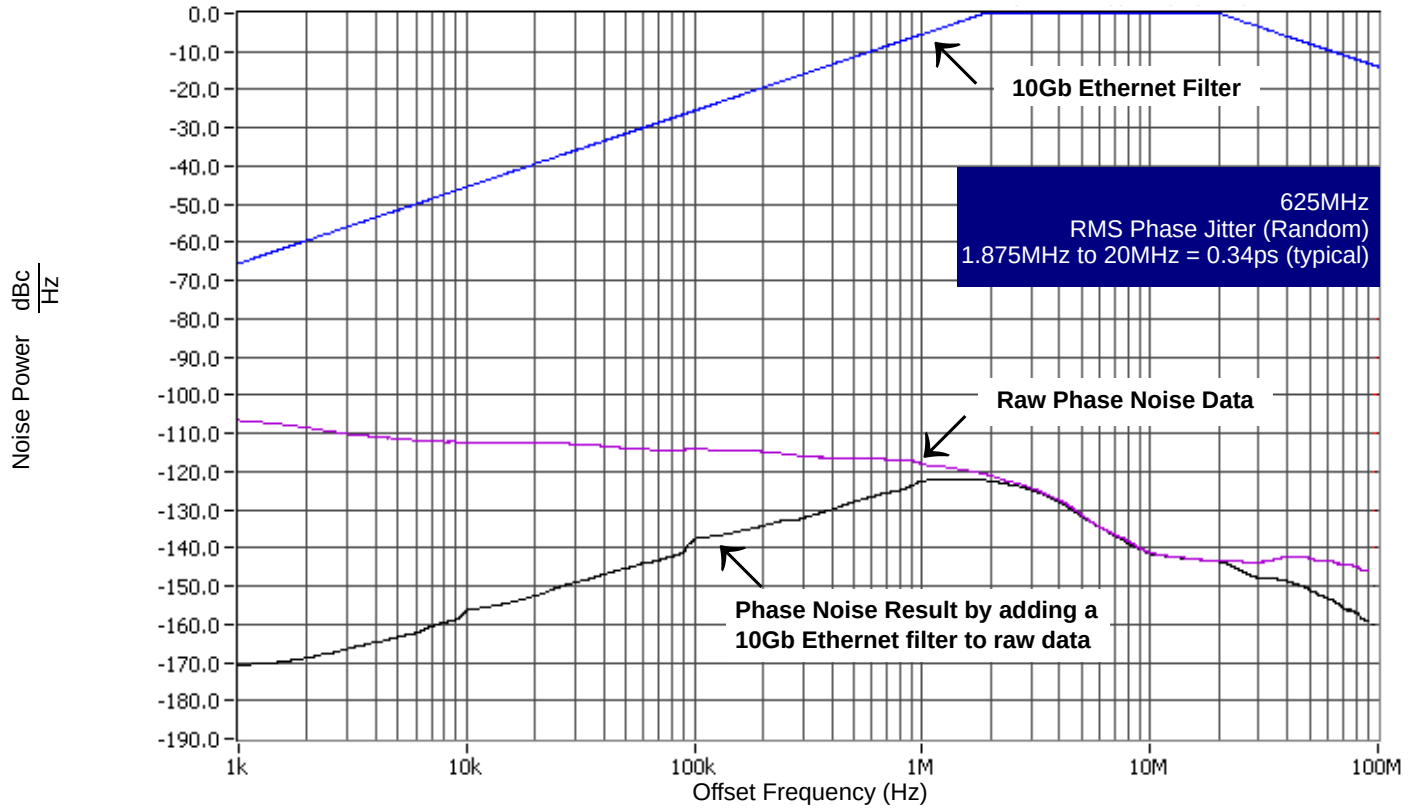
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		Output Divider = ÷1	490		680	MHz
			Output Divider = ÷2	245		340	MHz
			Output Divider = ÷3	163.33		226.67	MHz
			Output Divider = ÷4	122.5		170	MHz
			Output Divider = ÷5	98		136	MHz
			Output Divider = ÷8	61.25		85	MHz
*t*sk(b)	Bank Skew; NOTE 1					25	ps
*t*sk(o)	Output Skew	NOTE 2, 3	Outputs @ Same Frequency			50	ps
		NOTE 2, 3, 4	QB ≠ 1, Outputs @ Different Frequencies			250	ps
		NOTE 2, 3, 5	QB = 1, Outputs @ Different Frequencies			525	ps
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 6		625MHz, (1.875MHz - 20MHz)		0.34		ps
			312.5MHz, (1.875MHz - 20MHz)		0.34		ps
			250MHz, (1.875MHz - 20MHz)		0.42		ps
			125MHz, (1.875MHz - 20MHz)		0.50		ps
			100MHz, (1.875MHz - 20MHz)		0.41		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	150		550	ps
odc	Output Duty Cycle		Output Divider ≠ ÷1	48		52	%
			Output Divider = ÷1	44		56	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.
NOTE 2: Defined as skew between outputs at the same supply voltages and with equal load conditions.
Measured at the output differential cross points.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Characterized with DIV_SELA[1:0] = 11 and DIV_SELB[1:0] = 11.
NOTE 5: Characterized with DIV_SELA[1:0] = 00 and DIV_SELB[1:0] = 00.
NOTE 6: Please refer to the Phase Noise Plots.

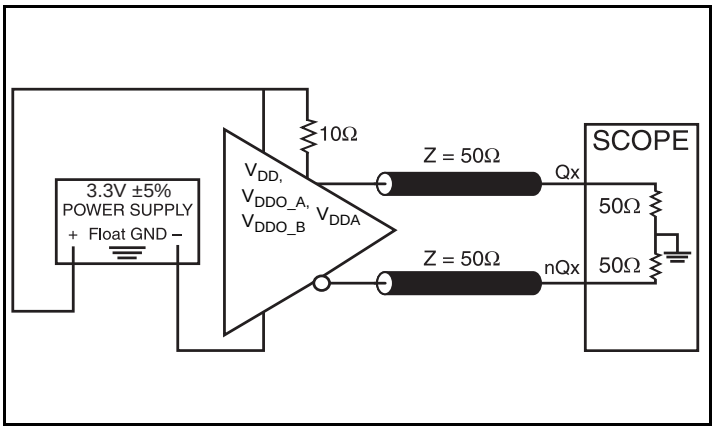
Typical Phase Noise at 100MHz



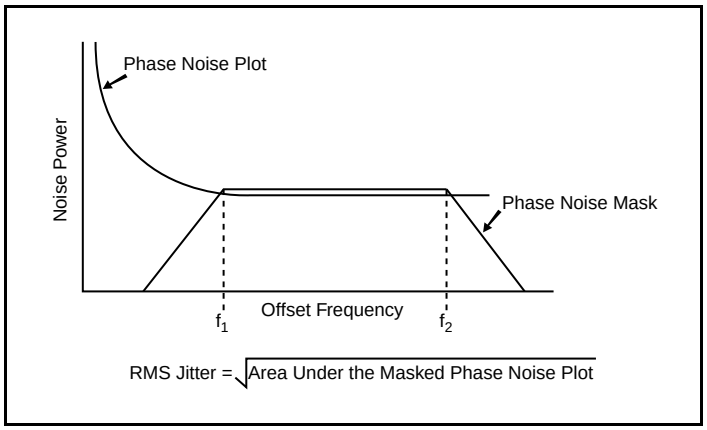
Typical Phase Noise at 625MHz



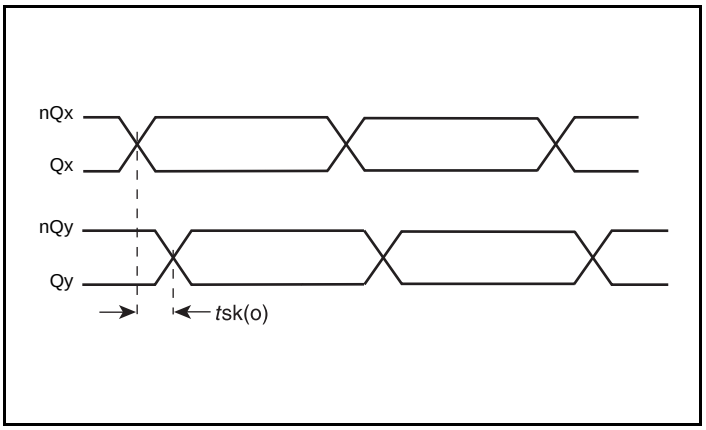
Parameter Measurement Information



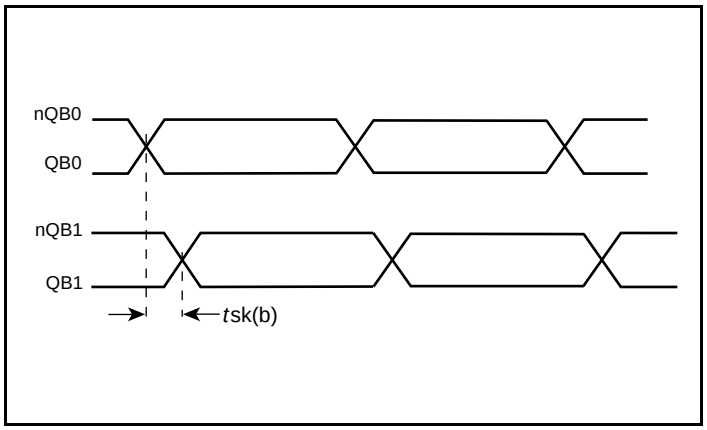
3.3V LVDS Output Load AC Test Circuit



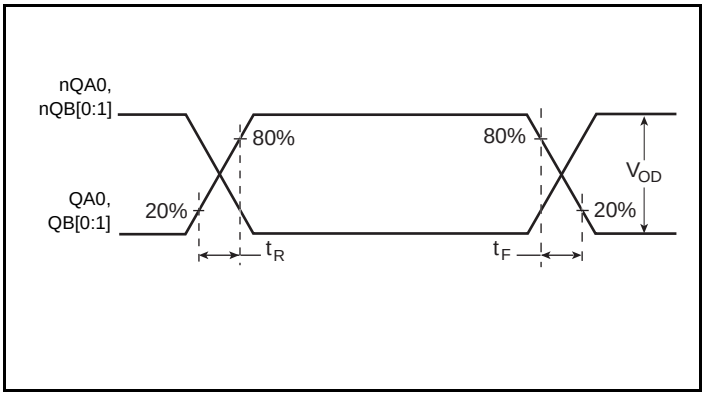
RMS Phase Jitter



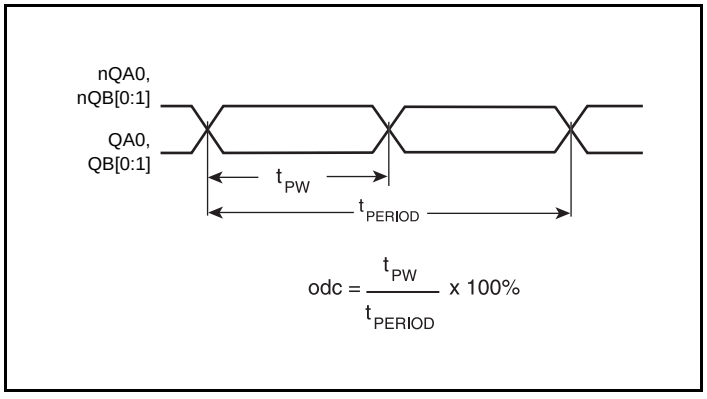
Output Skew



Bank Skew

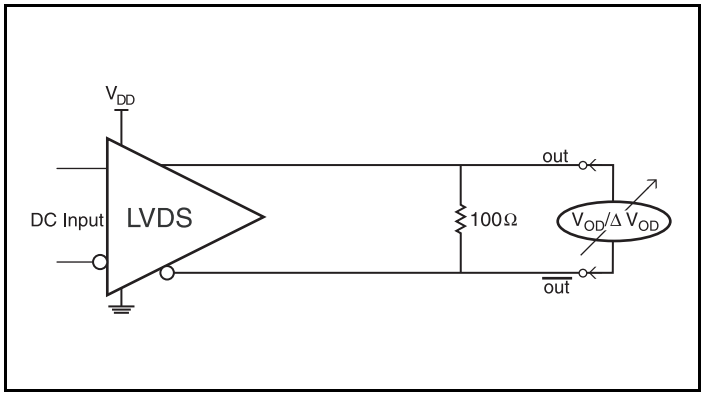


Output Rise/Fall Time

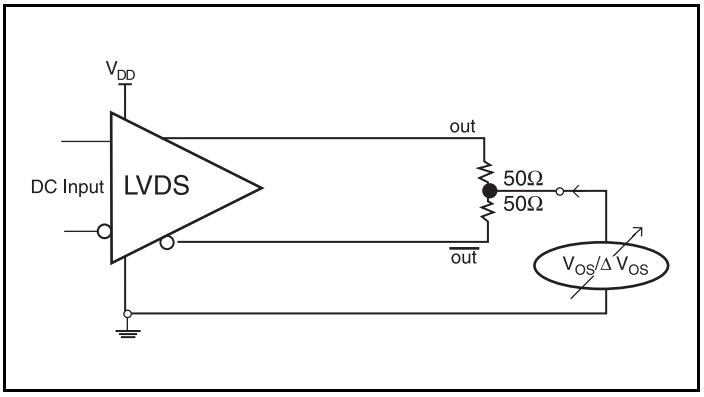


Output Duty Cycle/Pulse Width/Period

Parameter Measurement Information, continued



Differential Output Voltage Setup



Offset Voltage Setup

Applications Information

Power Supply Filtering Technique

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 844003I-04 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD}, V_{DDA}, V_{DDO_A} and V_{DDO_B} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.

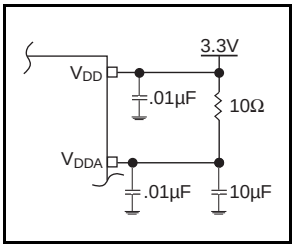


Figure 1. Power Supply Filtering

Crystal Input Interface

The 844003I-04 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

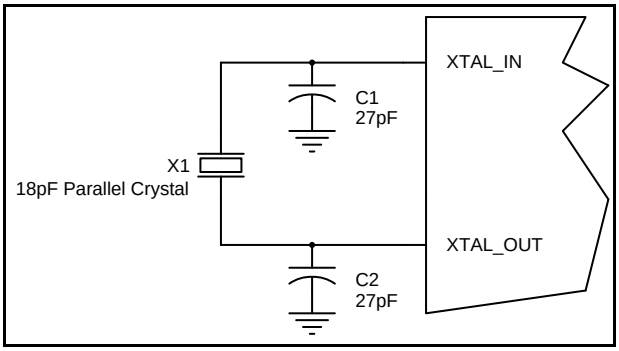


Figure 2. Crystal Input Interface

Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 3A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 3B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

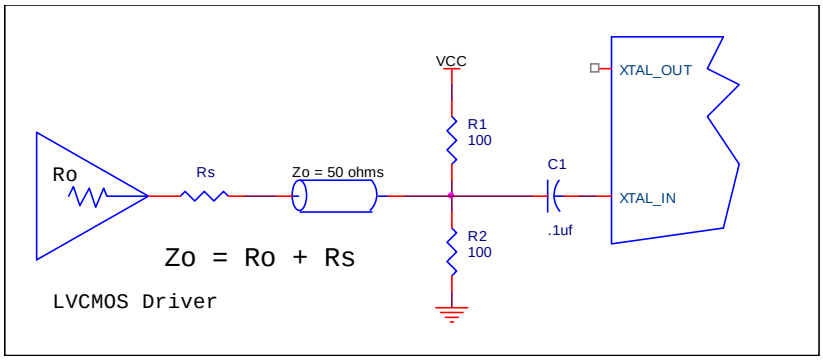


Figure 3A. General Diagram for LVCMOS Driver to XTAL Input Interface

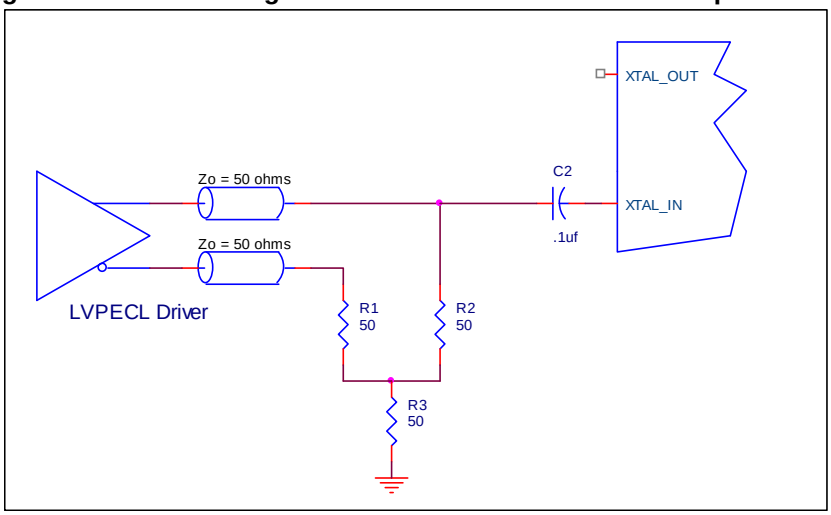


Figure 3B. General Diagram for LVPECL Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

LVCMOS Control Pins

All control pins have internal pullups and pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, we recommend that there is no trace attached.

LVDS Driver Termination

A general LVDS interface is shown in *Figure 4.* Standard termination for LVDS type output structure requires both a 100Ω parallel resistor at the receiver and a 100Ω differential transmission line environment. In order to avoid any transmission line reflection issues, the 100Ω resistor must be placed as close to the receiver as possible. IDT offers a full line of LVDS compliant devices with two types of output structures: current source and voltage source. The standard termination schematic as shown in Figure 4 can be used with either type of output structure. If using a non-standard termination, it is recommended to contact IDT and confirm if the output is a current source or a voltage source type structure. In addition, since these outputs are LVDS compatible, the amplitude and common mode input range of the input receivers should be verified for compatibility with the output.

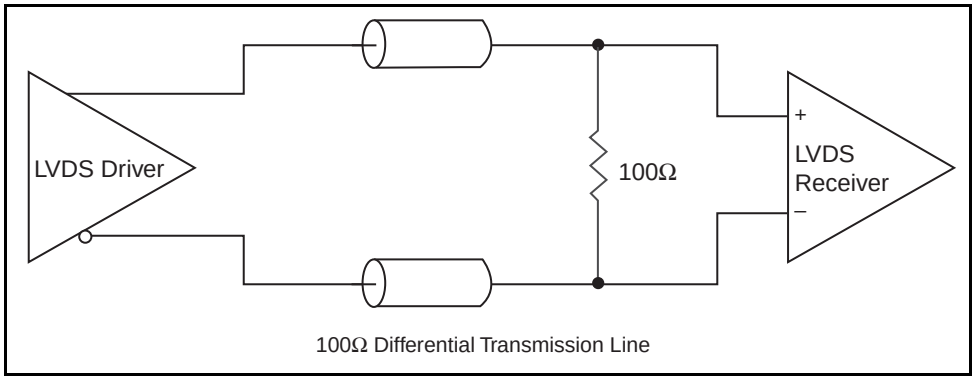


Figure 4. Typical LVDS Driver Termination

VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 5.* The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

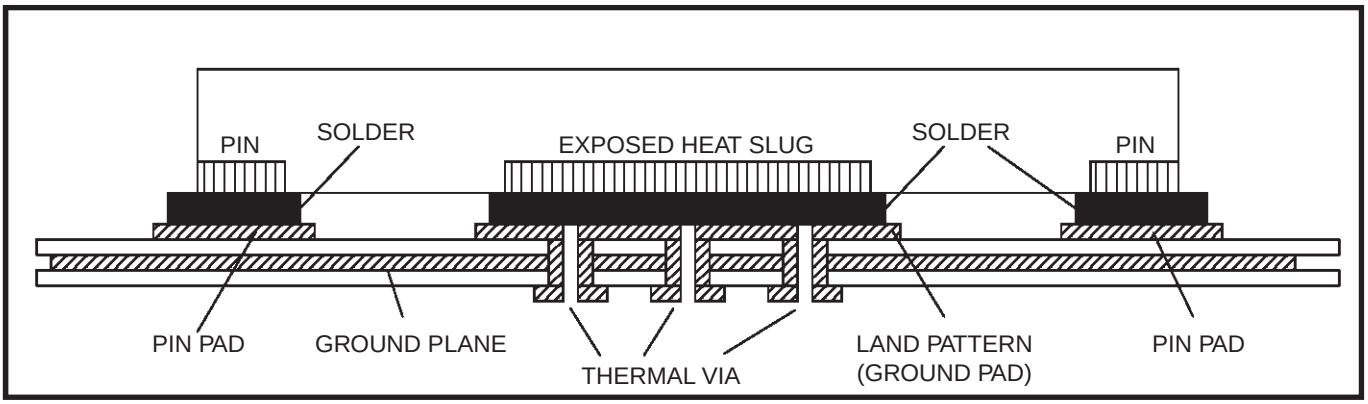


Figure 5. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)

Schematic Example

Figure 6 shows an example of an 844003I-04 application schematic. In this example, the device is operated at V_{DD} = V_{DDO_A} = V_{DDO_B} = 3.3V. The 18pF parallel resonant 25MHz crystal is used. The C1 and C2 = 27pF are recommended for frequency accuracy. For different board layouts, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVDS for receiver without built-in termination are shown in this schematic.

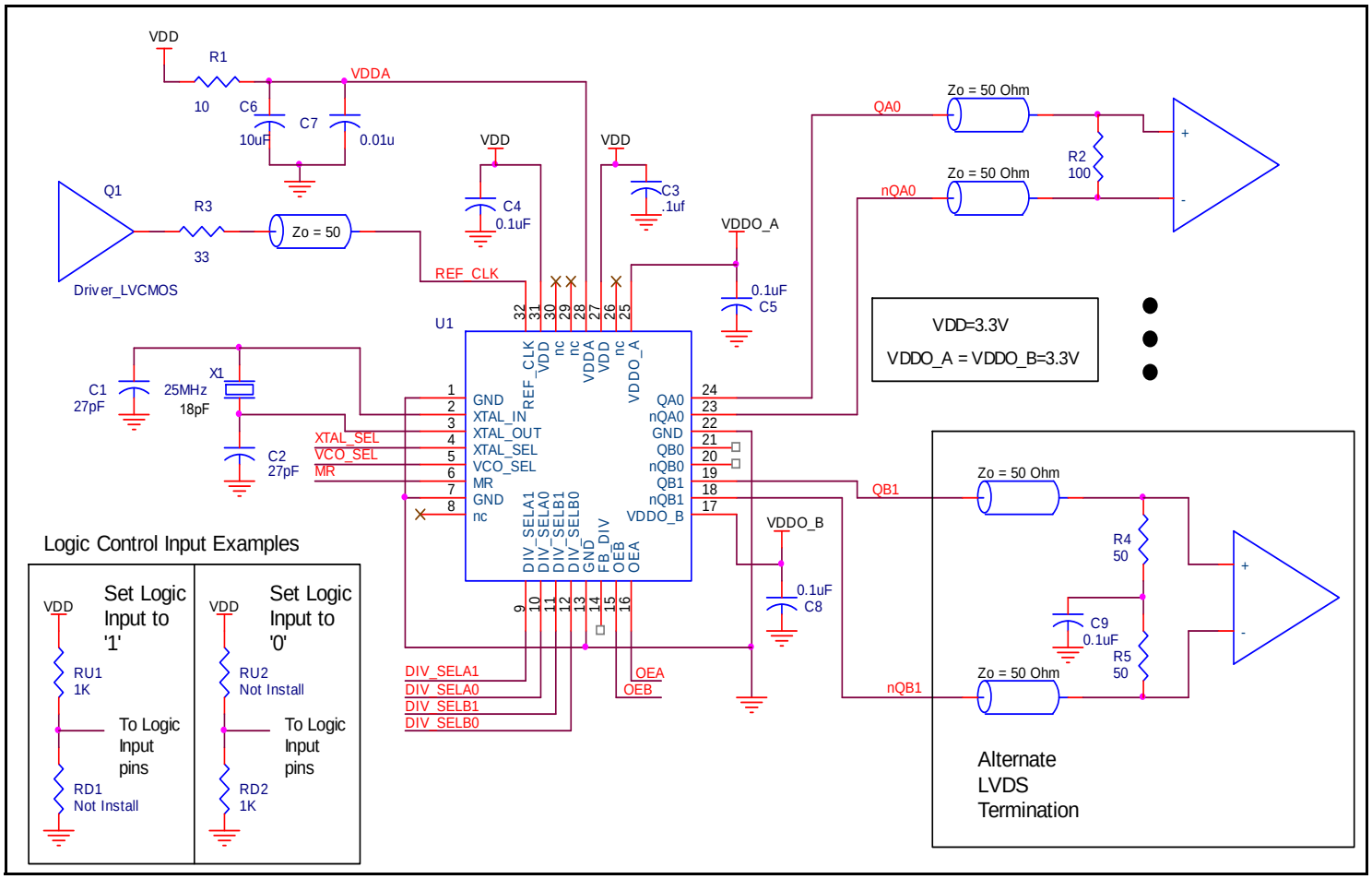


Figure 6. ICS870931I-01 Schematic Layout Example

Power Considerations

This section provides information on power dissipation and junction temperature for the 844003I-04.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 844003I-04 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for V_{DD} = 3.3V + 10% = 3.63V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{DD_MAX} * (I_{DD_MAX} + I_{DDA_MAX}) = 3.63V * (140mA + 20mA) = **580.80mW**
- Power (outputs)$_{MAX}$ = V_{DDO_MAX}* I_{DDO_MAX} = 3.63V * 70mA = **254.1mW**

Total Power$_{\_MAX}$ = 580.80mW + 254.1mW = **834.9mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.835W * 37°C/W = 115.9°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

Table 7. Thermal Resistance θ_{JA} for 32 Lead VFQFN, Forced Convection

θ_{JA} **vs. Air Flow**			
Meters per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29°C/W

Reliability Information

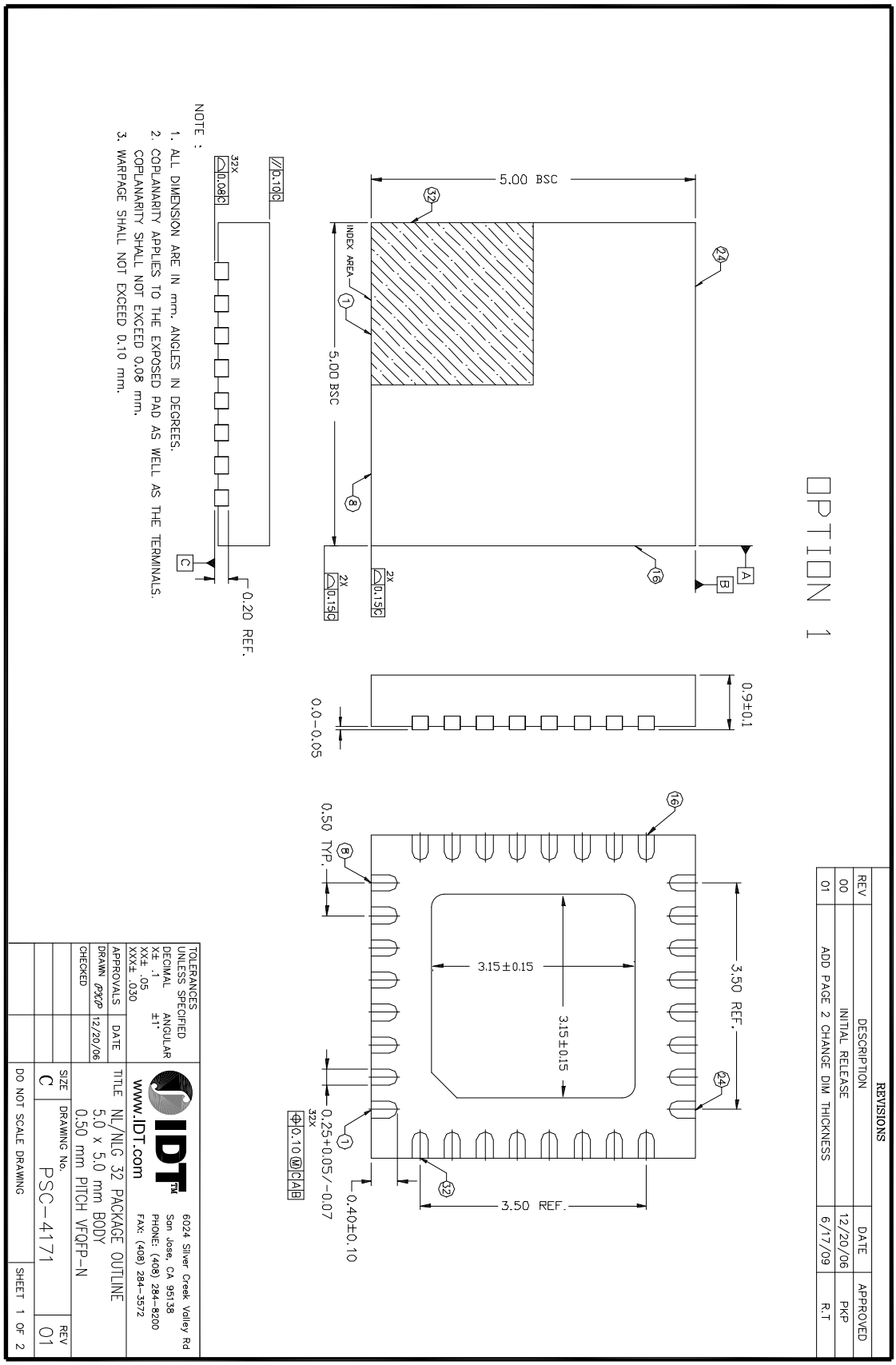
Table 8. θ_{JA} vs. Air Flow Table for a 32 Lead VFQFN

θ_{JA} vs. Air Flow			
Meter per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29°C/W

Transistor Count

The transistor count for 844003I-04 is: 4058

32 Lead VFQFN Package Outline and Package Dimensions



Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
844003AKI-04LF	ICS403AI04L	“Lead-Free” 32 Lead VFQFN	Tray	-40°C to 85°C
844003AKI-04LFT	ICS403AI04L	“Lead-Free” 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A		15	Added Layout Schematic.	6/10/09
B	 T4A T6	6 6 8 12 13 16 18	Absolute Maximum Ratings - updated Input Ratings. Power Supply DC Characteristics Table - changed I_{DDO} from 55mA max to 70mA max. AC Characteristics Table - corrected NOTES. Updated *Overdriving the XTAL Interface* application note. Updated *LVDS Driver Termination* application note. Updated Power Considerations to coincide with I_{DDO} spec change. Updated Package Drawing.	5/2/11
B		1	Product Discontinuation Notice - Last time buy expires November 2, 2016. PDN# CQ-15-05.	11/5/15
C	T10	19	Obsolete datasheet per PDN# CQ-15-05. Ordering Information table - deleted Tape & Reel count and table note. Updated datasheet header/footer.	11/10/16

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