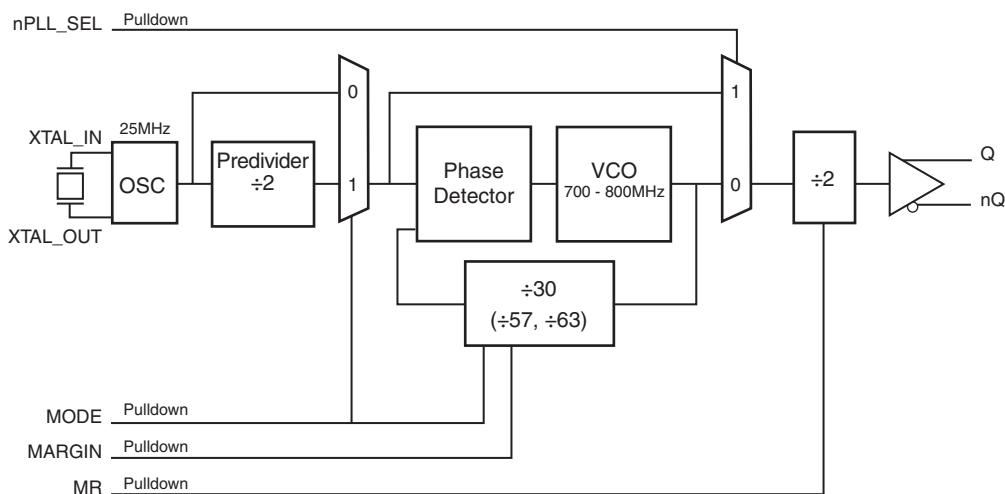


GENERAL DESCRIPTION

The 843201-375 is a low phase-noise frequency margining synthesizer. In the default mode, the device nominally generates a 375MHz LVPECL output clock signal from a 25MHz crystal input. There is also a frequency margining mode available where the device can be configured, using control pins, to vary the output frequency up or down from nominal by 5%. The 843201-375 is provided in a 16-pin TSSOP package.

FEATURES

- One 375MHz nominal LVPECL output
- Crystal oscillator interface designed for 25MHz, 18pF parallel resonant crystal
- Output frequency can be varied $\pm 5\%$ from nominal
- VCO range: 700MHz - 800MHz
- RMS phase jitter @ 375MHz, using a 25MHz crystal (12kHz - 20MHz): 0.72ps (typical) @ 3.3V
- Output supply modes
Core/Output
3.3V/3.3V
3.3V/2.5V
2.5V/2.5V
- 0°C to 70°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **Functional replacement part 8T49N241-dddNLGI**

BLOCK DIAGRAM**PIN ASSIGNMENT**

| | | | |
|-----------------|---|----|------------------|
| V _{CC} | 1 | 16 | Q |
| MODE | 2 | 15 | nQ |
| nc | 3 | 14 | V _{CCO} |
| XTAL_IN | 4 | 13 | V _{CC} |
| XTAL_OUT | 5 | 12 | V _{EE} |
| MARGIN | 6 | 11 | MR |
| V _{EE} | 7 | 10 | nPLL_SEL |
| nc | 8 | 9 | nc |

843201-375
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm
package body
G Package
Top View

FUNCTIONAL DESCRIPTION

The 843201-375 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 25MHz fundamental crystal is used as the input to the on chip oscillator. In regular mode, the 25MHz crystal frequency is applied directly to the phase detector. In frequency margining mode, the 25MHz crystal frequency is divided by 2 and a 12.5MHz reference frequency is applied to the phase detector. The VCO of the PLL operates over a range of 700MHz to 800MHz. The output of the M divider is also applied to the phase detector. The default mode for the 843201-375 is a nominal 375MHz output. The nominal output frequency can be changed by placing the device into the margining mode using the mode pin and using the margin pin to change the M

feedback divider. Frequency margining mode operation occurs when the MODE input is HIGH. The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. The output of the VCO is scaled by an output divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle. The relationship between the crystal input frequency, the M divider, the VCO frequency and the output frequency is provided in Table 1. When changing back from frequency margining mode to nominal mode, the device will return to the default nominal configuration described above.

TABLE 1. FREQUENCY MARGIN FUNCTION TABLE

| MODE | MARGIN | XTAL (MHz) | Pre-Divider (P) | Reference Frequency (MHz) | Feedback Divider | VCO (MHz) | % Change |
|------|--------|------------|-----------------|---------------------------|------------------|-----------|-----------|
| 1 | 0 | 25 | 2 | 12.5 | 57 | 712.5 | -5.0 |
| 0 | X | 25 | none | 25 | 30 | 750 | Nom. Mode |
| 1 | 1 | 25 | 2 | 12.5 | 63 | 787.5 | 5.0 |

TABLE 2. PIN DESCRIPTIONS

| Number | Name | Type | Description | |
|---------|-------------------|--------|-----------------------|---|
| 1, 13 | V_{cc} | Power | Positive supply pins. | |
| 2 | MODE | Input | Pulldown | MODE pin. LOW = default mode. HIGH = frequency margining mode. LVCMOS/LVTTL interface levels. |
| 3, 8, 9 | nc | Unused | | No connect. |
| 4, 5 | XTAL_IN, XTAL_OUT | Input | | Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. |
| 6 | Margin | Input | Pulldown | Sets the frequency margin to $\pm 5\%$ in frequency margining mode. See Table 1. LVCMOS/LVTTL interface levels. |
| 7, 12 | V_{ee} | Power | | Negative supply pins. |
| 10 | nPLL_SEL | Input | Pulldown | PLL select pin. When HIGH, PLL is bypassed and input is fed directly to the output dividers. When LOW, PLL is enabled. LVCMOS/LVTTL interface levels. |
| 11 | MR | Input | Pulldown | Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output Q to go low and the inverted output nQ to go high. When logic LOW, the internal dividers and the output is enabled. LVCMOS/LVTTL interface levels. |
| 14 | V_{cco} | Power | | Output supply pin. |
| 15, 16 | nQ, Q | Output | | Differential output pair. LVPECL interface levels. |

NOTE: Pulldown refers to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|-------------------------|-----------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | 4 | | pF |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | k Ω |

TABLE 4. MODE CONTROL INPUT FUNCTION TABLE

| Input | Condition |
|-------|--------------------------|
| MODE | Q, nQ |
| 0 | Default Mode |
| 1 | Frequency Margining Mode |

ABSOLUTE MAXIMUM RATINGS

| | |
|--|--------------------------|
| Supply Voltage, V_{cc} | 4.6V |
| Inputs, V_i | -0.5V to $V_{cc} + 0.5V$ |
| Outputs, I_o | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 99.9°C/W (0 lfpm) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS, $V_{cc} = V_{cco} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{cc} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{cco} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{EE} | Power Supply Current | | | | 108 | mA |
| I_{cc} | Power Supply Current | | | | 96 | mA |
| I_{cco} | Output Supply Current | | | | 12 | mA |

TABLE 5B. POWER SUPPLY DC CHARACTERISTICS, $V_{cc} = 3.3V \pm 5\%$, $V_{cco} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{cc} | Positive Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{cco} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{EE} | Power Supply Current | | | | 108 | mA |
| I_{cc} | Power Supply Current | | | | 96 | mA |
| I_{cco} | Output Supply Current | | | | 12 | mA |

TABLE 5C. POWER SUPPLY DC CHARACTERISTICS, $V_{cc} = V_{cco} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|-------------------------|-----------------|---------|---------|---------|-------|
| V_{cc} | Positive Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{cco} | Output Supply Voltage | | 2.375 | 2.5 | 2.625 | V |
| I_{EE} | Power Supply Current | | | | 101 | mA |
| I_{cc} | Power Supply Current | | | | 95 | mA |
| I_{cco} | Output Supply Current | | | | 6 | mA |

TABLE 5D. LVC MOS / LVTTL DC CHARACTERISTICS, $T_A = 0^\circ\text{C}$ TO 70°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|--------------------|----------------------------|---|---------|---------|----------------|---------------|
| V_{IH} | Input High Voltage | | $V_{cc} = 3.3\text{V}$ | 2 | | $V_{cc} + 0.3$ | V |
| | | | $V_{cc} = 2.5\text{V}$ | 1.7 | | $V_{cc} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | $V_{cc} = 3.3\text{V}$ | -0.3 | | 0.8 | V |
| | | | $V_{cc} = 2.5\text{V}$ | -0.3 | | 0.7 | V |
| I_{IH} | Input High Current | MARGIN, MODE, nPLL_SEL, MR | $V_{cc} = V_{IN} = 3.465$ or 2.625V | | | 150 | μA |
| I_{IL} | Input Low Current | MARGIN, MODE, nPLL_SEL, MR | $V_{cc} = 3.465\text{V}$ or 2.625V, $V_{IN} = 0\text{V}$ | -5 | | | μA |

TABLE 5E. LVPECL DC CHARACTERISTICS, $T_A = 0^\circ\text{C}$ TO 70°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{cco} - 1.4$ | | $V_{cco} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{cco} - 2.0$ | | $V_{cco} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{cco} - 2\text{V}$.

TABLE 6. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|---------------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 300 | μW |

NOTE: Characterized using an 18pF parallel resonant crystal.

NOTE: It is not recommended to overdrive the crystal input with an external clock.

TABLE 7A. AC CHARACTERISTICS, $V_{cc} = V_{cco} = 3.3V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|--------------------------------------|---|---------|---------|---------|-------|
| f_{out} | Output Frequency | | | 375 | | MHz |
| $t_{jitter}(F)$ | RMS Phase Jitter (Random); NOTE 1 | 375MHz, Integration Range: 12kHz - 20MHz | | 0.72 | | ps |
| t_r / t_f | Output Rise/Fall Time | 20% to 80% | 200 | | 550 | ps |
| odc | Output Duty Cycle | | 49 | | 51 | % |

NOTE 1: Refer to Phase Noise Plot.

TABLE 7B. AC CHARACTERISTICS, $V_{cc} = 3.3V \pm 5\%$, $V_{cco} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|--------------------------------------|---|---------|---------|---------|-------|
| f_{out} | Output Frequency | | | 375 | | MHz |
| $t_{jitter}(F)$ | RMS Phase Jitter (Random); NOTE 1 | 375MHz, Integration Range: 12kHz - 20MHz | | 0.72 | | ps |
| t_r / t_f | Output Rise/Fall Time | 20% to 80% | 200 | | 550 | ps |
| odc | Output Duty Cycle | | 49 | | 51 | % |

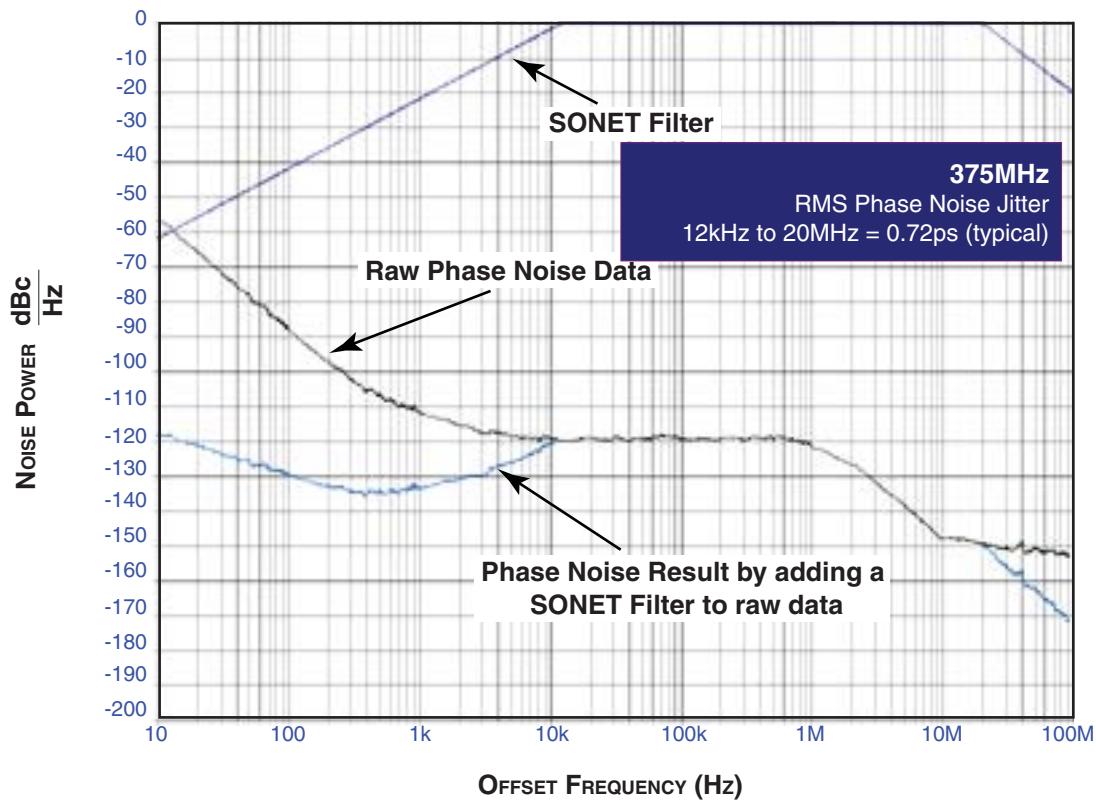
NOTE 1: Refer to Phase Noise Plot.

TABLE 7C. AC CHARACTERISTICS, $V_{cc} = V_{cco} = 2.5V \pm 5\%$, $T_A = 0^\circ C$ TO $70^\circ C$

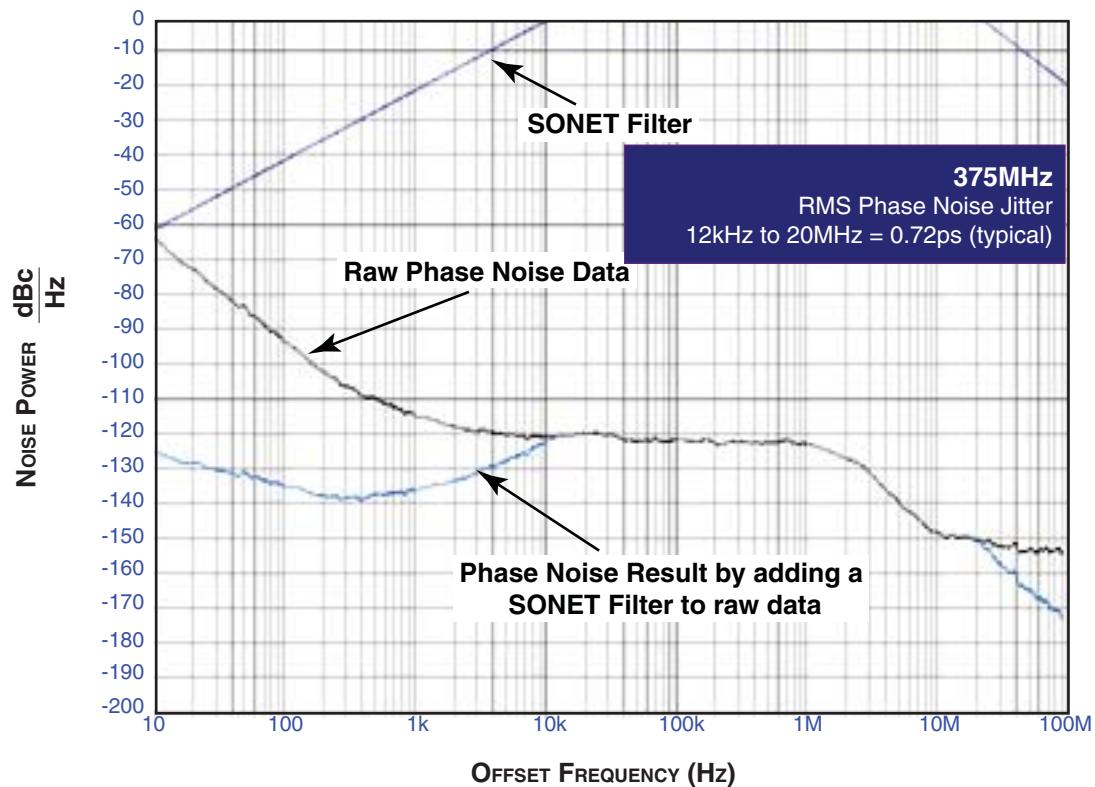
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------------|--------------------------------------|---|---------|---------|---------|-------|
| f_{out} | Output Frequency | | | 375 | | MHz |
| $t_{jitter}(F)$ | RMS Phase Jitter (Random); NOTE 1 | 375MHz, Integration Range: 12kHz - 20MHz | | 0.88 | | ps |
| t_r / t_f | Output Rise/Fall Time | 20% to 80% | 200 | | 550 | ps |
| odc | Output Duty Cycle | | 49 | | 51 | % |

NOTE 1: Refer to Phase Noise Plot.

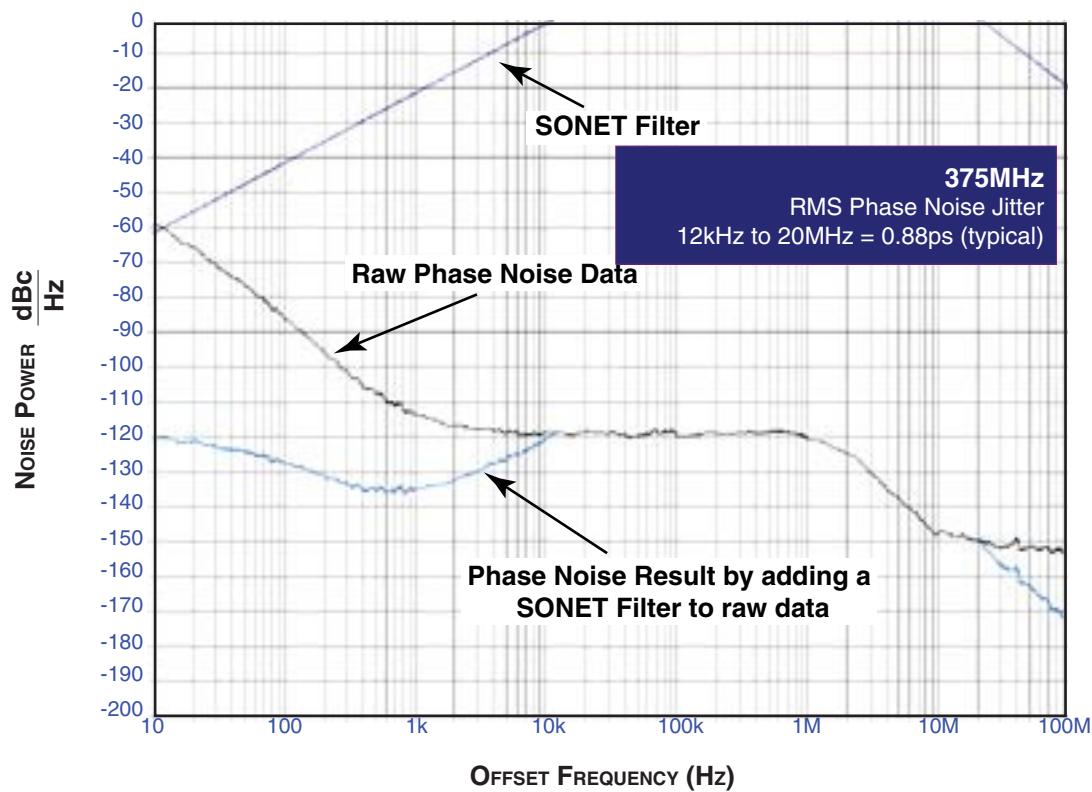
TYPICAL PHASE NOISE AT 375MHz @ 3.3V/3.3V



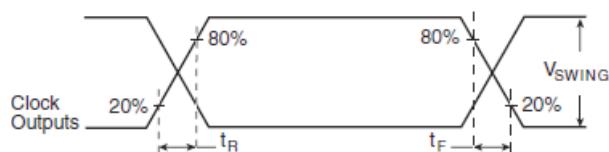
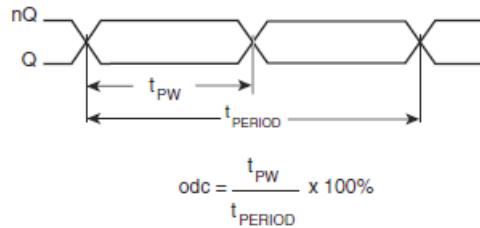
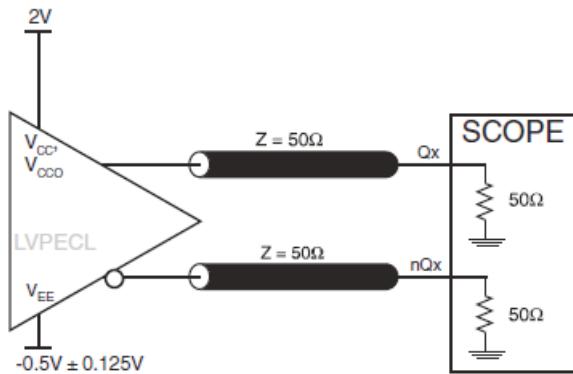
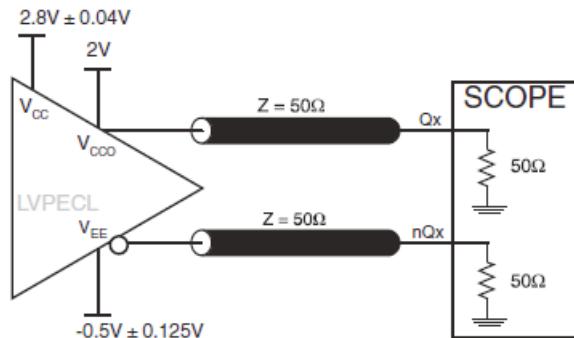
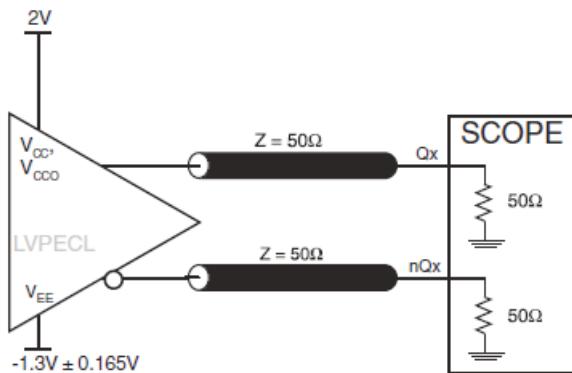
TYPICAL PHASE NOISE AT 375MHz @ 3.3V/2.5V



TYPICAL PHASE NOISE AT 375MHz @ 2.5V/2.5V



PARAMETER MEASUREMENT INFORMATION



APPLICATION INFORMATION

CRYSTAL INPUT INTERFACE

The 843201-375 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in

Figure 1 below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

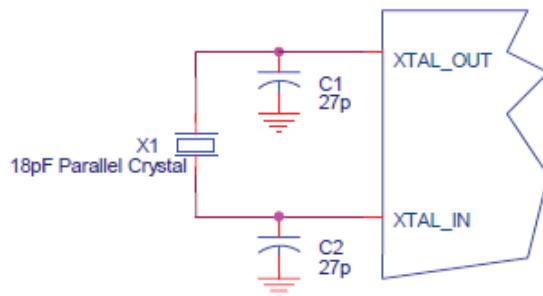


FIGURE 1. CRYSTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT PINS

INPUTS:

LVCMOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

TERMINATION FOR 3.3V LVPECL OUTPUT

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. Figures 2A and 2B show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

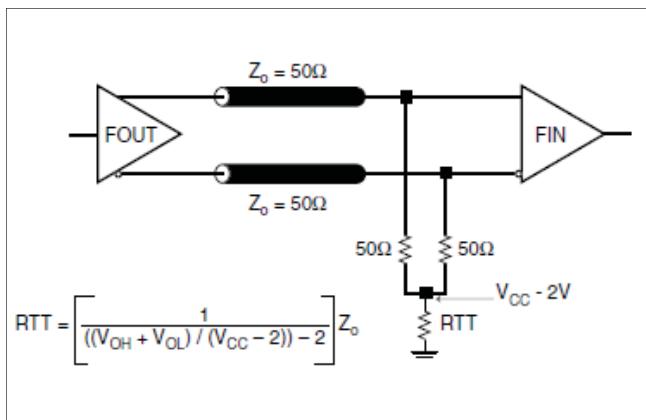


FIGURE 2A. LVPECL OUTPUT TERMINATION

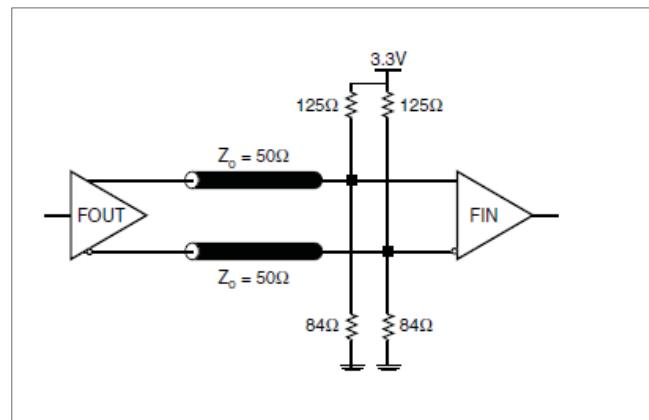


FIGURE 2B. LVPECL OUTPUT TERMINATION

TERMINATION FOR 2.5V LVPECL OUTPUT

Figure 3A and Figure 3B show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to $V_{cc} - 2V$. For $V_{cc} = 2.5V$, the $V_{cc} - 2V$ is

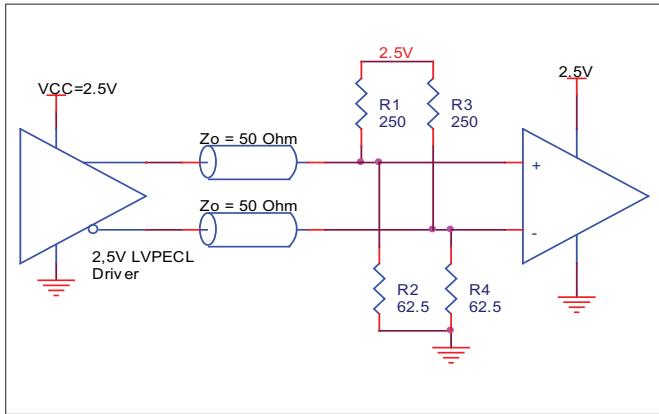


FIGURE 3A. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

very close to ground level. The R3 in Figure 3B can be eliminated and the termination is shown in Figure 3C.

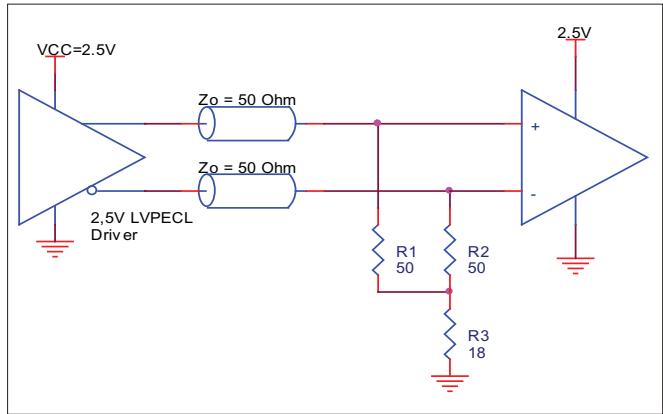


FIGURE 3B. 2.5V LVPECL DRIVER TERMINATION EXAMPLE

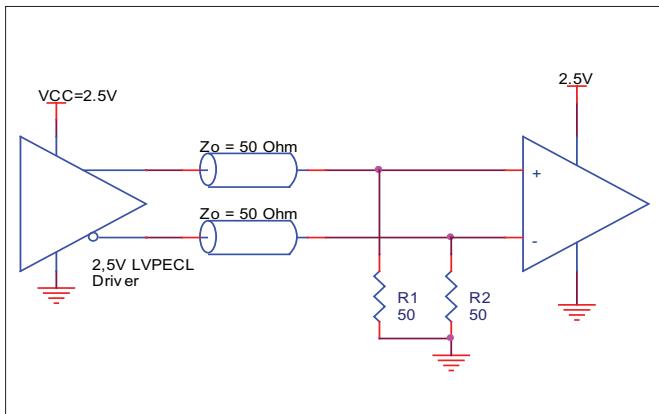


FIGURE 3C. 2.5V LVPECL TERMINATION EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843201-375. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843201-375 is the sum of the core power plus the power dissipated due to loading. The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power (core)_{MAX} = $V_{CC,MAX} * I_{EE,MAX} = 3.465V * 108mA = 374.2mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**

$$\text{Total Power}_{MAX} (3.465V) = 374.2mW + 30mW = \mathbf{404.2mW}$$

2. Junction Temperature.

Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_J , to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_J is as follows: $T_J = \theta_{JA} * P_{d_total} + T_A$

T_J = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

P_{d_total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming 0 air flow and a multi-layer board, the appropriate value is 99.9°C/W per Table 8 below.

Therefore, T_J for an ambient temperature of 70°C with all outputs switching is:

$$70^\circ\text{C} + 0.404\text{W} * 99.9^\circ\text{C/W} = 110^\circ\text{C}. \text{ This is well below the limit of } 125^\circ\text{C.}$$

This calculation is only an example. T_J will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (multi-layer).

TABLE 8. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP, FORCED CONVECTION

| θ_{JA} by Velocity (Linear Feet per Minute) | | | |
|--|----------------------|------------------------|------------------------|
| Multi-Layer PCB, JEDEC Standard Test Boards | 0 99.9°C/W | 200 35.6°C/W | 500 93.5°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5*.

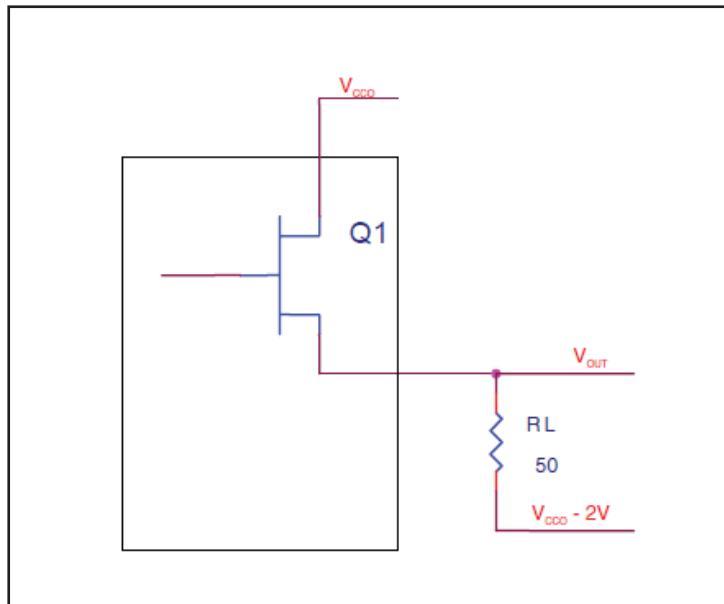


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate power dissipation due to loading, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_{MAX}} = V_{CCO_{MAX}} - 0.9V$

$$(V_{CCO_{MAX}} - V_{OH_{MAX}}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_{MAX}} = V_{CCO_{MAX}} - 1.7V$

$$(V_{CCO_{MAX}} - V_{OL_{MAX}}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_{MAX}} - (V_{CCO_{MAX}} - 2V))/R_L] * (V_{CCO_{MAX}} - V_{OH_{MAX}}) = [(2V - (V_{CCO_{MAX}} - V_{OH_{MAX}}))/R_L] * (V_{CCO_{MAX}} - V_{OH_{MAX}}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_{MAX}} - (V_{CCO_{MAX}} - 2V))/R_L] * (V_{CCO_{MAX}} - V_{OL_{MAX}}) = [(2V - (V_{CCO_{MAX}} - V_{OL_{MAX}}))/R_L] * (V_{CCO_{MAX}} - V_{OL_{MAX}}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair = $Pd_H + Pd_L = 30mW$

RELIABILITY INFORMATION

TABLE 9. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

| Multi-Layer PCB, JEDEC Standard Test Boards | θ_{JA} by Velocity (Linear Feet per Minute) | | |
|---|--|-----------------|-----------------|
| | 0 99.9°C/W | 200 35.6°C/W | 500 93.5°C/W |
| | | | |

TRANSISTOR COUNT

The transistor count for 843201-375 is: 2433

PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP

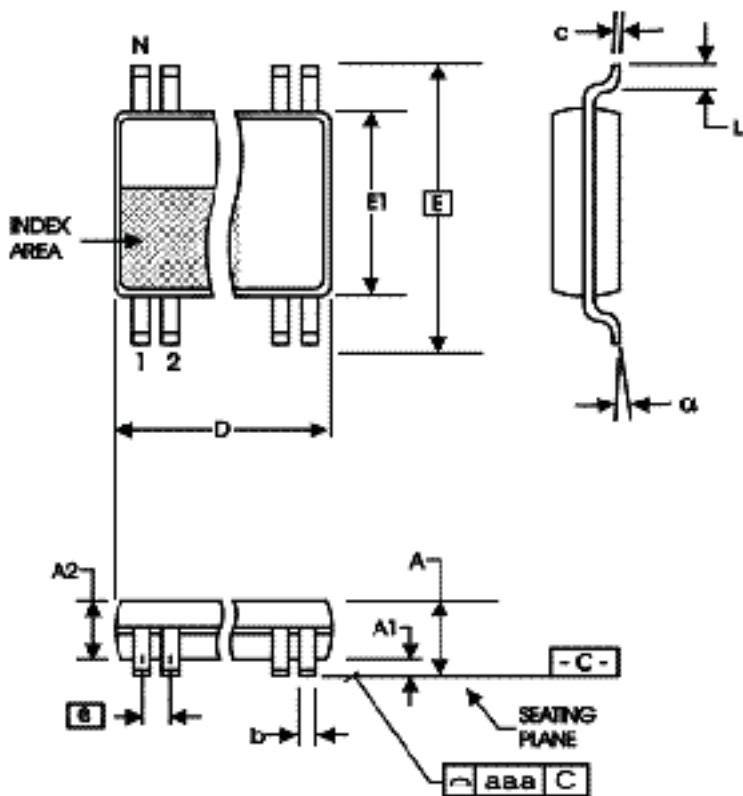


TABLE 10. PACKAGE DIMENSIONS

| SYMBOL | Millimeters | |
|----------|-------------|---------|
| | Minimum | Maximum |
| N | 16 | |
| A | -- | 1.20 |
| A1 | 0.05 | 0.15 |
| A2 | 0.80 | 1.05 |
| b | 0.19 | 0.30 |
| c | 0.09 | 0.20 |
| D | 4.90 | 5.10 |
| E | 6.40 BASIC | |
| E1 | 4.30 | 4.50 |
| e | 0.65 BASIC | |
| L | 0.45 | 0.75 |
| α | 0° | 8° |
| aaa | -- | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

TABLE 11. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|----------|---------------------------|--------------------|-------------|
| 843201AG-375LF | 201A375L | 16 Lead "Lead-Free" TSSOP | tube | 0°C to 70°C |
| 843201AG-375LFT | 201A375L | 16 Lead "Lead-Free" TSSOP | tape & reel | 0°C to 70°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|-----|----------|--------------------|---|---------|
| A | T6 T9 | 1 5 11 17 | Deleted HiPerClockS references. Crystal Characteristics Table - added note. Deleted application note, LVCMOS to XTAL Interface. Deleted quantity from tape and reel. | 4/26/13 |
| A | T11 | 17 | Ordering information - removed leaded devices. Updated data sheet format. | 5/27/15 |
| A | | | Product Discontinuation Notice - Last time buy expires August 14, 2016 PDN CQ-15-04 | 8/21/15 |

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.