

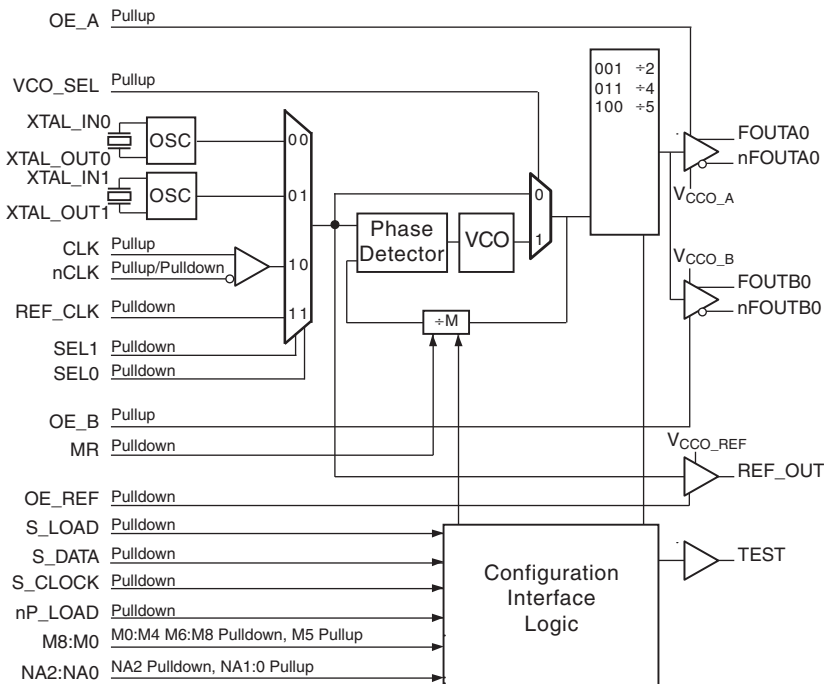
GENERAL DESCRIPTION

The 843034-06 is a general purpose, low phase noise LVPECL synthesizer which can generate frequencies for a wide variety of applications. The 843034-06 has a 4:1 input multiplexer from which the following inputs can be selected: one differential input, one single-ended input, or one of two crystal oscillators, thus making the device ideal for frequency translation or frequency generation. The 843034-06 has dual LVPECL outputs that may be programmed for $\div 2$, $\div 4$ or $\div 5$ of the VCO frequency. The 843034-06 also supplies a buffered copy of the reference clock or crystal frequency on the single-ended REF_OUT pin which can be enabled or disabled (disabled by default). The output frequency can be programmed using either a serial or parallel programming interface. This device supports Spread Spectrum Clocking (SSC) for EMI reduction.

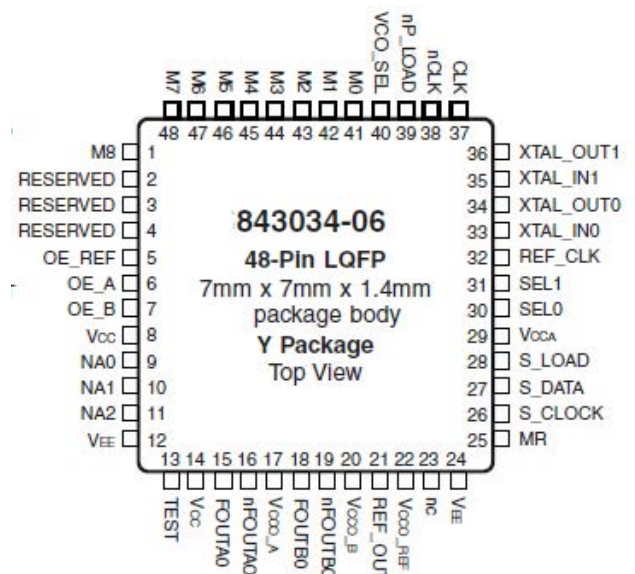
FEATURES

- Dual differential 3.3V LVPECL outputs
- 4:1 Input Mux:
 - One differential input
 - One single-ended input
 - Two crystal oscillator interfaces
- CLK, nCLK pair can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency range: 120MHz to 375MHz
- Crystal input frequency range: 12MHz to 40MHz
- VCO range: 600MHz to 750MHz
- Supports Spread Spectrum Clocking (SSC)
- Parallel or serial interface for programming feedback divider and output dividers
- RMS phase jitter at 166.6MHz, using a 22.222MHz crystal (12kHz to 30MHz): 1.33ps (typical), SSC - Off
- 3.3V supply mode
- 0°C to 75°C ambient operating temperature
- Available in lead-free (RoHS 6) package

BLOCK DIAGRAM



PIN ASSIGNMENT



FUNCTIONAL DESCRIPTION

NOTE: The functional description that follows describes operation using a 22.22MHz crystal. Valid PLL loop divider values for different crystal or input frequencies are defined in the Input Frequency Characteristics, Table 6, NOTE 1.

The 843034-06 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is fed into the phase detector. A 22.22MHz crystal provides a 22.22MHz phase detector reference frequency. The VCO of the PLL operates over a range of 600MHz to 750MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to each of the LVPECL output buffers. The divider provides a 50% output duty cycle.

The 843034-06 supports either serial or parallel programming modes to program the M feedback divider and N output divider. *Figure 1* shows the timing diagram for each mode. In parallel mode, the nP_LOAD input is initially LOW. The data on the M and NA inputs are passed directly to the M divider and N output dividers. On the LOW-to-HIGH transition of the nP_LOAD input, the data is latched and the M and N dividers remain loaded until the next LOW transition on nP_LOAD or until a serial event occurs. As a result, the M and NA bits can be hardwired to set the M divider and NA output divider to a specific default state that

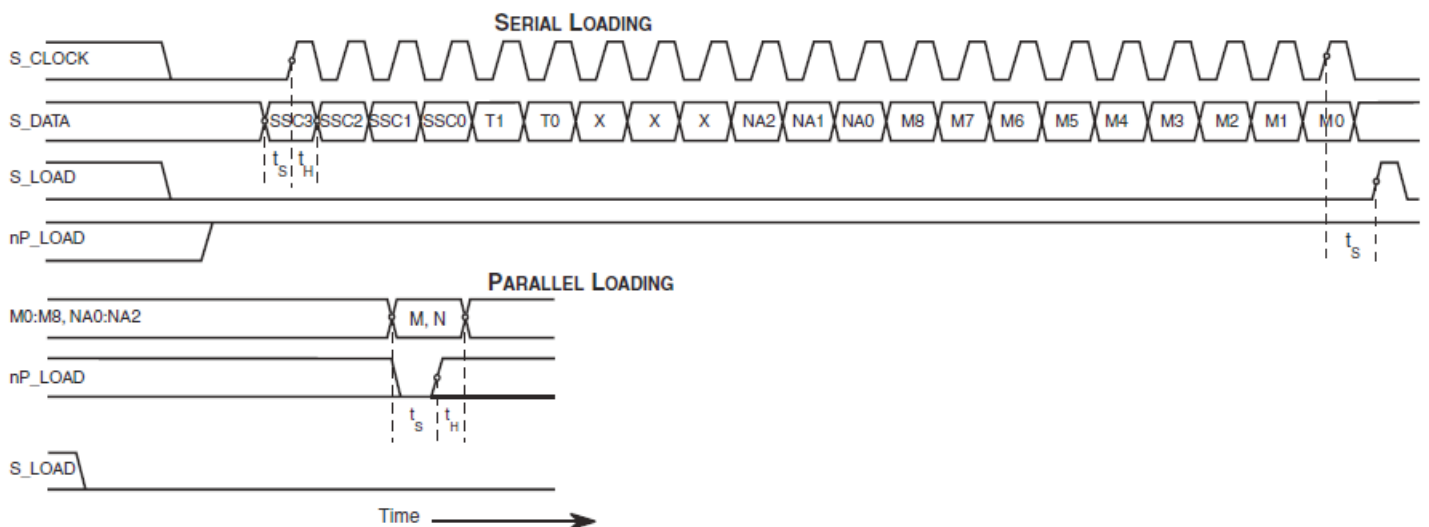
will automatically occur during power-up. The TEST output is LOW when operating in the parallel input mode. The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows: **$f_{VCO} = f_{xtal} \times M$**

The M value and the required values of M0 through M8 are shown in Table 4B to program the VCO Frequency Function Table. Valid M values for which the PLL will achieve lock for a 22.22MHz reference are defined as $26 \leq M \leq 33$. The frequency out is defined as follows:

$$FOUT = \frac{f_{VCO}}{N} = \frac{f_{xtal} \times M}{N}$$

Serial operation occurs when nP_LOAD is HIGH and S_LOAD is LOW. The shift register is loaded by sampling the S_DATA bits with the rising edge of S_CLOCK. The contents of the shift register are loaded into the M divider and NA output divider when S_LOAD transitions from LOW-to-HIGH. The M divide and NA output divide values are latched on the HIGH-to-LOW transition of S_LOAD. If S_LOAD is held HIGH, data at the S_DATA input is passed directly to the M divider and NA output divider on each rising edge of S_CLOCK. The serial mode can be used to program the M and NA bits and test bits T1 and T0. The internal registers T0 and T1 determine the state of the TEST output as follows:

| T1 | T0 | TEST Output |
|----|----|-------------------------------|
| 0 | 0 | LOW |
| 0 | 1 | S_Data, Shift Register Output |
| 1 | 0 | Output of M divider |
| 1 | 1 | Same frequency as FOUTA0 |



NOTE: X = Don't Care

FIGURE 1. PARALLEL & SERIAL LOAD OPERATIONS

TABLE 1. SSM OPERATION

| SS Bit Pattern | | | | Operation | |
|----------------|-----|-----|-----|-----------|------------|
| SS3 | SS2 | SS1 | SS0 | Mode | % |
| 0 | 0 | 0 | 0 | off | 0 |
| 0 | 0 | 0 | 1 | center | ± 0.25 |
| 0 | 0 | 1 | 0 | center | ± 0.25 |
| 0 | 0 | 1 | 1 | center | ± 0.85 |
| 0 | 1 | 0 | 0 | center | ± 0.85 |
| 0 | 1 | 0 | 1 | center | ± 1.45 |
| 0 | 1 | 1 | 0 | center | ± 1.45 |
| 0 | 1 | 1 | 1 | center | ± 1.7 |
| 1 | 0 | 0 | 0 | off | 0 |
| 1 | 0 | 0 | 1 | down | -0.25 |
| 1 | 0 | 1 | 0 | down | -0.25 |
| 1 | 0 | 1 | 1 | down | -0.75 |
| 1 | 1 | 0 | 0 | down | -0.75 |
| 1 | 1 | 0 | 1 | down | -1.25 |
| 1 | 1 | 1 | 0 | down | -1.25 |
| 1 | 1 | 1 | 1 | down | -1.5 |

NOTE: SS modulation frequency is approximately 32kHz using reference frequency of 22.22MHz, providing a VCO frequency of 666.66MHz.

SPREAD SPECTRUM MODULATION

The 843034-06 offers the option of a spread spectrum modulated output clock. The spread spectrum is controlled via 4 bits in the serial bit stream. These four bits configure the SSM to be enabled and the amount of spread modulation to be selected. See *Table 1* for the definition of the four bits. The four bits are added at the beginning of the serial data stream and are labeled SS3, SS2, SS1

and SS0. The initial state of SS3, SS2, SS1 and SS0 is 0, 0, 0, 0 which places the 843034-06 in the mode of spread spectrum off. Additionally, a parallel load will result in spread spectrum modulation being off. The 843034-06 offers down-spread or center-spread using triangle-wave modulation. NOTE: PLL operation not guaranteed for $M > 31$ when using center spread.

POWER-UP OPERATION

The 843034-06 has internal power-up reset circuitry that initiates the phase lock loop to automatically acquire lock on power-up. On power-up the M/N values for the feedback and output dividers will be acquired from the M and N pins if nP_Load is held Low. If nP_Load is High during power-up, M/N values are indeterminate. The M/N values may be changed by either changing the values on the M/N pins when nP_LOAD is low or with a serial load when nP_LOAD is high and S_LOAD is low.

MR PIN OPERATION

Any time there is a change in the input frequency, either due to an external change or a change in the SEL pins, the MR pin must go high and low to relock to the new input frequency. A change in the M feedback divider by either a serial or parallel load will also cause a relock to the new input frequency.

TABLE 2. PIN DESCRIPTIONS

| Number | Name | Type | | Description |
|-------------------------------------|--------------------------------------|---------|----------|--|
| 1, 41, 42, 43, 44, 45, 47, 48 | M8, M0, M1, M2, M3, M4, M6, M7 | Input | Pulldown | M divider input. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels. |
| 2, 3, 4 | RESERVED | Reserve | | Reserved pins. Do not connect. |
| 5 | OE_REF | Input | Pulldown | Output enable. Controls enabling and disabling of REF_OUT output. LVCMOS/LVTTL interface levels. |
| 6 | OE_A | Input | Pullup | Output enable. Controls enabling and disabling of FOUTA0, nFOUTA0 outputs. LVCMOS/LVTTL interface levels. |
| 7 | OE_B | Input | Pullup | Output enable. Controls enabling and disabling of FOUTB0, nFOUTB0 outputs. LVCMOS/LVTTL interface levels. |
| 8, 14 | V _{CC} | Power | | Core supply pins. |
| 9, 10 | NA0, NA1 | Input | Pullup | Determines output divider value as defined in Table 4C, Function Table. LVCMOS/LVTTL interface levels. |
| 11 | NA2 | Input | Pulldown | |
| 12, 24 | V _{EE} | Power | | Negative supply pins. |
| 13 | TEST | Output | | Test output which is ACTIVE in the serial mode of operation. Output driven LOW in parallel mode. LVCMOS/LVTTL interface levels. |
| 15, 16 | FOUTA0, nFOU- TA0 | Output | | Differential output for the synthesizer. LVPECL interface levels. |
| 17 | V _{CCO_A} | Power | | Output supply pin for FOUTA0, nFOUTA0. |
| 18, 19 | FOUTB0, nFOUTB0 | Output | | Differential output for the synthesizer. LVPECL interface levels. |
| 20 | V _{CCO_B} | Power | | Output supply pin for FOUTB0, nFOUTB0. |
| 21 | REF_OUT | Output | | Reference clock output. LVCMOS/LVTTL interface levels. |
| 22 | V _{CCO_REF} | Power | | Output supply pin for REF_OUT output. |
| 23 | nc | Unused | | No connect. |
| 25 | MR | Input | Pulldown | Active High Master Reset. When logic HIGH, forces the internal PLL to a reset condition which holds the VCO at the minimum value. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not affect loaded M, N, S and T values. LVCMOS/LVTTL interface levels. |
| 26 | S_CLOCK | Input | Pulldown | Clocks in serial data present at S_DATA input into the shift register on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels. |
| 27 | S_DATA | Input | Pulldown | Shift register serial input. Data sampled on the rising edge of S_CLOCK. LVCMOS/LVTTL interface levels. |
| 28 | S_LOAD | Input | Pulldown | Controls transition of data from shift register into the dividers. LVCMOS/LVTTL interface levels. |
| 29 | V _{CCA} | Power | | Analog supply pin. |
| 30, 31 | SEL0, SEL1 | Input | Pulldown | Clock select inputs. LVCMOS/LVTTL interface levels. |
| 32 | REF_CLK | Input | Pulldown | Reference clock input. LVCMOS/LVTTL interface levels. |
| 33, 34 | XTAL_IN0, XTAL_OUT0 | Input | | Crystal oscillator interface. XTAL_IN0 is the input, XTAL_OUT0 is the output. |
| 35, 36 | XTAL_IN1, XTAL_OUT1 | Input | | Crystal oscillator interface. XTAL_IN1 is the input, XTAL_OUT1 is the output. |

Continued on next page...

TABLE 2. PIN DESCRIPTIONS, CONTINUED

| Number | Name | Type | | Description |
|--------|---------|-------|---------------------|--|
| 37 | CLK | Input | Pulldown | Non-inverting differential clock input. |
| 38 | nCLK | Input | Pullup/ Pulldown | Inverting differential clock input. $V_{cc}/2$ default when left floating. |
| 39 | nP_LOAD | Input | Pulldown | Parallel load input. Determines when data present at M8:M0 is loaded into M divider, and when data present at NA2:NA0 is loaded into the N output dividers. LVCMOS/LVTTL interface levels. |
| 40 | VCO_SEL | Input | Pullup | Determines whether synthesizer is in PLL or bypass mode. LVCMOS/LVTTL interface levels. |
| 46 | M5 | Input | Pullup | M divider input. Data latched on LOW-to-HIGH transition of nP_LOAD input. LVCMOS/LVTTL interface levels. |

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 3, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|----------------|-------------------------|---------|-----------------|---------|---------|---------|------------|
| C_{IN} | Input Capacitance | | | | 4 | | pF |
| R_{PULLUP} | Input Pullup Resistor | | | | 51 | | k Ω |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | | 51 | | k Ω |
| R_{OUT} | Output Impedance | REF_OUT | | 5 | 7 | 12 | Ω |

TABLE 4A. PARALLEL AND SERIAL MODE FUNCTION TABLE

| Inputs | | | | | | | Conditions |
|--------|---------|------|------|--------|---------|--------|---|
| MR | nP_LOAD | M | N | S_LOAD | S_CLOCK | S_DATA | |
| H | X | X | X | X | X | X | Reset the PLL. |
| L | L | Data | Data | X | X | X | Data on M and N inputs passed directly to the M divider and N output divider. TEST output forced LOW. |
| L | ↑ | Data | Data | L | X | X | Data is latched into input registers and remains loaded until next LOW transition or until a serial event occurs. |
| L | H | X | X | L | ↑ | Data | Serial input mode. Shift register is loaded with data on S_DATA on each rising edge of S_CLOCK. |
| L | H | X | X | ↑ | L | Data | Contents of the shift register are passed to the M divider and N output divider. |
| L | H | X | X | ↓ | L | Data | M divider and N output divider values are latched. |
| L | H | X | X | L | X | X | Parallel or serial input do not affect shift registers. |
| L | H | X | X | H | ↑ | Data | S_DATA passed directly to M divider as it is clocked. |

NOTE: L = LOW
H = HIGH
X = Don't care
↑ = Rising edge transition
↓ = Falling edge transition

TABLE 4B. PROGRAMMABLE VCO FREQUENCY FUNCTION TABLE

| VCO Frequency (MHz) | M Divide | 256 | 128 | 64 | 32 | 16 | 8 | 4 | 2 | 1 |
|---------------------|----------|-----|-----|----|----|----|----|----|----|----|
| | | M8 | M7 | M6 | M5 | M4 | M3 | M2 | M1 | M0 |
| 600 | 27 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| • | • | • | • | • | • | • | • | • | • | • |
| 666.6 | 30 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| • | • | • | • | • | • | • | • | • | • | • |
| 711.04 (default) | 32 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 733.3 | 33 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |

NOTE 1: These M divide values and the resulting frequencies correspond to crystal, CLK, or REF_CLK input frequency of 22.22MHz.

TABLE 4C. PROGRAMMABLE OUTPUT DIVIDER FUNCTION TABLE

| Inputs | | | N Divider Value | Output Frequency (MHz) | |
|--------|------|------|-----------------|------------------------|-----------------|
| *NA2 | *NA1 | *NA0 | | Minimum | Maximum |
| 0 | 0 | 1 | 2 | 300 | 375 |
| 0 | 1 | 1 | 4 | 150 | 187.5 (default) |
| 1 | 0 | 0 | 5 | 120 | 150 |

*NOTE: Programming for Bank A and Bank B.

ABSOLUTE MAXIMUM RATINGS

| | |
|--|---------------------------|
| Supply Voltage, V_{CC} | 4.6V |
| Inputs, V_I | -0.5V to $V_{CC} + 0.5V$ |
| Outputs, V_O (LVCMOS) | -0.5V to $V_{CCO} + 0.5V$ |
| Outputs, I_O (LVPECL) | |
| Continuous Current | 50mA |
| Surge Current | 100mA |
| Package Thermal Impedance, θ_{JA} | 65.7°C/W (0 mps) |
| Storage Temperature, T_{STG} | -65°C to 150°C |

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = V_{CCO_REF} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ TO $75^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|--|-----------------------|-----------------|-----------------|---------|----------|-------|
| V_{CC} | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| V_{CCA} | Analog Supply Voltage | | $V_{CC} - 0.17$ | 3.3 | V_{CC} | V |
| V_{CCO_A} V_{CCO_B} V_{CCO_REF} | Output Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{EE} | Power Supply Current | | | | 173 | mA |
| I_{CCA} | Analog Supply Current | | | | 17 | mA |

TABLE 5B. LVCMOS/LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO_REF} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ TO $75^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|---------------------|---|---------|---------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{CC} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | REF_CLK, MR, SEL[1:0], OE_REF, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, NA2, M1:M4, M6:M8 $V_{CC} = V_{IN} = 3.465V$ | | | 150 | μA |
| | | OE_A, M5, OE_B, VCO_SEL, NA0, NA1 $V_{CC} = V_{IN} = 3.465V$ | | | 5 | μA |
| I_{IL} | Input Low Current | REF_CLK, MR, SEL[1:0], OE_REF, S_CLOCK, S_DATA, S_LOAD, nP_LOAD, NA2, M1:M4, M6:M8 $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -5 | | | μA |
| | | OE_A, M5, OE_B, VCO_SEL, NA0, NA1 $V_{CC} = 3.465V$, $V_{IN} = 0V$ | -150 | | | μA |
| V_{OH} | Output High Voltage | TEST; NOTE 1 $V_{CCO_REF} = 3.3V \pm 5\%$ | 2.6 | | | V |
| | | REF_OUT $V_{CCO_REF} - 0.3V$ | | | | V |
| V_{OL} | Output Low Voltage | TEST; NOTE 1 $V_{CCO_REF} = 3.3V \pm 5\%$ | | | 0.5 | V |
| | | REF_OUT | | | 0.4 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_REF}/2$. See *Parameter Measurement Information Section*, "Output Load Test Circuit Diagrams."

TABLE 5C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ TO $75^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-----------|--------------------------------------|-----------------|--------------------------------|---------|-----------------|---------|
| I_{IH} | Input High Current | nCLK | $V_{IN} = V_{CC} = 3.465V$ | | 150 | μA |
| | | CLK | $V_{IN} = V_{CC} = 3.465V$ | | 150 | μA |
| I_{IL} | Input Low Current | nCLK | $V_{IN} = 0V, V_{CC} = 3.465V$ | -150 | | μA |
| | | CLK | $V_{IN} = 0V, V_{CC} = 3.465V$ | -5 | | μA |
| V_{PP} | Peak-to-Peak Input Voltage; NOTE 1 | | 0.15 | | 1.3 | V |
| V_{CMR} | Common Mode Input Voltage; NOTE 1, 2 | | $V_{EE} + 0.5$ | | $V_{CC} - 0.85$ | V |

NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 5D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ TO $75^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|-------------|-----------------------------------|-----------------|-----------------|---------|-----------------|-------|
| V_{OH} | Output High Voltage; NOTE 1 | | $V_{CCO} - 1.4$ | | $V_{CCO} - 0.9$ | V |
| V_{OL} | Output Low Voltage; NOTE 1 | | $V_{CCO} - 2.0$ | | $V_{CCO} - 1.7$ | V |
| V_{SWING} | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CCO_A}, V_{CCO_B} - 2V$.

TABLE 6. INPUT FREQUENCY CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = V_{CCO_REF} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ TO $75^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|----------|-----------------|---|---------|---------|---------|-------|
| f_{IN} | Input Frequency | XTAL_IN0/XTAL_OUT0, XTAL_IN1/XTAL_OUT1 | 12 | | 40 | MHz |
| | | CLK/nCLK, REF_CLK | 12 | | 40 | MHz |
| | | S_CLOCK | | | 50 | MHz |

NOTE: For the input crystal, CLK/nCLK and REF_CLK frequency range, the M value must be set for the VCO to operate within the 600MHz to 750MHz range. Using the minimum input frequency of 12MHz, valid values of M are $50 \leq M \leq 62$. Using the maximum frequency of 40MHz, valid values of M are $15 \leq M \leq 18$.

TABLE 7. CRYSTAL CHARACTERISTICS

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|------------------------------------|-----------------|-------------|---------|---------|----------|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 12 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |

TABLE 8. AC CHARACTERISTICS, $V_{CC} = V_{CCO_A} = V_{CCO_B} = V_{CCO_REF} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = 0^\circ C$ TO $75^\circ C$

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---------------------|--|--|---------|---------|---------|-------|
| FOUT | Output Frequency | | 120 | | 375 | MHz |
| tjit(\emptyset) | Phase Jitter, RMS (Random), SSC-Off NOTE 1, 2 | 166.6MHz, Integration Range: 12kHz - 30MHz | | 1.33 | | ps |
| tjit(cc) | Cycle-to-Cycle Jitter; NOTE 2, 3, 4 | | | | 35 | ps |
| tsk(o) | Output Skew; NOTE 2, 4, 5 | | | | 120 | ps |
| tR / tF | Output Rise/Fall Time | LVPECL Outputs 20% to 80% | 200 | | 700 | ps |
| tS | Setup Time | M, N to nP_LOAD | 5 | | | ns |
| | | S_DATA to S_CLOCK | 5 | | | ns |
| | | S_CLOCK to S_LOAD | 5 | | | ns |
| tH | Hold Time | M, N to nP_LOAD | 5 | | | ns |
| | | S_DATA to S_CLOCK | 5 | | | ns |
| | | S_CLOCK to S_LOAD | 5 | | | ns |
| odc | Output Duty Cycle | N = 4 or N = 5 | 48 | | 52 | % |
| | | N = 2 | 45 | | 55 | % |
| tLOCK | PLL Lock Time | | | | 100 | ms |

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditons."

NOTE: Characterized using a 22.22MHz crystal producing a VCO frequency of 666.66MHz, unless otherwise noted.

NOTE: See Parameter Measurement Information section.

NOTE 1: Please refer to the Phase Noise Plot.

NOTE 2: Characterized with REF_OUT output disabled.

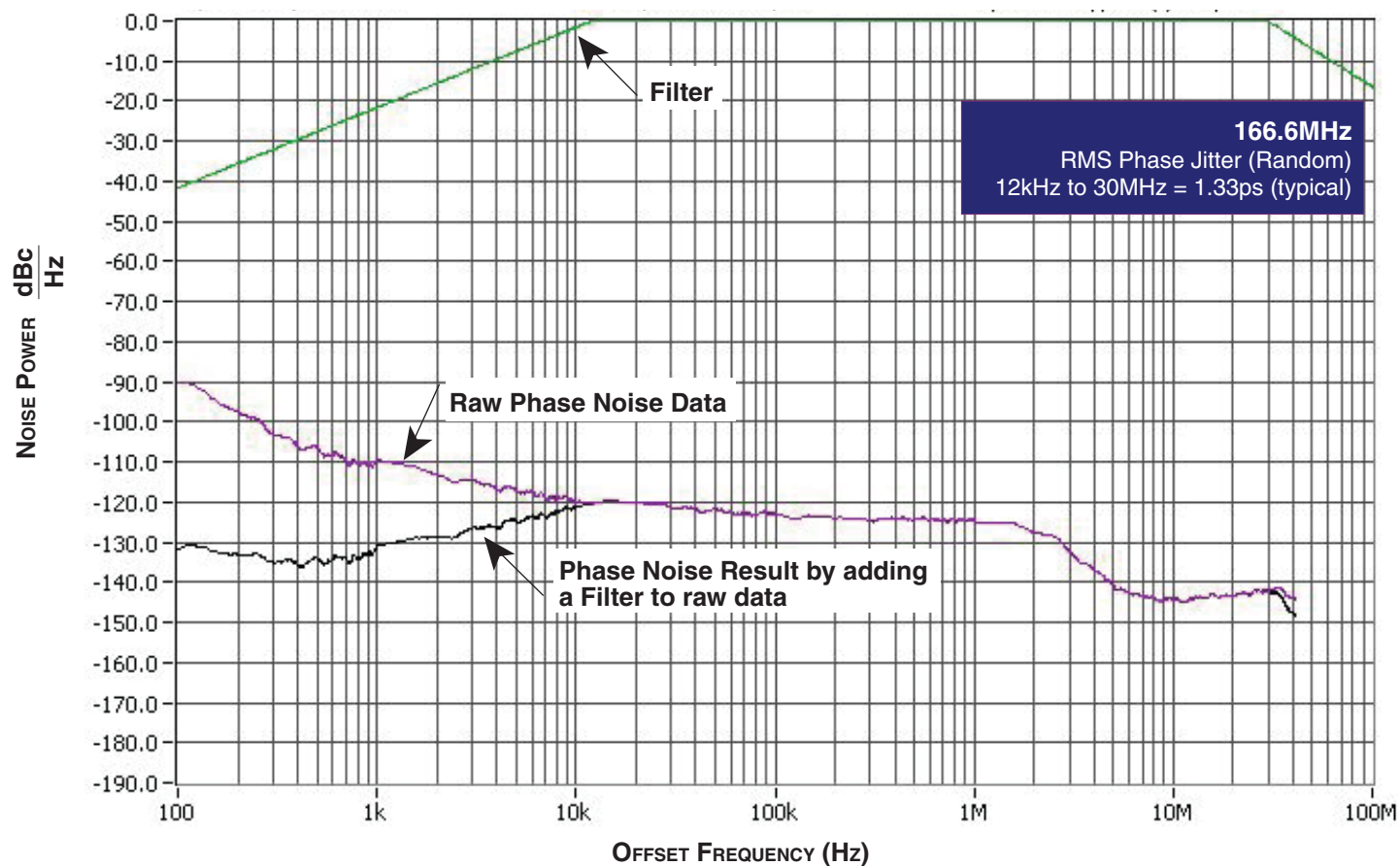
NOTE 3: Jitter performance using XTAL inputs.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

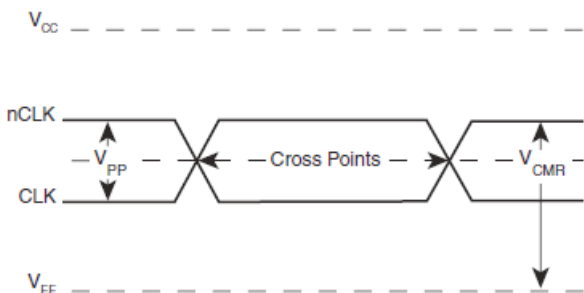
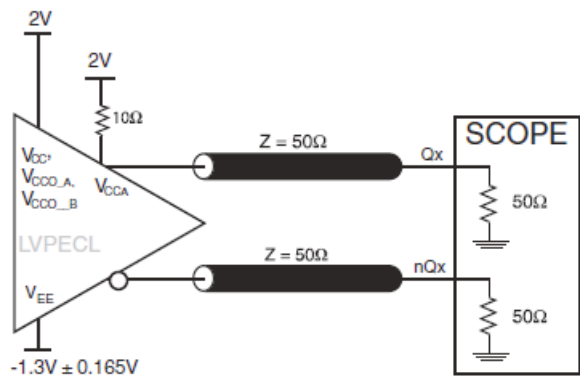
NOTE 5: Defined as skew between outputs at the same supply voltage and with equal load conditions.

Measured at the output differential cross points.

TYPICAL PHASE NOISE AT 166.6MHz

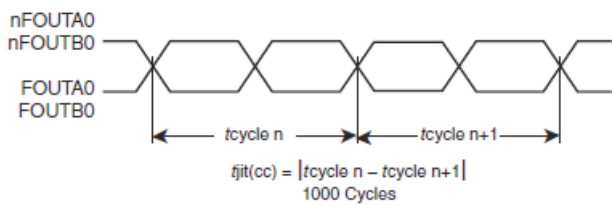
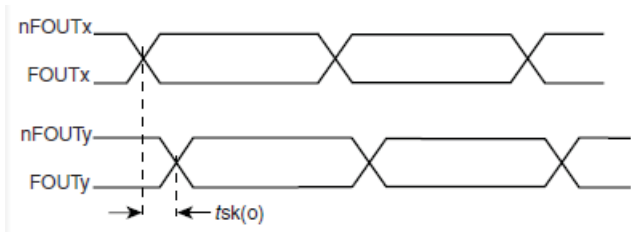


PARAMETER MEASUREMENT INFORMATION



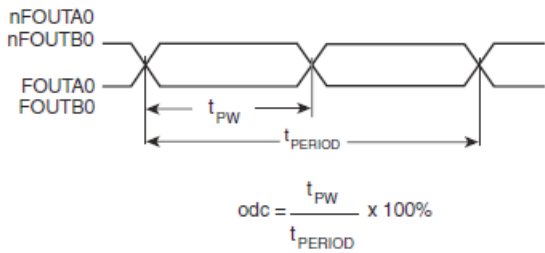
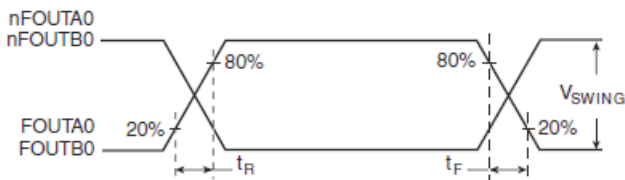
3.3V LVPECL OUTPUT LOAD AC TEST CIRCUIT

DIFFERENTIAL INPUT LEVELS



OUTPUT SKEW

CYCLE-TO-CYCLE JITTER



OUTPUT RISE/FALL TIME

OUTPUT DUTY CYCLE/OUTPUT PULSE WIDTH/PERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 843034-06 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCA} and V_{CCO_X} should be individually connected to the power supply plane through vias, and $0.01\mu\text{F}$ bypass capacitors should be used for each pin. Figure 2 illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a $10\mu\text{F}$ bypass capacitor be connected to the V_{CCA} pin.

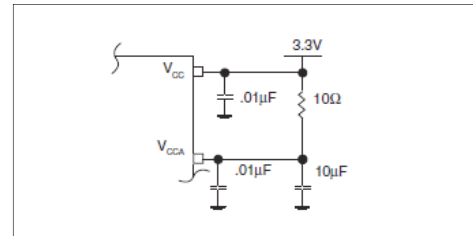


FIGURE 2. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LVCMOS/LVTTL LEVELS

Figure 3 shows how the differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors $R1$, $R2$ and $C1$. This bias circuit should be located as close as possible to the input pin. The ratio

of $R1$ and $R2$ might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and $V_{CC} = 3.3\text{V}$, V_{REF} should be 1.25V and $R2/R1 = 0.609$.

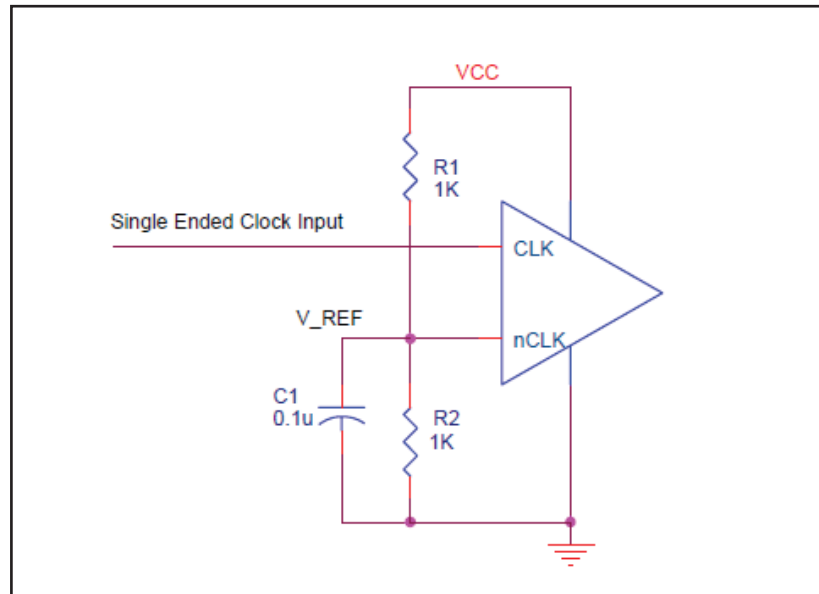


FIGURE 3. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 4A to 4F show interface examples for the HiPerClockS CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only.

Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in Figure 4A, the input termination applies for IDT HiPerClockS open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

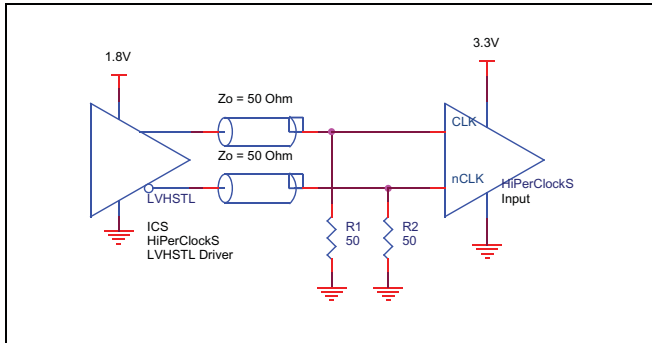


FIGURE 4A. HiPerClockS CLK/nCLK INPUT DRIVEN BY AN IDT OPEN EMITTER HiPerClockS LVHSTL DRIVER

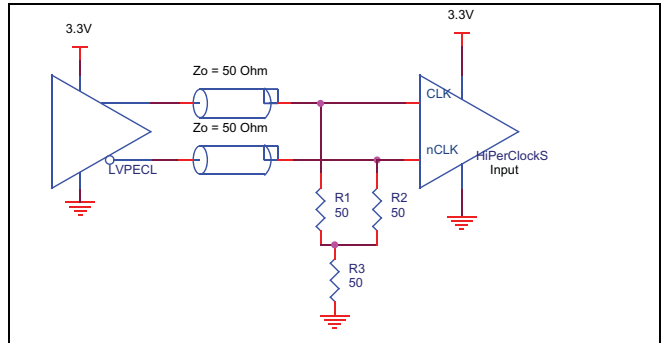


FIGURE 4B. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

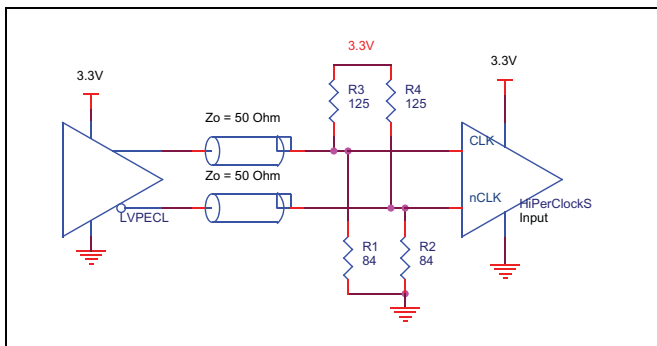


FIGURE 4C. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

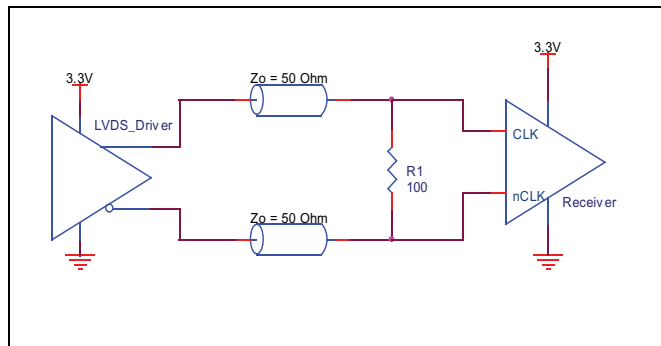


FIGURE 4D. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

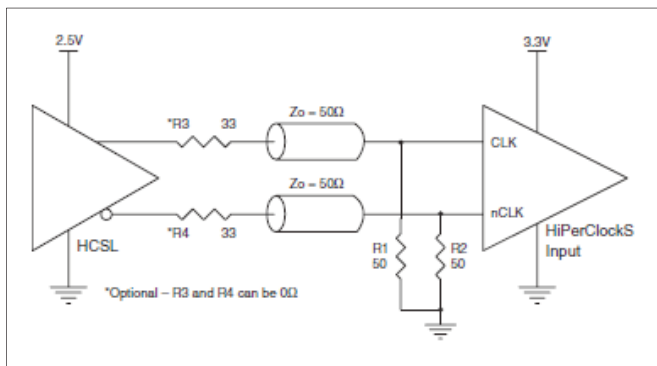


FIGURE 4E. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 3.3V HCSL DRIVER

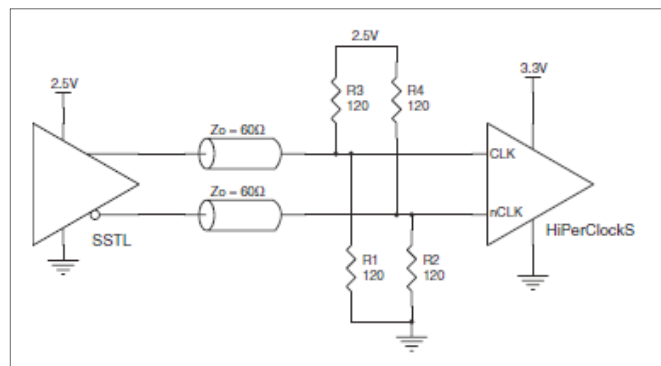


FIGURE 4F. HiPerClockS CLK/nCLK INPUT DRIVEN BY A 2.5V SSTL DRIVER

CRYSTAL INPUT INTERFACE

The 843034-06 has been characterized with 18pF parallel resonant crystals. The capacitor values, C1 and C2, shown in *Figure 5* below were determined using a 18pF parallel resonant crystal and were

chosen to minimize the ppm error. The optimum C1 and C2 values can be slightly adjusted for different board layouts.

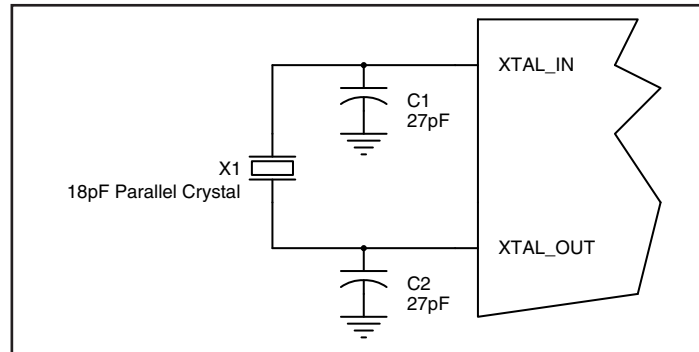


FIGURE 5. CRYSTAL INPUT INTERFACE

LVC MOS TO XTAL INTERFACE

The XTAL_IN input can accept a single-ended LVC MOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 6*. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVC MOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output

impedance of the driver (R_o) plus the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R_1 and R_2 in parallel should equal the transmission line impedance. For most 50Ω applications, R_1 and R_2 can be 100Ω. This can also be accomplished by removing R_1 and making R_2 50Ω.

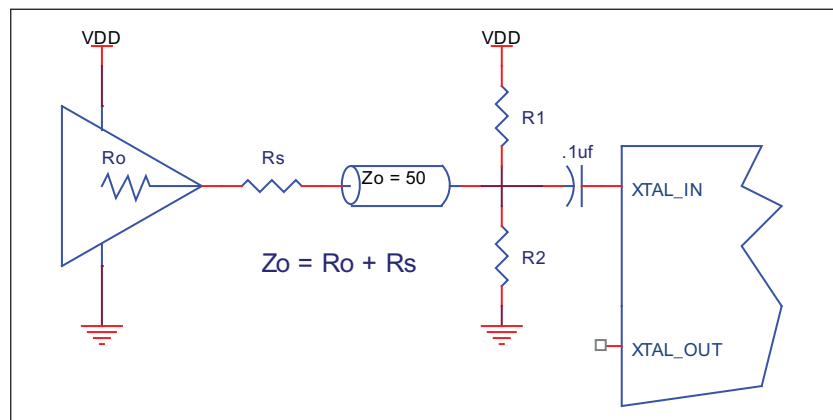


FIGURE 6. GENERAL DIAGRAM FOR LVC MOS DRIVER TO XTAL INPUT INTERFACE

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CRYSTAL INPUTS

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

REF_CLK INPUT

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVC MOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVC MOS OUTPUTS

The unused LVC MOS output can be left floating. We recommend that there is no trace attached.

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used

to maximize operating frequency and minimize signal distortion. *Figures 7A and 7B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

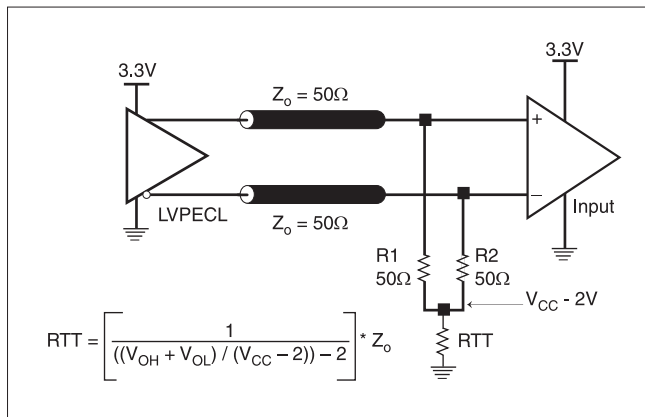


FIGURE 7A. LVPECL OUTPUT TERMINATION

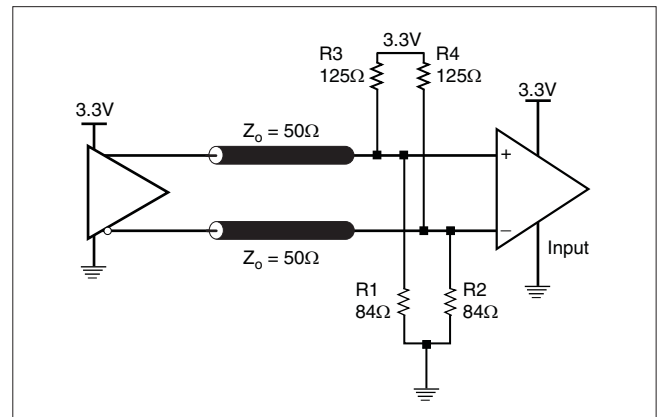


FIGURE 7B. LVPECL OUTPUT TERMINATION

APPLICATION SCHEMATIC EXAMPLE

Figure 8 shows an example of 843034-06 application schematic. In this example, the device is operated at $V_{CC}=V_{CCO}=3.3V$. The device are be driven by a crystal, LVCMOS or LVPECL input sources. The 18pF parallel resonant 25MHz crystal is used. The $C1 = 27pF$ and $C2 = 27pF$ are recommended for frequency accuracy. For different

board layout, the $C1$ and $C2$ may be slightly adjusted for optimizing frequency accuracy. For the LVPECL output drivers, only two termination examples are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

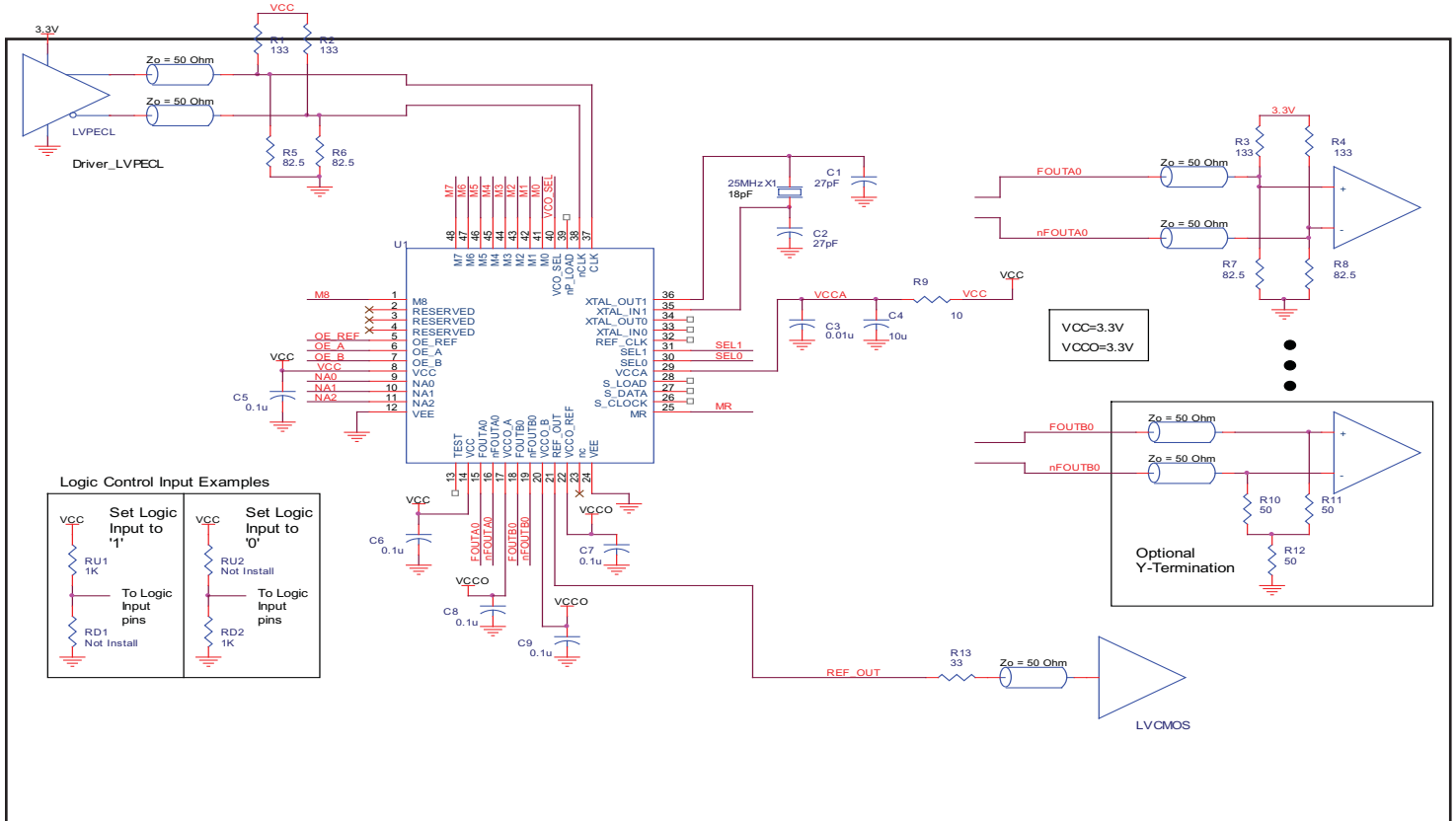


FIGURE 8. 843034-06 APPLICATION SCHEMATIC EXAMPLE

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the 843034-06. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 843034-06 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

Core and LVPECL Output Power Dissipation

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 173mA = 599.45mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30mW = 60mW$

LVC MOS Output Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to $V_{CCO_REF}/2$
Output Current $I_{OUT} = V_{CCO_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 7\Omega)] = 30.4mA$
- Power Dissipation on the R_{OUT} per LVC MOS output
 $Power (R_{OUT}) = R_{OUT} * (I_{OUT})^2 = 7\Omega * (30.4mA)^2 = 6.97mW \text{ per output}$

Total Power Dissipation

- Total Power**
= Power (LVPECL) + Power (R_{OUT})
= $599.45mW + 60mW + 6.47mW$
= **665.92mW**

2. Junction Temperature.

Junction temperature, T_j , is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for devices is 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 65.7°C/W per Table 9 below.

Therefore, T_j for an ambient temperature of 75°C with all outputs switching is:

$75^\circ\text{C} + 0.666\text{W} * 65.7^\circ\text{C/W} = 118^\circ\text{C}$. This is below the limit of 125°C.

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 9. THERMAL RESISTANCE θ_{JA} FOR 48-PIN LQFP, FORCED CONVECTION

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 65.7°C/W | 55.9°C/W | 52.4°C/W |

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 9*.

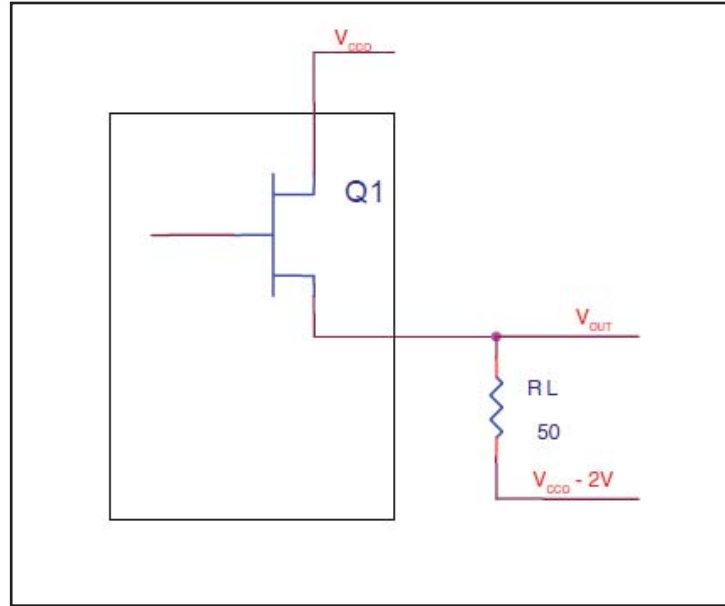


FIGURE 9. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CCO} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CCO_MAX} - 0.9V$

$$(V_{CCO_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CCO_MAX} - 1.7V$

$$(V_{CCO_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - (V_{CCO_MAX} - V_{OH_MAX}))/R_L] * (V_{CCO_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CCO_MAX} - 2V))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - (V_{CCO_MAX} - V_{OL_MAX}))/R_L] * (V_{CCO_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

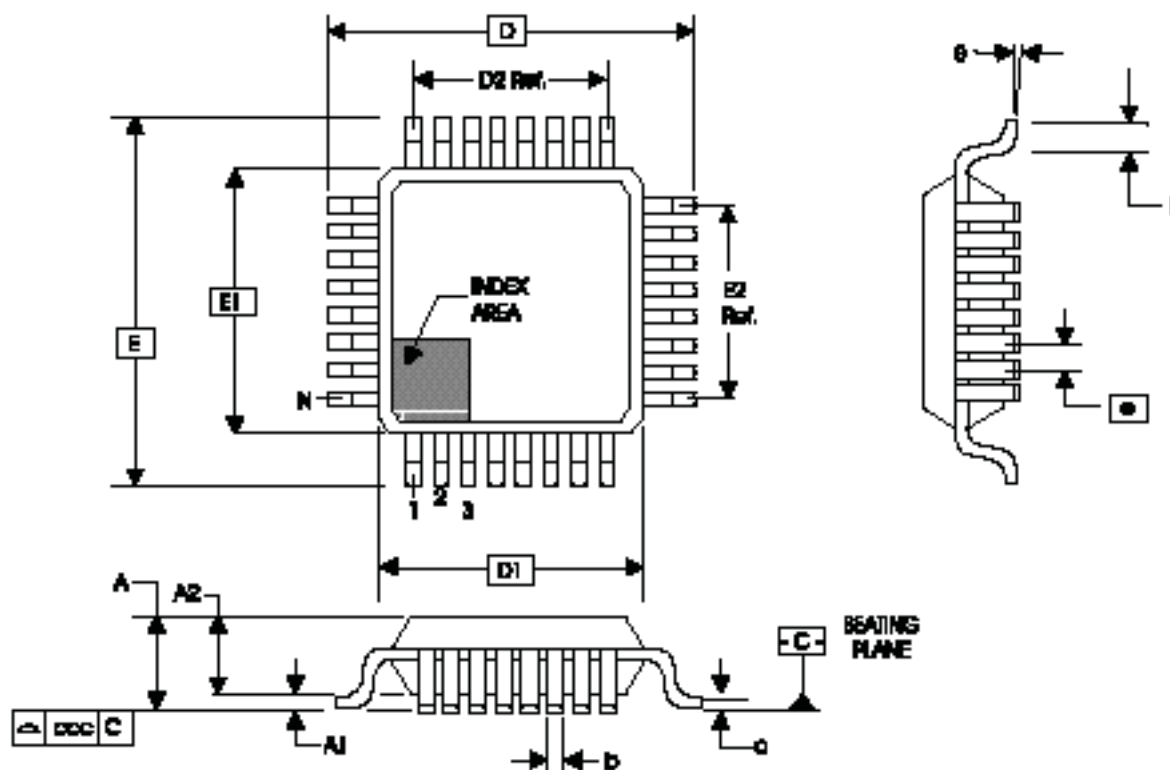
RELIABILITY INFORMATION

TABLE 10. θ_{JA} VS. AIR FLOW TABLE FOR 48 LEAD LQFP

| θ_{JA} by Velocity (Meters per Second) | | | |
|---|----------|----------|----------|
| | 0 | 1 | 2.5 |
| Multi-Layer PCB, JEDEC Standard Test Boards | 65.7°C/W | 55.9°C/W | 52.4°C/W |

TRANSISTOR COUNT

The transistor count for 843034-06 is: 7846

PACKAGE OUTLINE - Y SUFFIX FOR 48 LEAD LQFP

TABLE 11. PACKAGE DIMENSIONS

| JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS | | | |
|--|------------|---------|---------|
| SYMBOL | BBC | | |
| | MINIMUM | NOMINAL | MAXIMUM |
| N | 48 | | |
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | -- | 0.20 |
| D | 9.00 BASIC | | |
| D1 | 7.00 BASIC | | |
| D2 | 5.50 Ref. | | |
| E | 9.00 BASIC | | |
| E1 | 7.00 BASIC | | |
| E2 | 5.50 Ref. | | |
| e | 0.50 BASIC | | |
| L | 0.45 | 0.60 | 0.75 |
| θ | 0° | -- | 7° |
| ccc | -- | -- | 0.08 |

Reference Document: JEDEC Publication 95, MS-026

TABLE 12. ORDERING INFORMATION

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|-------------------|--------------|--------------------------|--------------------|-------------|
| 843034EY-06LF | ICS43034E06L | 48 Lead "Lead-Free" LQFP | tray | 0°C to 75°C |
| 843034EY-06LFT | ICS43034E06L | 48 Lead "Lead-Free" LQFP | tape & reel | 0°C to 75°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET

| Rev | Table | Page | Description of Change | Date |
|-----|-------|------|---|----------|
| A | 8 | 16 | Added Applications Schematic. | 11/19/08 |
| B | T4B | 1 | Features Section - changed min. VCO from 560MHz to 600MHz. | 8/10/09 |
| | T4C | 6 | Programmable VCO Frequency Table - changed first row VCO frequency from 577.7 to 600 and M Divide from 26 to 27. | |
| | T6 | 8 | Programmable Output Divider Table - change Output Frequency Minimum columns from (1st row) 280 to 300; (2nd row) 140 to 150; (3rd row) 112 to 120. | |
| | T8 | 9 | Input Frequency Characteristics - changed VCO min. from 560MHz to 600MHz. Change min. input frequency value from 47 to 50, changed max. value from 14 to 15. AC Characteristics Table - changed min. output frequency from 112MHz to 120MHz. | |
| B | | | Product Discontinuation Notice - Last time buy expires August 14, 2016. PDN CQ-15-04 Updated data sheet format. | 8/17/15 |

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