

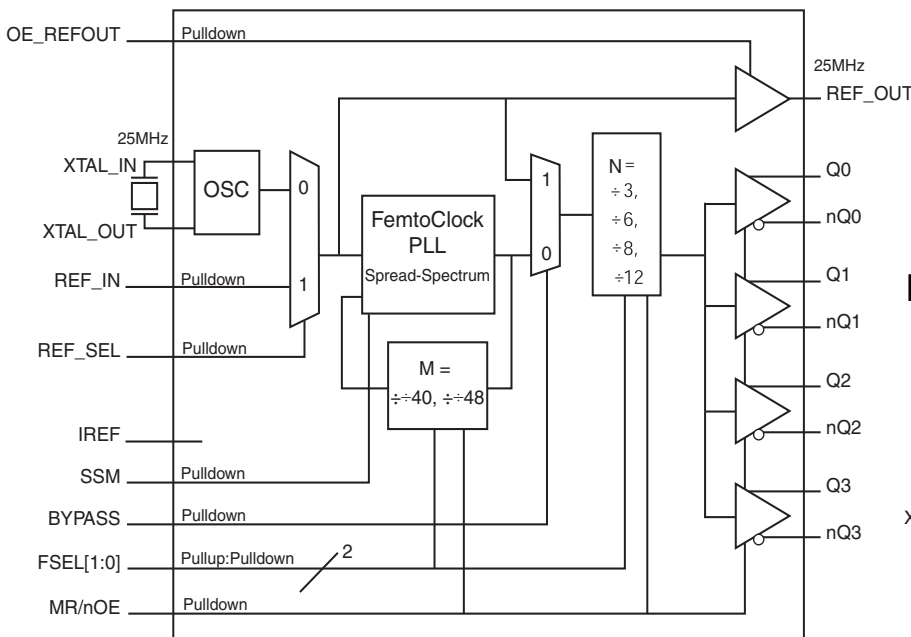
## General Description

The ICS841484I is an optimized PCIe and sRIO clock generator. The device uses a 25MHz parallel resonant crystal to generate 100MHz, 125MHz, 200MHz and 400MHz clock signals, replacing solutions requiring multiple oscillator and fanout buffer solutions. The device has excellent phase jitter suitable to clock components requiring precise and low jitter PCIe, sRIO or both clock signals. The device also supports a configurable spread-spectrum generation for PCIe applications. Designed for telecom, networking and industrial applications, the ICS841484I can also drive the high-speed sRIO and PCIe SerDes clock inputs of communications processors, DSPs, switches and bridges.

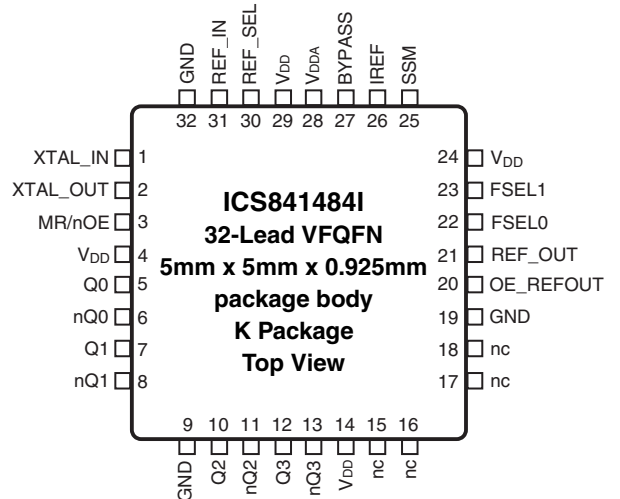
## Features

- Four 0.7V differential HCSL outputs: configurable for PCIe (100MHz or 200MHz) and sRIO (125MHz) clock signals
- One LVCMOS/LVTTL reference clock output
- Selectable crystal oscillator interface, 25MHz, 18pF parallel resonant crystal or LVCMOS/LVTTL single-ended reference clock input
- Supports the following output frequencies: 100MHz, 125MHz, 200MHz or 400MHz
- VCO frequency range: 950MHz - 1.25GHz
- Configurable spread-spectrum generation for PCIe
- PLL bypass and output enable
- RMS phase jitter @ 200MHz, using a 25MHz crystal (12kHz – 20MHz): 1.21ps (typical)
- PCI Express (2.5 Gb/S), Gen 2 (5 Gb/s) and Gen 3 (8 Gb/s) jitter compliant (REF\_OUT disabled)
- Full 3.3V operating supply
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) packages

## Block Diagram



## Pin Assignment



**Table 1. Pin Descriptions**

Number	Name	Type		Description
1, 2	XTAL_IN, XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input. (PLL reference.)
3	MR/nOE	Input	Pulldown	Master reset. LVCMOS/LVTTL interface levels. See Table 3D.
4, 14, 24, 29	V <sub>DD</sub>	Power		Core supply pins.
5, 6	Q0, nQ0	Output		Differential output pair. HCSL interface levels.
7, 8	Q1, nQ1	Output		Differential output pair. HCSL interface levels.
9, 19, 32	GND	Power		Power supply ground.
10, 11	Q2, nQ2	Output		Differential output pair. HCSL interface levels.
12, 13	Q3, nQ3	Output		Differential output pair. HCSL interface levels.
15, 16, 17, 18	nc	Unused		No connect.
20	OE_REFOUT	Input	Pulldown	Output enable pin. LVCMOS/LVTTL interface levels. See Table 3F.
21	REF_OUT	Output		Reference clock output. LVCMOS/LVTTL interface levels. In PCIe Gen 2 and Gen 3 applications, the REF_OUT output should be disabled.
22	F_SEL0	Input	Pulldown	Output frequency select pin. LVCMOS/LVTTL interface levels. See Table 3B.
23	F_SEL1	Input	Pullup	Output frequency select pin. LVCMOS/LVTTL interface levels. See Table 3B.
25	SSM	Input	Pulldown	Spread-spectrum selection. LVCMOS/LVTTL interface levels. See Table 3A.
26	IREF	Output		An external fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode Qx, nQx clock outputs.
27	BYPASS	Input	Pulldown	Selects PLL operation/PLL bypass operation. See Table 3C. LVCMOS/LVTTL interface levels.
28	V <sub>DDA</sub>	Power		Analog supply pin.
30	REF_SEL	Input	Pulldown	Reference select. Selects the input reference source. LVCMOS/LVTTL interface levels. See Table 3E.
31	REF_IN	Input	Pulldown	LVCMOS/LVTTL PLL reference clock input.

NOTE: *Pulldown* and *Pullup* refer to internal input resistors. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance				4		pF
R <sub>PULLDOWN</sub>	Input Pulldown Resistor				51		kΩ
R <sub>PULLUP</sub>	Input Pullup Resistor				51		kΩ
R <sub>OUT</sub>	Output Impedance	REF_OUT			27		Ω

## Function Tables

**Table 3A. Spread-Spectrum Modulation (SSM) Function Table ( $f_{REF} = 25\text{MHz}$ )**

Input	Outputs
<b>SSM</b>	<b>Q[0:3], nQ[0:3]</b>
0	SSM off (default)
1	SSM on (typical: 32kHz, -0.5%) See Table 6B

**Table 3B. FSEL Function Table ( $f_{REF} = 25\text{MHz}$ )**

Inputs				Outputs
FSEL1	FSEL0	M Divider	N Divider	Q[0:3], nQ[0:3]
0	0	48	12	VCO/12 (100MHz) PCIe
0	1	40	8	VCO/8 (125MHz) sRIO
1	0	48	6	VCO/6 (200MHz) PCIe (default)
1	1	48	3	VCO/3 (400MHz)

**Table 3C. BYPASS Function Table**

Input	
BYPASS	PLL Configuration
0	PLL on (default)
1	PLL bypassed ( $Q[0:3], nQ[0:3] = f_{REF}/N$ )

**Table 3E. REF\_SEL Function Table**

Input	
REF_SEL	Input Reference
0	XTAL (default)
1	REF_IN

**Table 3D. MR/nOE Function Table**

Input	
MR/nOE	Function <sup>NOTE1</sup>
0	Outputs enabled (default)
1	Device reset, outputs disabled (High Impedance)

**Table 3F. OE\_REFOUT Function Table**

Input	
OE_REFOUT	Function
0	REF_OUT disabled (High Impedance) (default)
1	REF_OUT enabled

NOTE 1: Asynchronous Function

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	4.6V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to $V_{DD}$ -0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	33.1°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Positive Supply Voltage		3.135	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.16$	3.3	$V_{DD}$	V
$I_{DD}$	Power Supply Current	Outputs unterminated			156	mA
$I_{DDA}$	Analog Supply Current	Outputs unterminated			16	mA

**Table 4B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	REF_IN, REF_SEL, BYPASS, SSM, F_SEL0, MR/nOE, OE_REFOUT	$V_{DD} = V_{IN} = 3.465V$		150	$\mu A$
		F_SEL1	$V_{DD} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	REF_IN, REF_SEL, BYPASS, SSM, F_SEL0, MR/nOE, OE_REFOUT	$V_{DD} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		F_SEL1	$V_{DD} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{OH}$	Output High Voltage	REF_OUT	$I_{OH} = -12mA$	2.6		V
$V_{OL}$	Output Low Voltage	REF_OUT	$I_{OL} = 12mA$		0.5	V

**Table 5. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	$\Omega$
Shunt Capacitance				7	pF

NOTE: Characterized using an 18pF parallel resonant crystal.

## AC Electrical Characteristics

**Table 6A. PCI Express Jitter Specifications,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Specification	Units
$t_j$ (PCIe Gen 1)	Phase Jitter Peak to Peak Note 1, 4	100MHz, 25MHz crystal input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		14.2	30.6	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	100MHz, 25MHz crystal input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.77	1.4	3.1	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	100MHz, 25MHz crystal input Low Band: 10kHz - 1.5MHz		0.17	0.45	3.0	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	100MHz, 25MHz crystal input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.16	0.35	0.8	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note* section in the datasheet.

NOTE: PCIe jitter parameters were obtained with Spread Spectrum Modulation disabled.

NOTE: PCIe Gen 2 and Gen 3 jitter parameters were obtained with REF\_OUT disabled.

NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of  $10^6$  clock periods.

NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for  $t_{REFCLK\_HF\_RMS}$  (High Band) and 3.0ps RMS for  $t_{REFCLK\_LF\_RMS}$  (Low Band).

NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the *PCI Express Base Specification Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.

NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

**Table 6B. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$** 

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency	Q[0:3], nQ[0:3]			100		MHz
					125		MHz
					200		MHz
		REF_OUT		400		MHz	
	REF_OUT			25		MHz	
$f_{IN}$	Input Frequency	REF_IN	REF_SEL = 1, BYPASS = 0			25	MHz
$t_{sk(o)}$	Output Skew; NOTE 1, 2					70	ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 2		$f_{OUT} = 100MHz, N = 12,$ $OE\_REFOUT = 1, SSM = 0$		60	100	ps
			$f_{OUT} = 125MHz, N = 8,$ $OE\_REFOUT = 1, SSM = 0$		35	92	ps
			$f_{OUT} = 200MHz, N = 6,$ $OE\_REFOUT = 1, SSM = 0$		20	72	ps
			$f_{OUT} = 400MHz, N = 3,$ $OE\_REFOUT = 1, SSM = 0$		15	36	ps
$f_{jit(\emptyset)}$	RMS Phase Jitter (Random); NOTE 3		$f_{OUT} = 100MHz (12kHz - 20MHz)$		1.21	1.6	ps
			$f_{OUT} = 125MHz (12kHz - 20MHz)$		1.47	1.6	ps
			$f_{OUT} = 200MHz (12kHz - 20MHz)$		1.23	1.6	ps
			$f_{OUT} = 400MHz (12kHz - 20MHz)$		1.32	2	ps
$t_L$	PLL Lock Time					85	ms
$V_{MAX}$	Absolute Maximum Output Voltage; NOTE 4, 5					1150	mV
$V_{MIN}$	Absolute Minimum Output Voltage; NOTE 4, 6			-300			mV
$V_{RB}$	Ringback Voltage; NOTE 7, 8			-100		100	mV
$t_{STABLE}$	Time before $V_{RB}$ is allowed; NOTE 7, 8			500			ps
$F_M$	SSC Modulation Frequency; NOTE 9			29	32	33.33	kHz
$F_{MF}$	SSC Modulation Factor; NOTE 9				-0.5		%
$SSC_{RED}$	Spectral Reduction; NOTE 9				10		dB
$V_{CROSS}$	Absolute Crossing Voltage; NOTE 4, 10, 11			125		560	mV
$\Delta V_{CROSS}$	Total Variation of $V_{CROSS}$ ; NOTE 4, 10, 12					140	mV
$t_{SLEW+}$ $t_{SLEW-}$	Rising/Falling Edge Rate; NOTE 7, 13		Measured between -150mV to +150mV	0.6		4.7	V/ns
$t_R / t_F$	Output Rise/Fall Time	REF_OUT		690		1550	ps
odc	Output Duty Cycle	Q[0:3], nQ[0:3]	N = 8, N = 12	45		55	%
		Q[0:3], nQ[0:3]	N = 6	44		56	%
		REF_OUT; NOTE 14	Using REF_IN Input	48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

NOTES continued on next page.

NOTE 1: Defined as skew between outputs at the same supply voltages and with equal load conditions. Measured at the output differential cross points.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

NOTE 3: Please refer to the Phase Noise Plots.

NOTE 4: Measurement taken from single-ended waveform.

NOTE 5: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

NOTE 6: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.

NOTE 7: Measurement taken from a differential waveform.

NOTE 8:  $T_{\text{STABLE}}$  is the time the differential clock must maintain a minimum  $\pm 150\text{mV}$  differential voltage after rising/falling edges before it is allowed to drop back into the  $V_{\text{RB}} \pm 100$  differential range. See Parameter Measurement Information Section.

NOTE 9: Spread Spectrum clocking enabled.

NOTE 10: Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.

See Parameter Measurement Information Section.

NOTE 11: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Parameter Measurement Information Section.

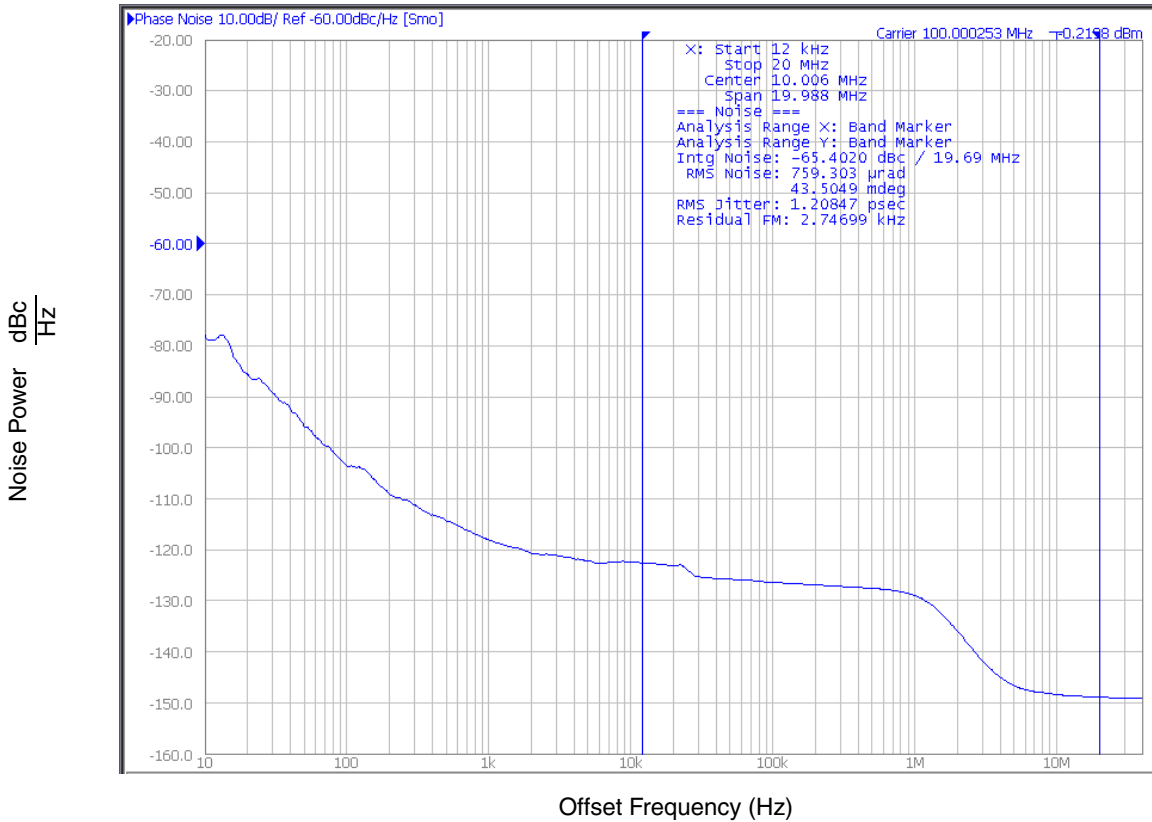
NOTE 12: Defined as the total variation of all crossing voltage of rising Qx and falling nQx. This is the maximum allowed variance in the  $V_{\text{CROSS}}$  for any particular system. See Parameter Measurement Information Section.

NOTE 13: Measured from  $-150\text{mV}$  to  $+150\text{mV}$  on the differential waveform (derived from Qx minus nQx). The signal must be monotonic through the measurement region for rise and fall time. The  $300\text{mV}$  measurement window is centered on the differential zero crossing.

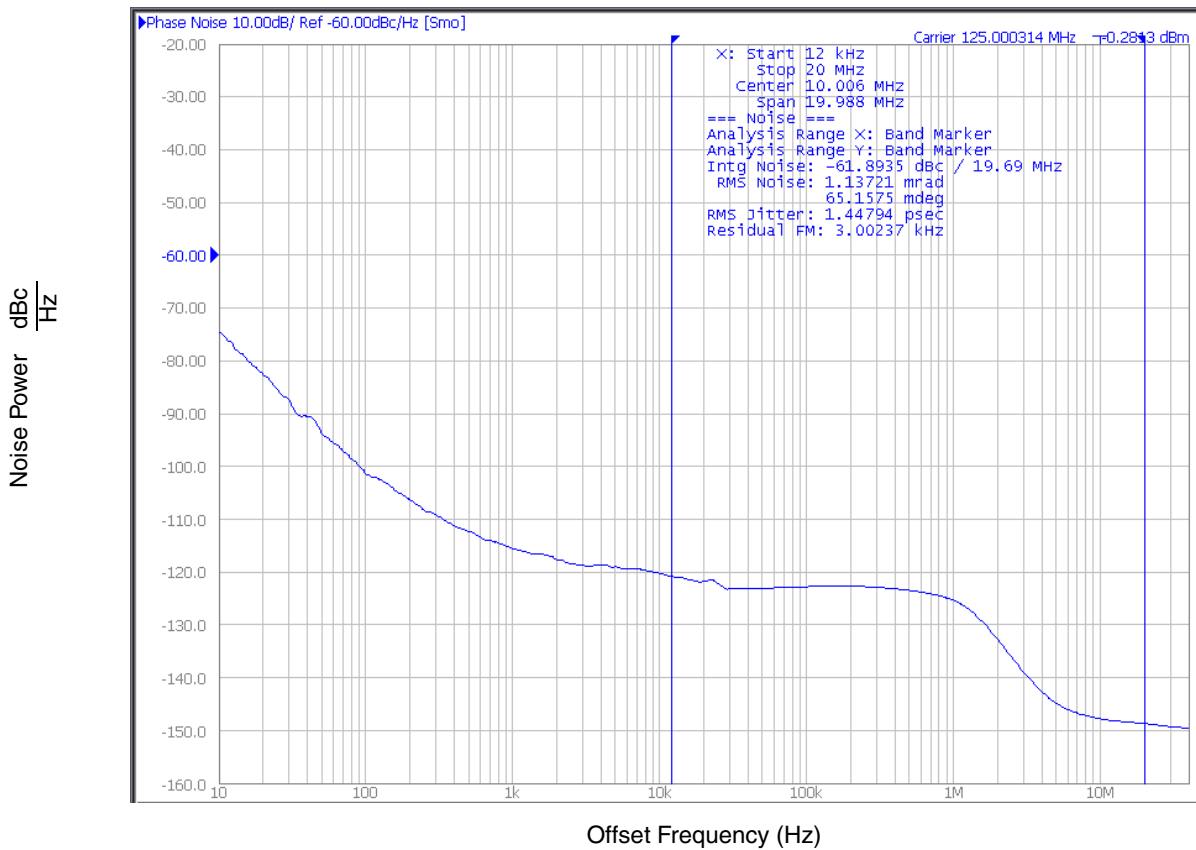
See Parameter Measurement Information Section.

NOTE 14: REF\_OUT duty cycle characterized with REF\_IN input duty cycle between 48% and 52%.

## Typical Phase Noise at 100MHz

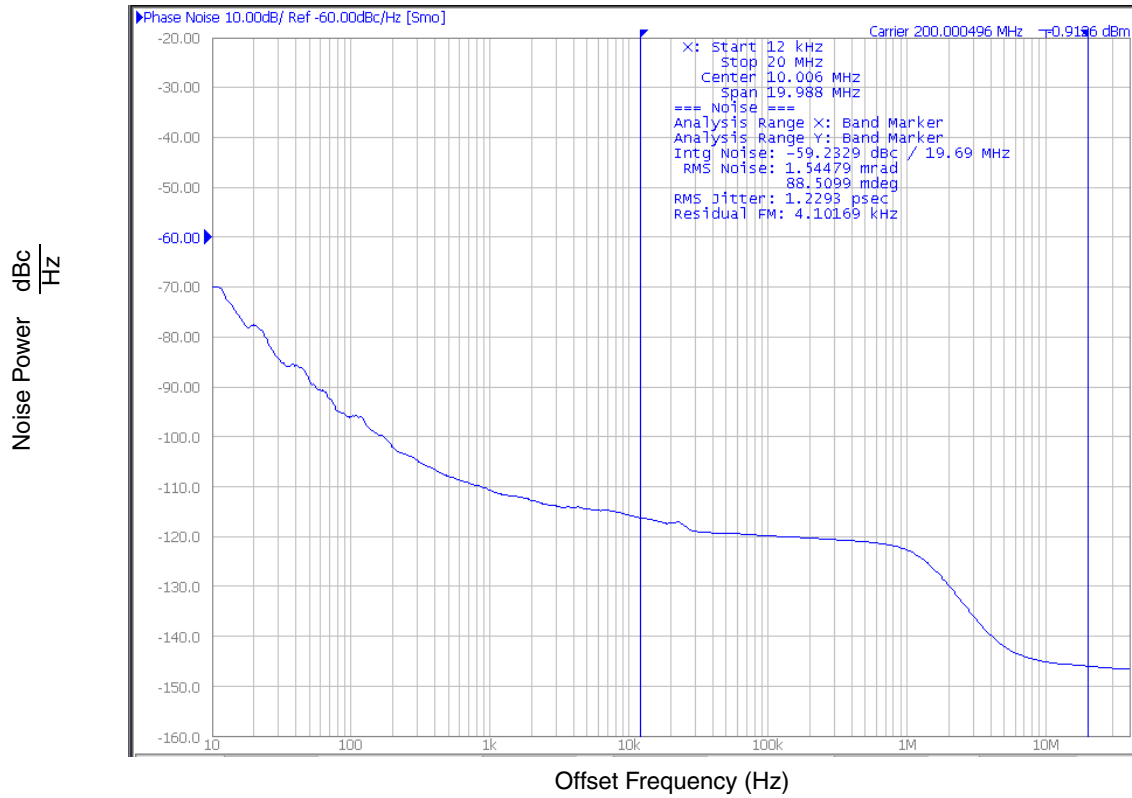


## Typical Phase Noise at 125MHz

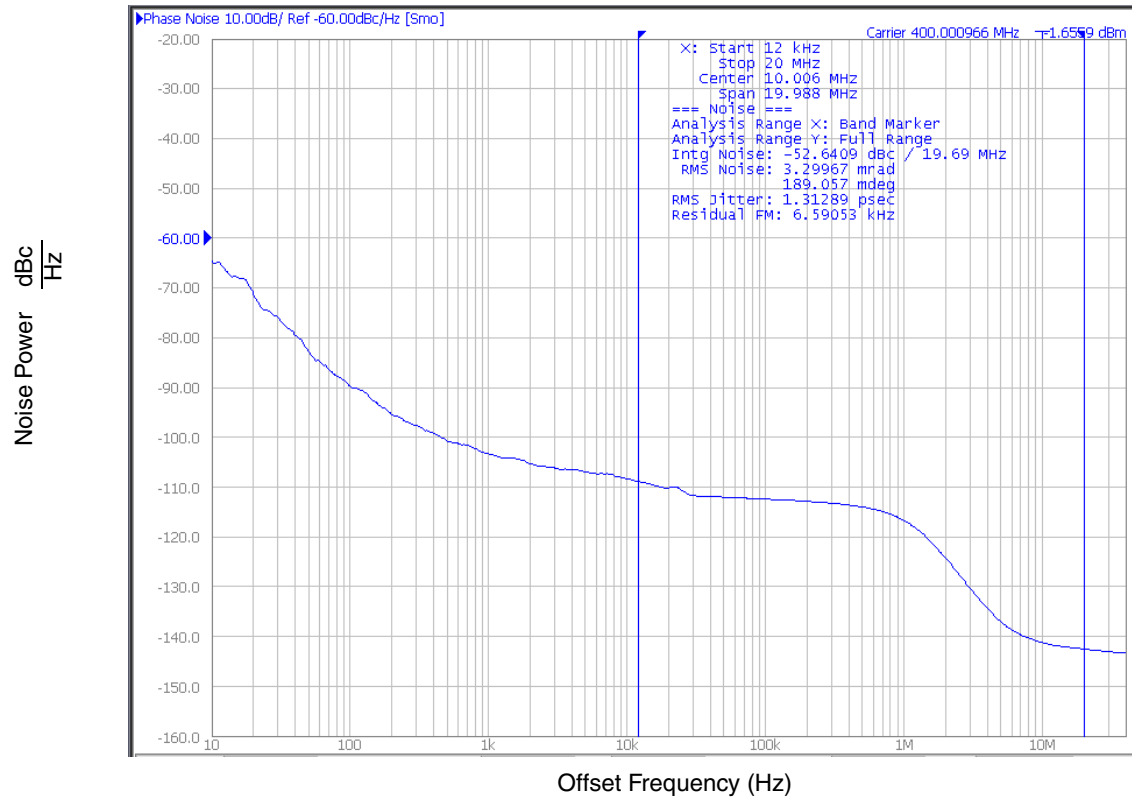




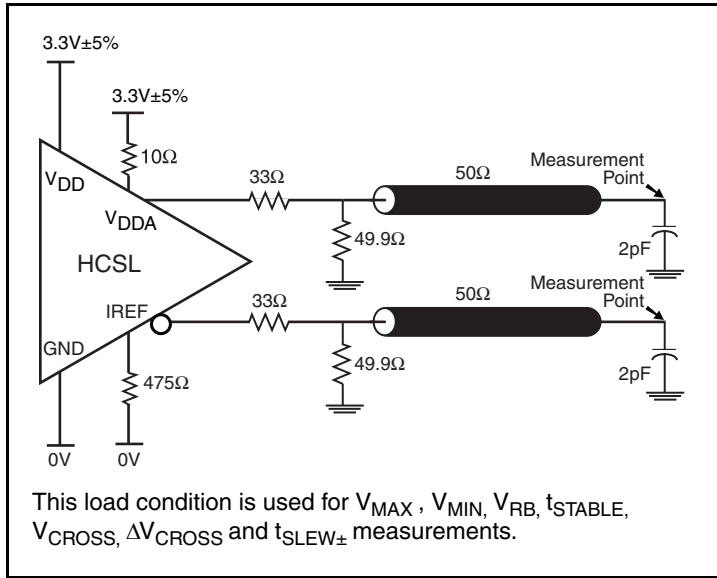
## Typical Phase Noise at 200MHz



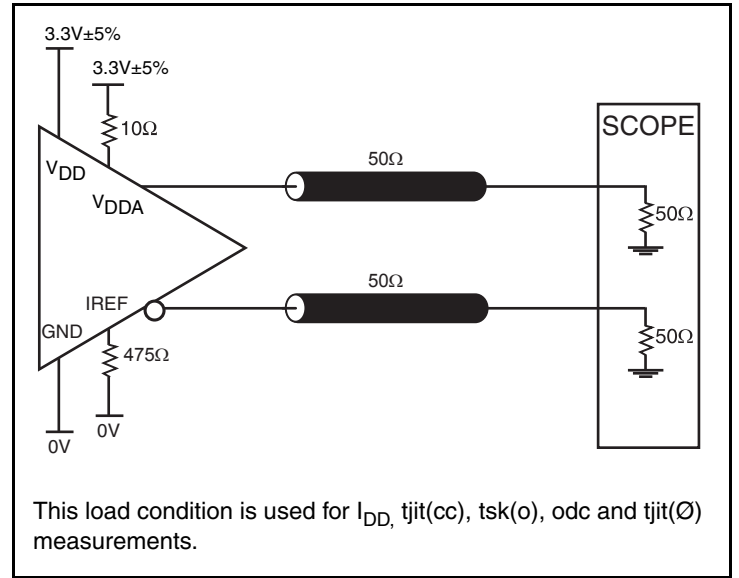
## Typical Phase Noise at 400MHz



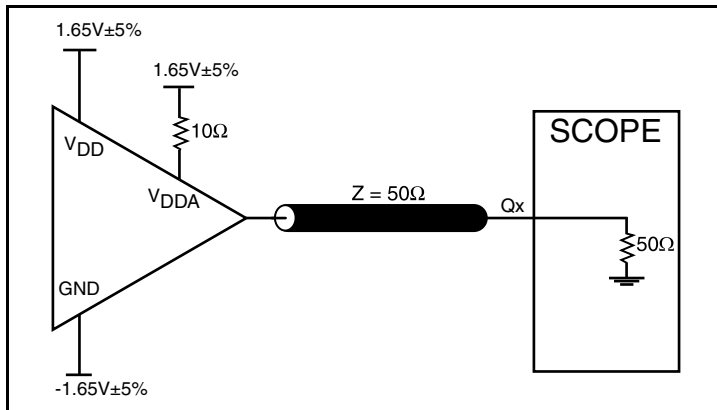
## Parameter Measurement Information



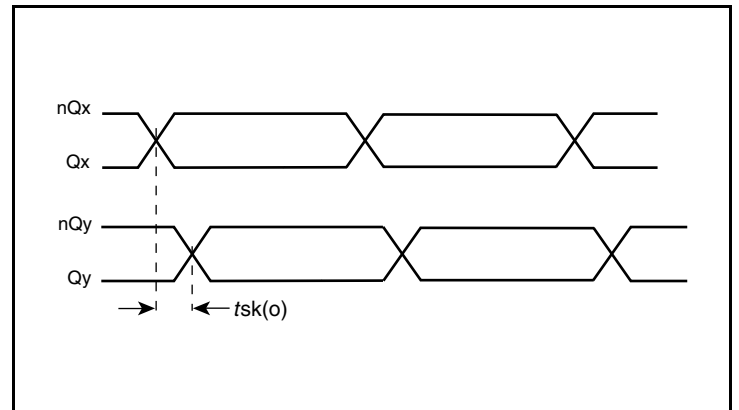
3.3V HCSL Output Load AC Test Circuit



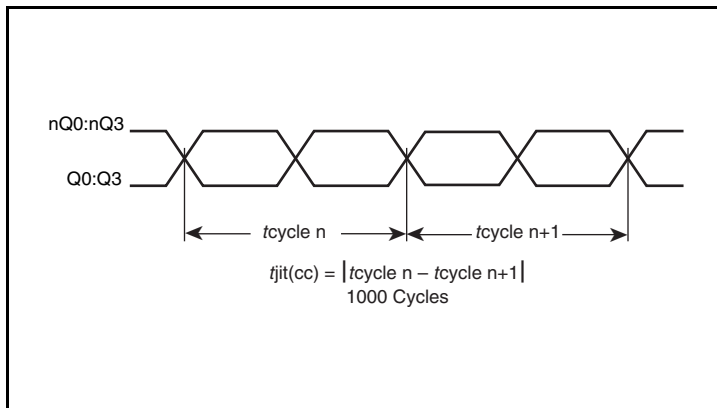
3.3V HCSL Output Load AC Test Circuit



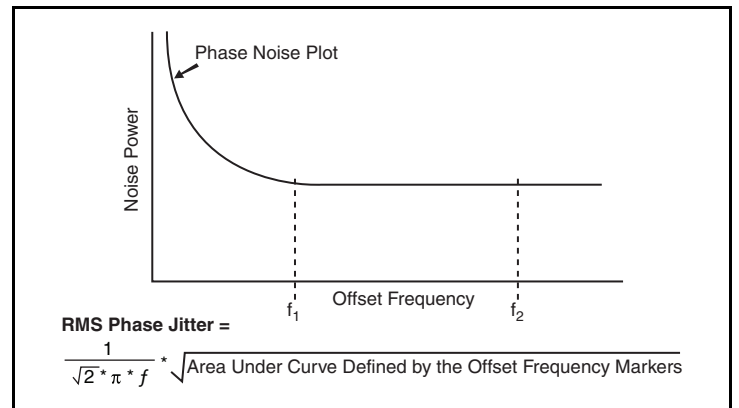
3.3V LVCMOS Output Load AC Test Circuit



Output Skew

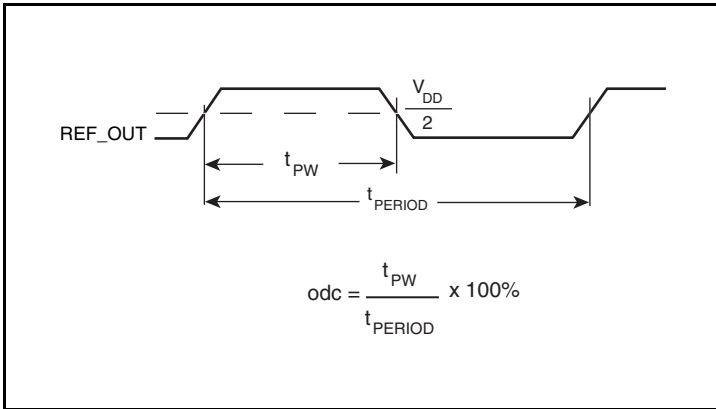


Cycle-to-Cycle Jitter

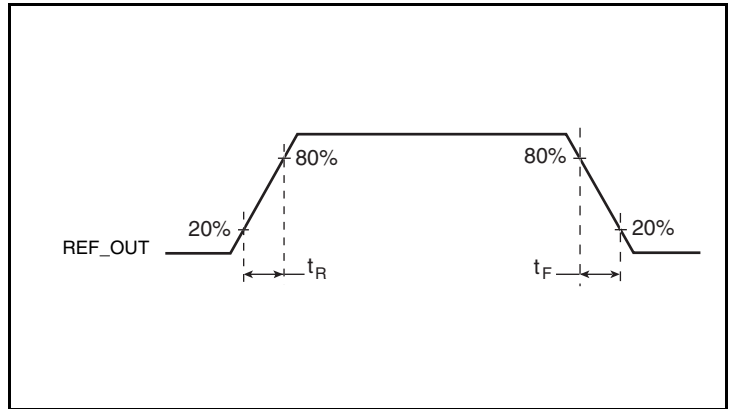


RMS Phase Jitter

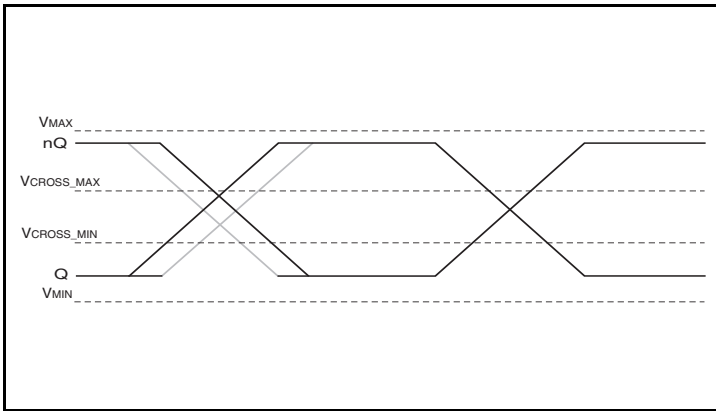
Parameter Measurement Information, continued



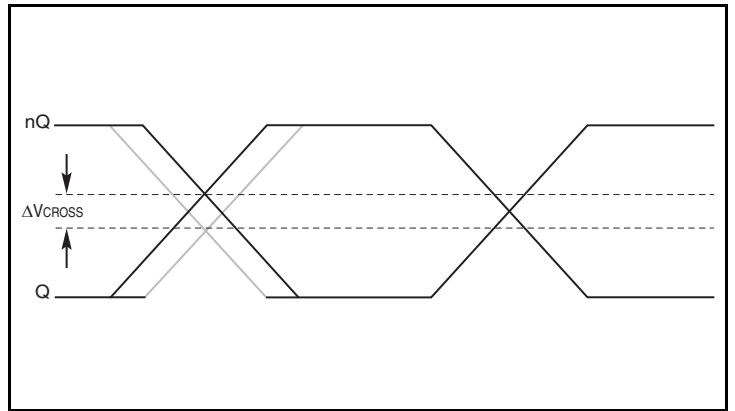
LVC MOS Output Duty Cycle



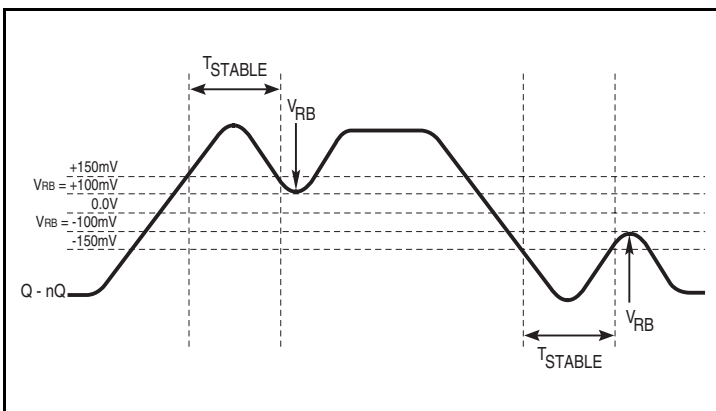
LVC MOS Rise/Fall Time



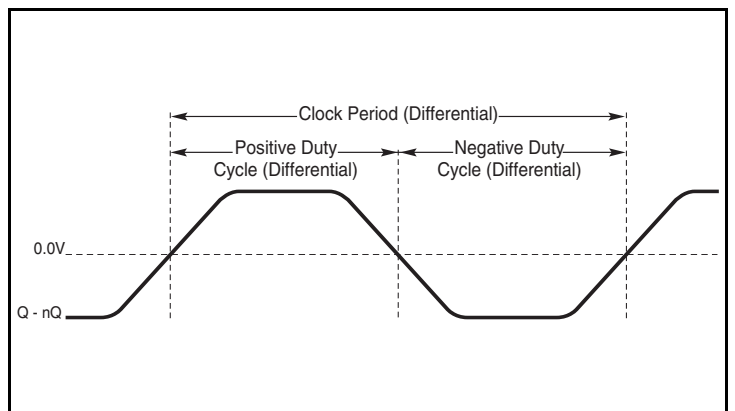
Single-ended Measurement Points for Absolute Cross Point/Swing



Single-ended Measurement Points for Delta Cross Point

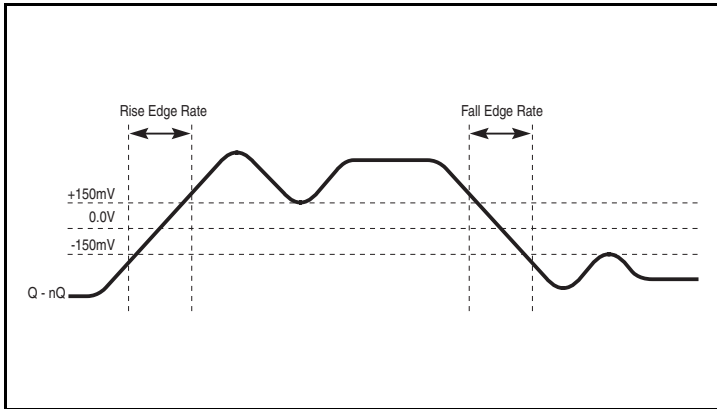


Differential Measurement Points for Ringback

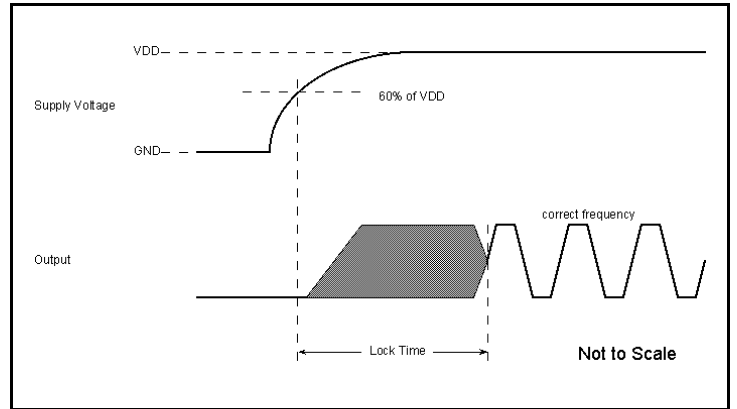


Differential Measurement Points for Duty Cycle/Period

## Parameter Measurement Information, continued



Differential Measurement Points for Rise/Fall Edge Rate



PLL Locktime

## Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 32kHz triangle waveform is used with 0.5% down-spread (+0.0% / -0.5%) from the nominal output frequency. An example of a triangle frequency modulation profile is shown in *Figure 1A* below. The ramp profile can be expressed as:

$F_{nom}$  = Nominal Clock Frequency in Spread Off mode (200MHz with 25MHz IN)

$F_m$  = Nominal Modulation Frequency (32kHz)

$\delta$  = Modulation Factor (0.5% down spread)

$$(1 - \delta) F_{nom} + 2 f_m \times \delta \times F_{nom} \times t \text{ when } 0 < t < \frac{1}{2f_m}$$

$$(1 - \delta) F_{nom} + 2 f_m \times \delta \times F_{nom} \times t \text{ when } \frac{1}{2f_m} < t < \frac{1}{f_m}$$

An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 1B*. The ratio of this width to the fundamental frequency is typically 0.5%. The resulting spectral reduction is typically 10dB, as shown in *Figure 1B*. It is important to note the ICS841484 10dB typical spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

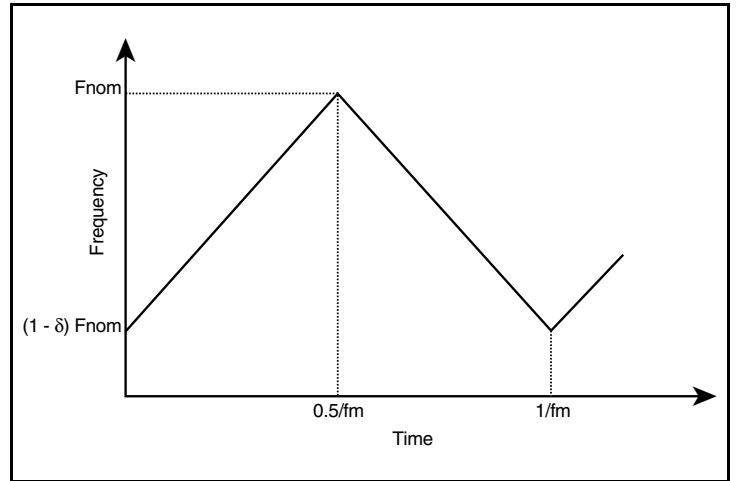


Figure 1A. Triangle Frequency Modulation

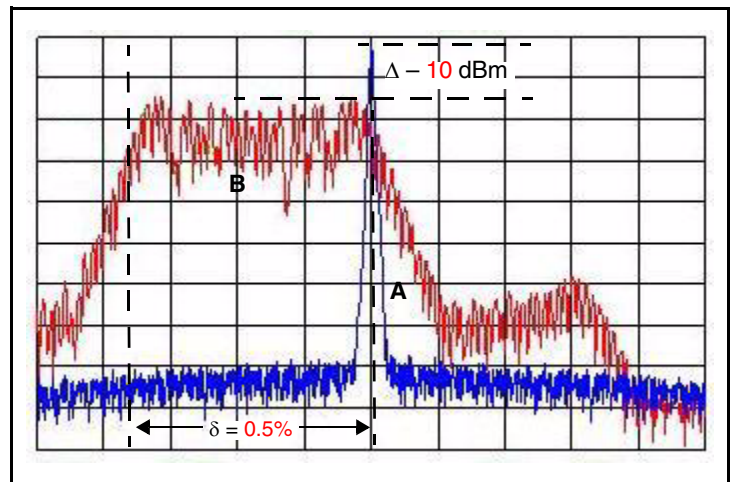


Figure 1B. 200MHz Clock Output In Frequency Domain  
 (A) Spread-Spectrum OFF  
 (B) Spread-Spectrum ON

## Applications Information

### Recommendations for Unused Input and Output Pins

#### Inputs:

##### LVC MOS Control Pins

All control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1k $\Omega$  resistor can be used.

##### REF\_IN

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from the REF\_IN to ground.

##### Crystal Input

For applications not requiring the use of the crystal oscillator input, both XTAL\_IN and XTAL\_OUT can be left floating. Though not required, but for additional protection, a 1k $\Omega$  resistor can be tied from XTAL\_IN to ground.

#### Outputs:

##### LVC MOS Output

The unused LVC MOS output can be left floating. There should be no trace attached.

##### Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 2A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most 50Ω applications,  $R_1$  and  $R_2$  can be 100Ω. This can also be accomplished by removing  $R_1$  and changing  $R_2$  to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 2B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

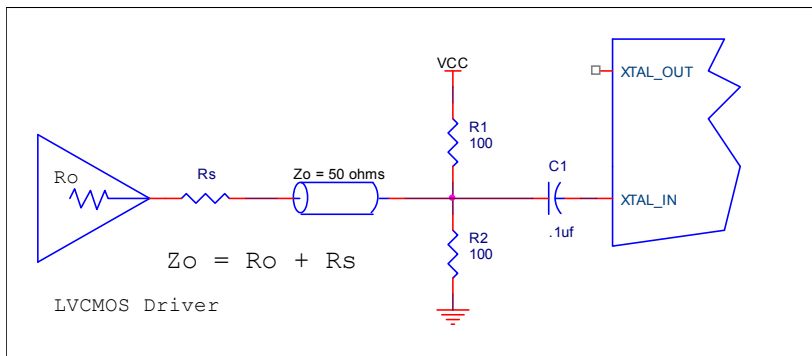


Figure 2A. General Diagram for LVCMOS Driver to XTAL Input Interface

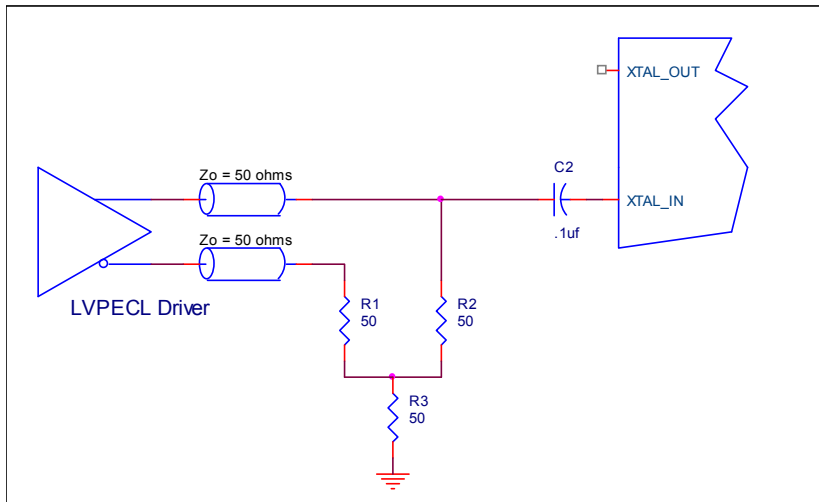


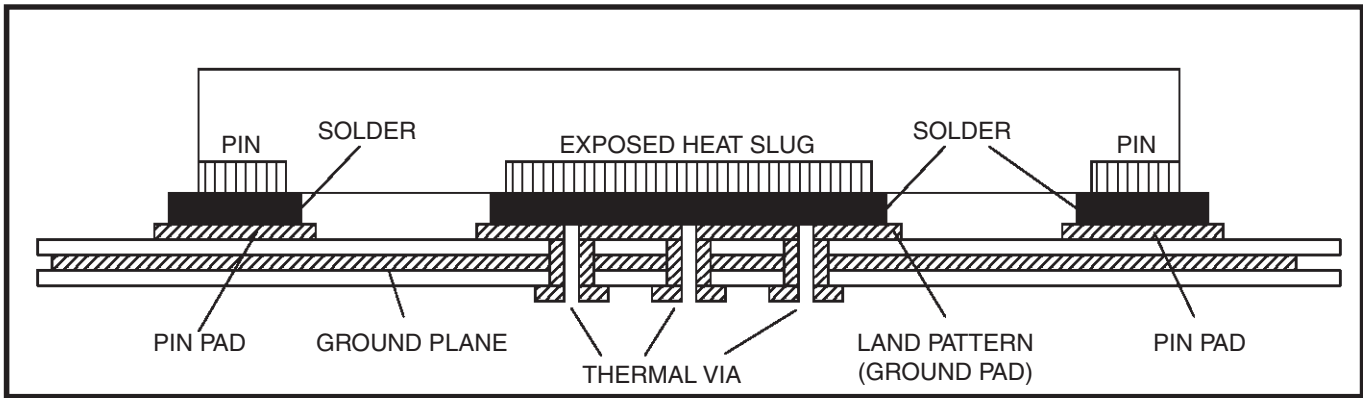
Figure 2B. General Diagram for LVPECL Driver to XTAL Input Interface

### VFQFN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 3*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific

and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.



**Figure 3. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)**



## Recommended Termination

Figure 4A is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types.

All traces should be 50Ω impedance single-ended or 100Ω differential.

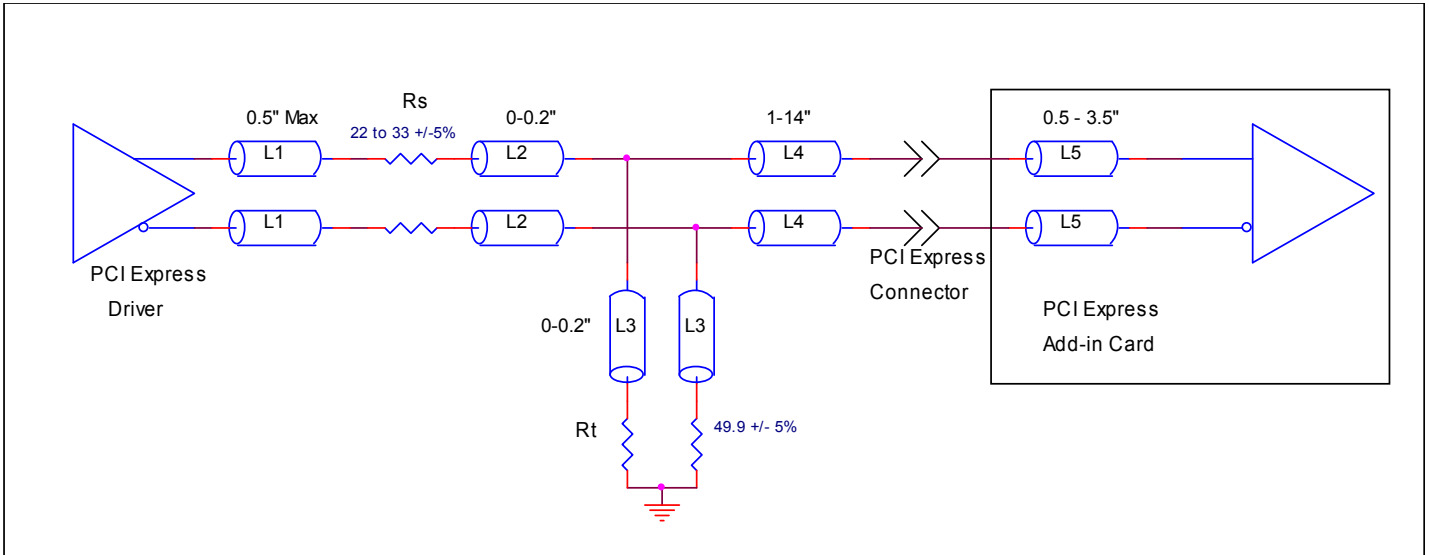


Figure 4A. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

Figure 4B is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will

be minimized. In addition, a series resistor ( $R_s$ ) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

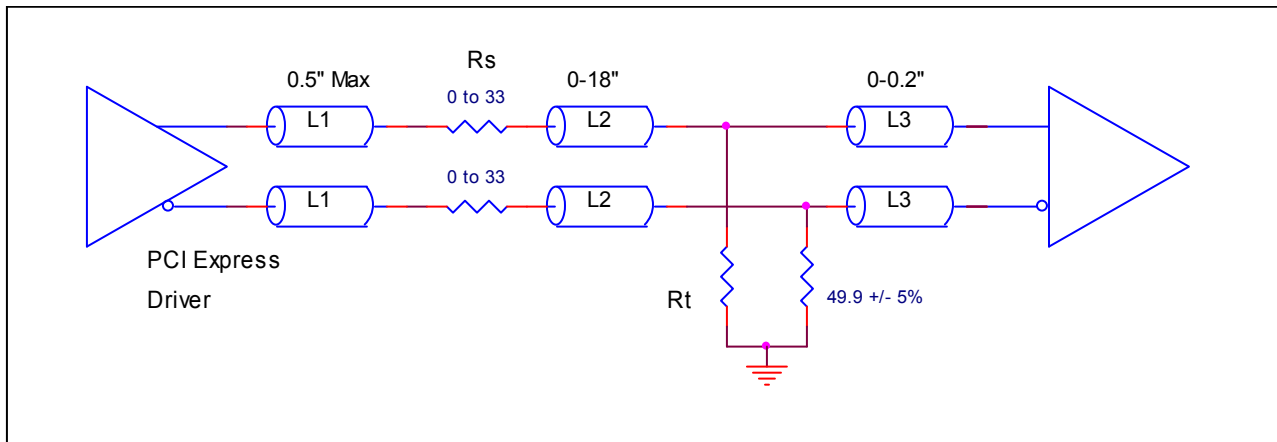


Figure 4B. Recommended Termination (where a point-to-point connection can be used)

### PCI Express Application Note

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

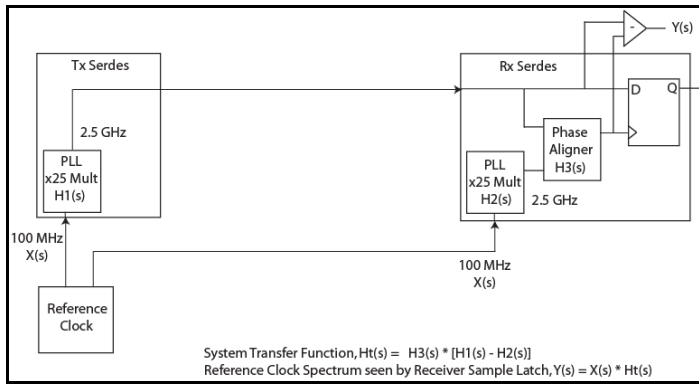
In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

$$H_t(s) = H_3(s) \times [H_1(s) - H_2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

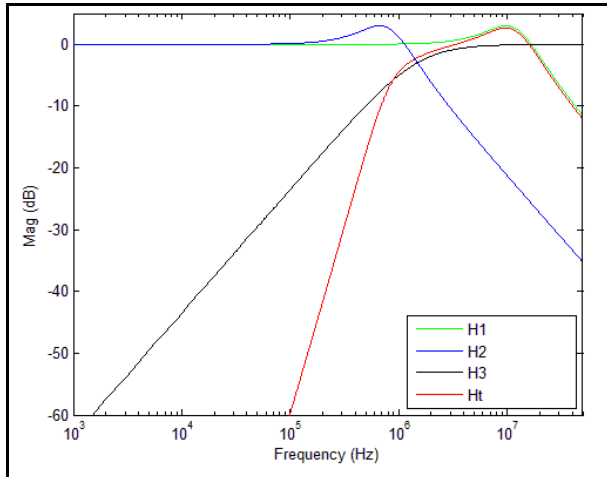
$$Y(s) = X(s) \times H_3(s) \times [H_1(s) - H_2(s)]$$

In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)\*H3(s) \* [H1(s) - H2(s)].



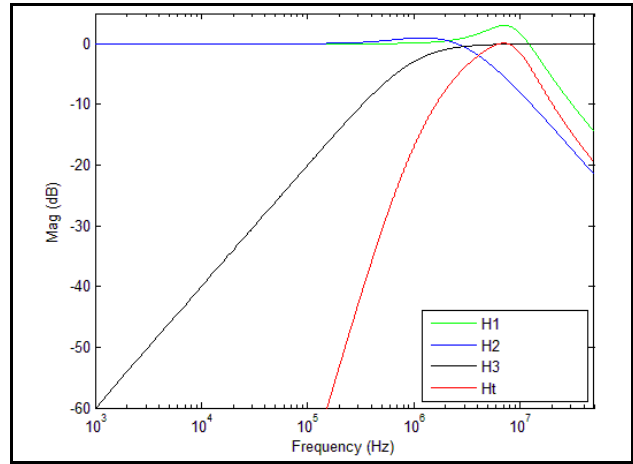
#### PCI Express Common Clock Architecture

For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

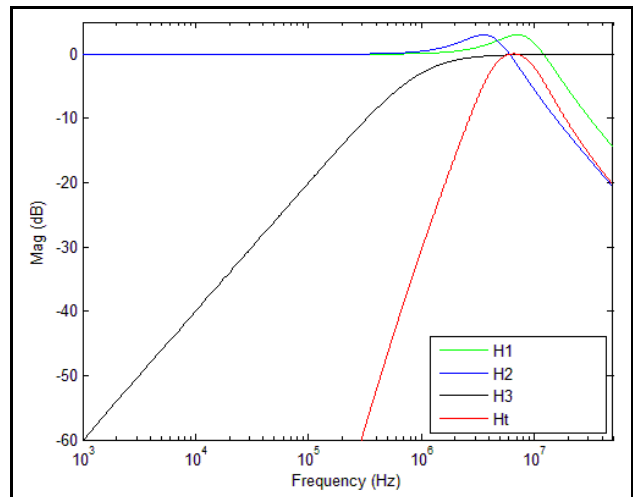


#### PCI Express Gen 1 Magnitude of Transfer Function

For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in rms. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

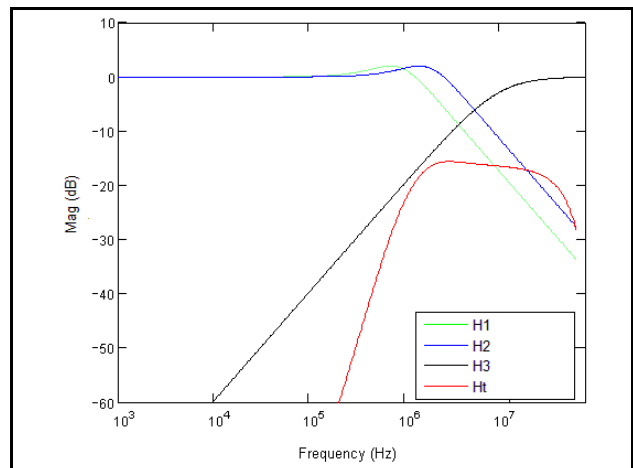


#### PCI Express Gen 2A Magnitude of Transfer Function



#### PCI Express Gen 2B Magnitude of Transfer Function

For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.



#### PCI Express Gen 3 Magnitude of Transfer Function

For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements*.

## Schematic Example

Figure 5 (next page) shows an example of ICS841484I application schematic. In this example, the device is operated at  $V_{DD} = 3.3V$ . The 18pF parallel resonant 25MHz crystal is used. The load capacitance  $C1 = 22pF$  and  $C2 = 22pF$  are recommended for frequency accuracy. Depending on the parasitic of the printed circuit board layout, these values might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used. This will require adjusting C1 and C2. For this device, the crystal load capacitors are required for proper operation.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS841484I provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the

0.1uf capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10 kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

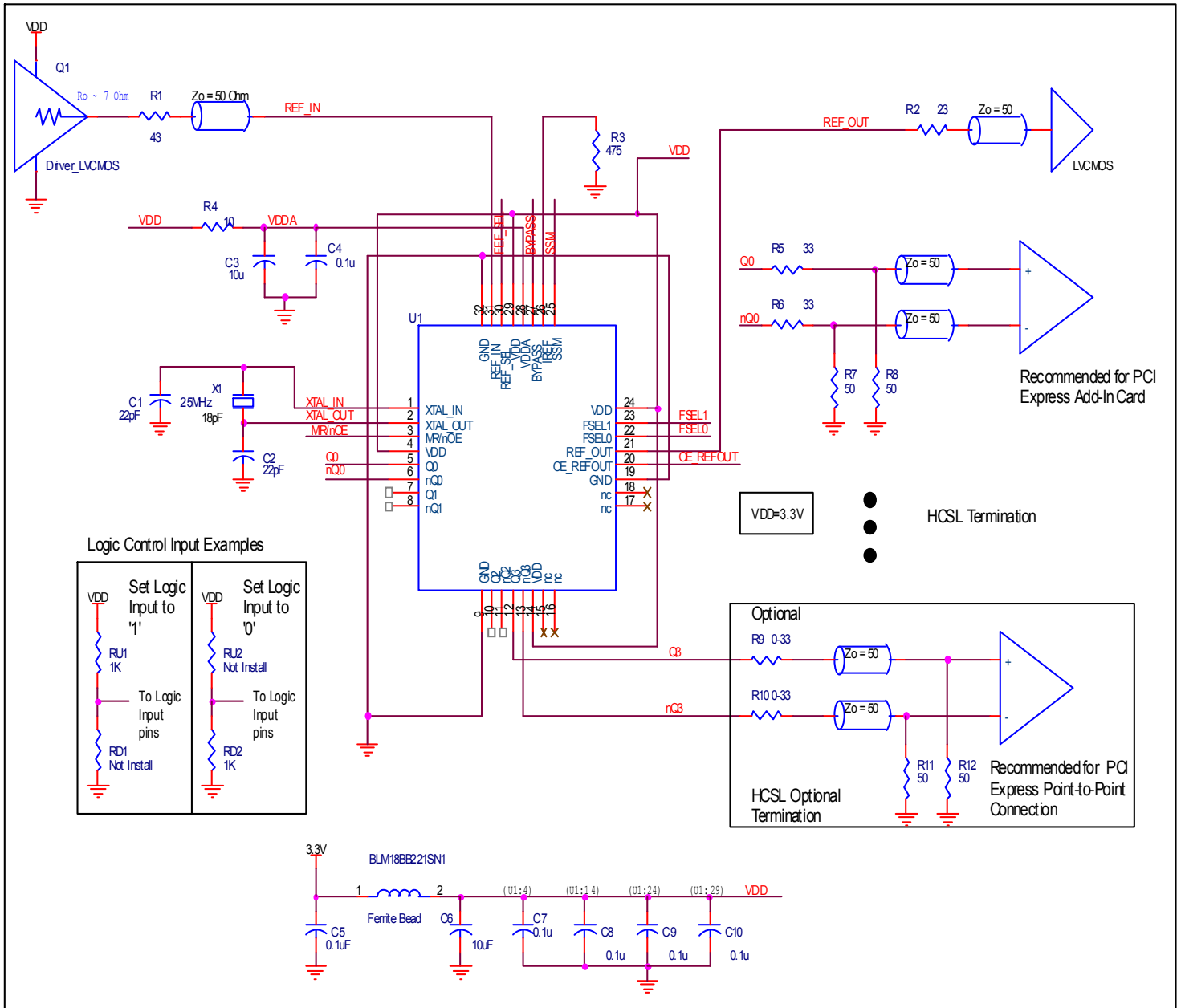


Figure 5. ICS81484I Schematic Example

## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS841484I. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS841484I is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (156mA + 16mA) = \mathbf{596mW}$
- Power (HCSL)<sub>MAX</sub> =  $4 \times 44.5mW = 178mW$

#### LVC MOS Driver Power Dissipation

- Output Impedance  $R_{OUT}$  Power Dissipation due to Loading  $50\Omega$  to  $V_{DD}/2$   
Output Current  $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 27\Omega)] = \mathbf{22.5mA}$
- Power Dissipation on the  $R_{OUT}$  per LVC MOS output  
Power (LVC MOS) =  $R_{OUT} * (I_{OUT})^2 = 27\Omega * (22.5mA)^2 = \mathbf{13.7mW \text{ per output}}$

#### Total Power

$$\begin{aligned} &= \text{Power (core)} + \text{Power (HCSL)} + \text{Power (LVC MOS)} \\ &= 596mW + 178mW + 13.7mW \\ &= \mathbf{787.7mW} \end{aligned}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is  $125^\circ\text{C}$ . Limiting the internal transistor junction temperature,  $T_j$ , to  $125^\circ\text{C}$  ensures that the bond wire and bond pad temperature remains below  $125^\circ\text{C}$ .

The equation for  $T_j$  is as follows:  $T_j = \theta_{JA} * Pd_{total} + T_A$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$Pd_{total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is  $33.1^\circ\text{C/W}$  per Table 7 below.

Therefore,  $T_j$  for an ambient temperature of  $85^\circ\text{C}$  with all outputs switching is:

$$85^\circ\text{C} + 0.788W * 33.1^\circ\text{C/W} = 111.1^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

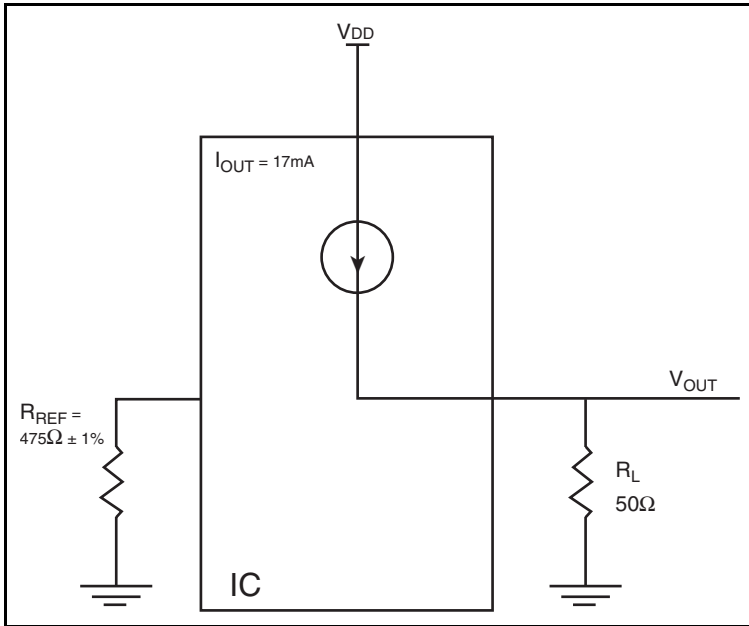
**Table 7. Thermal Resistance  $\theta_{JA}$  for 32 Lead VFQFN, Forced Convection**

$\theta_{JA}$ vs. Air Flow			
Meters per Second	0	1	3
Multi-Layer PCB, JEDEC Standard Test Boards	$33.1^\circ\text{C/W}$	$28.1^\circ\text{C/W}$	$25.4^\circ\text{C/W}$

### 3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pairs.

HCSL output driver circuit and termination are shown in *Figure 6*.



**Figure 6. HCSL Driver Circuit and Termination**

HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when  $V_{DD\_MAX}$ .

$$\text{Power} = (V_{DD\_MAX} - V_{OUT}) * I_{OUT}$$

since  $V_{OUT} = I_{OUT} * R_L$

$$\begin{aligned} \text{Power} &= (V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT} \\ &= (3.465V - 17mA * 50\Omega) * 17mA \end{aligned}$$

Total Power Dissipation per output pair = **44.5mW**

## Reliability Information

**Table 8.  $\theta_{JA}$  vs. Air Flow Table for a 32 Lead VFQFN**

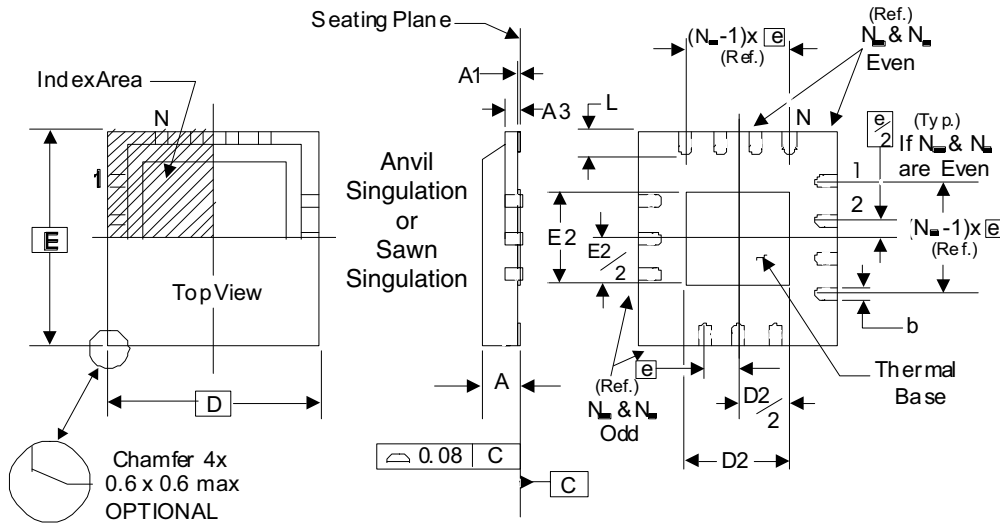
$\theta_{JA}$ vs. Air Flow			
Meters per Second	<b>0</b>	<b>1</b>	<b>3</b>
Multi-Layer PCB, JEDEC Standard Test Boards	33.1°C/W	28.1°C/W	25.4°C/W

## Transistor Count

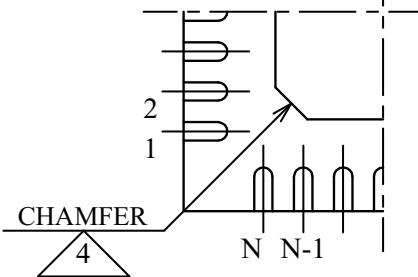
The transistor count for ICS841484I is: 12,330

# Package Outline and Package Dimensions

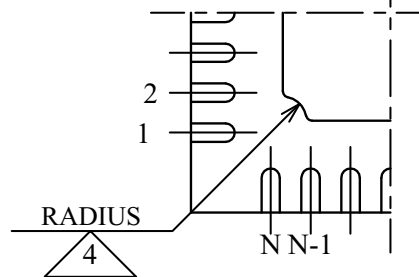
## Package Outline - K Suffix for 32 Lead VFQFN



**Bottom View w/Type A ID**



**Bottom View w/Type C ID**



There are 2 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type C: Mouse bite on the paddle (near pin 1)

**Table 9. Package Dimensions**

JEDEC Variation: VHHD-2/-4			
All Dimensions in Millimeters			
Symbol	Minimum	Nominal	Maximum
N	32		
A	0.80		1.00
A1	0		0.05
A3	0.25 Ref.		
b	0.18	0.25	0.30
N <sub>D</sub> & N <sub>E</sub>	8		
D & E	5.00 Basic		
D2 & E2	3.0		3.3
e	0.50 Basic		
L	0.30	0.40	0.50

NOTE: The following package mechanical drawing is a generic drawing that applies to any pin count VFQFN package. This drawing is not intended to convey the actual pin count or pin layout of this device. The pin count and pinout are shown on the front page. The package dimensions are in Table 9.

Reference Document: JEDEC Publication 95, MO-220



## Ordering Information

Table 10. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
841484DKILF	ICS41484DIL	"Lead-Free" 32 Lead VFQFN	Tray	-40°C to 85°C
841484DKILFT	ICS41484DIL	"Lead-Free" 32 Lead VFQFN	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

## Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T6B	6	AC Characteristics Table, Output Duty Cycle - corrected typo from Q[0:1], nQ[0:1] to Q[0:3], nQ[0:3].	7/6/2012
	T10	25	Ordering Information Table - deleted tray count.	
A	4A	4	I <sub>DD</sub> , I <sub>DDA</sub> ; Test Conditions; added "Outputs Unterminated"	11/7/12



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