

## General Description

The ICS840N021I-01 is a LVCMOS/LVTTL clock synthesizer designed for Ethernet applications. The device generates a 125MHz clock signal from a 25MHz crystal with excellent phase jitter performance. The device uses IDT's fourth generation FemtoClock® NG technology for an optimum of high clock frequency, low phase noise performance and low power consumption. The device supports 2.5V or 3.3V voltage supply and is packaged in a small, lead-free (RoHS 6) 8-lead TSSOP package. The extended temperature range supports wireless infrastructure, telecommunication and networking end equipment requirements.

### Frequency Table

$f_{XTAL}$ (MHz)	Output Frequency (MHz)
25	125
30.72	153.6

### Function Table

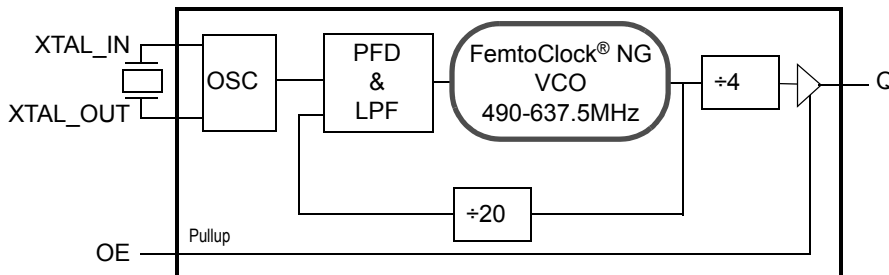
Input	Output Enable
OE	
0	Output Q is disabled in high-impedance state
1 (default)	Output Q is enabled.

NOTE: OE is an asynchronous control.

## Features

- Fourth generation FemtoClock® NG technology
- 125MHz output clock synthesized from a 25MHz fundamental mode crystal
- One 2.5V or 3.3V LVCMOS/LVTTL clock output
- Crystal interface designed for 25MHz, 12pF parallel resonant crystal
- RMS phase jitter @ 125MHz, using a 25MHz crystal (1.875MHz - 20MHz): 0.151ps (maximum)
- RMS phase jitter @ 125MHz, using a 25MHz crystal (12kHz - 20MHz): 0.478ps (maximum)
- LVCMOS/LVTTL interface level for the output enable input
- Full 2.5V or 3.3V supply voltage
- Available in lead-free (RoHS 6) package
- -40°C to 85°C ambient operating temperature

## Block Diagram



## Pin Assignment

VDDA	1	8	VDD
OE	2	7	Q
XTAL_OUT	3	6	GND
XTAL_IN	4	5	DNU

**ICS840N021I-01**  
**8-lead TSSOP**  
**4.40mm x 3.0mm x 0.925mm**  
**package body**  
**G Package**  
**Top View**

**Table 1. Pin Descriptions**

Number	Name	Type		Description
1	V <sub>DDA</sub>	Power		Analog power supply.
2	OE	Input	Pullup	Output enable pin. LVCMOS interface levels.
3, 4	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input, XTAL_OUT is the output.
5	DNU			Do not use.
6	GND	Power		Power supply ground.
7	Q	Output		Single-ended clock output. LVCMOS/LVTTL interface levels.
8	V <sub>DD</sub>	Power		Core supply pin.

NOTE: *Pullup* refers to an internal input resistor. See Table 2, *Pin Characteristics*, for typical values.

**Table 2. Pin Characteristics**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			3.5		pF
C <sub>PD</sub>	Power Dissipation Capacitance	V <sub>DD</sub> = 3.465V		11		pF
		V <sub>DD</sub> = 2.625V		9		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>OUT</sub>	Output Impedance	V <sub>DD</sub> = 3.3V		15		Ω
		V <sub>DD</sub> = 2.5V		19		Ω

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, $V_{DD}$	3.63V
Inputs, $V_I$ XTAL_IN Other Inputs	0V to 2V -0.5V to $V_{DD} + 0.5V$
Outputs, $V_O$	-0.5V to $V_{DD} + 0.5V$
Package Thermal Impedance, $\theta_{JA}$	117°C/W (0 mps)
Storage Temperature, $T_{STG}$	-65°C to 150°C

## DC Electrical Characteristics

**Table 3A. Power Supply DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{DD}$	Core Supply Voltage		2.375	3.3	3.465	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.18$	3.3	$V_{DD}$	V
$V_{DDA}$	Analog Supply Voltage		$V_{DD} - 0.18$	2.5	$V_{DD}$	V
$I_{DDA}$	Analog Supply Current				18	mA
$I_{DD}$	Power Supply Current				67	mA

**Table 3B. LVCMOS/LVTTL DC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ C$  to  $85^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage	$V_{DD} = 3.3V$	2		$V_{DD} + 0.3$	V
		$V_{DD} = 2.5V$	1.7		$V_{DD} + 0.3$	V
$V_{IL}$	Input Low Voltage	$V_{DD} = 3.3V$	-0.3		0.8	V
		$V_{DD} = 2.5V$	-0.3		0.7	V
$I_{IH}$	Input High Current	OE $V_{DD} = V_{IN} = 3.465V$ or $2.625V$			5	$\mu A$
$I_{IL}$	Input Low Current	OE $V_{DD} = 3.465V$ or $2.625V$ , $V_{IN} = 0V$	-150			$\mu A$
$V_{OH}$	Output High Voltage; NOTE 1	Q $V_{DD} = 3.465V$	2.6			V
		Q $V_{DD} = 2.625V$	1.8			V
$V_{OL}$	Output Low Voltage; NOTE 1	Q $V_{DD} = 3.465V$ or $2.625V$			0.5	V

NOTE 1: Output terminated with  $50\Omega$  to  $V_{DD}$  / 2. See Parameter Measurement Information Section, *LVCMOS Output Load Test Circuit Diagrams*.

**Table 4. Crystal Characteristics**

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		24.50	25	31.88	MHz
Equivalent Series Resistance (ESR)				80	$\Omega$
Shunt Capacitance				7	pF

## AC Characteristics

**Table 5. AC Characteristics,  $V_{DD} = 3.3V \pm 5\%$  or  $2.5V \pm 5\%$ ,  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$** 

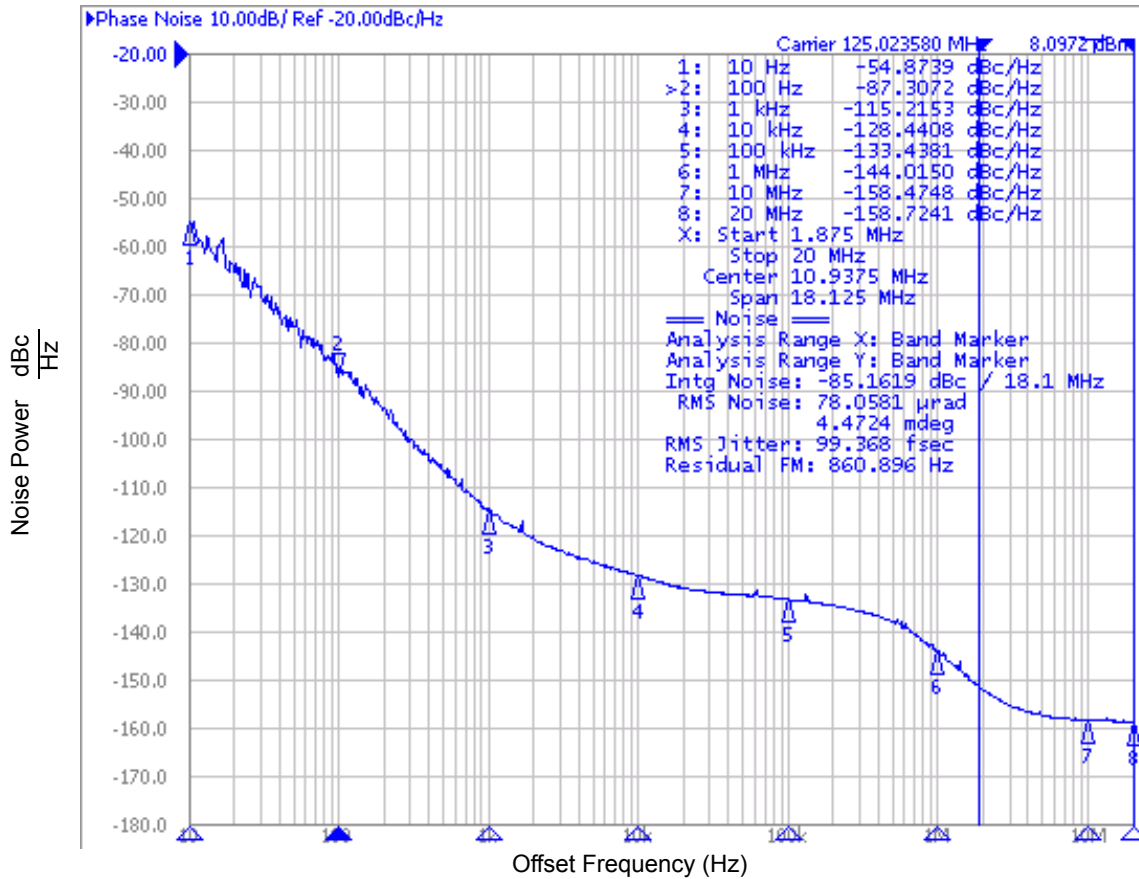
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{OUT}$	Output Frequency		122.50	125	159.38	MHz
$f_{jit}(\emptyset)$	RMS Phase Jitter (Random); NOTE 1	$f_{OUT} = 125\text{MHz}$ , 25MHz Crystal, Integration Range: 1.875MHz – 20MHz		0.099	0.151	ps
		$f_{OUT} = 125\text{MHz}$ , 25MHz Crystal, Integration Range: 12kHz – 20MHz		0.288	0.478	ps
$\Phi_N$	Single-Side Band Noise Power	$f_{OUT} = 125\text{MHz}$ , Offset: 10Hz		-55.5		dBc/Hz
		$f_{OUT} = 125\text{MHz}$ , Offset: 100Hz		-85.9		dBc/Hz
		$f_{OUT} = 125\text{MHz}$ , Offset: 1kHz		-115.4		dBc/Hz
		$f_{OUT} = 125\text{MHz}$ , Offset: 10kHz		-128.2		dBc/Hz
		$f_{OUT} = 125\text{MHz}$ , Offset: 100kHz		-133.2		dBc/Hz
		$f_{OUT} = 125\text{MHz}$ , Offset: 1MHz		-143.8		dBc/Hz
		$f_{OUT} = 125\text{MHz}$ , Offset: 10MHz		-158.3		dBc/Hz
$t_R / t_F$	Output Rise/Fall Time	20% to 80%	200		600	ps
odc	Output Duty Cycle		48		52	%

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

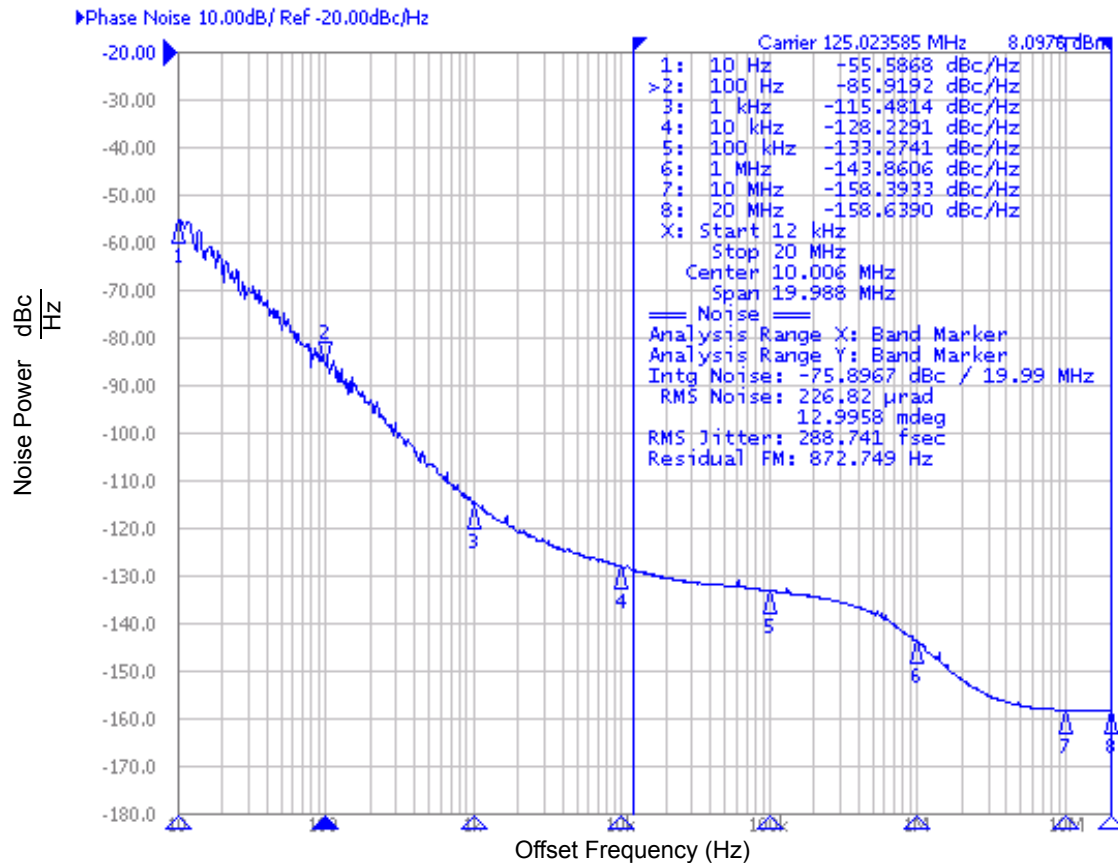
NOTE: Characterized with a 25MHz and 30.72MHz crystal.

NOTE 1: Please refer to the phase noise plots.

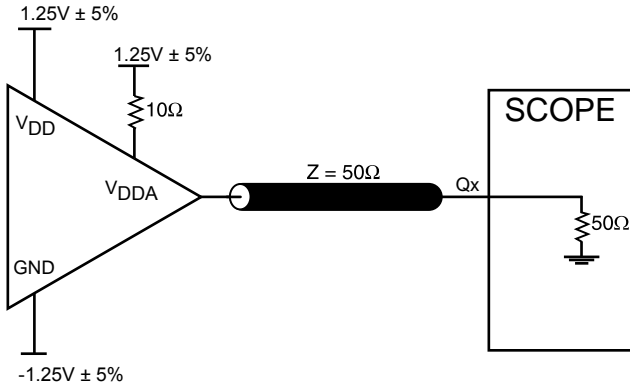
## Typical Phase Noise at 125MHz (1.875MHz-20MHz)



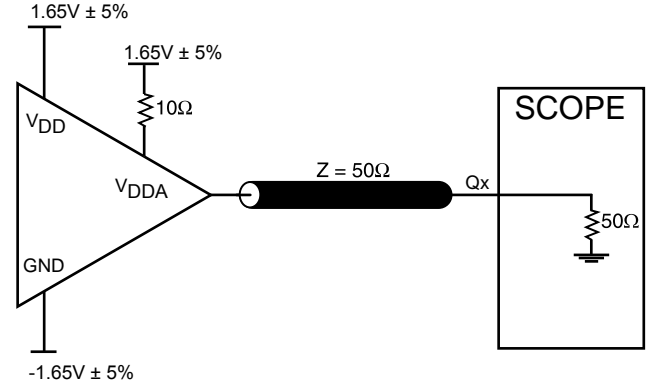
## Typical Phase Noise at 125MHz (12kHz-20MHz)



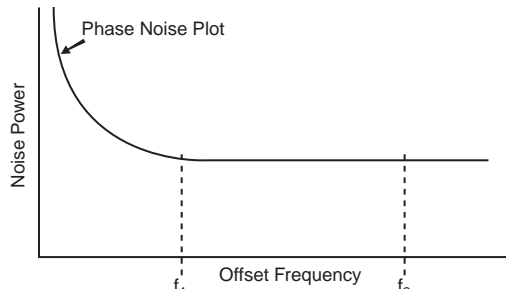
## Parameter Measurement Information



2.5V LVCMOS/LVTTL Output Load AC Test Circuit

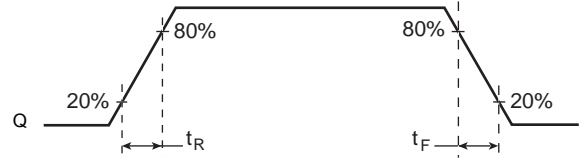


3.3V LVCMOS/LVTTL Output Load AC Test Circuit

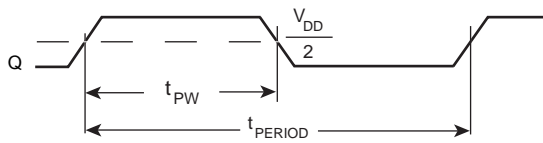


$$\text{RMS Phase Jitter} = \frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

RMS Phase Jitter



Output Rise/Fall Time



$$\text{odc} = \frac{t_{PW}}{t_{PERIOD}} * 100\%$$

Output Duty Cycle/Pulse Width/Period

## Applications Information

### Overdriving the XTAL Interface

The XTAL\_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL\_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. *Figure 1A* shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver ( $R_o$ ) and the series resistance ( $R_s$ ) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This

can be done in one of two ways. First,  $R_1$  and  $R_2$  in parallel should equal the transmission line impedance. For most  $50\Omega$  applications,  $R_1$  and  $R_2$  can be  $100\Omega$ . This can also be accomplished by removing  $R_1$  and changing  $R_2$  to  $50\Omega$ . The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. *Figure 1B* shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL\_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

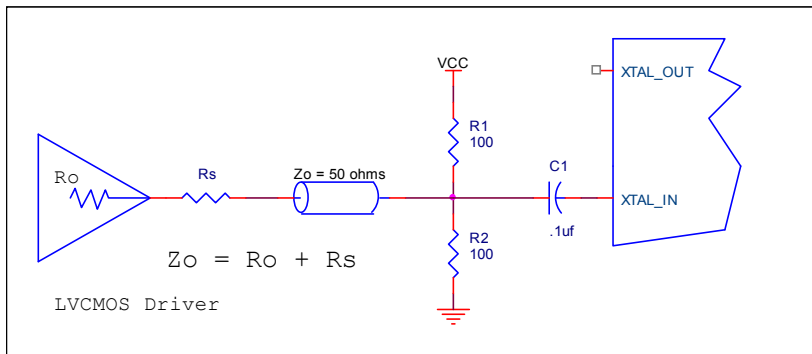


Figure 1A. General Diagram for LVCMOS Driver to XTAL Input Interface

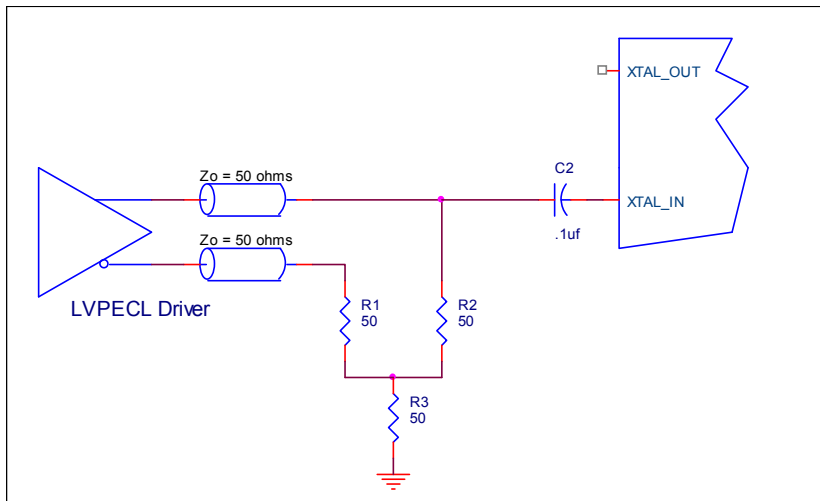


Figure 1B. General Diagram for LVPECL Driver to XTAL Input Interface

## Schematic Layout

Figure 2 shows an example ICS840N021I-01 application schematic in which the device is operated at  $V_{DD} = V_{DDA} = 3.3V$ . The schematic example focuses on functional connections and is intended as an example only and may not represent the exact user configuration. Refer to the pin description and functional tables in the datasheet to ensure the logic control inputs are properly set. For example OE can be configured from an FPGA instead of set with a pullup resistor as shown.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise, so to achieve optimum jitter performance isolation of the  $V_{DD}$  pin from power supply is required. In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the

PCB as close to the power pins as possible. If space is limited, the  $0.1\mu F$  capacitor on the  $V_{DD}$  pin must be placed on the device side with direct return to the ground plane through vias. The remaining filter components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supply frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitances in the local area of all devices.

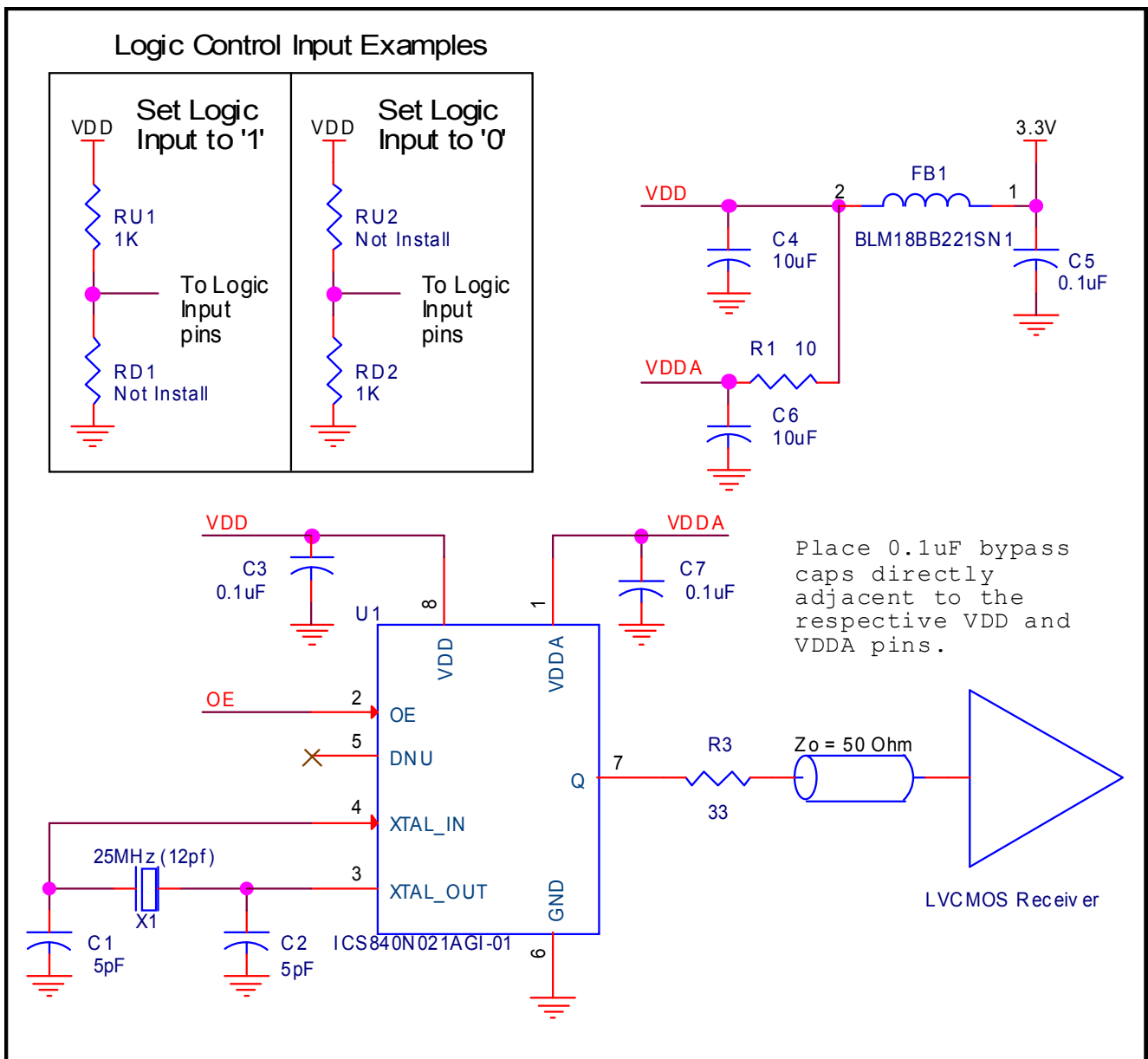


Figure 2. ICS840N021I-01 Application Schematic



## Power Considerations

This section provides information on power dissipation and junction temperature for the ICS840N021I-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS840N021I-01 is the sum of the core power plus the analog power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{DD} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

- Power (core)<sub>MAX</sub> =  $V_{DD\_MAX} * (I_{DD} + I_{DDA}) = 3.465V * (67mA + 18mA) = \mathbf{294.53mW}$
- Output Impedance  $R_{OUT}$  Current due to Loading  $50\Omega$  to  $V_{DD}/2$   
Output Current  $I_{OUT} = V_{DD\_MAX} / [2 * (50\Omega + R_{OUT})] = 3.465V / [2 * (50\Omega + 15\Omega)] = \mathbf{26.7mA}$
- Power Dissipation on the  $R_{OUT}$  per LVCMOS output  
Power ( $R_{OUT}$ ) =  $R_{OUT} * (I_{OUT})^2 = 15\Omega * (26.7mA)^2 = \mathbf{10.7mW}$
- Total Power ( $R_{OUT}$ ) =  $10.7mW * 1 = \mathbf{10.7mW}$

### Dynamic Power Dissipation at 153.6MHz

$$\text{Power (153.6MHz)} = C_{PD} * \text{Frequency} * (V_{DD})^2 = 11pF * 153.6MHz * (3.465V)^2 = \mathbf{20.29mW}$$

$$\text{Total Power (153.6MHz)} = 20.29mW * 1 = \mathbf{20.29mW}$$

### Total Power Dissipation

- Total Power

$$= \text{Power (core)}_{MAX} + \text{Power (R}_{OUT}) + \text{Power (153.6MHz)}$$

$$= 294.53mW + 10.7mW + 20.29mW$$

$$= \mathbf{325.52mW}$$

### 2. Junction Temperature.

Junction temperature,  $T_j$ , is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is  $125^\circ\text{C}$ . Limiting the internal transistor junction temperature,  $T_j$ , to  $125^\circ\text{C}$  ensures that the bond wire and bond pad temperature remains below  $125^\circ\text{C}$ .

$$\text{The equation for } T_j \text{ is as follows: } T_j = \theta_{JA} * P_{d\_total} + T_A$$

$T_j$  = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

$P_{d\_total}$  = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$  = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming no air flow and a multi-layer board, the appropriate value is  $117^\circ\text{C/W}$  per Table 6 below.

Therefore,  $T_j$  for an ambient temperature of  $85^\circ\text{C}$  with all outputs switching is:

$$85^\circ\text{C} + 0.326W * 117^\circ\text{C/W} = 123.2^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example.  $T_j$  will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 6. Thermal Resistance  $\theta_{JA}$  for 8 Lead TSSOP, Forced Convection**

$\theta_{JA}$ by Velocity	
Meters per Second	<b>0</b>
Multi-Layer PCB, JEDEC Standard Test Boards	$117^\circ\text{C/W}$

## Reliability Information

Table 7.  $\theta_{JA}$  vs. Air Flow Table for a 8-lead TSSOP

$\theta_{JA}$ vs. Air Flow	
Meters per Second	0
Multi-Layer PCB, JEDEC Standard Test Boards	117°C/W

## Transistor Count

The transistor count for ICS840N021I-01 is: 24,811

## Package Outline and Package Dimensions

Package Outline - G Suffix for 8 Lead TSSOP

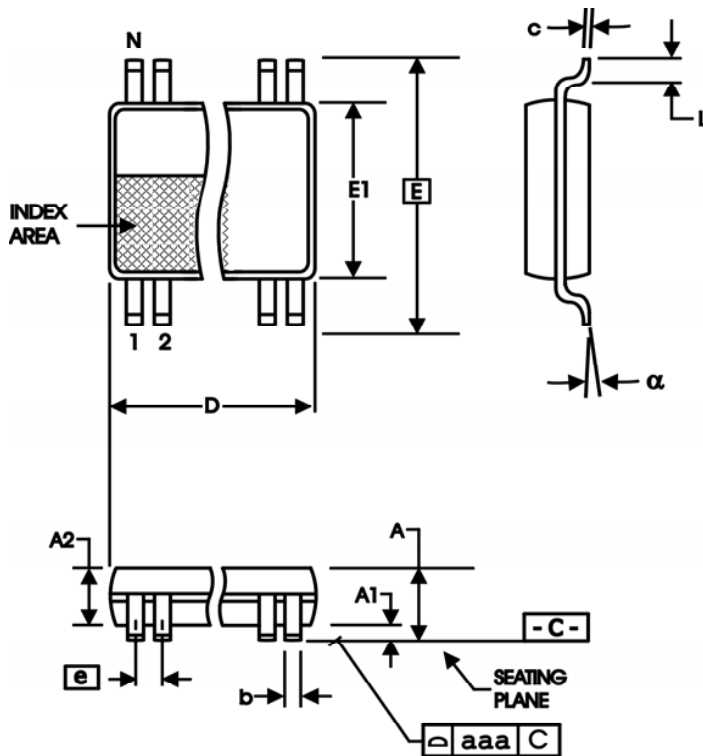


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	Minimum	Maximum
N	8	
A		1.20
A1	0.5	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	2.90	3.10
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
$\alpha$	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

## Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
840N021BGI-01LF	2BI1L	Lead-Free, 8-lead TSSOP	Tube	-40°C to 85°C
840N021BGI-01LFT	2BI1L	Lead-Free, 8-lead TSSOP	Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant



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