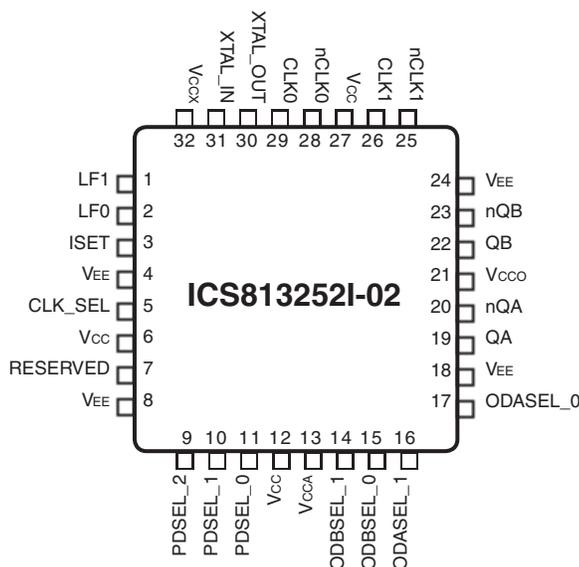


GENERAL DESCRIPTION

The ICS813252I-02 is a PLL based synchronous multiplier that is optimized for PDH or SONET to Ethernet clock jitter attenuation and frequency translation. The device contains two internal frequency multiplication stages that are cascaded in series. The first stage is a VCXO PLL that is optimized to provide reference clock jitter attenuation. The second stage is a FemtoClock® frequency multiplier that provides the low jitter, high frequency Ethernet output clock that easily meets Gigabit and 10 Gigabit Ethernet jitter requirements. Pre-divider and output divider multiplication ratios are selected using device selection control pins. The multiplication ratios are optimized to support most common clock rates used in PDH, SONET and Ethernet applications. The VCXO requires the use of an external, inexpensive pullable crystal. The VCXO uses external passive loop filter components which allows configuration of the PLL loop bandwidth and damping characteristics. The device is packaged in a space-saving 32-VFQFN package and supports industrial temperature range.

PIN ASSIGNMENT



32-Lead VFQFN
5mm x 5mm x 0.925 package body
K Package
Top View

FEATURES

- Two LVPECL outputs
Each output supports independent frequency selection at 25MHz, 125MHz, 156.25MHz and 312.5MHz
- Two differential inputs support the following input types: LVPECL, LVDS, LVHSTL, SSTL, HCSL
- Accepts input frequencies from 8kHz to 155.52MHz including 8kHz, 1.544MHz, 2.048MHz, 19.44MHz, 25MHz, 77.76MHz, 125MHz and 155.52MHz
- Attenuates the phase jitter of the input clock by using a low-cost pullable fundamental mode VCXO crystal
- VCXO PLL bandwidth can be optimized for jitter attenuation and reference tracking using external loop filter connection
- FemtoClock frequency multiplier provides low jitter, high frequency output
- Absolute pull range: 50ppm
- FemtoClock VCO frequency: 625MHz
- RMS phase jitter @ 125MHz, using a 25MHz crystal (10kHz – 20MHz): 1.3ps (maximum)
- 3.3V supply voltage
- -40°C to 85°C ambient operating temperature
- Available in lead-free (RoHS 6) package
- **For functional replacement device use 813N252CKI-02LF**

BLOCK DIAGRAM

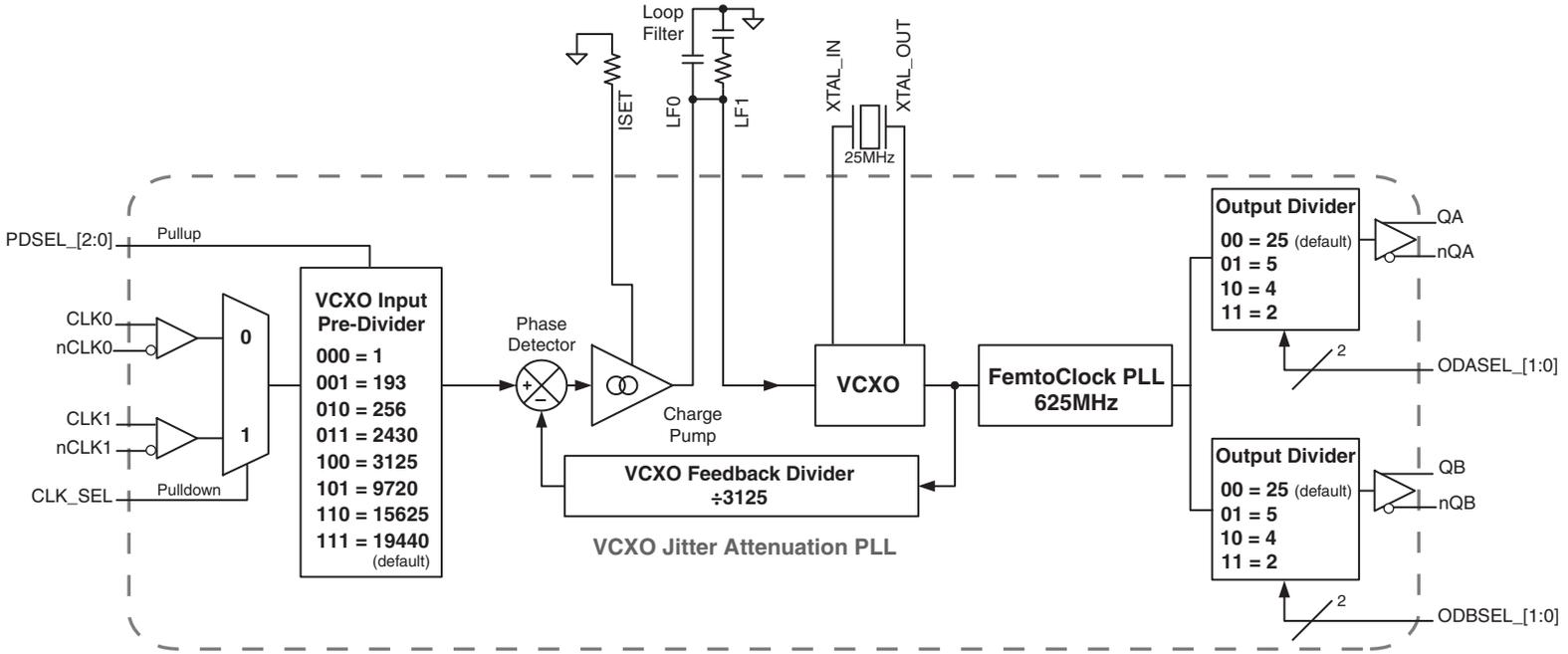


TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2	LF1, LF0	Analog Input/ Output		Loop filter connection node pins. LF0 is the output. LF1 is the input.
3	ISSET	Analog Input/ Output		Charge pump current setting pin.
4, 8, 18, 24	V _{EE}	Power		Negative supply pins.
5	CLK_SEL	Input	Pulldown	Input clock select. When HIGH selects CLK1/nCLK1. When LOW, selects CLK0/nCLK0. LVCMOS/LVTTL interface levels.
6, 12, 27	V _{CC}	Power		Core power supply pins.
7	RESERVED	Reserved		Reserved pin. Do not connect.
9, 10, 11	PDSEL_2, PDSEL_1, PDSEL_0	Input	Pullup	Pre-divider select pins. LVCMOS/LVTTL interface levels. See Table 3A.
13	V _{CCA}	Power		Analog supply pin.
14, 15	ODBSEL_1, ODBSEL_0	Input	Pulldown	Frequency select pins for Bank B output. See Table 3B. LVCMOS/LVTTL interface levels.
16, 17	ODASEL_1, ODASEL_0	Input	Pulldown	Frequency select pins for Bank A output. See Table 3B. LVCMOS/LVTTL interface levels.
19, 20	QA, nQA	Output		Differential Bank A clock outputs. LVPECL interface levels.
21	V _{CCO}	Power		Output power supply pin.
22, 23	QB, nQB	Output		Differential Bank B clock outputs. LVPECL interface levels.
25	nCLK1	Input	Pullup/ Pulldown	Inverting differential clock input. V _{CC} /2 bias voltage when left floating.
26	CLK1	Input	Pulldown	Non-inverting differential clock input.
28	nCLK0	Input	Pullup/ Pulldown	Inverting differential clock input. V _{CC} /2 bias voltage when left floating.
29	CLK0	Input	Pulldown	Non-inverting differential clock input.
30, 31	XTAL_OUT, XTAL_IN	Input		Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output.
32	V _{CCX}	Power		Power supply pin for VCXO charge pump.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C	Input Capacitance			4		pF
R	Input Pullup Resistor			51		kΩ
R	Input Pulldown Resistor			51		kΩ

TABLE 3A. PRE-DIVIDER FUNCTION TABLE

Inputs			Pre-Divider Value
PDSEL_2	PDSEL_1	PDSEL_0	
0	0	0	1
0	0	1	193
0	1	0	256
0	1	1	2430
1	0	0	3125
1	0	1	9720
1	1	0	15625
1	1	1	19440 (default)

TABLE 3B. OUTPUT DIVIDER FUNCTION TABLE

Inputs		Output Divider Value
ODxSEL_1	ODxSEL_0	
0	0	25 (default)
0	1	5
1	0	4
1	1	2

TABLE 3C. FREQUENCY FUNCTION TABLE

Input Frequency (MHz)	Pre-Divider Value	VCXO Frequency (MHz)	FemtoClock Feed-back Divider Value	Femtoclock VCO Frequency (MHz)	Output Divider Value	Output Frequency (MHz)
0.008	1	25	25	625	25	25
0.008	1	25	25	625	5	125
0.008	1	25	25	625	4	156.25
0.008	1	25	25	625	2	312.5
1.544	193	25	25	625	25	25
1.544	193	25	25	625	5	125
1.544	193	25	25	625	4	156.25
1.544	193	25	25	625	2	312.5
2.048	256	25	25	625	25	25
2.048	256	25	25	625	5	125
2.048	256	25	25	625	4	156.25
2.048	256	25	25	625	2	312.5
19.44	2430	25	25	625	25	25
19.44	2430	25	25	625	5	125
19.44	2430	25	25	625	4	156.25
19.44	2430	25	25	625	2	312.5
25	3125	25	25	625	25	25
25	3125	25	25	625	5	125
25	3125	25	25	625	4	156.25
25	3125	25	25	625	2	312.5
77.76	9720	25	25	625	25	25
77.76	9720	25	25	625	5	125
77.76	9720	25	25	625	4	156.25
77.76	9720	25	25	625	2	312.5
125	15625	25	25	625	25	25
125	15625	25	25	625	5	125
125	15625	25	25	625	4	156.25
125	15625	25	25	625	2	312.5
155.52	19440	25	25	625	25	25
155.52	19440	25	25	625	5	125
155.52	19440	25	25	625	4	156.25
155.52	19440	25	25	625	2	312.5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	
XTAL_IN	0V to V_{CC}
Other Inputs	-0.5V to $V_{CC} + 0.5V$
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	37°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		$V_{CC} - 0.15$	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{CCX}	Charge Pump Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				235	mA
I_{CCA}	Analog Supply Current				15	mA

TABLE 4B. LVCMOS / LVTTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		2		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage		-0.3		0.8	V
I_{IH}	Input High Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	$V_{CC} = V_{IN} = 3.465V$		150	μA
		PDSEL[0:2]	$V_{CC} = V_{IN} = 3.465V$		5	μA
I_{IL}	Input Low Current	CLK_SEL, ODASEL_[0:1], ODBSEL_[0:1]	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		μA
		PDSEL[0:2]	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		μA

TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK0/nCLK0, CLK1/nCLK1	$V = V = 3.465V$		150	μA
I_{IL}	Input Low Current	CLK0, CLK1	$V = 0V, V = 3.465V$	-5		μA
		nCLK0, nCLK1	$V = 0V, V = 3.465V$	-150		μA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1		0.15		1.3	
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2		$V + 0.5$		$V - 0.85$	

NOTE 1: V_{IL} should not be less than -0.3V.

NOTE 2: Common mode voltage is defined as V_{IH} .

TABLE 4D. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
V_{OL}	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to $V_{CCO} - 2V$.

TABLE 5. AC CHARACTERISTICS, $V_{CC} = V_{CCO} = V_{CCX} = 3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40^\circ C$ TO $85^\circ C$

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{IN}	Input Frequency		0.008		155.52	MHz
f_{OUT}	Output Frequency		25		312.5	MHz
j _{jit} (\emptyset)	RMS Phase Jitter (Random); NOTE 1	125MHz f_{OUT} , 25MHz crystal Inte- gration Range: 10kHz – 20MHz			1.3	ps
j _{jit} (acc)	Accumulated Jitter, RMS; NOTE 2	125MHz f_{OUT} , 25MHz crystal, 20K Cycles			10	ps
j _{jit} (pk-pk)	Peak-to-Peak Jitter	100K Random Cycles			35	ps
sk(o)	Output Skew; NOTE 2, 3				75	ps
odc	Output Duty Cycle		45		55	%
t_R / t_F	Output Rise/Fall Time	20% to 80%	200		700	ps
t_{LOCK}	PLL Lock Time				175	ms

NOTE: Characterized with outputs at the same frequency using the loop filter components for the mid loop bandwidth.

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfm. The device will meet specifications after thermal equilibrium has been reached under these conditions.

Refer to *Vcxo-PLL Loop Bandwidth Selection Table*.

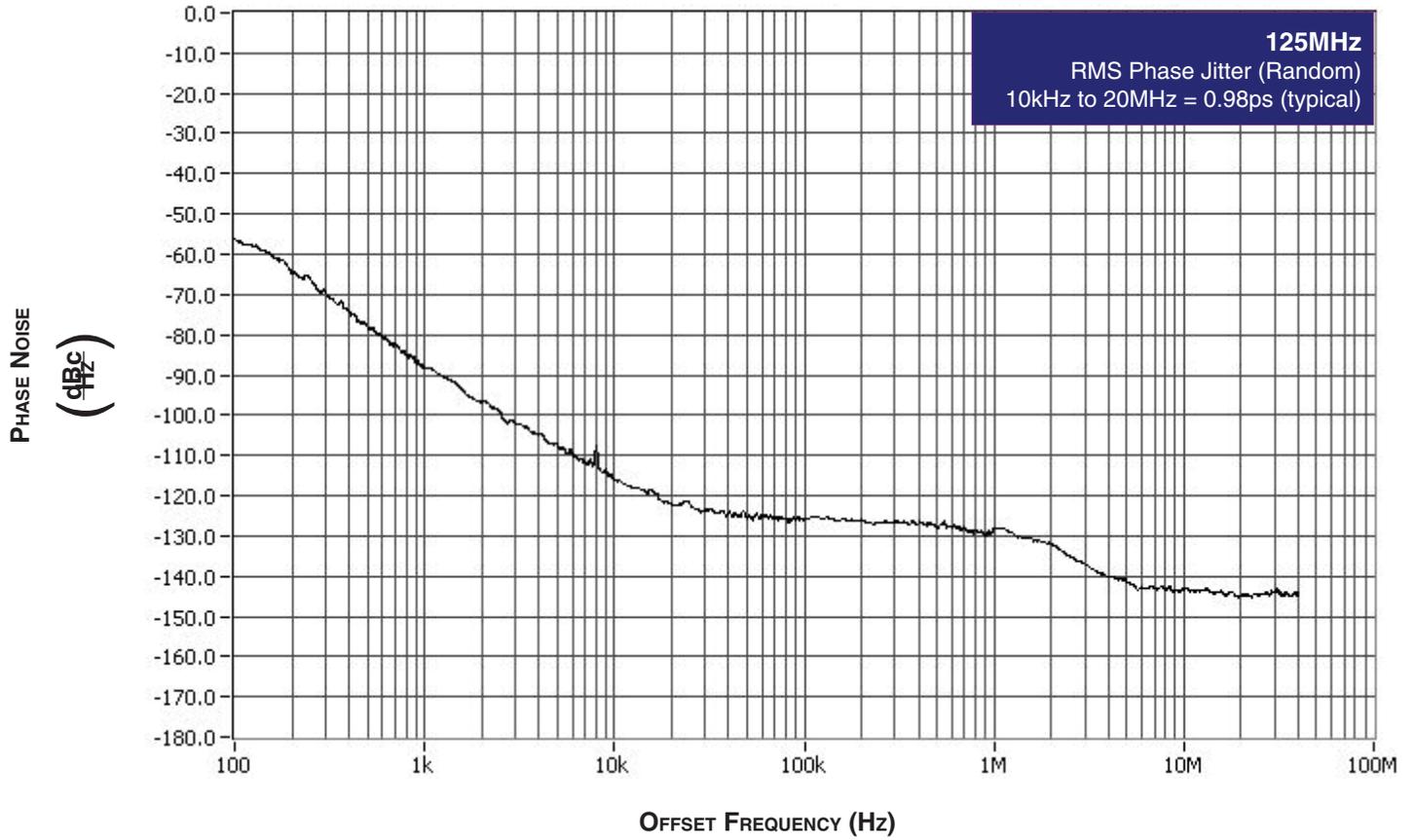
NOTE 1: Please refer to the Phase Noise Plot.

NOTE 2: This parameter is defined in accordance with JEDEC Standard 65.

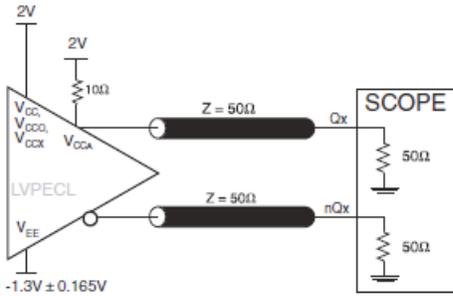
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load condions.

Measured at the output differential cross points.

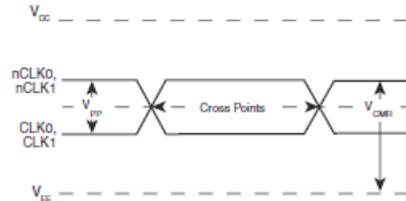
TYPICAL PHASE NOISE @ 125MHz



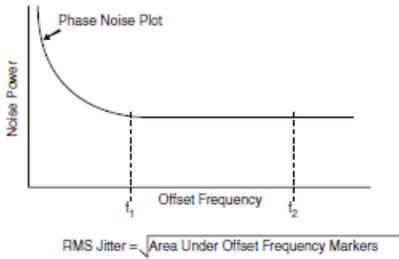
PARAMETER MEASUREMENT INFORMATION



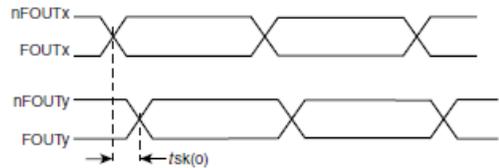
3.3V OUTPUT LOAD AC TEST CIRCUIT



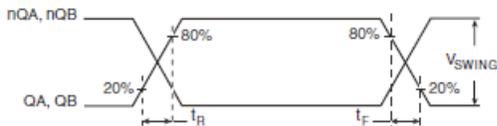
DIFFERENTIAL INPUT LEVEL



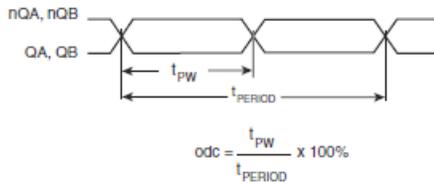
PHASE JITTER



OUTPUT SKEW



OUTPUT RISE/FALL TIME



OUTPUT DUTY CYCLE/PULSE WIDTH/tPERIOD

APPLICATION INFORMATION

POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS813252I-02 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC} , V_{CCX} , V_{CCA} , and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01 μ F bypass capacitors should be used for each pin. Figure 1 illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10 Ω resistor along with a 10 μ F bypass capacitor be connected to the V_{CCA} pin.

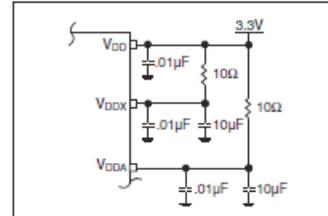


FIGURE 1. POWER SUPPLY FILTERING

WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

Figure 2 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_{REF} = V_{CC}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_{REF} in the center of the input voltage swing. For example, if the input clock swing is 2.5V and $V_{CC} = 3.3V$, R1 and R2 value should be adjusted to set V_{REF} at 1.25V. The values below are for when both the single-ended swing and V_{DD} are at the same voltage. This configuration requires that the sum of the output impedance of the driver (R_o) and the series resistance (R_s) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50 applications, R3 and R4

can be 100 Ω . The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_L cannot be less than -0.3V and V_H cannot be more than $V_{CC} + 0.3V$. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

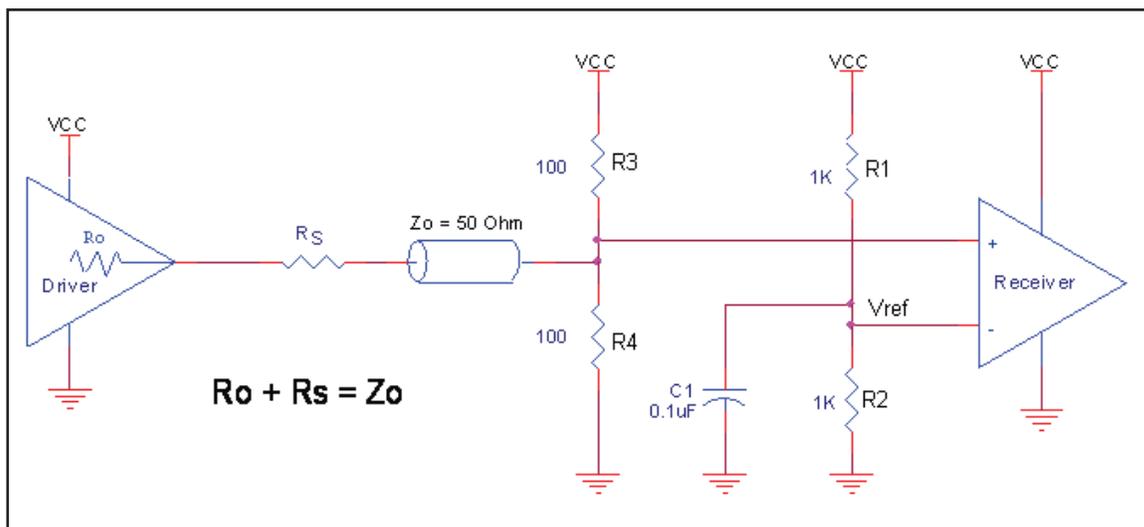


FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT

DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSSL and other differential signals. V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figures 3A to 3F show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the

driver termination requirements. For example in Figure 3A, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

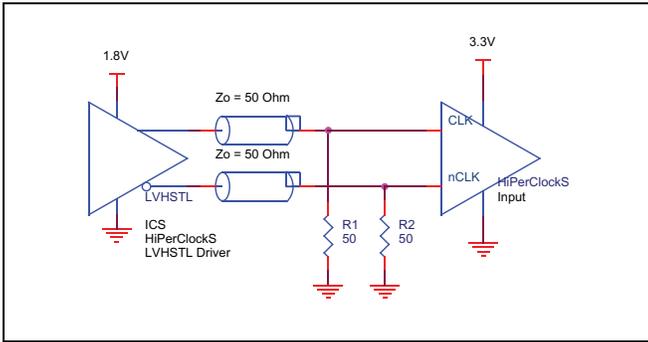


FIGURE 3A. CLK/nCLK INPUT DRIVEN BY AN IDT OPEN EMITTER LVHSTL DRIVER

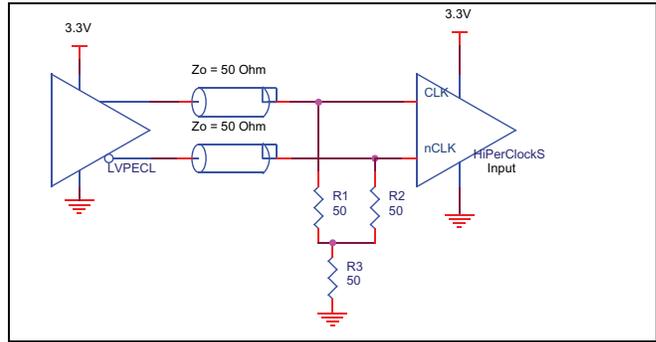


FIGURE 3B. CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

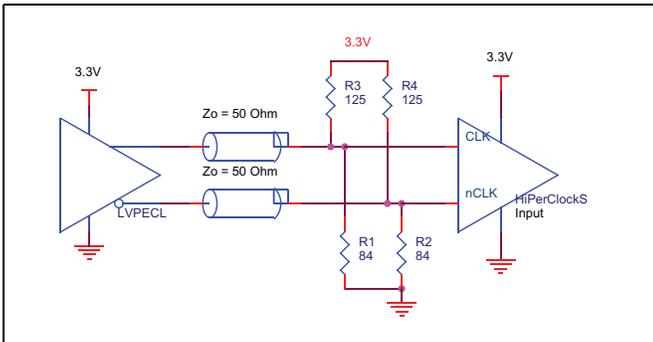


FIGURE 3C. CLK/nCLK INPUT DRIVEN BY A 3.3V LVPECL DRIVER

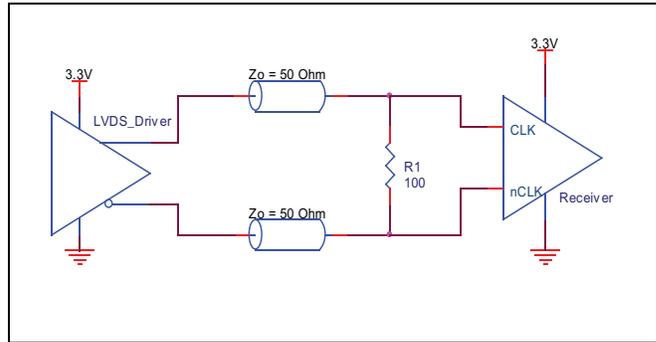


FIGURE 3D. CLK/nCLK INPUT DRIVEN BY A 3.3V LVDS DRIVER

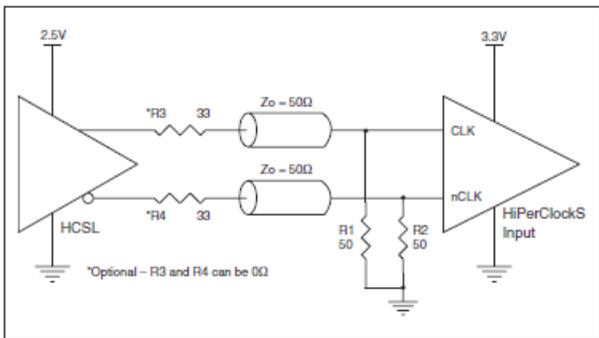


FIGURE 3E. CLK/nCLK INPUT DRIVEN BY A 3.3V HCSSL DRIVER

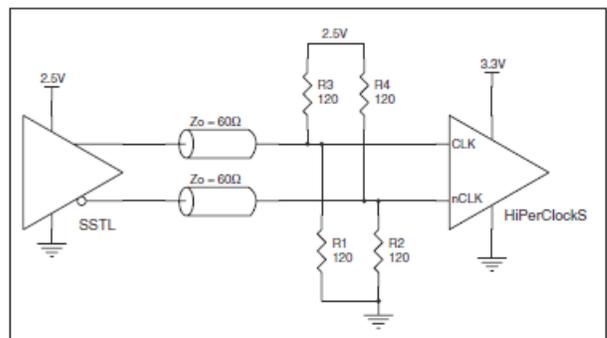


FIGURE 3F. CLK/nCLK INPUT DRIVEN BY A 2.5V SSTL DRIVER

VFQFN EPAD THERMAL RELEASE PATH

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in *Figure 4*. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical

analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, refer to the Application Note on the *Surface Mount Assembly* of Amkor’s Thermally/Electrically Enhance Leadframe Base Package, Amkor Technology.

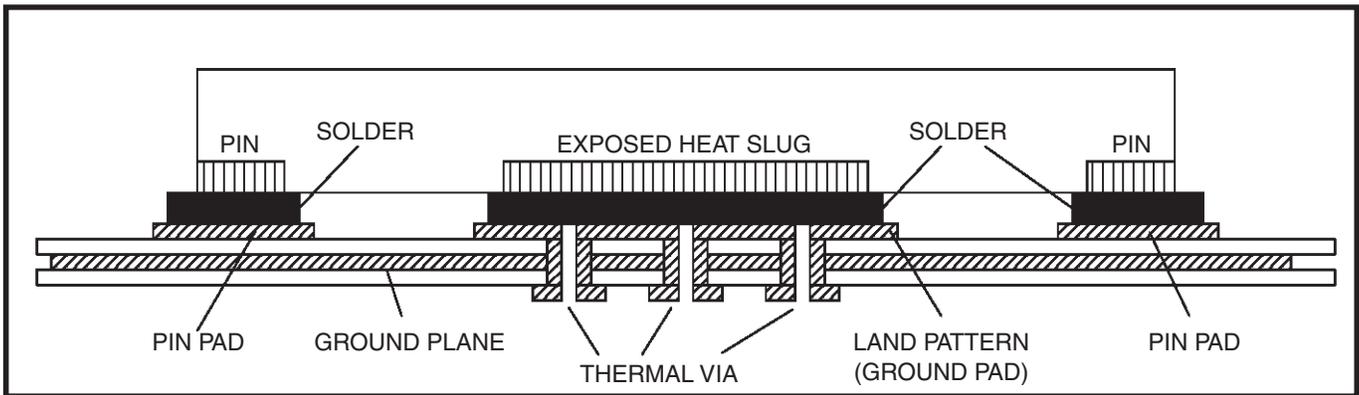


FIGURE 4. P.C.ASSEMBLY FOR EXPOSED PAD THERMAL RELEASE PATH –SIDE VIEW (DRAWING NOT TO SCALE)

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

INPUTS:

CLK/nCLK INPUTS

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

LVC MOS CONTROL PINS

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:

LVPECL OUTPUTS

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

TERMINATION FOR 3.3V LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω

transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 5A and 5B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

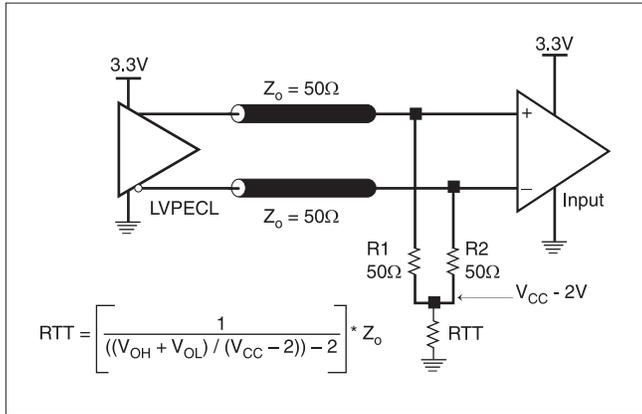


FIGURE 5A. LVPECL OUTPUT TERMINATION

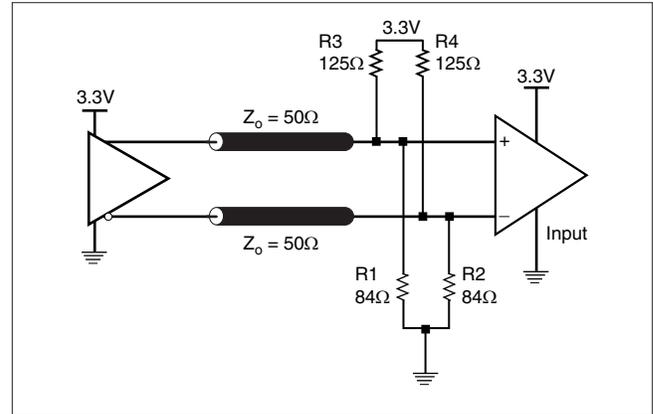


FIGURE 5B. LVPECL OUTPUT TERMINATION

SCHEMATIC EXAMPLE

Figure 6 shows an example of the ICS813252I-02 application schematic. In this example, the device is operated at $V_{CC} = V_{CCX} = V_{CCO} = 3.3V$. The decoupling capacitors should be located as close as possible to the power pin. The input is driven by a 3.3V LVPECL driver. An optional 3-pole filter can also be used for additional spur reduction. It is recommended that

the loop filter components be laid out for the 3-pole option. This will also allow the 2-pole filter to be used.

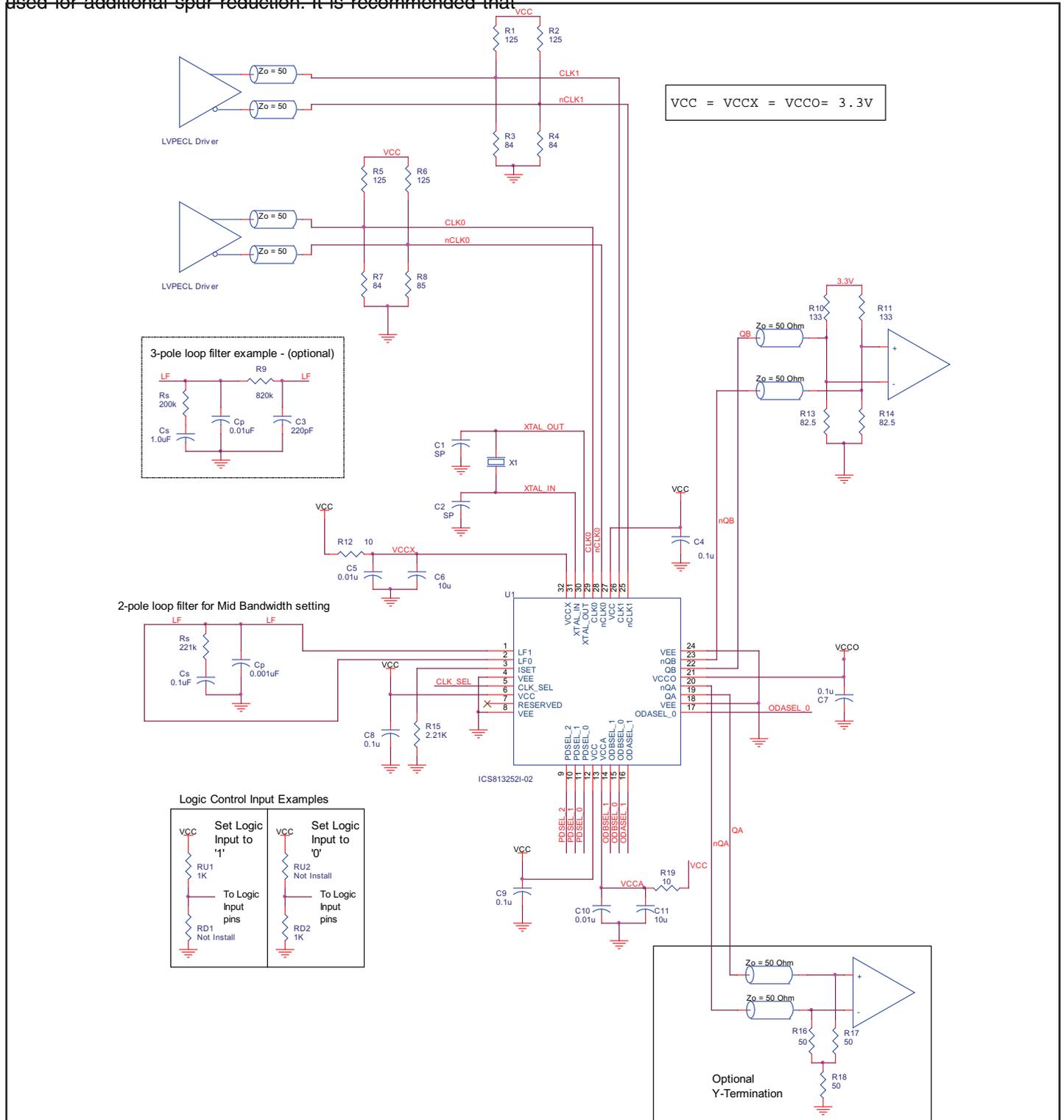


FIGURE 6. ICS813252I-02 SCHEMATIC EXAMPLE

VCXO-PLL EXTERNAL COMPONENTS

Choosing the correct external components and having a proper printed circuit board (PCB) layout is a key task for quality operation of the VCXO-PLL. In choosing a crystal, special precaution must be taken with the package and load capacitance (C_L). In addition, frequency, accuracy and temperature range must also be considered. Since the pulling range of a crystal also varies with the package, it is recommended that a metal-canned package like HC49 be used. Generally, a metal-canned package has a larger pulling range than a surface mounted device (SMD). For crystal selection information, refer to the *VCXO Crystal Selection Application Note*.

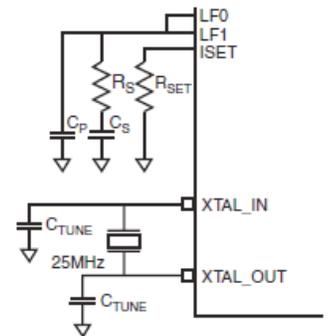
The crystal's load capacitance C_L characteristic determines its resonating frequency and is closely related to the VCXO tuning range. The total external capacitance seen by the crystal when installed on a board is the sum of the stray board capacitance, IC package lead capacitance, internal varactor capacitance and any installed tuning capacitors (C_{TUNE}).

If the crystal's C_L is greater than the total external capacitance, the VCXO will oscillate at a higher frequency than the crystal specification. If the crystal's C_L is lower than the total external capacitance, the VCXO will oscillate at a lower frequency than the

crystal specification. In either case, the absolute tuning range is reduced. The correct value of C_L is dependent on the characteristics of the VCXO. The recommended C_L in the *Crystal Parameter Table* balances the tuning range by centering the tuning curve.

The *VCXO-PLL Loop Bandwidth Selection Table* shows R_s , C_s and C_p values for recommended high, mid and low loop bandwidth configurations. The device has been characterized using these parameters. For other configurations, refer to the *Loop Filter Component Selection for VCXO Based PLLs Application Note*.

The crystal and external loop filter components should be kept as close as possible to the device. Loop filter and crystal traces should be kept short and separated from each other. Other signal traces should be kept separate and not run underneath the device, loop filter or crystal components.



VCXO CHARACTERISTICS TABLE

Symbol	Parameter	Typical	Unit
k_{VCXO}	VCXO Gain	15,700	Hz/V
C_{V_LOW}	Low Varactor Capacitance	9.9	pF
C_{V_HIGH}	High Varactor Capacitance	22.2	pF

VCXO-PLL APPROXIMATE LOOP BANDWIDTH SELECTION TABLE

Bandwidth	Crystal Frequency (MHz)	R_s (k Ω)	C_s (μ F)	C_p (μ F)	R_{SET} (k Ω)
10Hz (Low)	25MHz	121	1.0	0.01	9.09
90Hz (Mid)	25MHz	221	0.1	0.001	2.21
300Hz (High)	25MHz	680	0.1	0.0001	2.21

CRYSTAL CHARACTERISTICS

Symbol	Parameter	Minimum	Typical	Maximum	Units
f_N	Mode of Operation	Fundamental			MHz
	Frequency		25		
f_T	Frequency Tolerance			± 20	ppm
f_S	Frequency Stability			± 20	ppm
	Operating Temperature Range	-40		85	$^{\circ}$ C
C_L	Load Capacitance		10		pF
C_o	Shunt Capacitance		4		pF
C_o/C_1	Pullability Ratio		220	240	
ESR	Equivalent Series Resistance			20	
	Drive Level			1	mW
	Aging @ 25 $^{\circ}$ C			± 3 per year	ppm

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS813252I-02. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS813252I-02 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for $V_{CC} = 3.3V + 5\% = 3.465V$, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)_{MAX} = $V_{CC_MAX} * I_{EE_MAX} = 3.465V * 235mA = 814.275mW$
- Power (outputs)_{MAX} = **30mW/Loaded Output pair**
If all outputs are loaded, the total power is $2 * 30mW = 60mW$

$$\text{Total Power}_{MAX} (3.465V, \text{ with all outputs switching}) = 814.275mW + 60mW = 874.275mW$$

2. Junction Temperature.

Junction temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, T_j, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for T_j is as follows: $T_j = \theta_{JA} * Pd_total + T_A$

T_j = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_{total} = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 37°C/W per Table 6 below.

Therefore, T_j for an ambient temperature of 85°C with all outputs switching is:

$$85^\circ\text{C} + 0.874W * 37^\circ\text{C/W} = 117.3^\circ\text{C}. \text{ This is below the limit of } 125^\circ\text{C}.$$

This calculation is only an example. T_j will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 32 LEAD VFQFN, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the LVPECL output pair.

LVPECL output driver circuit and termination are shown in Figure 7.

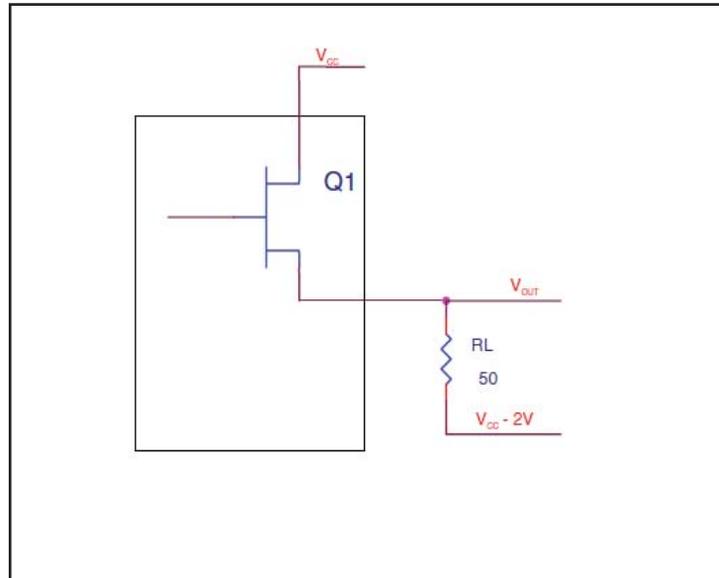


FIGURE 7. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC} - 2V$.

- For logic high, $V_{OUT} = V_{OH_MAX} = V_{CC_MAX} - 0.9V$

$$(V_{CC_MAX} - V_{OH_MAX}) = 0.9V$$

- For logic low, $V_{OUT} = V_{OL_MAX} = V_{CC_MAX} - 1.7V$

$$(V_{CC_MAX} - V_{OL_MAX}) = 1.7V$$

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$$Pd_H = [(V_{OH_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - (V_{CC_MAX} - V_{OH_MAX}))/R_L] * (V_{CC_MAX} - V_{OH_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.8mW$$

$$Pd_L = [(V_{OL_MAX} - (V_{CC_MAX} - 2V))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - (V_{CC_MAX} - V_{OL_MAX}))/R_L] * (V_{CC_MAX} - V_{OL_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

$$\text{Total Power Dissipation per output pair} = Pd_H + Pd_L = 30mW$$

RELIABILITY INFORMATION

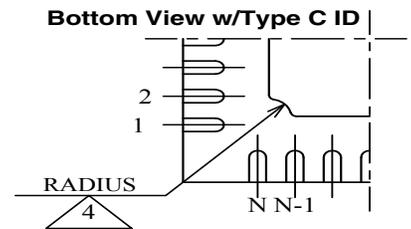
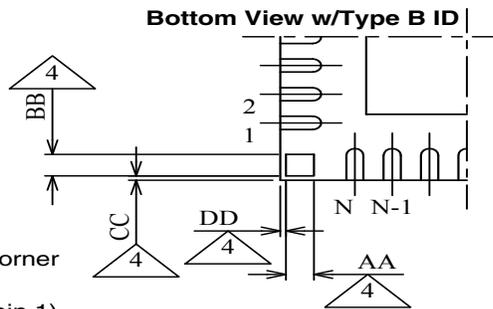
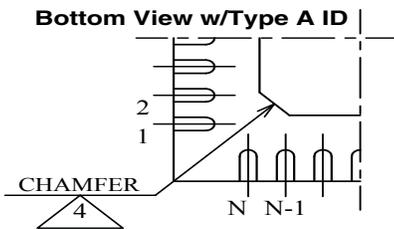
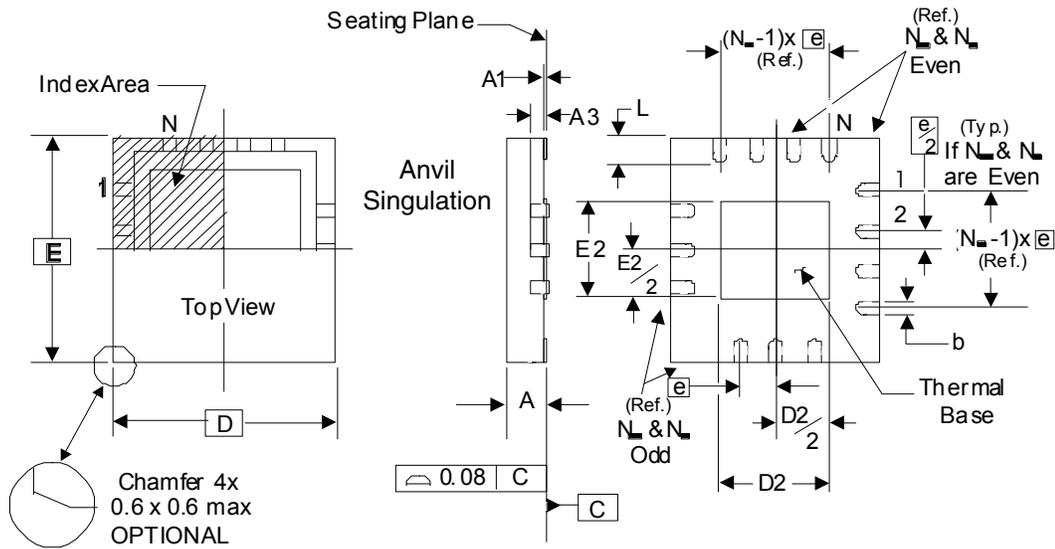
TABLE 7. θ_{JA} vs. AIR FLOW TABLE FOR 32 LEAD VFQFN

θ_{JA} vs. 0 Air Flow (Meters per Second)			
	0	1	2.5
Multi-Layer PCB, JEDEC Standard Test Boards	37.0°C/W	32.4°C/W	29.0°C/W

TRANSISTOR COUNT

The transistor count for ICS813252I-02 is: 6579

PACKAGE OUTLINE AND DIMENSIONS - K SUFFIX FOR 32 LEAD VFQFN



There are 3 methods of indicating pin 1 corner at the back of the VFQFN package are:

1. Type A: Chamfer on the paddle (near pin 1)
2. Type B: Dummy pad between pin 1 and N.
3. Type C: Mouse bite on the paddle (near pin 1)

TABLE 8. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS (VHHD -2/ -4)		
SYMBOL	Minimum	Maximum
N	32	
A	0.80	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.18	0.30
e	0.50 BASIC	
N_b	8	
N_e	8	
D, E	5.0 BASIC	
D2, E2	3.0	3.3
L	0.30	0.50

Reference Document: JEDEC Publication 95, MO-220

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
813252CKI-02LF	ICS352CI02L	32 Lead "Lead-Free" VFQFN	tray	-40°C to 85°C
813252CKI-02LFT	ICS352CI02L	32 Lead "Lead-Free" VFQFN	2500 tape & reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
A	T9	20	Ordering Information Table - added ICS prefix in the Part/Order Number.	5/6/08
	T5 T9	7 10 13 19 20	AC Characteristics Table - added Thermal Note. Updated "Wiring the Differential Input to Accept Single-ended Levels" application note. Updated Figure 5A & 5B, LVPECL Termination Output drawings. Updated Package Outline drawing. Deleted "ICS" prefix from Part/Order Number.	4/13/10
A		19	Added method package drawing. Corrected typo in inside page header. from ICS1325I-02 to ICS81325I-02.	8/25/10
A		1	Product Discontinuation Notice - PDN CQ-14-05	8/22/14
	T9	20	Features - removed reference to leaded parts Ordering Information - removed leaded devices	
A		1	Product Discontinuation Notice to Obsolete.	8/4/16

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.