Data Path Interface (DPI) to Utopia Level 1 Translation Device

IDT77010

Features

- **Single chip ATM Layer UTOPIA Level 1 to 4-bit DPI interface.**
- **Supports ATM Forum UTOPIA Level 1 interface.**
- **Supports ATM device interface in Cell mode.**
- **Capable of full-duplex operation up-to 160 Mbps.**
- **Utility bus interface to access PHY registers.**
- **In-stream control to access PHY registers.**

Description

The 77010 interfaces a UTOPIA PHY device to a device that uses a Data Path Interface (DPI). Examples of PHY devices may include the IDT77105, and the IDT77V400 Switching Memory is an example of a component that utilizes a DPI interface. Figure 1 illustrates a typical application using the IDT77010.

The UTOPIA level 1 bus interface runs at speeds up to 155 Mbps, with the DPI-4 interface capable of full duplex operation at 160 Mbps.

In-stream programming is used to read and write to the PHY registers, with the Control Cells being generated from a remote controlling agent. The Control Cells are used to configure, control and retrieve status of the PHY device.

Theory of Operation

UTOPIA receive cells are transferred to the DPI-4 interface one cell at a time. The DPI-4 clock rate is twice the frequency of receive UTOPIA clock.

DPI-4 transmit cells are transferred to the UTOPIA transmit bus one cell at a time. Transmit flow control is used to match the transmit cell rate to the PHY's transmit cell rate.

Control cells are inserted and decoded by the control cell decoder. The control cells are filtered and will not be transferred to the UTOPIA transmit bus.

The control cell decoder block identifies the control cells and signals the Utility Bus Interface to execute the commands. For a Utility bus write command cell, the Utility bus does a one byte write to the specified Utility bus address. For a Utility bus read command cell, the Utility bus reads one byte from the specified Utility bus address and loads this byte to the Cell Generator logic. The Cell Generator makes a request to the receive cell arbiter to process the cell, and generates a status cell if no UTOPIA receive cell is detected.

A status cell is a complete ATM cell generated and loaded to the Receive DPI-4 I/F logic.

A receive cell on the DPI-4 bus is either an ATM cell from the receive UTOPIA bus or a status ATM cell locally generated. Internally generated ATM cells are output to the Receive DPI-4 Interface only when there are no UTOPIA Receive cell. Figure 2 below shows the device data flow.

Block Diagram

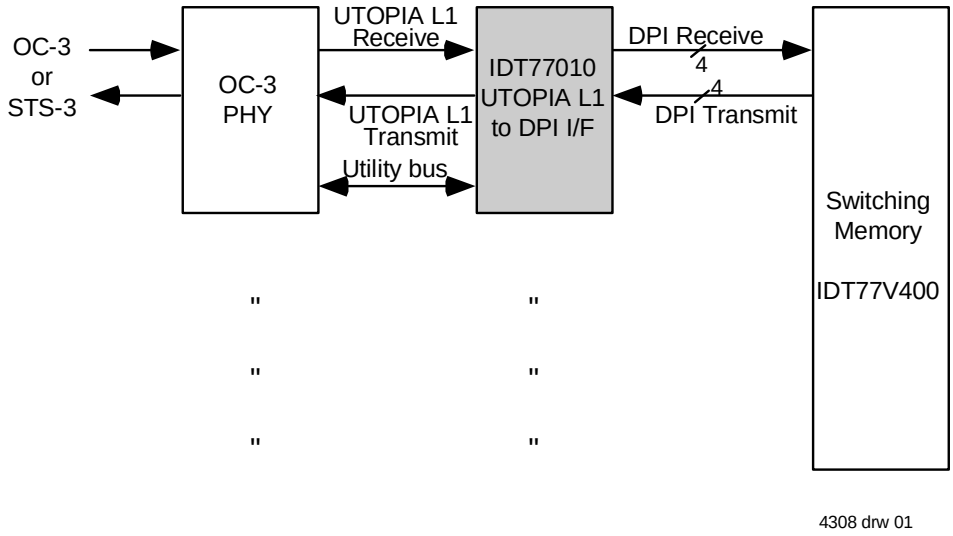


Figure 1 Typical IDT77010 Application

Block Diagram

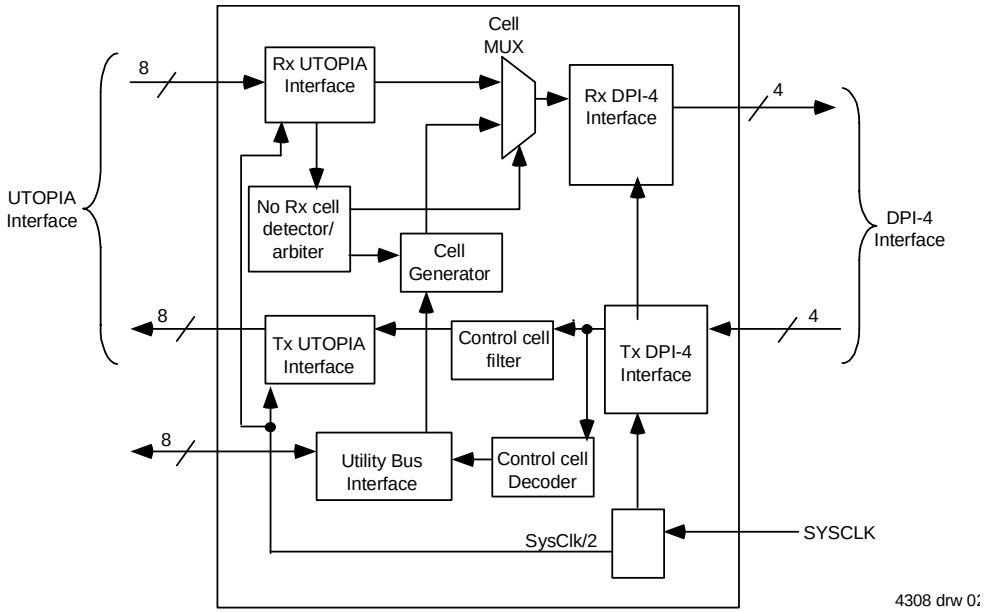
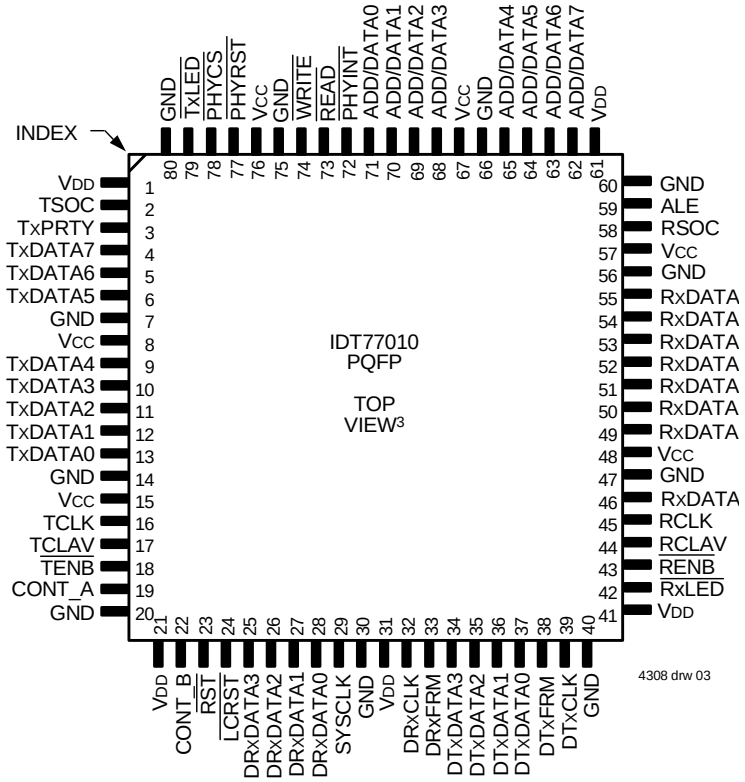


Figure 2 Functional Block Diagram

Pin Configuration[1,2]



1. All power pins must be connected to the appropriate power supply. VCC pins to 5.0V ± 0.25V; VDD pins to 3.3V ± 0.3V.
2. All GND pins must be connected to ground supply.
3. This text does not indicate orientation of the actual part-marking.

Pin Definitions

Signal Name	Pin Number	Input/ Output	Description
SysClk	29	I	System Clock. All the device circuits are synchronized to this clock.
$\overline{RST}$	23	I	System Reset. When low the 77010 and the PHY are reset. This is used as a global line card reset where all the $\overline{RST}$ signals from all line cards are connected together.
$\overline{LCRST}$	24	I	Line Card reset. When low the 77010 and the PHY are reset. This is a local line card reset used to reset a specific 77010 and PHY on a specific line card.
CONT_A	19	O	Output Control Pin A. This pin is controlled by a receive control cell. Default output = low.
CONT_B	22	O	Output Control Pin B. This pin is controlled by a receive control cell. Default output = low.
RxLED	42	O	Active low. When low a receive cell is being transferred. This pin may be used for receive activity LED.
TxLED	79	O	Active low. When low a transmit cell is being transferred. This pin may be used for transmit activity LED.
$\overline{READ}$	73	O	Utility bus read signal.
$\overline{WRITE}$	74	O	Utility bus write signal.
ALE	59	O	Utility bus address latch enable. Used for latching the address on the address phase of the Add/Data bus.
Add/Data0	71	I/O	Utility bus multiplexed address and data bus.
Add/Data1	70	I/O	Utility bus multiplexed address and data bus.
Add/Data2	69	I/O	Utility bus multiplexed address and data bus.
Add/Data3	68	I/O	Utility bus multiplexed address and data bus.
Add/Data4	65	I/O	Utility bus multiplexed address and data bus.
Add/Data5	64	I/O	Utility bus multiplexed address and data bus.
Add/Data6	63	I/O	Utility bus multiplexed address and data bus.
Add/Data7	62	I/O	Utility bus multiplexed address and data bus.
$\overline{PHYCS}$	78	O	Utility bus PHY chip select.
$\overline{PHYINT}$	72	I	Utility bus PHY interrupt signal
$\overline{PHYRST}$	77	O	Utility bus PHY reset.
RCLK	45	O	UTOPIA bus receive clock.
RSOC	58	I	UTOPIA bus receive start of cell.
$\overline{RENB}$	43	O	UTOPIA bus receive enable.
RCLAV	44	I	UTOPIA bus receive cell available.
RxData0	46	I	UTOPIA bus receive data bit.
RxData1	49	I	UTOPIA bus receive data bit.
RxData2	50	I	UTOPIA bus receive data bit.
RxData3	51	I	UTOPIA bus receive data bit.
RxData4	52	I	UTOPIA bus receive data bit.
RxData5	53	I	UTOPIA bus receive data bit.
RxData6	54	I	UTOPIA bus receive data bit.

Signal Name	Pin Number	Input/ Output	Description
RxData7	55	I	UTOPIA bus receive data bit.
$\overline{\text{TENB}}$	18	O	UTOPIA bus Transmit enable.
TCLK	16	O	UTOPIA bus transmit clock.
TCLAV	17	I	UTOPIA bus transmit cell available.
TSOC	2	O	UTOPIA bus transmit start of cell.
TxData0	13	O	UTOPIA bus transmit data bit.
TxData1	12	O	UTOPIA bus transmit data bit.
TxData2	11	O	UTOPIA bus transmit data bit.
TxData3	10	O	UTOPIA bus transmit data bit.
TxData4	9	O	UTOPIA bus transmit data bit.
TxData5	6	O	UTOPIA bus transmit data bit.
TxData6	5	O	UTOPIA bus transmit data bit.
TxData7	4	O	UTOPIA bus transmit data bit.
TxPrty	3	O	UTOPIA bus transmit data parity bit.
DTxClk	39	O	DPI-4 bus transmit clock. 3.3V Interface.
DTxFRM	38	I	DPI-4 bus transmit start of frame. 3.3V Interface.
DTxData0	37	I	DPI-4 bus transmit data bit. 3.3V Interface.
DTxData1	36	I	DPI-4 bus transmit data bit. 3.3V Interface.
DTxData2	35	I	DPI-4 bus transmit data bit. 3.3V Interface.
DTxData3	34	I	DPI-4 bus transmit data bit. 3.3V Interface.
DRxClk	32	O	DPI-4 bus receive clock. 3.3V Interface.
DRxFRM	33	O	DPI-4 bus receive start of frame. 3.3V Interface.
DRxData0	28	O	DPI-4 bus receive data bit. 3.3V Interface.
DRxData1	27	O	DPI-4 bus receive data bit. 3.3V Interface.
DRxData2	26	O	DPI-4 bus receive data bit. 3.3V Interface.
DRxData3	25	O	DPI-4 bus receive data bit. 3.3V Interface.
V_{CC}	8,15,48,57,67,76	Power	5.0V Power Supply Pins.
V_{DD}	1,21,31,41,61	Power	3.3V Power Supply Pins for DPI Interface.
GND	7,14,20,30,40,47 ,56,60,66,75,80	GND	Ground Pins.

1. All signals are 5.0V unless otherwise indicated.

2. 3.3V signals are 5.0V tolerant.

Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{CC}	5V Digital Supply Voltage	-0.3	6.0	V
V_{DD}	3.3V Digital Supply Voltage	-0.3	4.6	V
V_{IN}	Digital Input Voltage	V_{SS}	V_{CC} + 0.5	V
I_{OUT}	Output Current	___	50	mA
T_{STG}	Storage Temperature	-55	140	°C

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{CC}	5V Digital Supply Voltage	4.75	5.25	V
V_{DD}	3.3V Digital Supply Voltage	3.0	3.6	V
V_{IN}	TTL Input Voltage	-0.3	VCC+0.3	V
T_A	Operating Temperature	0	70	°C
titr	Input TTL rise time	___	2	ns
titf	Input TTL fall time	___	2	ns
V_{IH}	TTL Input High Voltage	2.0	___	V
V_{IL}	TTL Input Low Voltage	___	0.8	V

DC Electrical Characteristics

Symbol	Parameter	Test Conditions	77010		Unit
			Min	Max	
[I_{LI}]	Input Leakage Current	V_{CC} = 5.5V, VIN = 0V to VCC	10	10	µA
[I_{LO}]	Output Leakage Current	V_{OUT} = 0V to VCC	10	10	µA
V_{OH}	TTL Output High Voltage	I_{OH} = -4mA	2.4	___	V
V_{OL}	TTL Output Low Voltage	I_{OL} = +4mA	___	0.4	V
I_{DD}	Power Supply Current	155.52 Mbps	___	60	mA
I_{CC}	Power Supply Current	155.52 Mbps	___	12	mA

Capacitance

Symbol	Parameter	Test Conditions	Min	Type	Max	Unit
C_{IN}	Input Capacitance	All Inputs	___	4	___	pF
C_{OUT}	Output Capacitance	All Outputs	___	6	___	pF
C_{BID}	Bi-Directional Capacitance	All Bi-directional Pins	___	10	___	pF

Device Interface

This 77010 uses a UTOPIA level 1 interface to receive and transmit ATM cells to and from the PHY device. It mirrors the ATM layer as shown in Figure 3 below.

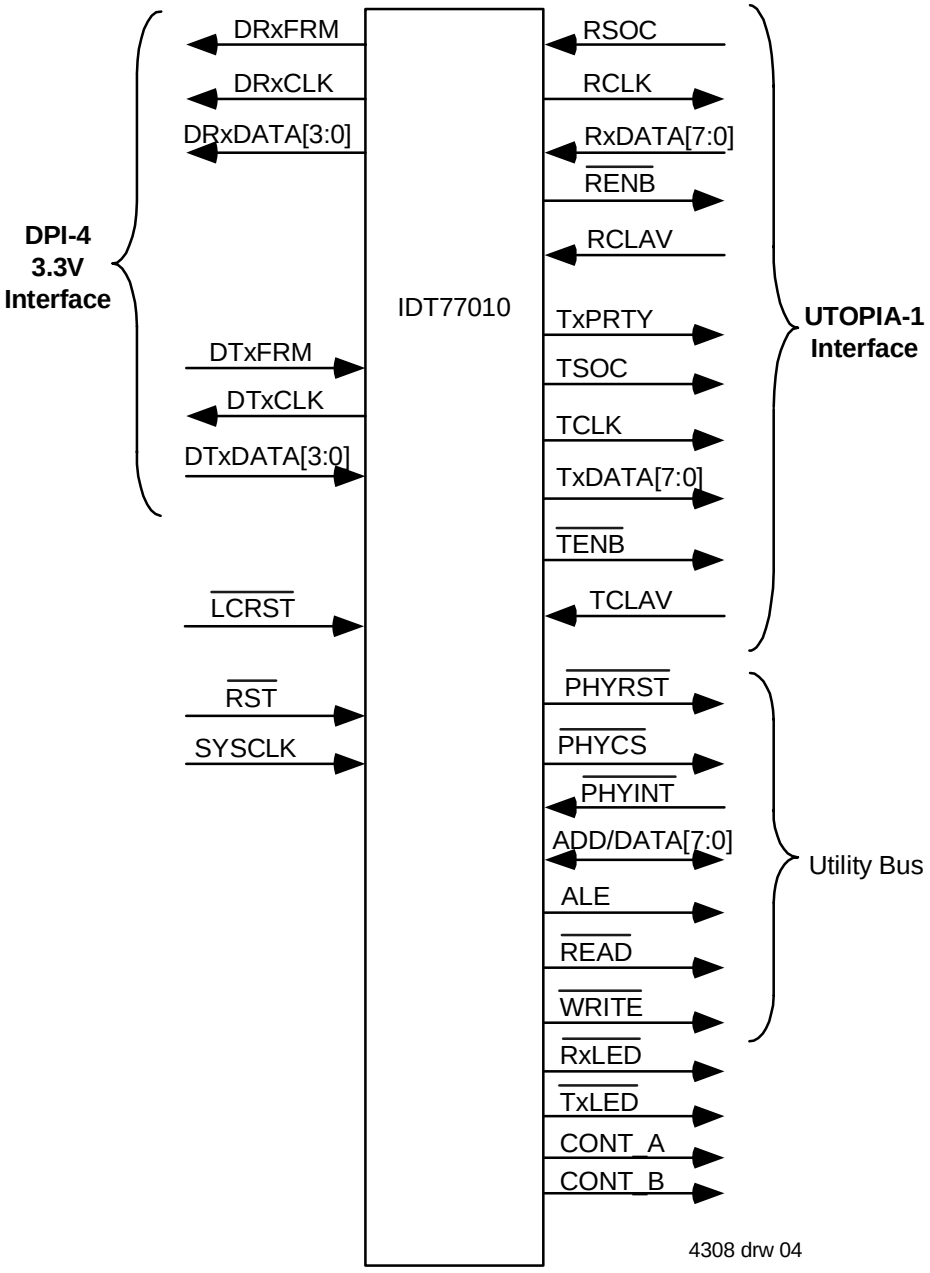


Figure 3 DPI-4 to UTOPIA 1 Interface Device

UTOPIA Receive Interface Operation

UTOPIA cell level handshake is used to receive an ATM cell from a UTOPIA PHY device. The UTOPIA Receive Clock (RCLK) is a continuous clock generated from the System Clock (SYSCLK) and is half the frequency of the DPI Receive Clock (DRxCLK).

The receive cell header, including the HEC, and payload are transferred over the Receive Data bus (RxDATA[7:0]), which is 8-bits wide. Receive Parity (RxPRTY) is not supported by the 77010, nor does it calculate the HEC in the header field.

The 77010 will assert Receive Enable ($\overline{\text{RENB}}$) low two clock cycles after detecting a high Receive Cell Available (RCLAV), if it is not executing a control cell. Refer to the UTOPIA Receive Flow Control section for description on muxing internally generated control cells with UTOPIA receive cells.

Once Receive Start Of Cell (RSOC) is detected the 77010 will receive the entire cell without interruption.

UTOPIA Receive Flow Control

The UTOPIA data rate is higher than the cell rate on the transport media. This provides additional bandwidth for the insertion of control cells.

The 77010 will only generate an internal control cell when RCLAV and $\overline{\text{RENB}}$ are de-asserted and a cell transfer is not taking place. When a control cell is inserted $\overline{\text{RENB}}$ is de-asserted high for 55 RCLK cycles, which prevents the PHY from transferring a cell. During this 55 clock period the 77010 inserts the control cell and sends it out to the DPI receive interface.

Internally generated control cells should be paced so that the sum of receive UTOPIA status cells and internally generated control cells do not exceed 160 Mbps.

The PHY is expected to buffer at least two receive cells for the flow control to function without the loss of a cell. Figure 4 shows the receive cell muxing with the internally generated status cells.

UTOPIA Transmit Interface Operation

UTOPIA cell level handshake is used to transfer an ATM cell to a UTOPIA PHY device. The UTOPIA Transmit Clock (TCLK) is a continuous clock generated from the System Clock (SYSCLK) and is half the frequency of the DPI Transmit Clock (DTxCLK).

Two TCLK cycles after detection of a high Transmit Cell Available (TCLAV) the 77010 will assert $\overline{\text{TENB}}$ low. One TCLK cycle after $\overline{\text{TENB}}$ assertion the 77010 will assert Transmit Start Of Cell (TSOC) and the first valid byte of data. TSOC is one TCLK cycle long and coincides with the first valid byte of data (TxDATA[7:0]). When the entire cell has been transferred the 77010 will sample TCLAV for cell availability.

The PHY will de-assert TCLAV if it cannot accept another cell. The 77010 will continue transferring the current cell and store up to nine bytes of the next cell in its pipeline if TCLAV is de-asserted during a cell transfer.

Control cells from the DPI interface are filtered and not forwarded to the transmit UTOPIA bus.

Figure 5 shows UTOPIA transmit data flow.

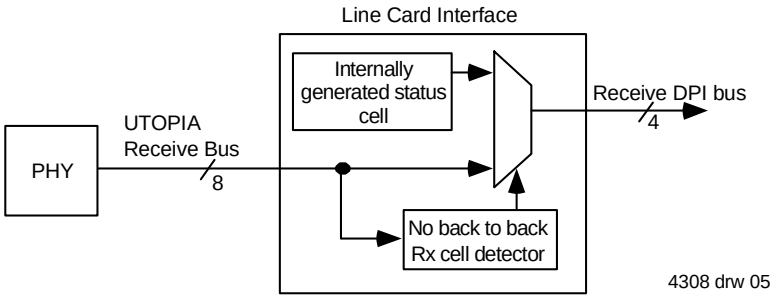


Figure 4 UTOPIA Receive Data Flow

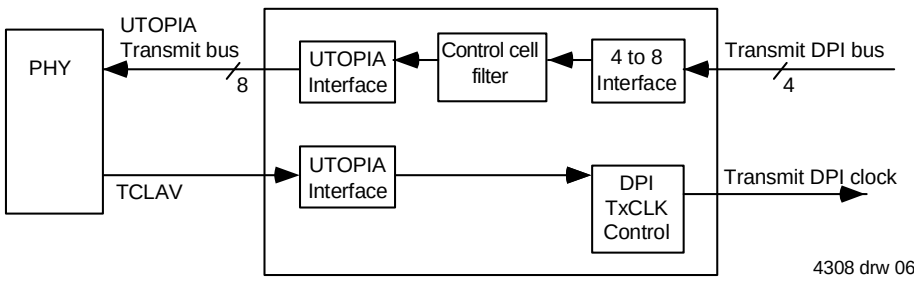


Figure 5 UTOPIA Transmit Data Flow

Input Control Cell Formatting

Control cells are generated by a remote computer and are used to configure and monitor the PHY registers. All cells having the header VPI = 0x00 hex and VCI = 0x1F hex (VCI bits 11-4) are decoded and executed as control cells by the 77010.

Control Cell Filter Operation

All cells transferred over the DTxDATA[3:0] bus are tested to see if they are control cells.Cells containing the header VPI = 00 Hex and VCI = 1F Hex (VCI bits 11-4) are filtered as control cells and not forwarded to the TxDATA[7:0] bus. The filter ignores the GFC, PTI and CLP bits. The default control cell identifier value is 00x1F. It can be programmed to a user defined value via the Change Control Cell Address Command (see page 16).

Control Cell Frequency

The control cells arrive multiplexed with data cells in random combinations, and are terminated (filtered) by the 77010.

The RxDATA[3:0] bus multiplexes the receive UTOPIA cells and any internally generated control cells. The control cell is ignored if a previous control cell is being executed at that time. A gap in the UTOPIA cell stream must occur before the new control cell is processed, because the UTOPIA receive cells have higher priority.

Control cells may be input back-to-back. However, the second control cell will not be processed and could be dropped, even though the 77010 can filter both of them. Worst case condition is when the receive UTOPIA bus is at full rate. In this case it is recommended that the control cells be at least 50 cells apart.

DPI Interface Operation

Data Path Interface (DPI) is a synchronous bus interface designed to transfer ATM cells between two devices. The 77010 contains a DPI-4 bus interface, which contains a four bit wide data bus. Therefore, 107 clock cycles are required to transfer a 53 byte ATM cell.

The 77010 has separate DPI-4 transmit and receive interfaces, with each requiring six signals. The signals are a clock, a start of cell marker and a four bit data bus. All signals are sampled on the rising edge of their respective clock.

Transmit DPI Bus Interface

The Transmit DPI Clock (DTxCLK) is generated from SYSCLK and is twice the frequency of TCLK. This clock is not continuous and is used to control data flow to the PHY device. DTxCLK is initially low and not driven until the 77010 detects a high TCLAV from the PHY device. On the rising edge of DTxCLK the 77010 samples Transmit Start of Cell (DTxFRM), which is generated by the transmitting device for one DTxCLK cycle. When DTxFRM is asserted high the 77010 will sample valid data (DTxDATA[3:0]) on the next rising edge of DTxCLK. Cell transfer will continue without interruption once it has started.

When TCLAV is de-asserted low the current cell is transferred and DTxCLK goes low until another high TCLAV is detected.

DTxFRM and DTxDATA[3:0] are sampled on the rising edge of DTxCLK.

Control ATM Cell Format

Cell Byte Number	Bit Number	Function Name	Bit Contents	Description
0	7-4	GFC	0xX	Don't care.
0	3-0	VPI 7-4	0x0	Must be set to 0x0.
1	7-4	VPI 3-0	0x0	Must be set to 0x0.
1	3-0	VCI 15-12	0x0	Must be set to 0x0.
2	7-0	VCI 11-4	0xYY	Special VCI value for control and status cells. Default is 0x1F.[1]
3	7-4	VCI 3-0	0x0	Don't care.
3	3-1	PTI	000'b	Don't care.
3	0	CLP	0'b	Don't care.
4	7-0	HEC	0x00	Don't care.
5	7-0	Command	00-FF Hex	Command cell byte.
6	7-0	Data A	0x0 - 0xFF	Parameter for control cell.
7	7-0	Data B	0x0 - 0xFF	Parameter for control cell.
8	7-0	reserved	0x00	Always set to 0x00.

Cell Byte Number	Bit Number	Function Name	Bit Contents	Description
.	7-0	reserved	0x00	Always set to 0x00.
.	7-0	reserved	0x00	Always set to 0x00.
52	7-0	reserved	0x00	Always set to 0x00.

1. This value can be programmed by instream control cells.

DPI Bus Data Sequence

For Transmit and Receive DPI bus in the 53 byte configuration, the following table shows the data nibble sequence.

DPI Nibble Count	DPI Content	Comments
0	GFC [3:0]	GFC bits for the ATM cell header. First nibble to be transmitted/received.
1	VPI [7:4]	VPI bits MSB of the ATM cell header.
2	VPI [3:0]	VPI bits LSB of the ATM cell header.
3	VCI [15:12]	VCI bits MSB of the ATM cell header.
4	VCI [11:8]	VCI bits of the ATM cell header.
5	VCI [7:4]	VCI bits of the ATM cell header.
6	VCI [3:0]	VCI bits of the ATM cell header.
7	PTI [2:0], CLP	PTI and CLP bits of the ATM cell header.
8	HEC [7:4]	HEC Most Significant nibble.
9	HEC [3:0]	HEC Least Significant nibble.
10	First data byte [7:4]	First data Most Significant nibble of the ATM cell header.
11	First data byte [3:0]	First data Least Significant nibble of the ATM cell header.
____	____	____
____	____	____
104	Last data byte [7:4]	Last data byte Most Significant nibble of the ATM cell.
105	Last data byte [3:0]	Last data byte Least Significant nibble of the ATM cell.

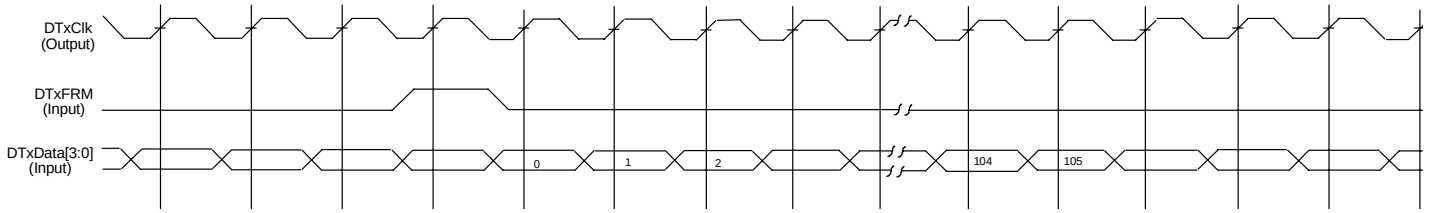


Figure 6 DPI-4 Transmit Bus with only one cell

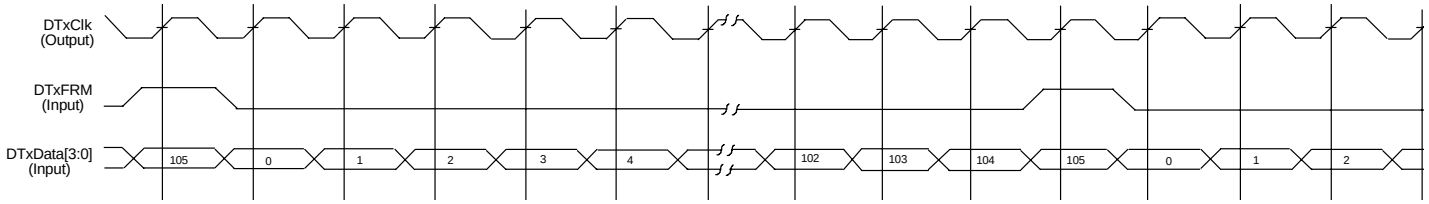


Figure 7 DPI-4 Transmit Bus with back to back cell

Receive DPI Bus Interface

The Receive DPI Clock (DRxCLK) is a continuous clock generated from SYSCLK and is twice the frequency of RCLK. The Receive Start of Cell marker (DRxFRM) is also generated by the 77010 and is asserted for one clock cycle prior to the first nibble of valid data (DRxDATA[3:0]).

There is no flow control in the receive DPI path. It is assumed that the receiving device can accept the incoming cell.

DRxFRM and DRxDATA[3:0] are sampled on the rising edge of DRxCLK.

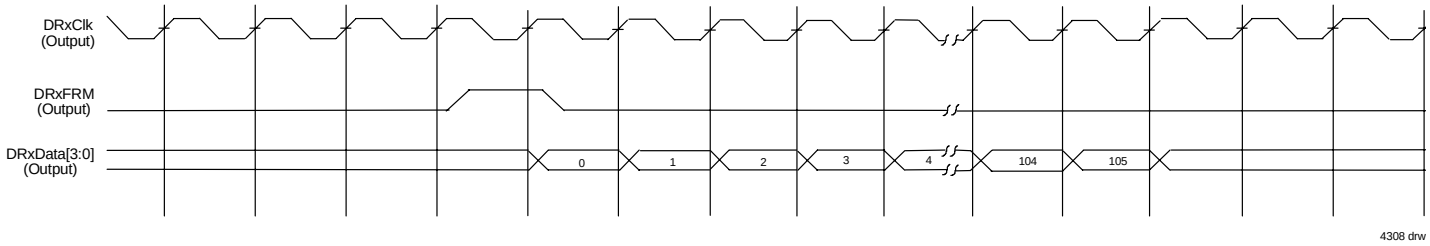


Figure 8 DPI-4 Receive Bus with only one cell

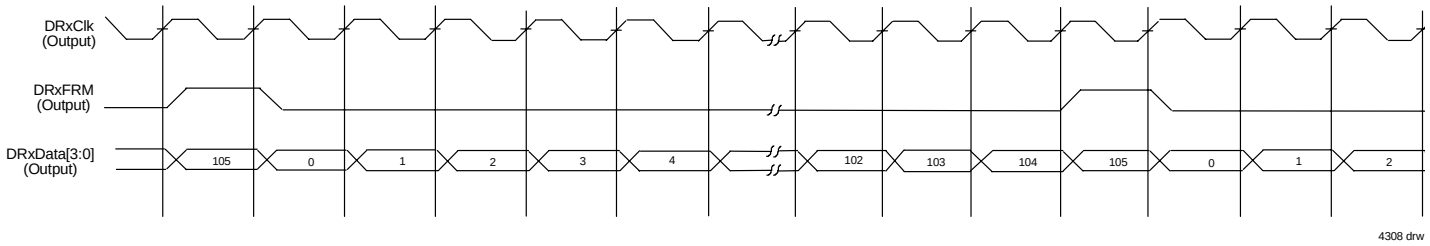


Figure 9 DPI-4 Receive Bus with back to back cell

Utility Bus

The Utility bus is used for accessing the internal PHY registers. An 8-bit read or write command is implemented via instream (in-band) programming to access the registers. The commands are input to the 77010 via the DPI-4 transmit path. The PHY register commands are decoded by the 77010 and executed using the Utility bus.

Figure 10 shows the Utility bus interface.

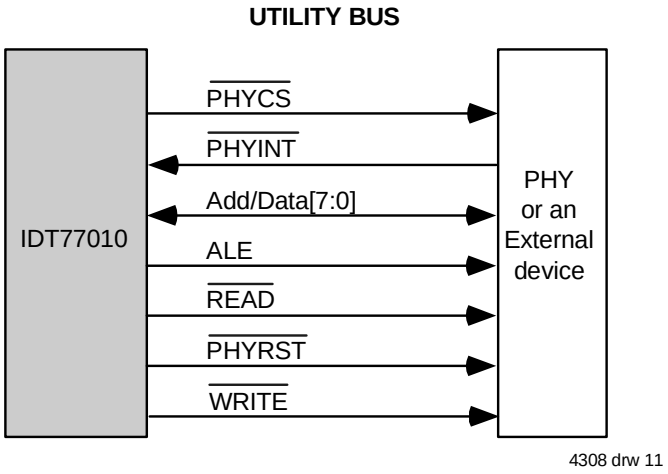


Figure 10 Utility Bus Interface

Utility Bus Read Operation

When the 77010 decodes the command cells for a Utility bus read operation, it drives the PHY chip select ($\overline{\text{PHYCS}}$), Address Latch Enable (ALE),Read($\overline{\text{READ}}$) and the Address Data bus (Add/Data[7:0]). At the falling edge of ALE, the PHY samples the address phase of the Add/Data[7:0]. The 77010 then floats the Add/Data[7:0] bus. The PHY drives the Add/Data[7:0] bus until rising edge of PHYCS or $\overline{\text{READ}}$. See Figure 11 below.

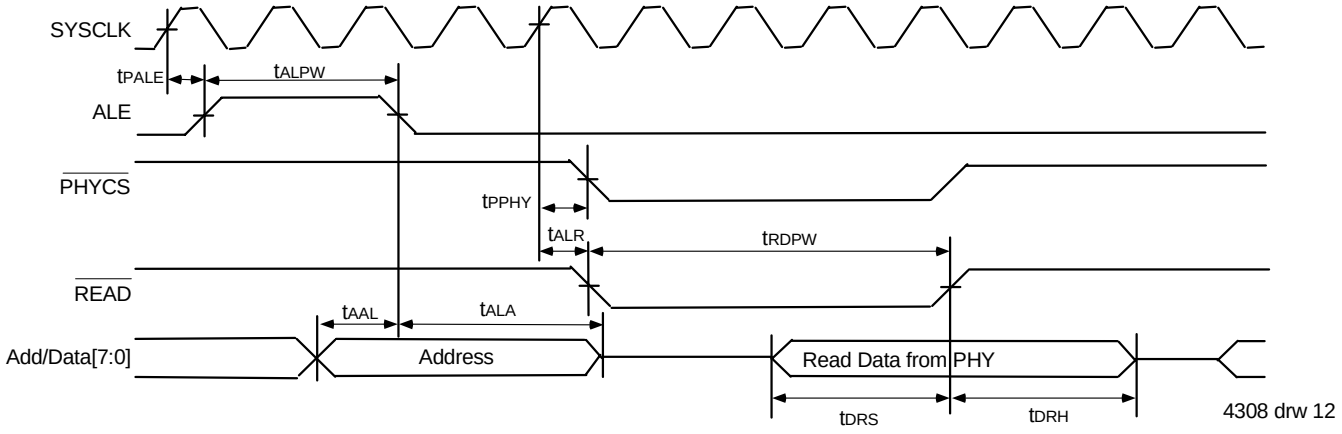


Figure 11 Utility Bus Read Operation

Utility Bus Write Operation

When the 77010 decodes the command cell for a Utility bus write operation, it drives the PHY chip select ($\overline{\text{PHYCS}}$), Address Latch Enable (ALE), Write ($\overline{\text{WRITE}}$), and the Address Data bus (Add/Data[7:0]). At the falling edge of ALE, the PHY samples the address phase of the Add/Data[7:0]. The PHY samples the write data byte on the Add/Data[7:0] bus at the rising edge of $\overline{\text{PHYCS}}$ or $\overline{\text{WRITE}}$. See Figure 12 below.

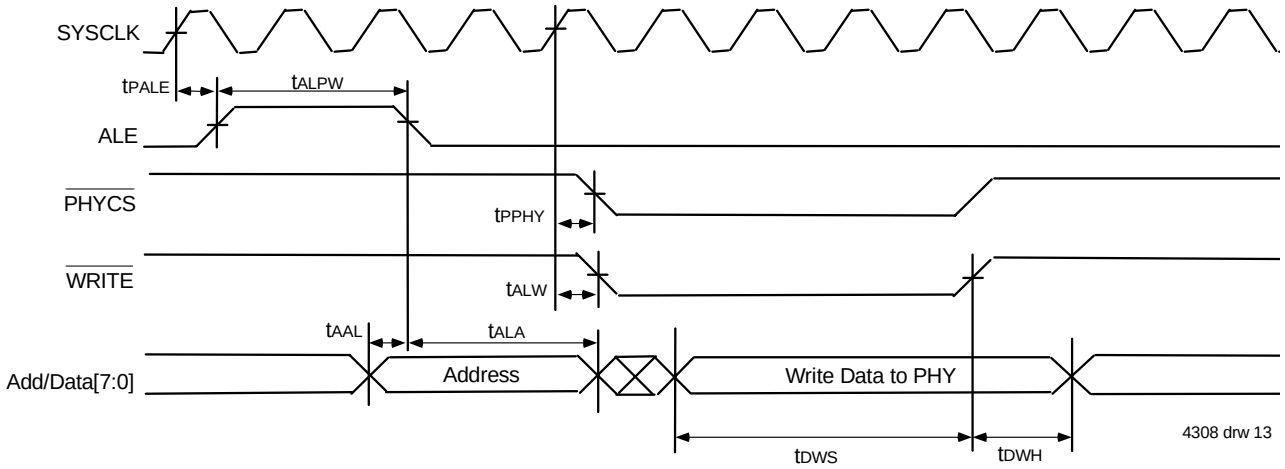


Figure 12 Utility Bus Write Operation

Reply Command Cell

Interrupt Reply Cell Notification

Return command cell indicating an interrupt has occurred on the Utility bus.

Command Fields	Field Value (Hex)	Description
Command	00	Interrupt Cell Return Command
DataA	xx	See Data A and Data B Tables on page 14.
DataB	xx	See Data A and Data B Tables on page 14.

Command Cells

Reset PHY Chip Command

Resets the PHY device and the Utility bus. $\overline{\text{PHYRST}}$ will assert low for 16 SYSCLK cycles. This command does not generate nor return a command cell.

Command Fields	Field Value (Hex)	Description
Command	01	Reset Phy Chip.
DataA	xx	Don't care. It may contain any number.
DataB	xx	Don't care. It may contain any number.

Utility Bus Write Command

Writes one byte per command cell to the Utility bus. The Utility bus is used to write to the PHY registers. This command does not generate nor return a command cell.

Command Fields	Field Value (Hex)	Description
Command	02	Write to Utility bus.
DataA	00 - FF	Utility bus address.
DataB	00 - FF	Utility bus data byte to be written.

Utility Bus Read Command

Reads one byte per command cell from the Utility bus. The Utility bus is used to read the PHY registers. This command generates a return command cell. See Reply Cell Format Table.

Command Fields	Field Value (Hex)	Description
Command	03	Read to Utility bus.
DataA	00 - FF	Utility bus address.
DataB	xx	Don't care on command. Will return value from Data B Table.

Output Pin Control Command

This command controls the output pins CONT_A and CONT_B, and causes an internally generated cell. See internally generated cell format section.

Command Fields	Field Value (Hex)	Description
Command	04	Define CONT_A and CONT_B Output State.
DataA	xx	Don't Care.
DataB	 00 01 02 03	Control pins output state. CONT_A CONT_B Low Low Low High High Low High High

Status Read Command

This command reads the 77010 Revision number and the Interrupt pin state, and causes an internally generated cell. See internally generated cell format section.

Command Fields	Field Value (Hex)	Description
Command	05	Status cell.
DataA	xx	See Data A and Data B Tables on page 14.
DataB	xx	See Data A and Data B Tables on page 14.

Change Control Cell Address Command

This command is used to change the control cell address. Once modified the IDT77010 will not filter old (default = 0x1Fx) values from the ATM cell stream. The command does not return a command cell.

Command Fields	Field Value (Hex)	Description
Command	06	Status cell.
DataA	00--FF	New Control Cell Address; placed in lower byte of VCI Field
DataB	xx	Don't care.

Internally Generated Reply Cell Format

Internal cells are generated in response to a command cell or PHY interrupt. The cells are remotely sent and switched to the 77010. The cell format of an internally generated cell is as follows:

Cell Byte Number	Bit Number	Function Name	Bit Contents	Description
0	7-4	GFC	0x0	Always set to 0x0
0	3-0	VPI 7-4	0x0	Always set to 0x0
1	7-4	VPI 3-0	0x0	Always set to 0x0
1	3-0	VCI 15-12	0x0	Always set to 0x0
2	7-0	VCI 11-4	0x02	Special VCI value for control and status cells.
3	7-4	VCI 3-0	0x0	Special VCI value for control and status cells.
3	3-1	PTI	000'b	Always set to 000'b.
3	0	CLP	0'b	Always set to 0.
4	7-0	HEC	0x00	Transmit HEC byte, always set to 0x00. The PHY device generates and calculates the HEC byte.
5	7-0	Command	00-FF Hex	This returned cell value is the same as the command cells Command byte. For interrupt cell this byte = 00 hex.
6	7-0	Data 1	See below	See below.
7	7-0	Data 2	See below	See below.
8	7-0	reserved	0x00	Always set to 0x00.
.	7-0	reserved	0x00	Always set to 0x00.
.	7-0	reserved	0x00	Always set to 0x00.
52	7-0	reserved	0x00	Always set to 0x00.

Internally Generated Reply Cell Table - Data A

Internally Generated Cell Type	Data A Byte Bit Number	Description
Utility Bus Read	7-0	Address of the Utility bus read.
Status Read Cell	7 6-0	This bit has the value of the interrupt pin at the time of this cell's generation. Reserved. Set to 0.
Interrupt Cell Return	7 6-0	This bit has the value of the interrupt pin at the time of this cell's generation. Reserved. Set to 0.

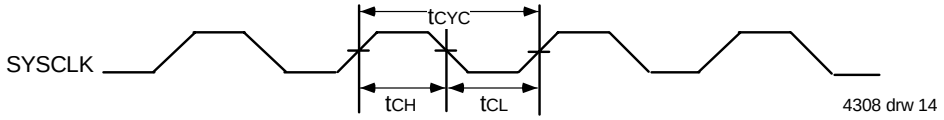
Internally Generated Reply Cell Table - Data B

Internally Generated Cell Type	Data A Byte Bit Number	Description
Utility Bus Read	7-0	Data value of the Utility bus read.
Status Read Cell	7-0	Revision number of the device.
Interrupt Cell Return	7-0	Revision number of the device.

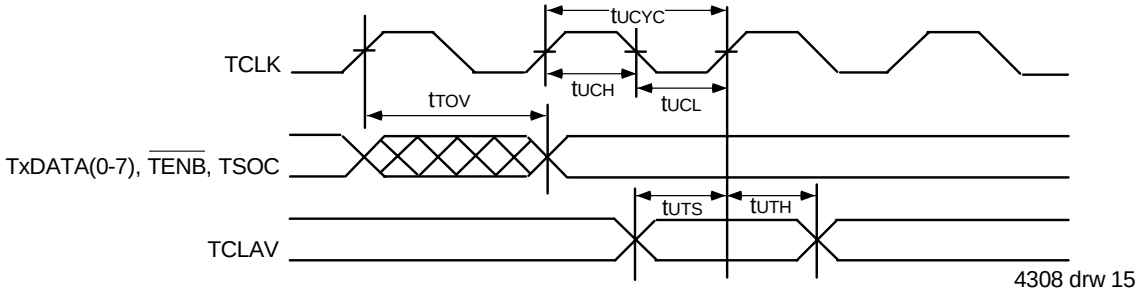
Symbol	Parameter	77010		Unit
		Min	Max	
t_{CYC}	SCLK Cycle Time	20	____	ns
t_{CH}	SCLK High Time	8	____	ns
t_{CL}	SCLK Low Time	8	____	ns
t_{UCYC}	UTOPIA TCLK/RCLK Cycle Time	50	____	ns
t_{UCH}	UTOPIA TCLK/RCLK High Time	20	____	ns
t_{UCL}	UTOPIA TCLK/RCLK Low Time	20	____	ns
t_{TOV}	TxDATA, TxPRTY, $\overline{TENB}$, TSOC Output Valid from TCLK	1	20	ns
t_{UTS}	TCLAV to TCLK Setup Time	10	____	ns
t_{UTH}	TCLAV to TCLK Hold Time	1	____	ns
t_{ROV}	$\overline{RENB}$ Output Valid from RCLK	1	20	ns
t_{URS}	RxDATA, RSOC, RCLAV to RCLKSetup Time	10	____	ns
t_{URH}	RxDATA, RSOC, RCLAV to RCLK Hold Time	1	____	ns
t_{DCYC}	DPI DTxCLK/DRxCLK Cycle Time	25	____	ns
t_{DCH}	DPI DTxCLK/DRxCLK High Time	9	____	ns
t_{DCL}	DPI DTxCLK/DRxCLK Low Time	9	____	ns
t_{DTS}	DTxFRM, DTxDATA to DTCLK Setup Time	6	____	ns
t_{DTH}	DTxFRM, DTxDATA to DTCLK Hold Time	2	____	ns
t_{PDRD}	DRxCLK to DRxDATA(0-3), DRxFRM Propagation Delay	____	13	ns
t_{ALPW}	ALE Pulse Width	40	____	ns
t_{ALR}	System Clock to $\overline{READ}$ Low Propagation Delay	____	22	ns
t_{ALW}	System Clock to $\overline{WRITE}$ Low Propagation Delay	____	22	ns
t_{RDPW}	Read Pulse Width	80	____	ns
t_{AAL}	Address to ALE Falling Edge Setup Time	20	____	ns
t_{ALA}	Address to ALE Falling Edge Hold Time	10	____	ns
t_{DRS}	Data to rising edge of $\overline{READ}$ Setup Time	5	____	ns
t_{DRH}	Data to rising edge of $\overline{READ}$ Hold Time	1	____	ns
t_{DWS}	Data to rising edge of $\overline{WRITE}$ Setup Time	5	____	ns
t_{DWH}	Data to rising edge of $\overline{WRITE}$ Hold Time	1	____	ns
t_{WRPW}	Write Pulse Width	40	____	ns
t_{PINTS}	System Clock to $\overline{PHYINT}$ Setup Time	10	____	ns
t_{PINTH}	System Clock to $\overline{PHYINT}$ Hold Time	1	____	ns
t_{PALE}	ALE to System Clock Propagation Delay	____	22	ns
t_{PPHY}	System Clock to $\overline{PHYCS}$ Propagation Delay	____	22	ns
t_{PPHYR}	System Clock to $\overline{PHYRST}$ Propagation Delay	____	22	ns
t_{PRCLK}	System Clock to Utopia Receive Clock Propagation Delay	____	20	ns

Symbol	Parameter	77010		Unit
		Min	Max	
t_{PTCLK}	System Clock to Utopia Transmit Clock Propagation Delay	____	20	ns
$t_{PDRxCLK}$	System Clock to DPI Receive Clock Propagation Delay	____	10	ns
$t_{PDTxCLK}$	System Clock to DPI Transmit Clock Propagation Delay	____	10	ns
t_{PRLED}	System Clock to $\overline{RxLED}$ Propagation Delay	____	19	ns
t_{PTLED}	System Clock to $\overline{TxLED}$ Propagation Delay	____	9	ns
t_{PCNTA}	System Clock to CONT_A Propagation Delay	____	22	ns
t_{PCNTB}	System Clock to CONT_B Propagation Delay	____	22	ns
t_{PRSTS}	Rising Edge of $\overline{RST}$ and $\overline{LCRST}$ to Rising Edge of System Clock Setup Time	10	____	ns
t_{PRSTH}	Rising Edge of $\overline{RST}$ and $\overline{LCRST}$ to Rising Edge of System Clock Hold Time	3	____	ns

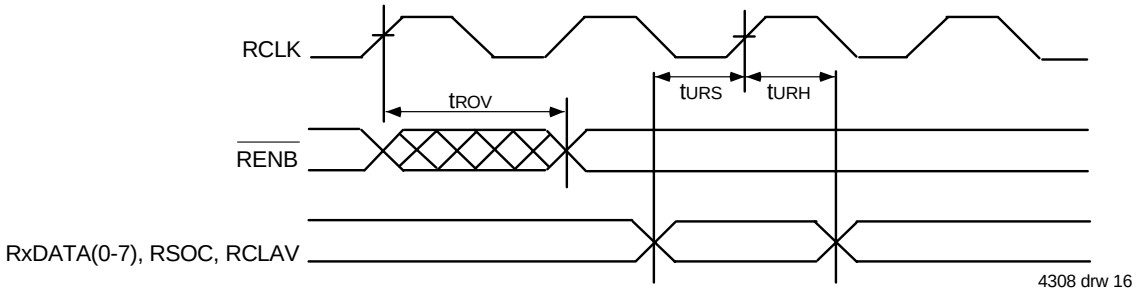
System Clock Timing Waveform



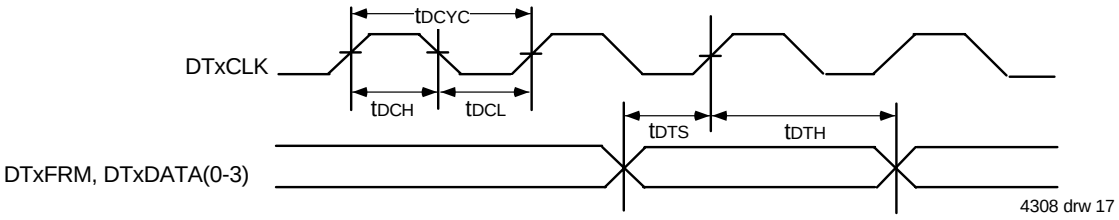
UTOPIA Transmit Timing Waveform



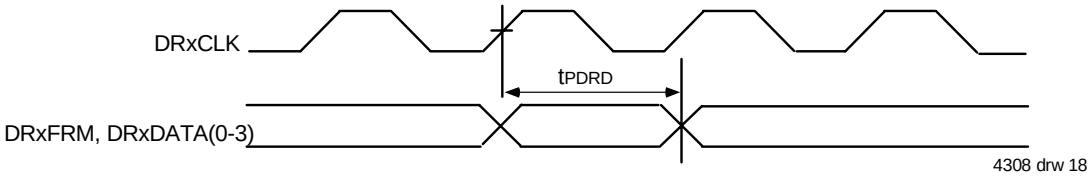
UTOPIA Receive Timing Waveform



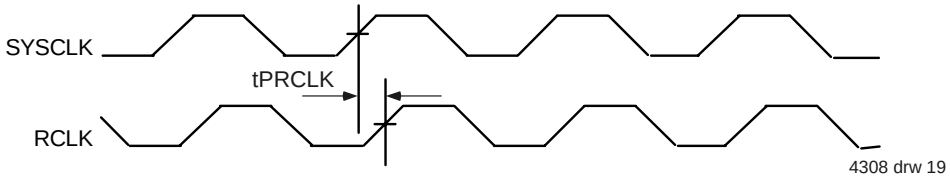
DPI Transmit Timing Waveform



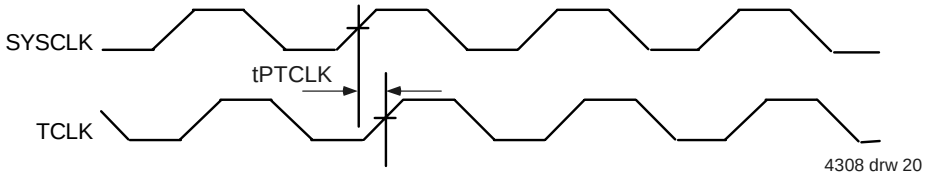
DPI Receive Timing Waveform



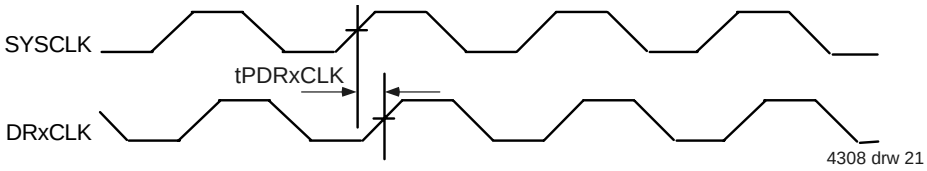
System Clock to UTOPIA Receive Clock Propagation Delay



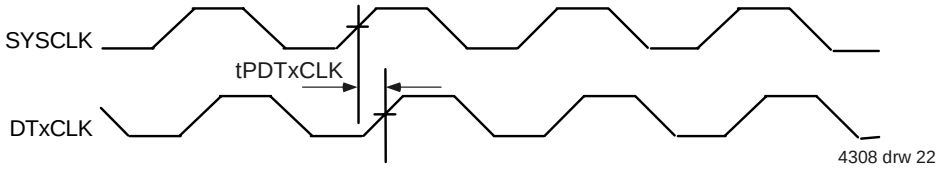
System Clock to UTOPIA Transmit Clock Propagation Delay



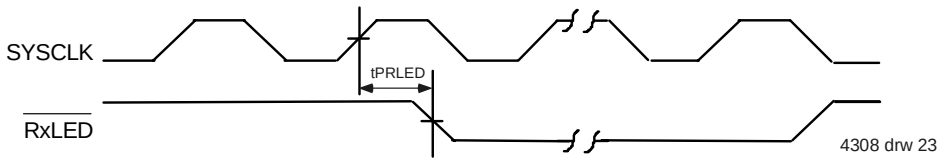
System Clock to DPI Receive Clock Propagation Delay



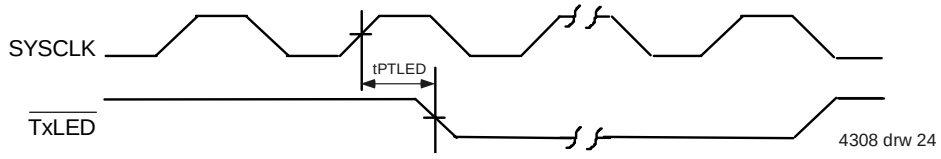
System Clock to DPI Transmit Clock Propagation Delay



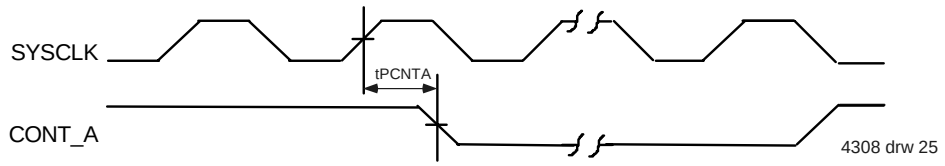
System Clock to $\overline{\text{RxLED}}$ Propagation Delay



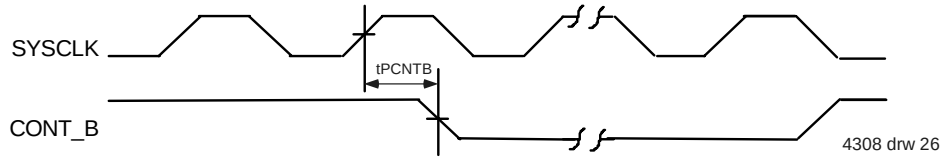
System Clock to $\overline{\text{TxLED}}$ Propagation Delay



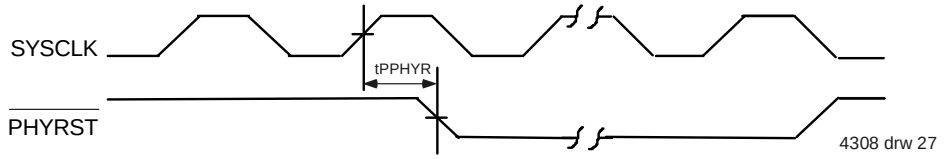
System Clock to Count_A Propagation Delay



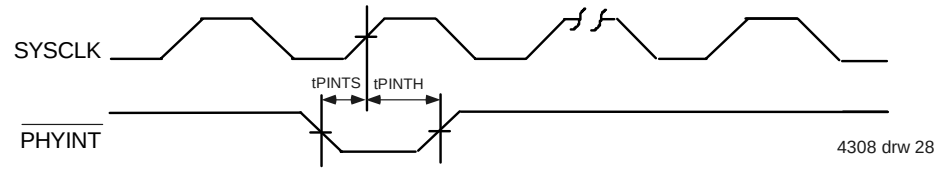
System Clock to Count_B Propagation Delay



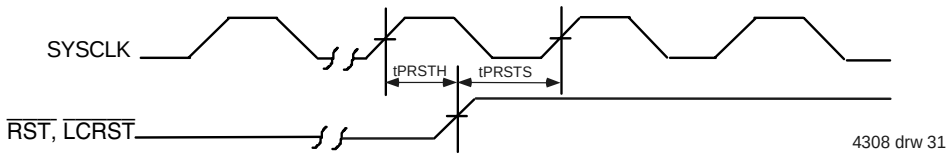
System Clock to $\overline{\text{PHYRST}}$ Propagation Delay



System Clock to $\overline{\text{PHYINT}}$ Setup and Hold Times

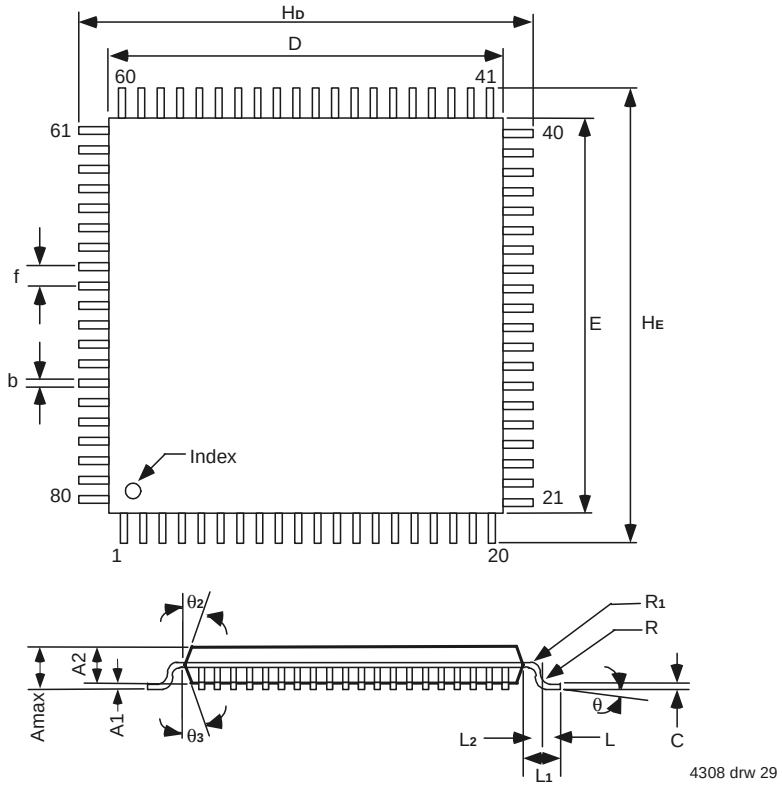


System Clock to $\overline{\textbf{RST}}$ and $\overline{\textbf{LCRST}}$ Setup Time



Package Information

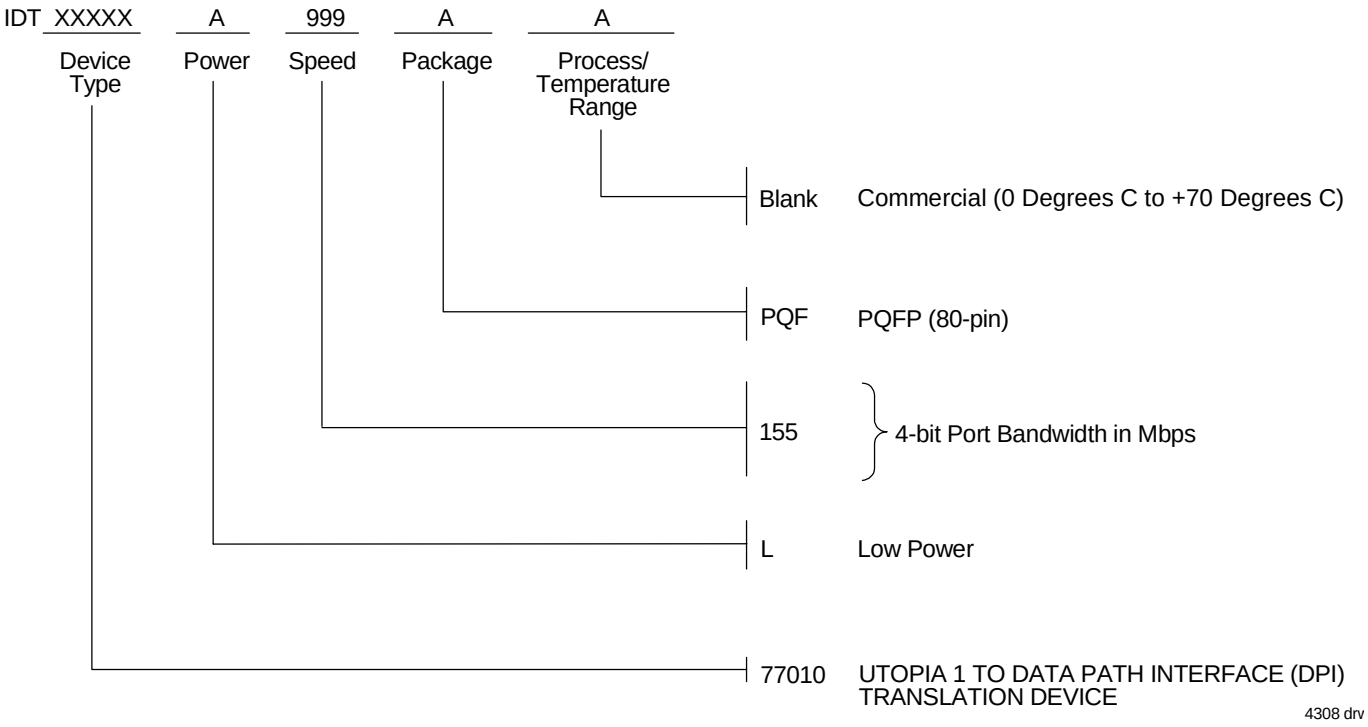
Plastic QFP 80pin Body size 12 x 12 x 1.4mm (QFP14)



Symbol	Dimension in Millimeters			Dimension in Inches[1]		
	Min	Norm	Max	Min	Norm	Max
E	11.9	12	12.1	(0.469)	(0.472)	(0.476)
D	11.9	12	12.1	(0.469)	(0.472)	(0.476)
A			1.7			(0.066)
A1		0.1			(0.004)	
A2	1.3	1.4	1.5	(0.052)	(0.055)	(0.059)
f		0.5			(0.020)	
b	0.13	0.18	0.28	(0.006)	(0.007)	(0.011)
C	0.1	0.125	0.175	(0.004)	(0.005)	(0.006)
q	0o		10o	(0o)		(10o)
L	0.3	0.5	0.7	(0.012)	(0.020)	(0.027)
L1		1			(0.039)	
L2		0.5			(0.020)	
HE	13.6	14	14.4	(0.536)	(0.551)	(0.566)
HD	13.6	14	14.4	(0.536)	(0.551)	(0.566)
q2						
q3						
R		0.2			(0.008)	
R1		0.2			(0.008)	

1. for reference

Ordering Information



Data Sheet Document History

4/02/99	Changed format
5/18/99	Changed tDTH from 6ns to 2ns, changed tALPW from 20ns to 40ns, added TxPRTY prop. delay.
6/24/99	Changed tDCH and tDCL from 8ns to 9ns, added tTOV and tROV min of 1ns.
7/06/99	Changed tPTCLK from 11ns to 20ns to match RCLK.
2/12/01	Changed to Final. Made general corrections. No parameters changed.
6/24/02	Added drawing 4308d31, System Clock to $\overline{RST}$ and $\overline{LCRST}$ Setup Time. Added tPRSTS and tPRSTH timing to timing parameters table. Changed e-mail URL from atmhelp@idt.com to switchstarhelp@idt.com.

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