

FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance:  $7\Omega$
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Available in QSOP and TSSOP packages

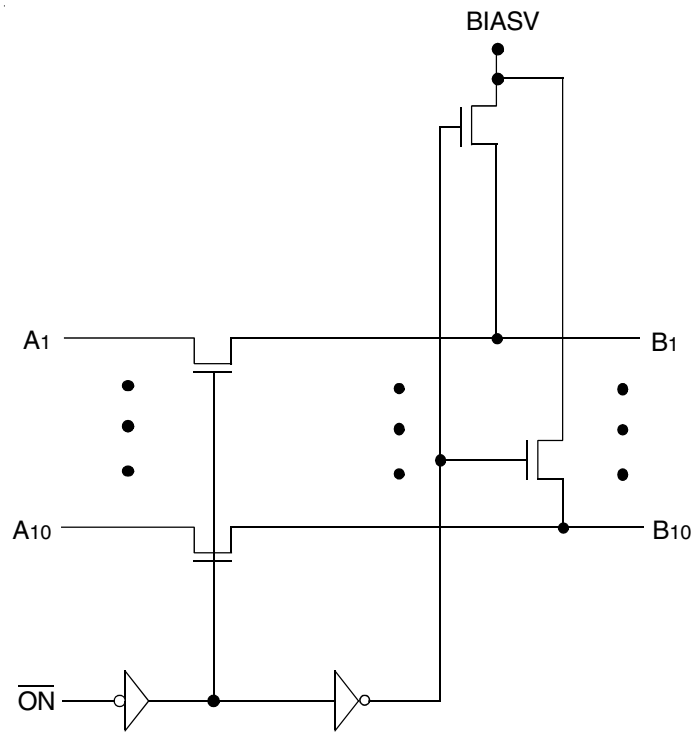
DESCRIPTION:

The FST6800 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no VCC applied, the device has hot insertion capability.

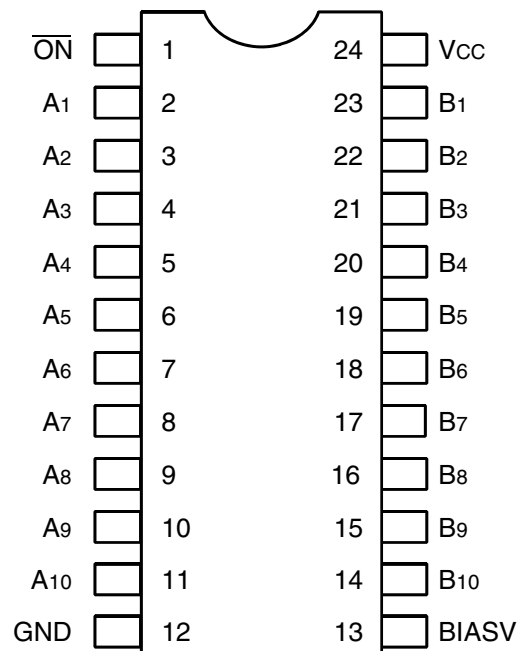
The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

The FST6800 provides a 10-Bit TTL-compatible interface. The  $\overline{ON}$  pin serves as the enable pin. When  $\overline{ON}$  is high, A and B ports are isolated and B outputs are precharged to the BIASV voltage, through the equivalent of a 10K $\Omega$  resistor.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



QSOP / TSSOP  
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	Maximum Continuous Channel Current	128	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>CC</sub>, Control, and Switch terminals.

## CAPACITANCE<sup>(1)</sup>

Symbol	Parameter	Conditions <sup>(2)</sup>	Typ.	Unit
C <sub>IN</sub>	Control Input Capacitance		4	pF
C <sub>I/O</sub>	Switch Input/Output Capacitance	Switch Off		pF

### NOTES:

- Capacitance is characterized but not tested.
- T<sub>A</sub> = 25°C, f = 1MHz, V<sub>IN</sub> = 0V, V<sub>OUT</sub> = 0V.

## PIN DESCRIPTION

Pin Names	I/O	Description
A1-10, B1-10	I/O	Buses A, B
$\overline{\text{ON}}$	I	Bus Switch Enable (Active LOW)
BIASV	I	BIAS Voltage

## FUNCTION TABLE<sup>(1)</sup>

$\overline{\text{ON}}$	B1-10	Description
L	A1-10	Connect
H	BIASV	Precharge

### NOTE:

- H = HIGH Voltage Level  
L = LOW Voltage Level

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: T<sub>A</sub> = -40°C to +85°C, V<sub>CC</sub> = 5.0V ± 5%, BIASV = 0 to V<sub>CC</sub>

Symbol	Parameter	Test Conditions <sup>(1)</sup>	Min.	Typ. <sup>(2)</sup>	Max.	Unit
V <sub>IH</sub>	Input HIGH Voltage	Guaranteed Logic HIGH for Control Inputs	2	—	—	V
V <sub>IL</sub>	Input LOW Voltage	Guaranteed Logic LOW for Control Inputs	—	—	0.8	V
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> = Max. V <sub>I</sub> = V <sub>CC</sub> V <sub>I</sub> = GND	—	—	±1	μA
I <sub>IL</sub>	Input LOW Current		—	—	±1	
I <sub>O</sub>	Precharge Output Current	V <sub>CC</sub> = Min., BIASV = 2.4V, V <sub>O</sub> = 0V	0.15	—	—	mA
I <sub>OZH</sub>	High Impedance Output Current (3-State Output Pins)	V <sub>CC</sub> = Max. V <sub>O</sub> = V <sub>CC</sub> V <sub>O</sub> = GND	—	—	±1	μA
I <sub>OZL</sub>			—	—	±1	
I <sub>OS</sub>	Short Circuit Current	V <sub>CC</sub> = Min., V <sub>O</sub> = GND <sup>(3)</sup>	—	300	—	mA
V <sub>IK</sub>	Clamp Diode Voltage	V <sub>CC</sub> = Min., I <sub>IN</sub> = -18mA	—	-0.7	-1.2	V
R <sub>ON</sub>	Switch On Resistance <sup>(4)</sup>	V <sub>CC</sub> = 4.75V, V <sub>IN</sub> = 0.0V I <sub>ON</sub> = 64mA	—	—	7	Ω
		V <sub>CC</sub> = 4.75V, V <sub>IN</sub> = 2.4V I <sub>ON</sub> = 15mA	—	—	15	
I <sub>OFF</sub>	Input/Output Power Off Leakage	V <sub>CC</sub> = 0V, V <sub>IN</sub> or V <sub>O</sub> ≤ 4.5V	—	—	1	μA
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> = Max., V <sub>I</sub> = GND or V <sub>CC</sub>	—	0.1	3	μA

### NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V<sub>CC</sub> = 5.0V, +25°C ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- Measured by voltage drop between ports at indicated current through the switch.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	1.5	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Enable Pin Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	30	40	$\mu A/$ MHz/ Enable
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open Enable Pin Toggling (Ten Switches Toggling) $f_i = 10\text{MHz}$ 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = GND$	—	3	4	mA
			$V_{IN} = 3.4V$ $V_{IN} = GND$	—	3.3	4.8	

### NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ C$  ambient.

3. Per TTL driven input ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $GND$ .

4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.

5. Values for these conditions are examples of  $I_{CC}$  formula. These limits are guaranteed but not tested.

6.  $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_i N)$

$I_{CC} = \text{Quiescent Current}$

$\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$

$D_H = \text{Duty Cycle for TTL Inputs High}$

$N_T = \text{Number of TTL Inputs at } D_H$

$I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$

$f_{CP} = \text{Clock Frequency for Register Devices (zero for non-register devices)}$

$f_i = \text{Input Frequency}$

$N = \text{Number of Switches Toggling at } f_i$

All currents are in milliamps and all frequencies are in megahertz

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ C$  to  $+85^\circ C$ ,  $V_{CC} = 5.0V \pm 5\%$

Symbol	Description	Condition <sup>(1)</sup>	Min. <sup>(2)</sup>	Typ.	Max.	Unit
$t_{PLH}$	Data Propagation Delay	$C_L = 50pF$ $R_L = 500\Omega$	—	—	0.25	ns
$t_{PHL}$	$A_x, B_x$ to $B_x, A_x^{(3,4)}$		1.5	—	6.5	ns
$t_{PZH}$	Switch Turn On Delay					
$t_{PZL}$	$\overline{O}N$ to $A_x, B_x$	1.5	—	5.5	ns	
$t_{PHZ}$	Switch Turn Off Delay					
$t_{PLZ}$	$\overline{O}N$ to $A_x, B_x^{(3)}$					

### NOTES:

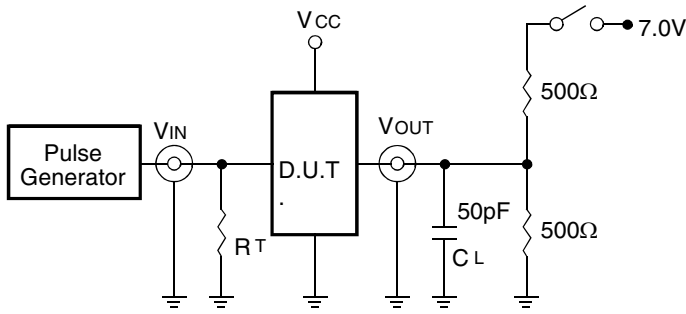
1. See test circuit and waveforms.

2. Minimum limits guaranteed but not tested.

3. This parameter is guaranteed by design but not tested.

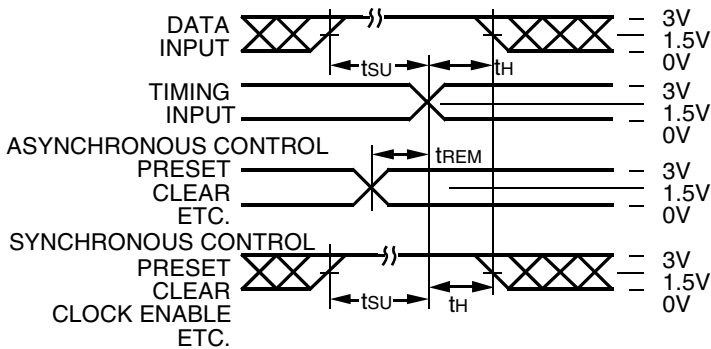
4. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the load capacitance. The time constant for the switch alone is of the order of 0.25 ns for 50 pF load. Since this time is constant and much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the bus switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

TEST CIRCUITS AND WAVEFORMS



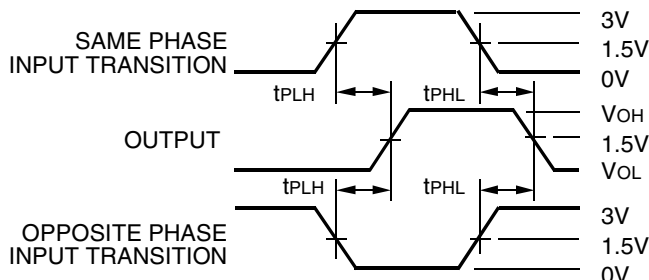
Octal Link

Test Circuits for All Outputs



Octal Link

Set-up, Hold, and Release Times



Octal Link

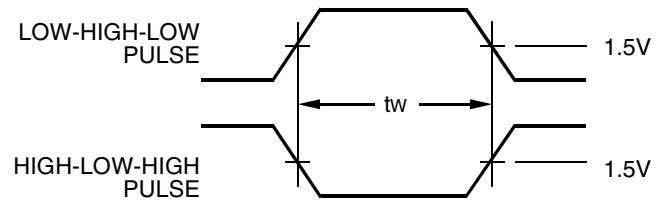
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

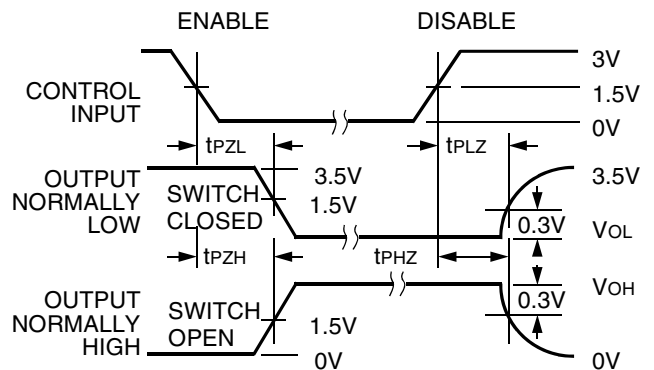
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.  
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

Octal Link



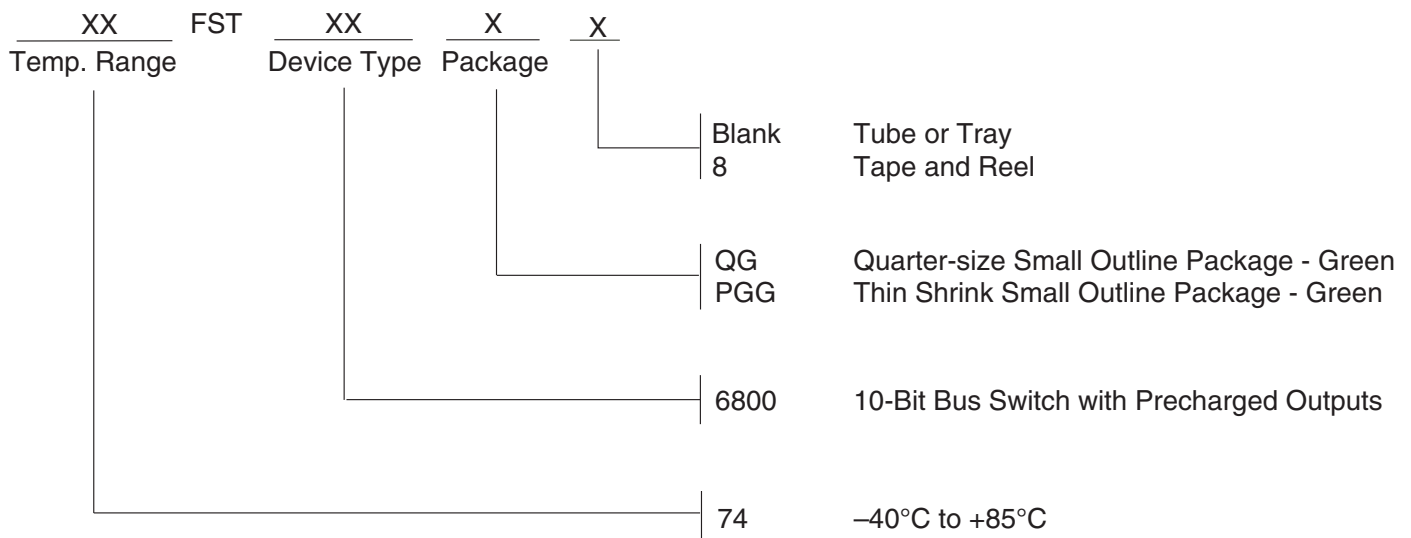
Enable and Disable Times

Octal Link

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

## ORDERING INFORMATION



## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).