FAST CMOS OCTAL LATCHED TRANSCEIVER

74FCT543AT/CT

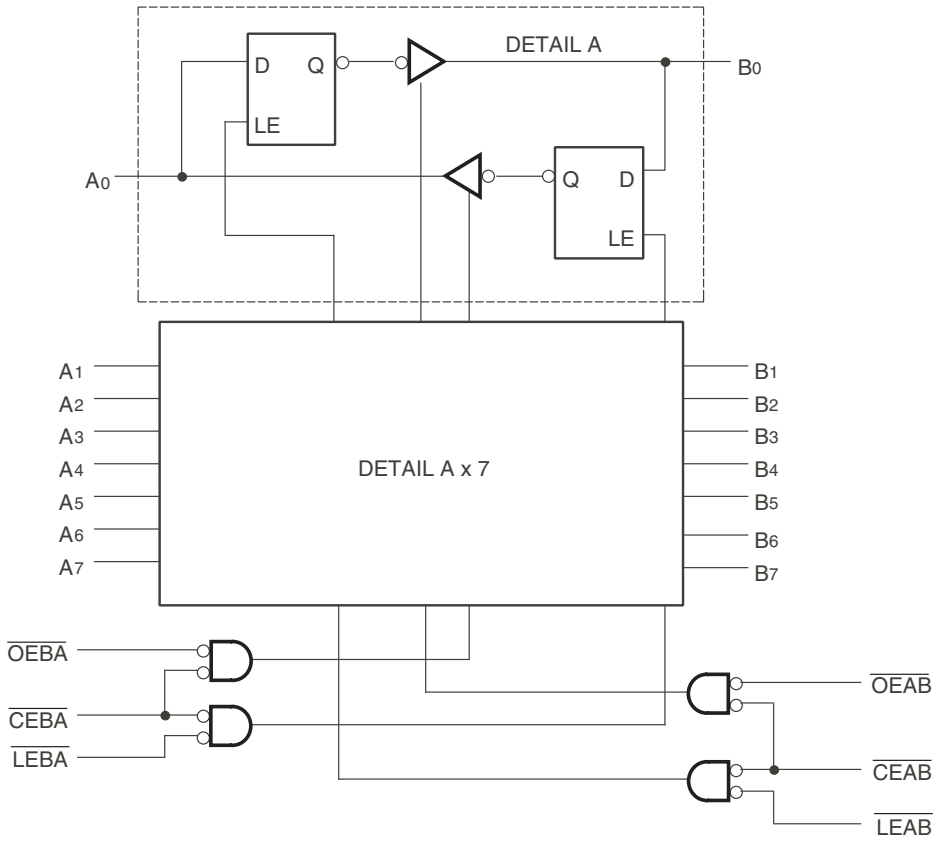
FEATURES:

- **A and C grades**
- **Low input and output leakage ≤1µA (max.)**
- **CMOS power levels**
- **True TTL input and output compatibility:**
  - *V_{OH} = 3.3V (typ.)*
  - *V_{OL} = 0.3V (typ.)*
- **High Drive outputs (-15mA I_{OH}, 64mA I_{OL})**
- **Meets or exceeds JEDEC standard 18 specifications**
- **Power off disable outputs permit "live insertion"**
- **Available in SOIC and QSOP packages**

DESCRIPTION:

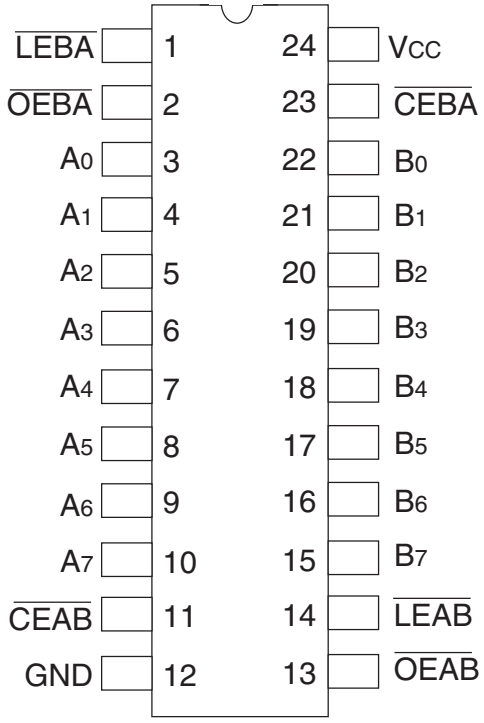
The FCT543T is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. This device contains two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be low in order to enter data from A_0–A_7 or to take data from B_0–B_7, as indicated in the Function Table. With $\overline{CEAB}$ low, a low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
QSOP	PCG24	QG
SOIC	PSG24	SOG

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +7	V
V_{TERM}(3)	Terminal Voltage with Respect to GND	–0.5 to V_{CC}+0.5	V
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	DC Output Current	–60 to +120	mA

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	6	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	8	12	pF

NOTE:
1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A_0–A_7	A-to-B Data Inputs or B-to-A 3-State Outputs
B_0–B_7	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE[1, 2]

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	B_0–B_7
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES:
1. * Before LEAB LOW-to-HIGH Transition
   H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
2. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: T_A = –40°C to +85°C, V_{CC} = 5.0V ±5%

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current[4]	V_{CC} = Max.	V_I = 2.7V	—	—	±1	µA
I_{IL}	Input LOW Current[4]	V_{CC} = Max.	V_I = 0.5V	—	—	±1	µA
I_{OZH}	High Impedance Output Current	V_{CC} = Max	V_O = 2.7V	—	—	±1	µA
I_{OZL}	(3-State output pins)[4]		V_O = 0.5V	—	—	±1	
I_I	Input HIGH Current[4]	V_{CC} = Max., V_I = V_{CC} (Max.)		—	—	±1	µA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min, I_{IN} = -18mA		—	–0.7	–1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max., V_{IN} = GND or V_{CC}		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min	I_{OH} = –8mA	2.4	3.3	—	V
		V_{IN} = V_{IH} or V_{IL}	I_{OH} = –15mA	2	3	—	
V_{OL}	Output LOW Voltage	V_{CC} = Min V_{IN} = V_{IH} or V_{IL}	I_{OL} = 64mA	—	0.3	0.55	V
I_{OS}	Short Circuit Current	V_{CC} = Max., V_O = GND[3]		–60	–120	–225	mA
I_{OFF}	Input/Output Power Off Leakage[5]	V_{CC} = 0V, V_{IN} or $V_O \leq$ 4.5V		—	—	±1	µA

NOTES:
1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is ±5µA at T_A = –55°C.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions[1]		Min.	Typ.[2]	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V_{CC} = Max. V_{IN} = 3.4V[3]		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current[4]	V_{CC} = Max., Outputs Open $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Input Toggling 50% Duty Cycle	V_{IN} = V_{CC} V_{IN} = GND	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} One Bit Toggling at fi = 5MHz 50% duty cycle	V_{IN} = V_{CC} V_{IN} = GND	—	1.5	3.5	mA
			V_{IN} = 3.4V V_{IN} = GND	—	2	5.5	
		V_{CC} = Max., Outputs Open f_{CP} = 10MHz ($\overline{LEAB}$) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB}$ = GND $\overline{CEBA}$ = V_{CC} Eight Bits Toggling at fi = 2.5MHz 50% duty cycle	V_{IN} = V_{CC} V_{IN} = GND	—	3.8	7.3[5]	mA
			V_{IN} = 3.4V V_{IN} = GND	—	6	16.3[5]	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_i = Output Frequency
   N_i = Number of Outputs at f_i

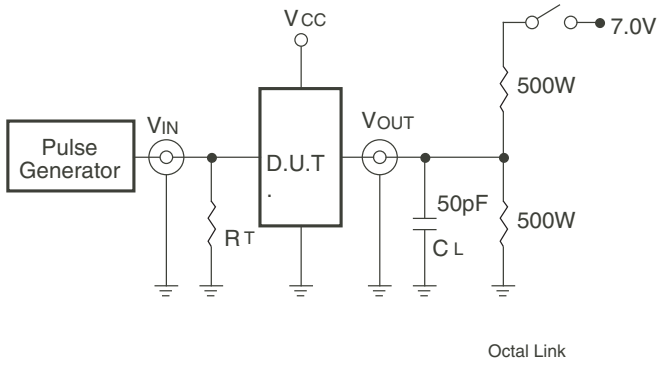
All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition[1]	74FCT543AT		74FCT543CT		
			Min.[2]	Max.	Min.[2]	Max.	Unit
t_{PLH} t_{PHL}	Propagation Delay Transparant Mode Ax to Bx or Bx to Ax	C_L = 50pF R_L = 500Ω	1.5	6.5	1.5	5.3	ns
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to Ax, $\overline{LEAB}$ to Bx		1.5	8	1.5	7	ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to Ax or Bx $\overline{CEBA}$ or $\overline{CEAB}$ to Ax or Bx		1.5	9	1.5	8	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to Ax or Bx $\overline{CEBA}$ or $\overline{CEAB}$ to Ax or Bx		1.5	7.5	1.5	6.5	ns
t_{SU}	Set-up Time, HIGH or LOW Ax or Bx to $\overline{LEBA}$ or $\overline{LEAB}$		2	—	2	—	ns
t_H	Hold Time, HIGH or LOW Ax or Bx to $\overline{LEBA}$ or $\overline{LEAB}$		2	—	2	—	ns
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5	—	5	—	ns

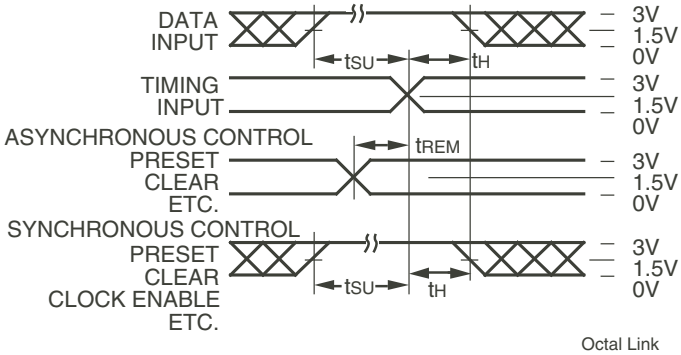
NOTES:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS



Octal Link

Test Circuits for All Outputs



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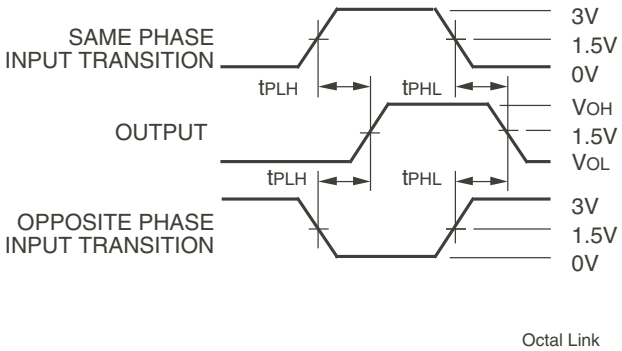
Set-Up, Hold, and Release Times



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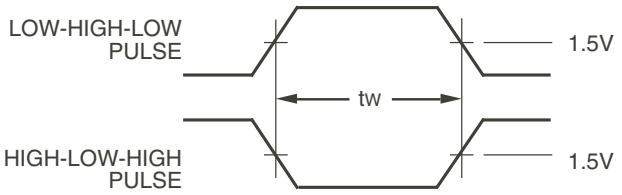
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

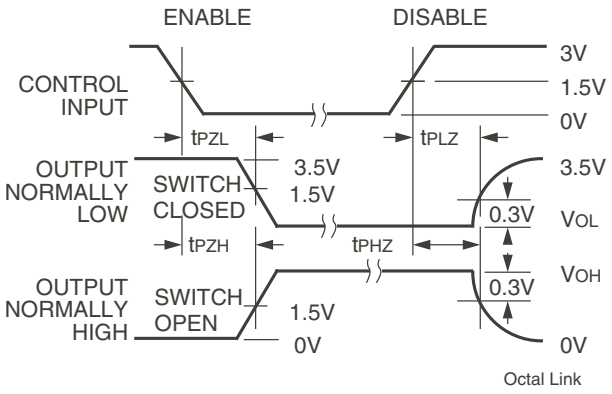
DEFINITIONS:

C_L = Load capacitance: includes jig and probe capacitance.
R_T = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

Octal Link



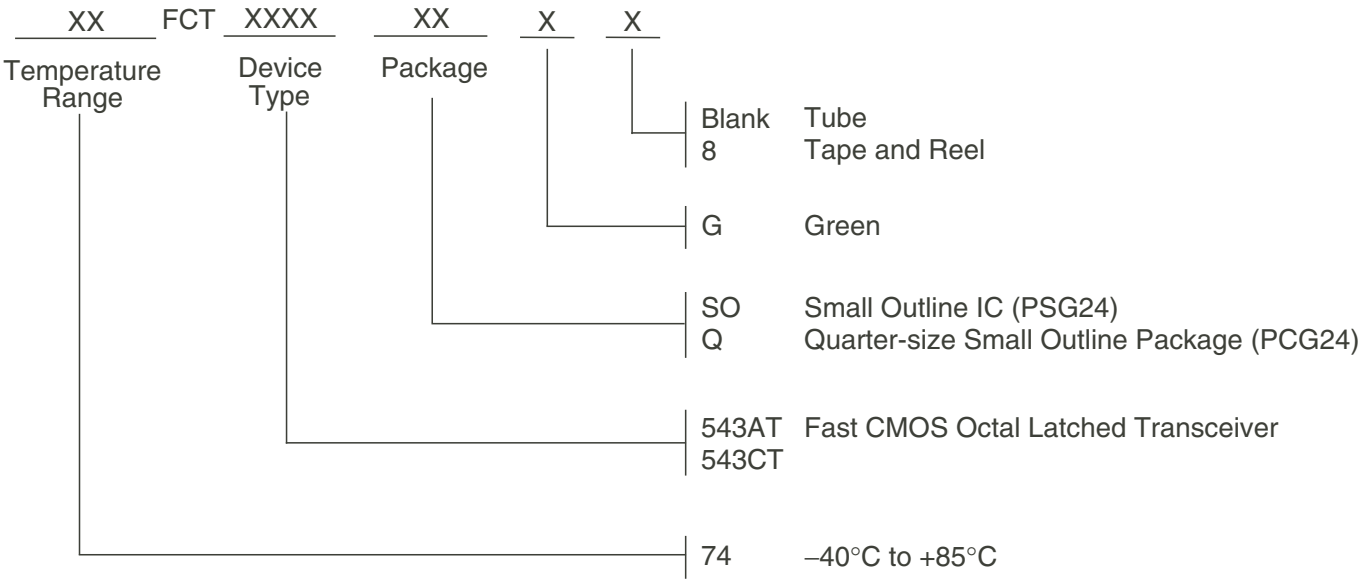
Octal Link

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; t_F ≤ 2.5ns; t_R ≤ 2.5ns.

ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT543ATQG	PCG24	QSOP	I
	74FCT543ATQG8	PCG24	QSOP	I
	74FCT543ATSOG	PSG24	SOIC	I
	74FCT543ATSOG8	PSG24	SOIC	I
C	74FCT543CTQG	PCG24	QSOP	I
	74FCT543CTQG8	PCG24	QSOP	I
	74FCT543CTSOG	PSG24	SOIC	I
	74FCT543CTSOG8	PSG24	SOIC	I

Datasheet Document History

10/10/2009	Pg. 6	Updated the ordering information by removing the "IDT" notation and non RoHS part.
05/16/2018	Pgs. 2, 7	Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram adding Tube, Tape and Reel. Added new table of orderable part information.
05/10/2019	Pg. 7	Updated ordering information diagram.
02/11/2020	Pgs. 1-8	Rebranded as Renesas datasheet.

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