

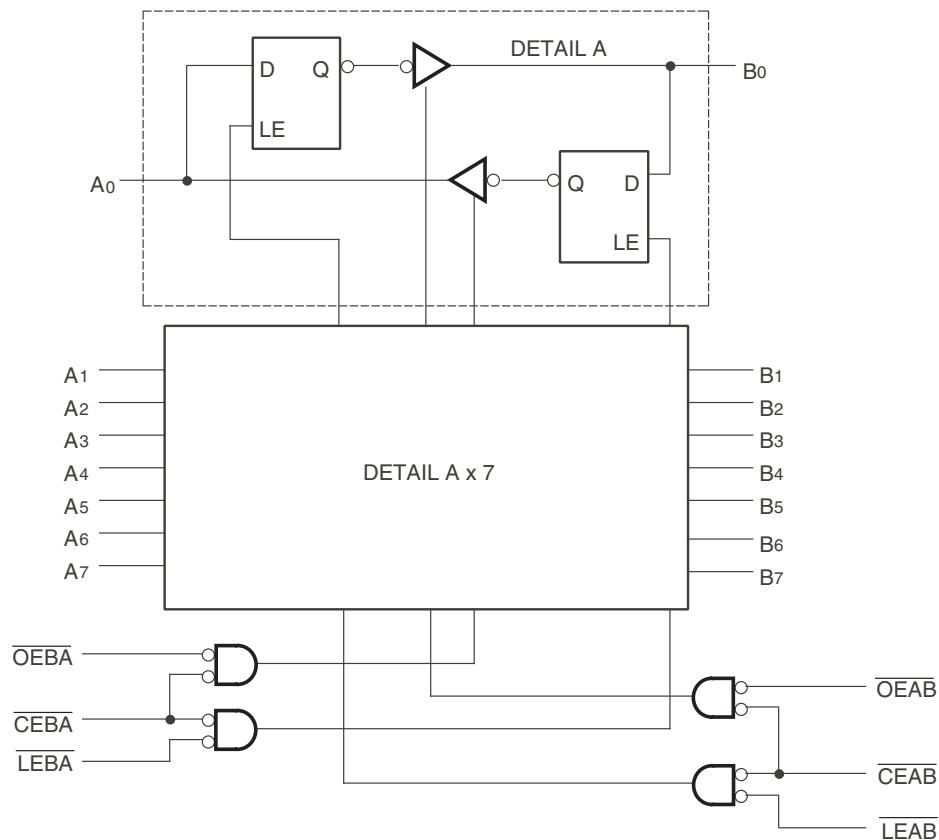
FEATURES:

- A and C grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- High Drive outputs (-15mA I_{OH} , 64mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

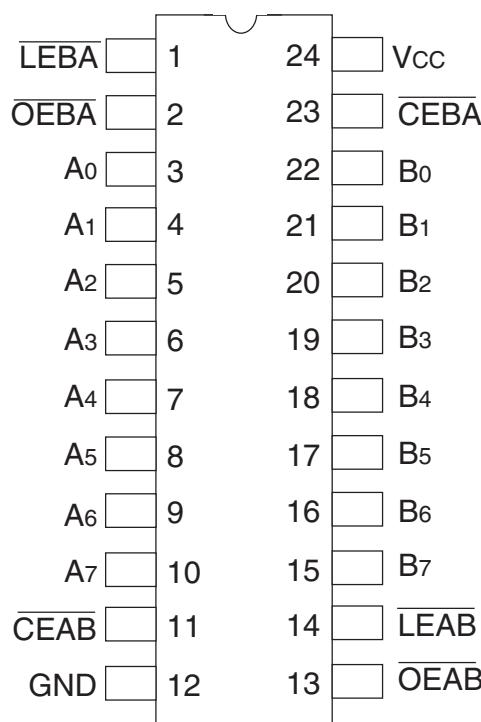
The FCT543T is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. This device contains two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable (\overline{CEAB}) input must be low in order to enter data from A_0 - A_7 or to take data from B_0 - B_7 , as indicated in the Function Table. With \overline{CEAB} low, a low signal on the A-to-B Latch Enable (\overline{LEAB}) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the \overline{LEAB} signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With \overline{CEAB} and \overline{OEAB} both low, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the \overline{CEBA} , \overline{LEBA} and \overline{OEBA} inputs.

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
QSOP	PCG24	QG
SOIC	PSG24	SOG

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
VTERM ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed Vcc by +0.5V unless otherwise noted.
2. Inputs and Vcc terminals only.
3. Output and I/O terminals only.

CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
OEAB	A-to-B Output Enable Input (Active LOW)
OEBA	B-to-A Output Enable Input (Active LOW)
CEAB	A-to-B Enable Input (Active LOW)
CEBA	B-to-A Enable Input (Active LOW)
LEAB	A-to-B Latch Enable Input (Active LOW)
LEBA	B-to-A Latch Enable Input (Active LOW)
A ₀ -A ₇	A-to-B Data Inputs or B-to-A 3-State Outputs
B ₀ -B ₇	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE^(1, 2)

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
CEAB	LEAB	OEAB	A-to-B	Bo-B7
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

NOTES:

1. * Before LEAB LOW-to-HIGH Transition

H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

2. A-to-B data flow shown; B-to-A flow control is the same, except using \overline{CEBA} , \overline{LEBA} and \overline{OEBA} .

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $TA = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current	$V_{CC} = \text{Max}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}	(3-State output pins) ⁽⁴⁾		$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$, $V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min}$, $I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}$, $V_{IN} = \text{GND}$ or V_{CC}		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit	
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V	
			$I_{OH} = -15\text{mA}$	2	3	—		
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min}$		$I_{OL} = 64\text{mA}$	—	0.3	0.55	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}$, $V_O = \text{GND}$ ⁽³⁾		-60	-120	-225	mA	
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}$, V_{IN} or $V_O \leq 4.5\text{V}$		—	—	± 1	μA	

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.

2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.

3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.

4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $TA = -55^{\circ}\text{C}$.

5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = 3.4V ⁽³⁾		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max., Outputs Open \overline{CEAB} and \overline{OEAB} = GND $CEBA$ = V _{CC} One Input Toggling 50% Duty Cycle		V _{IN} = V _{CC} V _{IN} = GND	—	0.15	0.25
I_C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open $f_{CP} = 10\text{MHz}$ (\overline{LEAB}) 50% Duty Cycle $CEAB$ and \overline{OEAB} = GND $CEBA$ = V _{CC} One Bit Toggling at $f_i = 5\text{MHz}$ 50% duty cycle		V _{IN} = V _{CC} V _{IN} = GND	—	1.5	3.5
				V _{IN} = 3.4V V _{IN} = GND	—	2	5.5
				V _{IN} = V _{CC} V _{IN} = GND	—	3.8	7.3 ⁽⁵⁾
				V _{IN} = 3.4V V _{IN} = GND	—	6	16.3 ⁽⁵⁾

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient.
3. Per TTL driven input; (V_{IN} = 3.4V). All other inputs at V_{CC} or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.

6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

I_{CC} = Quiescent Current

ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)

D_H = Duty Cycle for TTL Inputs High

N_T = Number of TTL Inputs at D_H

I_{CCD} = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)

f_i = Output Frequency

N_i = Number of Outputs at f_i

All currents are in millamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

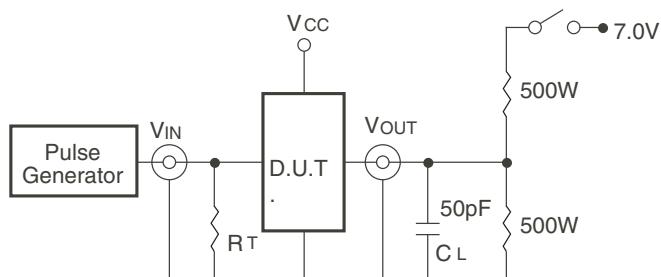
Symbol	Parameter	Condition ⁽¹⁾	74FCT543AT		74FCT543CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t_{PLH}	Propagation Delay Transparent Mode Ax to Bx or Bx to Ax	$CL = 50\text{pF}$ $RL = 500\Omega$	1.5	6.5	1.5	5.3	ns
t_{PHL}	Propagation Delay \overline{LEBA} to Ax, \overline{LEAB} to Bx		1.5	8	1.5	7	ns
t_{PZH}	Output Enable Time \overline{OEBA} or \overline{OEAB} to Ax or Bx \overline{CEBA} or \overline{CEAB} to Ax or Bx		1.5	9	1.5	8	ns
t_{PHZ}	Output Disable Time \overline{OEBA} or \overline{OEAB} to Ax or Bx \overline{CEBA} or \overline{CEAB} to Ax or Bx		1.5	7.5	1.5	6.5	ns
t_{SU}	Set-up Time, HIGH or LOW Ax or Bx to \overline{LEBA} or \overline{LEAB}		2	—	2	—	ns
t_H	Hold Time, HIGH or LOW Ax or Bx to \overline{LEBA} or \overline{LEAB}		2	—	2	—	ns
t_W	\overline{LEBA} or \overline{LEAB} Pulse Width LOW		5	—	5	—	ns

NOTES:

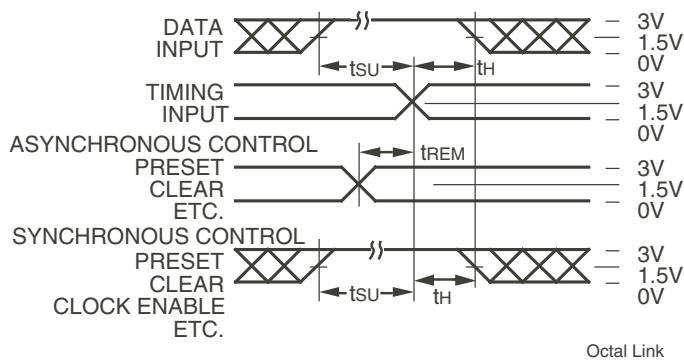
1. See test circuit and waveforms.

2. Minimum limits are guaranteed but not tested.

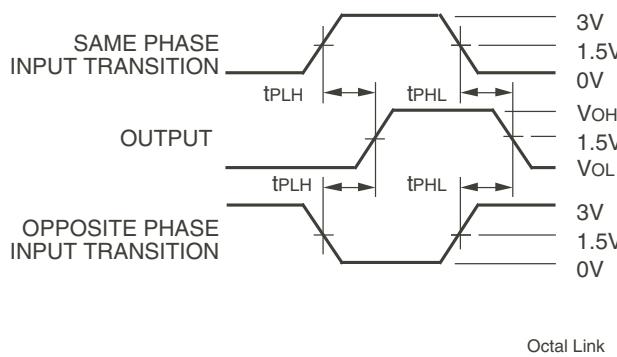
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



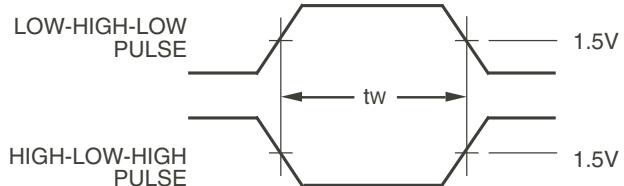
Propagation Delay

SWITCH POSITION

Test	Switch
Open Drain	Closed
Disable Low	
Enable Low	
All Other Tests	Open

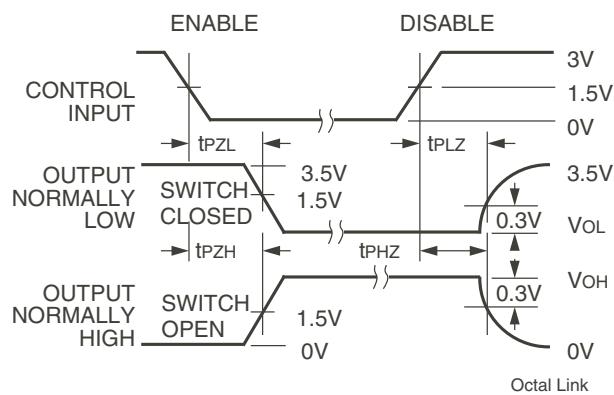
DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Z_{OUT} of the Pulse Generator.



Pulse Width

Octal Link

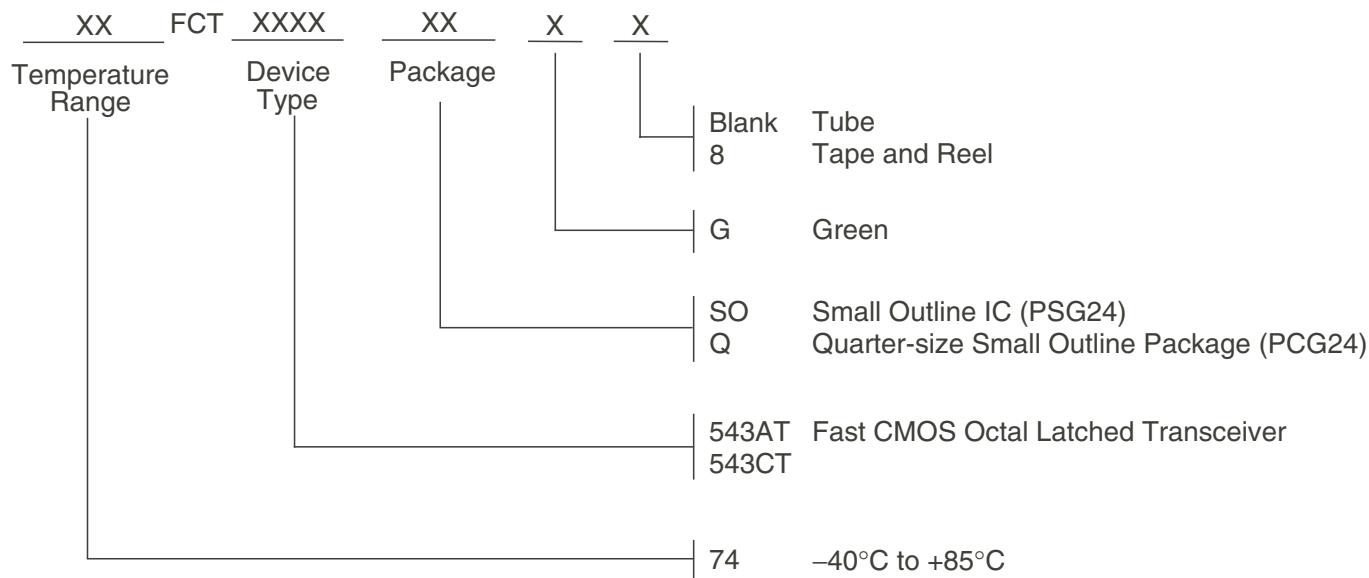


Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; t_F $\leq 2.5\text{ns}$; t_R $\leq 2.5\text{ns}$.

ORDERING INFORMATION



Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT543ATQG	PCG24	QSOP	I
	74FCT543ATQG8	PCG24	QSOP	I
	74FCT543ATSOG	PSG24	SOIC	I
	74FCT543ATSOG8	PSG24	SOIC	I
C	74FCT543CTQG	PCG24	QSOP	I
	74FCT543CTQG8	PCG24	QSOP	I
	74FCT543CTSOG	PSG24	SOIC	I
	74FCT543CTSOG8	PSG24	SOIC	I

Datasheet Document History

10/10/2009	Pg. 6	Updated the ordering information by removing the "IDT" notation and non RoHS part.
05/16/2018	Pgs. 2, 7	Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram adding Tube, Tape and Reel. Added new table of orderable part information.
05/10/2019	Pg. 7	Updated ordering information diagram.
02/11/2020	Pgs. 1-8	Rebranded as Renesas datasheet.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.