SERIALLY PROGRAMMABLE CLOCK SOURCE IDT6V40277

Description

The IDT6V40277 is a small, versatile serially programmable clock source for Freescale systems. It can generate any frequency from 6 to 200 MHz and have a second configurable output. The outputs can be reprogrammed on the fly and will lock to a new frequency in 10 ms or less. Smooth transitions (in which the clock duty cycle remains near 50%) are guaranteed if the output divider is not changed.

The device includes a $\overline{\text{PDTS}}$ pin which tri-states the output clocks and powers down the entire chip.

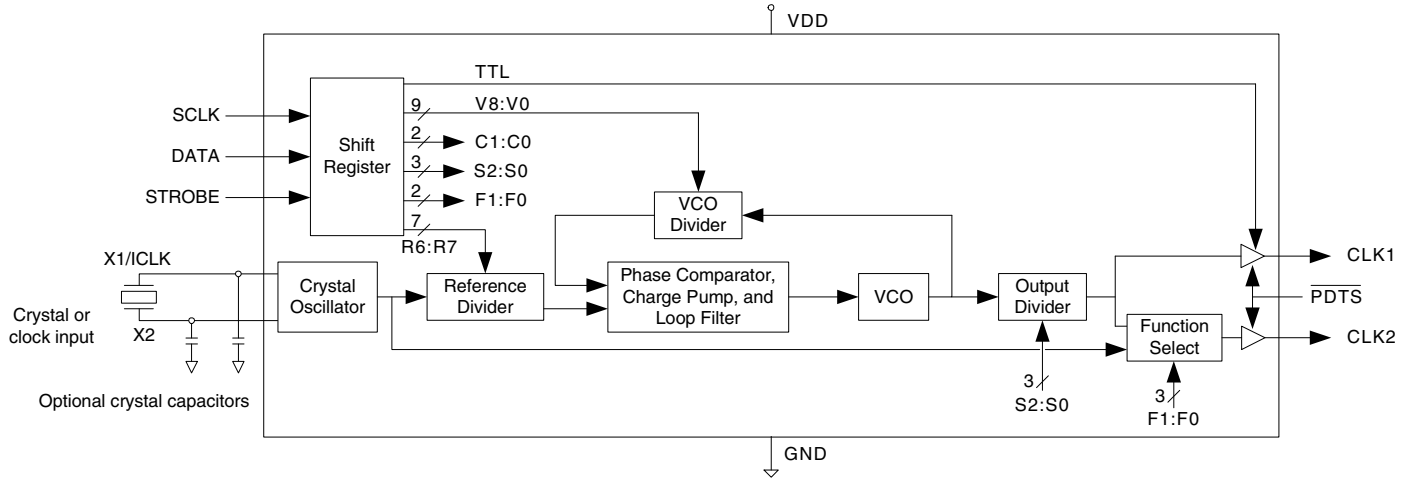
The IDT6V40277 features a default clock output at start-up.

This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed.

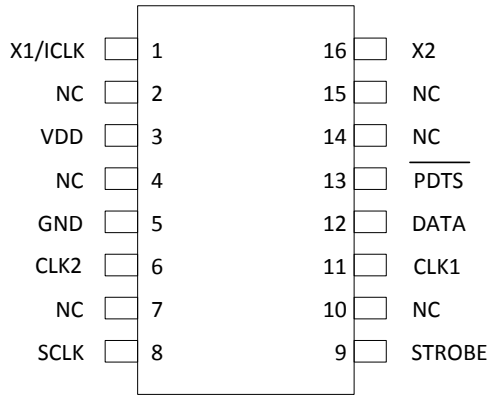
Features

- Packaged in 16-pin DCG (150 mil wide SOIC) – Pb-free, RoHS compliant
- Highly accurate frequency generation
- Serially programmable: user determines the output frequency via a 3 wire interface
- Eliminates need for custom quartz
- Input crystal frequency of 5 - 27 MHz
- Output clock frequencies up to 200 MHz
- Power down tri-state mode
- Very low jitter
- Operating voltage of 3.3 V or 5 V
- 25 mA drive capability at TTL levels
- Industrial temperature operating range (-40°C to +85°C)

Block Diagram



Pin Assignment



16-pin DCG (150 mil SOIC)

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	XI	Crystal connection (REF frequency). Connect to a parallel resonant crystal or an input clock.
2	NC	-	No connect. Do not connect anything to this pin.
3	VDD	Power	Connect to 3.3 V or 5 V.
4	NC	-	No connect. Do not connect anything to this pin.
5	GND	Power	Connect to ground.
6	CLK2	Output	Output clock 2, determined by F0 - F1. Can be reference, REF/2, CLK1/2 , or off.
7	NC	-	No connect. Do not connect anything to this pin.
8	SCLK	Input	Serial clock. See timing diagram.
9	STROBE	Input	Strobe to load data. See timing diagram.
10	NC	-	No connect. Do not connect anything to this pin.
11	CLK1	Output	Output clock 1, determined by R0 - R6, V0 - V8, S0 - S2, and input frequency.
12	DATA	Input	Data input. Serial input for three words which set the output clock(s).
13	$\overline{\text{PDTS}}$	Input	Powers down entire chip, tri states CLK1 and CLK2 outputs when low. Internal pull-up.
14	NC	–	No connect. Do not connect anything to this pin.
15	NC	–	No connect. Do not connect anything to this pin.
16	X2	XO	Input crystal connection. Connect to a crystal or leave unconnected for clock input.

Determining the Output Frequency

On power-up, the IDT6V40277 on-chip registers can have random values so almost any frequency may be output from the part. CLK1 will always have some clock signal present, but CLK2 could possibly be OFF (low).

The IDT6V40277 on-chip registers are initially configured to provide a x1 output clock on both the CLK1 and CLK2 outputs. The output frequency will be the same as the input clock or crystal. This is useful if the IDT6V40277 will provide the initial system clock at power-up. Since this feature is an advantage in most systems, the IDT6V40277 is recommended for new designs.

With programming, the user has full control in changing the desired output frequency to any value over the range shown in Table 1 on page 4. The output of the IDT6V40277 can be determined by the following equation:

$$CLK1Frequency = InputFrequency \cdot 2 \cdot \frac{VDW + 8}{(RDW + 2) \cdot OD}$$

Where:

VCO Divider Word (VDW) = 4 to 511 (0, 1, 2, 3 are not permitted)

Reference Divider Word (RDW) = 1 to 127 (0 is not permitted)

Output Divider = values on page 4

The following operating ranges should be observed. For the commercial temperature range:

$$55MHz < InputFrequency \cdot 2 \cdot \frac{VDW + 8}{RDW + 2} < 400MHz$$

$$200kHz < \frac{InputFrequency}{RDW + 2}$$

And for the industrial temperature range:

$$60MHz < InputFrequency \cdot 2 \cdot \frac{VDW + 8}{RDW + 2} < 360MHz$$

$$200kHz < \frac{Input\ Frequency}{RDW + 2}$$

To determine the best combination of VCO, reference, and output dividers, see the online calculator at www.idt.com or contact IDT by sending your inquiry to www.idt.com/go/clockhelp with the desired input crystal or clock and the desired output frequency.

Setting the Device Characteristics

The tables below show the settings which can be configured, as well as the VCO and Reference dividers.

Table 1. Output Divide and Maximum Output Frequency

S2	S1	S0	CLK1 Output Divide	Max. Frequency 5 V or 3.3 V (MHz)	Max. Frequency Industrial Temp. Version
0	0	0	10	40	36
0	0	1	2	200	180
0	1	0	8	50	45
0	1	1	4	100	90
1	0	0	5	80	72
1	0	1	7	55	50
1	1	0	3	135	120
1	1	1	6	67	60

Table 2. CLK2 Output

F1	F0	CLK2
0	0	REF
0	1	$F_{REF}/2$
1	0	OFF (Low)
1	1	$F_{CLK1}/2$

Table 3. Output Duty Cycle Configuration

TTL	Duty Cycle Measured At	Recommended VDD
0	1.4 V	5 V
1	VDD/2	3.3 V

Note: The TTL bit optimizes the duty cycle at different VDD. When VDD is 5 V, set to 0 for a near-50% duty cycle with TTL levels. When VDD is 3.3 V, set this bit to 1 so the 50% duty cycle is achieved at VDD/2.

Table 4. Crystal Load Capacitance

C1	C0	VDD = 5V	VDD = 3.3V
0	0	22.3 - 0.083 f	22.1 - 0.094 f
0	1	23.1 - 0.093 f	22.9 - 0.108 f
1	0	23.7 - 0.106 f	23.5 - 0.120 f
1	1	24.4 - 0.120 f	24.2 - 0.135 f

Note: f is the crystal frequency in MHz between 10 and 27 MHz. Effective load capacitance will be higher for crystal frequencies lower than 10 MHz. If a clock input is used, set C1 = 0 and C0 = 0.

Bypass Mode

If R6:0 is programmed to 0000000, the PLL is powered down and bypassed; the reference frequency will come from both CLK1 and CLK2. It is possible to generate glitches going into and out of this mode.

Configuring the IDT6V40277

The IDT6V40277 can be programmed to set the output functions and frequencies. The three data bytes are written in DATA pin in this order:

C1	C0	TTL	F1	F0	S2	S1	S0	V8	V7	V6	V5	V4	V3	V2	V1	V0	R6	R5	R4	R3	R2	R1	R0
MSB							LSB	MSB							LSB	MSB							LSB

C1 is loaded into the port first and R0 last.

R6:R0 Reference Divder Word (RDW)
V8:V0 VCO Divider Word (VDW)
S2:S0 Output Divider Select (OD)
F1:F0 Function of CLK2 Output
TTL Duty Cycle Settings
C1:C0 Internal Load Capacitance for Crystal

The IDT6V40277 can be reprogrammed at any time during operation. If R6:0, V8:0, TTL, or C1:0 are changed, the frequency will transition smoothly to the new value over about 1 ms, without glitches or short cycles. If S2:0 is changed, it is possible to generate glitches on CLK1 and also on CLK2 for F1:0 = 1 1.

Changing F1:0 will generate glitches on CLK2.

Power up default values for IDT6V40277

0	0	1	0	0	0	1	1

0	0	0	0	0	1	0	0

0	0	0	0	0	1	1	0

The input frequency will come from both outputs.

A warning about using the default configuration with input frequencies lower than 13.75 MHz

The VCO will run only as low as its minimum frequency, which is guaranteed to be no more than 55 MHz. So, in the powerup default condition, the PLL is guaranteed to lock to the input frequency down to 55/4 = 13.75 MHz. However, the part will typically run much slower. The typical minimum VCO frequency is about 30 - 40 MHz, depending on voltage, temperature, and lot variation; so in the powerup default setting, the CLK2 output will be a minimum of 7.5 - 10 MHz even if the input frequency is lower than that. The output is not locked to the reference input and so the frequency is not very stable and the phase noise is higher. In this condition, the CLK2 output will accurately provide the reference frequency down to 0 Hz because this signal path bypasses the PLL.

Power-down Mode

When the $\overline{\text{PDTS}}$ pin is pulled low, the chip will enter the power-down mode, where the output clocks are tri-stated and the rest of the chip is powered down. The chip can be programmed during power-down mode, however, if the chip is programmed during operation and enters power-down mode, the registers will return to their settings and not reset when exiting power-down mode ($\overline{\text{PDTS}}$ pin is pulled high).

Programming Example

To generate 66.66 MHz from a 14.31818 MHz input, the RDW should be 59, the VDW should be 276, and the Output Divide is 2. Selecting the minimum internal load capacitance, CMOS duty cycle, and CLK2 to be OFF means that the following three bytes are sent to the IDT6V40277:

00110001	10001010	00111011
Byte 1	Byte 2	Byte 3

As show in Figure 2, after these 24 bits are clocked into the IDT6V40277, taking STROBE high will send this data to the internal latch and the CLK output will lock within 10 ms.

Note: If STROBE is in the high state and SCLK is pulsed, DATA is clocked directly to the internal latch and the output conditions will change accordingly. Although this will not damage the IDT6V40277, it is recommended that STROBE be kept low while DATA is being clocked into the device in order to avoid unintended changes on the output clocks.

AC Parameters for Writing to the IDT6V40277

Parameter	Condition	Min.	Max.	Units
t_{SETUP}	Setup time	10		ns
t_{HOLD}	Hold time after SCLK	10		ns
t_W	Data wait time	10		ns
t_S	Strobe pulse width	40		ns
	SCLK Frequency		50	MHz

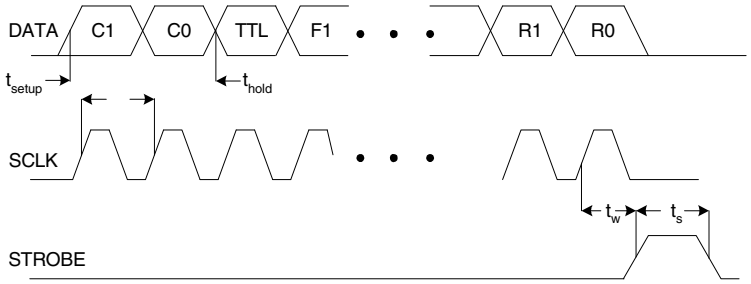


Figure 2. Timing Diagram for Programming

External Components/Crystal Selection

The IDT6V40277 requires a 0.01μF decoupling capacitor to be connected between VDD and GND. It must be connected close to the device to minimize lead inductance. A 33Ω terminating resistor can be used in series with CLK1 and CLK2 outputs. A parallel resonant, fundamental mode crystal with a load (correlation) capacitance of C should be used, where C is the value calculated from Table 4. For crystals with a specified load capacitance greater than C, additional crystal capacitors may be connected from each of the pins X1 and X2 to ground as shown in the Block Diagram on page 1. The value (in pF) of these crystal caps should be = $(C_L\text{-}C)*2$, where C_L is the crystal load capacitance in pF and C is the capacitance value from Table 4. These external capacitors are only required for applications where the exact frequency is critical. For a clock input, connect to X1 and leave X2 unconnected (no capacitors on either pin).

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT6V40277. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature, Industrial	-40 to +85°C
Storage Temperature	-65 to +150°C
Soldering Temperature	260°C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	-40		+85	°C
Power Supply Voltage (measured in respect to GND)	+3.0		+5.5	V

DC Electrical Characteristics

VDD=3.3 V ±5% , Ambient temperature -40° to +85°C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.0		5.5	V
Input High Voltage	V_{IH}	X1/ICLK only	(VDD/2)+1	VDD/2		V
Input Low Voltage	V_{IL}	X1/ICLK only		VDD/2	(VDD/2)-1	V
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}	$\overline{PDTS}$			0.4	V
		All other inputs			0.8	V
Output High Voltage	V_{OH}	I_{OH} = -25 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 25 mA			0.4	V
Output High Voltage, CMOS level	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Operating Supply Current	IDD	20 MHz crystal No load, 100 MHz out		26		mA
		100 MHz out, 3.3 V		13		mA
Short Circuit Current		CLK outputs		±70		mA
Input Capacitance	C_{IN}			4		pF
On-Chip Pull-up Resistor	R_{PU}	Pin 13		270		kΩ

AC Electrical Characteristics

VDD = 3.3 V ±5%, Ambient Temperature -40° to +85° C, unless stated otherwise

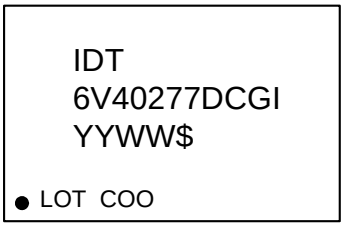
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	F_{IN}	Fundamental crystal	5		27	MHz
		Clock	2		50	MHz
Output Frequency (see Table 1)			6		200	MHz
		I-temp version	6		180	MHz
Output Clock Rise Time	t_{OR}	0.8 to 2.0 V, Note 1		1		ns
Output Clock Fall Time	t_{OF}	2.0 to 8.0 V, Note 1		1		ns
Output Clock Duty Cycle		even output divides	45	49-51	55	%
		odd output divides	40		60	%
Power-up Time		STROBE goes high until CLK out		3	10	ms
One Sigma Clock Period Jitter				50		ps
Maximum Absolute Jitter	t_{ja}	Deviation from mean		±120		ps

Note 1: Measured with 15 pF load.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		120		°C/W
	θ_{JA}	1 m/s air flow		115		°C/W
	θ_{JA}	3 m/s air flow		105		°C/W
Thermal Resistance Junction to Case	θ_{JC}			58		°C/W

Marking Diagram

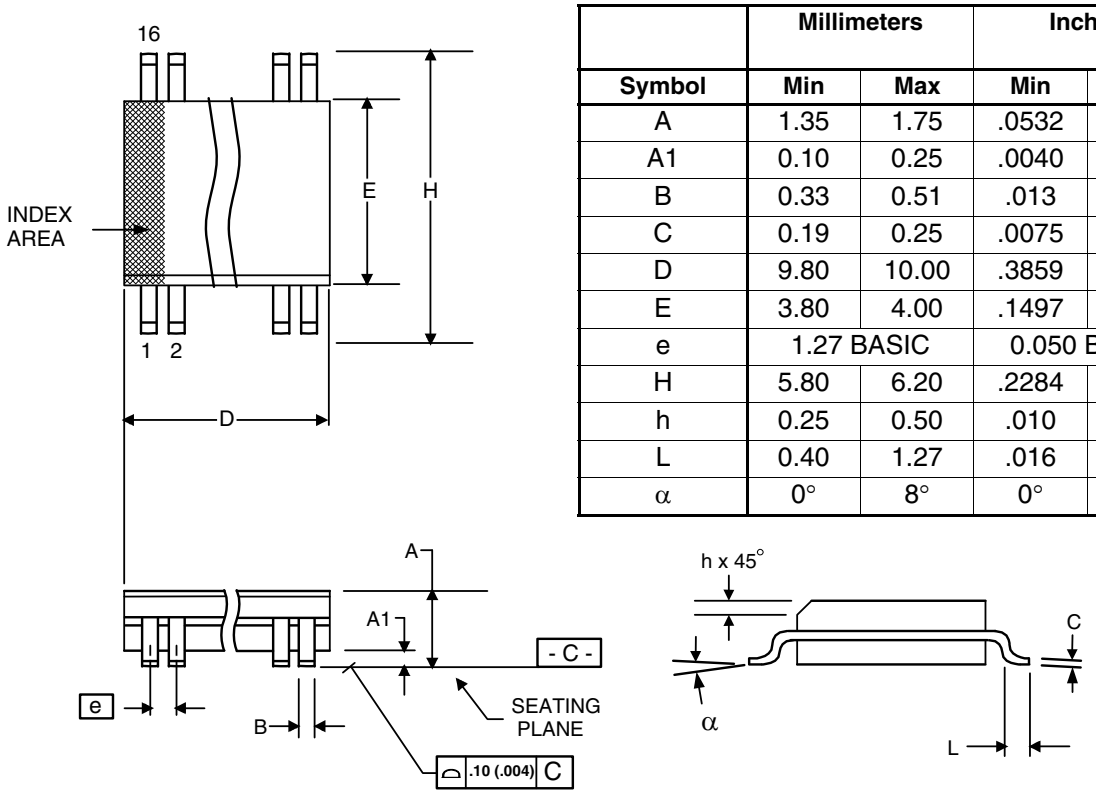


Notes:

1. “G” denotes RoHS compliant package.
2. “I” denotes industrial temperature grade.
3. “YYWW” is the last two digits of the year and week that the part was assembled.
4. “$” is the assembly mark code.
5. “LOT” is the lot number.
6. “COO” is the country of origin.

Package Outline and Package Dimensions (16-pin DCG, 150 Mil. Narrow Body SOIC)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
A	1.35	1.75	.0532	.0688
A1	0.10	0.25	.0040	.0098
B	0.33	0.51	.013	.020
C	0.19	0.25	.0075	.0098
D	9.80	10.00	.3859	.3937
E	3.80	4.00	.1497	.1574
e	1.27 BASIC		0.050 BASIC	
H	5.80	6.20	.2284	.2440
h	0.25	0.50	.010	.020
L	0.40	1.27	.016	.050
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping packaging	Package	Temperature
6V40277DCGI	see page 8	Tubes	16-pin SOIC	-40 to +85° C
6V40277DCGI8		Tape and Reel	16-pin SOIC	-40 to +85° C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

Revision History

Rev.	Date	Originator	Description of Change
A	06/14/12	J.Chao	Initial release - preliminary.
B	04/18/13	RDW	1. Updated front page to include "for Freescale systems" 2. Removed commercial operating temperature - industrial only. 3. Updated ordering information. 4. Added marking diagram. 5. Moved from Preliminary to Final

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