

Pin Assignment

| | | | |
|----------|----|----|--------|
| ^SEL | 1 | 20 | DIF_0 |
| VDDIN | 2 | 19 | DIF_0# |
| DIF_IN1 | 3 | 18 | DIF_1 |
| DIF_IN1# | 4 | 17 | DIF_1# |
| ^PD# | 5 | 16 | GND |
| DIF_IN2 | 6 | 15 | VDD |
| DIF_IN2# | 7 | 14 | DIF_2 |
| ^OE | 8 | 13 | DIF_2# |
| GND | 9 | 12 | DIF_3 |
| IREF | 10 | 11 | DIF_3# |

Note: Pins preceded by ^^ have internal
120K ohm pull up resistors
20-pin (173mil) TSSOP

Select Table

| SEL | Outputs |
|-----|---------|
| 0 | DIF_IN2 |
| 1 | DIF_IN1 |

Pin Descriptions

| PIN # | PIN NAME | PIN TYPE | DESCRIPTION |
|-------|----------|----------|---|
| 1 | ^SEL | IN | Selects between one of two inputs. This pin has internal pull up resistor. |
| 2 | VDDIN | PWR | Power pin for the Inputs, nominal 3.3V |
| 3 | DIF_IN1 | IN | 0.7 V Differential TRUE input |
| 4 | DIF_IN1# | IN | 0.7 V Differential Complementary Input |
| 5 | ^PD# | IN | Asynchronous active low input pin used to power down the device. The internal clocks are disabled and the VCO and the crystal osc. (if any) are stopped. |
| 6 | DIF_IN2 | IN | 0.7 V Differential TRUE input |
| 7 | DIF_IN2# | IN | 0.7 V Differential Complementary Input |
| 8 | ^OE | IN | Active high input for enabling outputs. This pin has an internal pull up resistor. 0 = disable outputs, 1= enable outputs |
| 9 | GND | PWR | Ground pin. |
| 10 | IREF | OUT | This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet. |
| 11 | DIF_3# | OUT | 0.7V differential Complementary clock output |
| 12 | DIF_3 | OUT | 0.7V differential true clock output |
| 13 | DIF_2# | OUT | 0.7V differential Complementary clock output |
| 14 | DIF_2 | OUT | 0.7V differential true clock output |
| 15 | VDD | PWR | Power supply, nominal 3.3V |
| 16 | GND | PWR | Ground pin. |
| 17 | DIF_1# | OUT | 0.7V differential Complementary clock output |
| 18 | DIF_1 | OUT | 0.7V differential true clock output |
| 19 | DIF_0# | OUT | 0.7V differential Complementary clock output |
| 20 | DIF_0 | OUT | 0.7V differential true clock output |

Application Information

Decoupling Capacitors

As with any high-performance mixed-signal IC, the IDT5V41067A must be isolated from system power supply noise to perform optimally.

Decoupling capacitors of 0.01 μ F must be connected between each VDD and the PCB ground plane.

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

Each 0.01 μ F decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.

2) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (the ferrite bead and bulk decoupling capacitor can be mounted on the back). Other signal traces should be routed away from the IDT5V41067A.

This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

External Components

A minimum number of external components are required for proper operation. Decoupling capacitors of 0.01 μ F should be connected between VDD and GND pairs (2,9 and 15,16) as close to the device as possible.

Current Reference Source R_r (I_{ref})

If board target trace impedance (Z) is 50 Ω , then $R_r = 475\Omega$ (1%), providing IREF of 2.32 mA, output current (I_{OH}) is equal to 6*IREF.

Load Resistors R_L

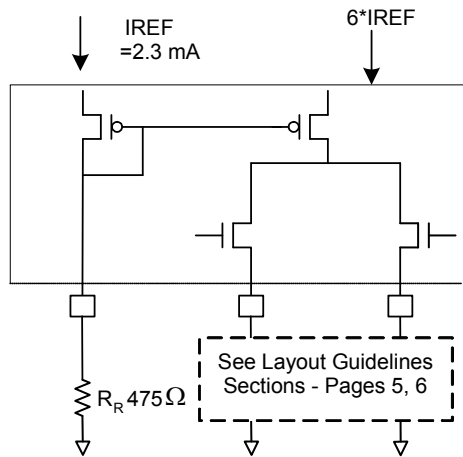
Since the clock outputs are open source outputs, 50 ohm external resistors to ground are to be connected at each clock output.

Output Termination

The PCI-Express differential clock outputs of the IDT5V41067A are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **Layout Guidelines** section.

The IDT5V41067A can also be terminated to LVDS compatible voltage levels. See the **Layout Guidelines** section.

Output Structures



General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1. Each $0.01 \mu\text{F}$ decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias should be used between decoupling capacitor and VDD pin.
3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41067A. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Layout Guidelines

| PCIe (SRC) Reference Clock | | | |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace | 0.5 max | inch | 1 |
| L2 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| L3 length, route as non-coupled 50ohm trace | 0.2 max | inch | 1 |
| Rs | 33 | ohm | 1 |
| Rt | 49.9 | ohm | 1 |

| Down Device Differential Routing | | | |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector | | | |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace | 0.225 min to 12.6 max | inch | 2 |

Figure 1: Down Device Routing

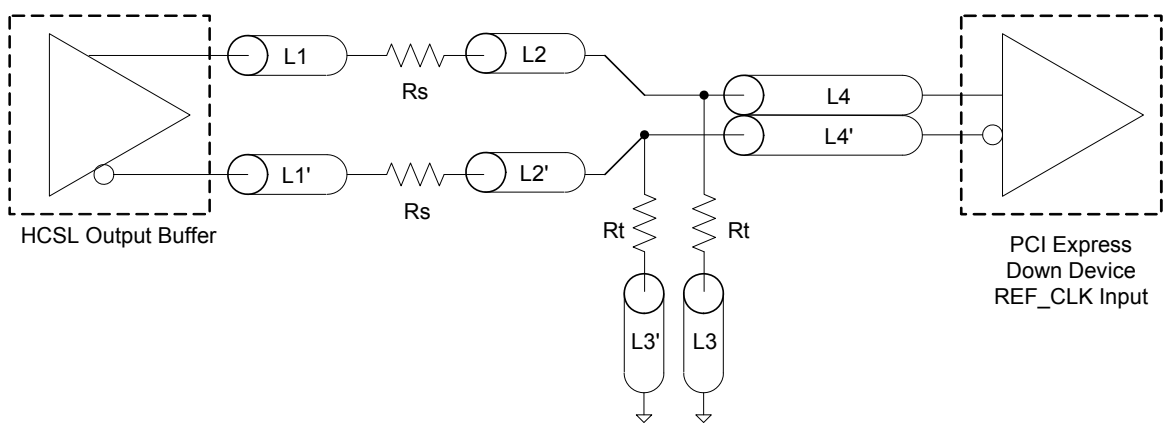
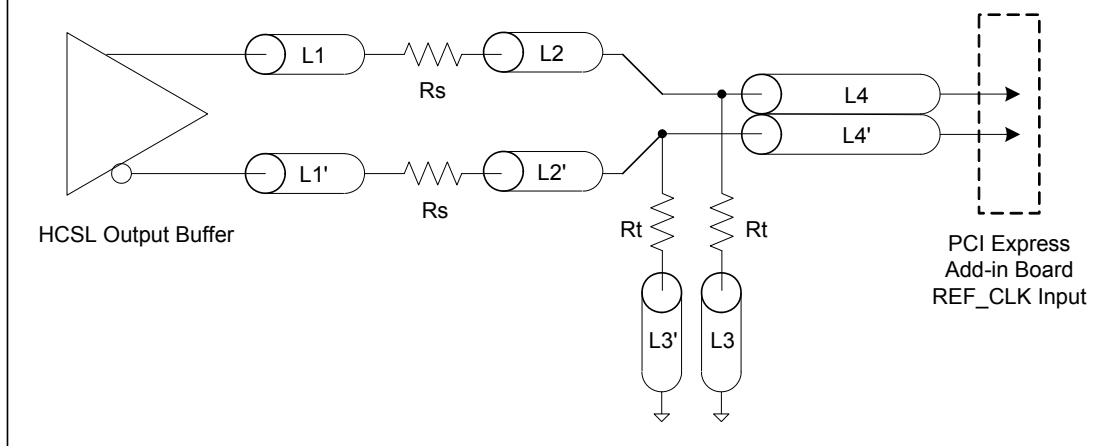
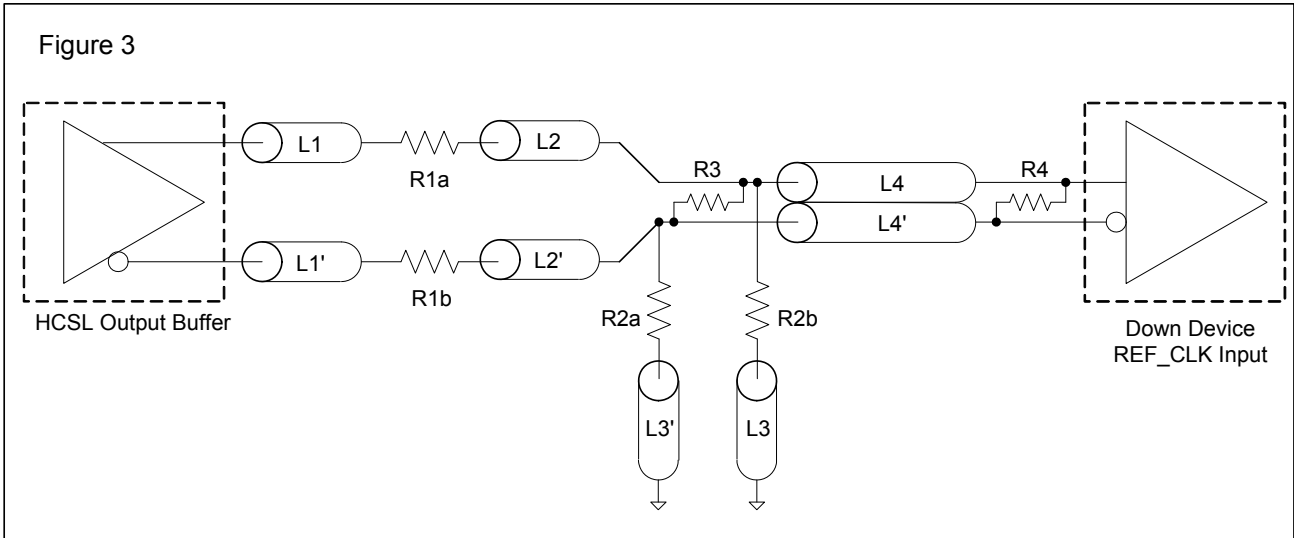


Figure 2: PCI Express Connector Routing

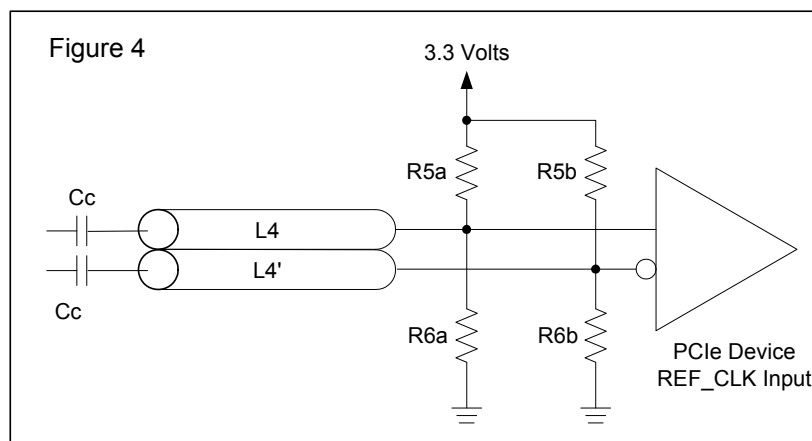


| Alternative Termination for LVDS and other Common Differential Signals (figure 3) | | | | | | | |
|---|-------|------|----|------|------|-----|--------------------------------|
| Vdiff | Vp-p | Vcm | R1 | R2 | R3 | R4 | Note |
| 0.45v | 0.22v | 1.08 | 33 | 150 | 100 | 100 | |
| 0.58 | 0.28 | 0.6 | 33 | 78.7 | 137 | 100 | |
| 0.80 | 0.40 | 0.6 | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60 | 0.3 | 1.2 | 33 | 174 | 140 | 100 | Standard LVDS |

R1a = R1b = R1
R2a = R2b = R2



| Cable Connected AC Coupled Application (figure 4) | | |
|---|-------------|------|
| Component | Value | Note |
| R5a, R5b | 8.2K 5% | |
| R6a, R6b | 1K 5% | |
| Cc | 0.1 μ F | |
| Vcm | 0.350 volts | |



Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41067A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|---------------------------|-----------------|------------------|---------|-----|-----------------------|-------|-------|
| 3.3V Logic Supply Voltage | VDD | | | | 4.6 | V | 1,2 |
| Input Low Voltage | V _{IL} | | GND-0.5 | | | V | 1 |
| Input High Voltage | V _{IH} | | | | V _{DD} +0.5V | V | 1 |
| Storage Temperature | T _s | | -65 | | 150 | °C | 1 |
| Junction Temperature | T _j | | | | 125 | °C | 1 |
| Input ESD protection | ESD prot | Human Body Model | 2000 | | | V | 1 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Operation under these conditions is neither implied nor guaranteed.

Electrical Characteristics—Input/Supply/Common Parameters

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|-------------------------------|-----------------------|---|-----------|-----|-----------------------|--------|-------|
| Ambient Operating Temperature | T _{COM} | Commercial range | 0 | | 70 | °C | 1 |
| | T _{IND} | Industrial range | -40 | | 85 | °C | 1 |
| Input High Voltage | V _{IH} | Single-ended inputs, <i>except</i> SMBus, low threshold and tri-level inputs, if present | 2.2 | | V _{DD} + 0.3 | V | 1 |
| Input Low Voltage | V _{IL} | Single-ended inputs, <i>except</i> SMBus, low threshold and tri-level inputs, if present | GND - 0.3 | | 0.8 | V | 1 |
| Input Current | I _{IN} | Single-ended inputs, V _{IN} = GND, V _{IN} = VDD | -5 | | 5 | uA | 1 |
| | I _{INP} | Single-ended inputs V _{IN} = 0 V; Inputs with internal pull-up resistors V _{IN} = VDD; Inputs with internal pull-down resistors | -200 | | 200 | uA | 1 |
| Input Frequency | F _{ibyp} | V _{DD} = 3.3 V, Bypass mode | | | 200 | MHz | 2 |
| Pin Inductance | L _{pin} | | | | 7 | nH | 1 |
| Capacitance | C _{IN} | Logic Inputs, <i>except</i> DIF_IN | 1.5 | | 5 | pF | 1 |
| | C _{INDIF_IN} | Differential clock inputs | 1.5 | | 2.7 | pF | 1,4 |
| | C _{OUT} | Output pin capacitance | | | 6 | pF | 1 |
| OE Latency | t _{LATOE#} | DIF start after OE# assertion DIF stop after OE# deassertion | 1 | | 3 | clocks | 1,3,5 |
| PD# Latency | t _{STABPD#} | DIF driven to 200mV after PDE# assertion | | | 300 | usec | 1,3,5 |
| T _{fall} | t _F | Fall time of control inputs | | | 5 | ns | 1,2 |
| T _{rise} | t _R | Rise time of control inputs | | | 5 | ns | 1,2 |

¹Guaranteed by design and characterization, not 100% tested in production.

²Control input must be monotonic from 20% to 80% of input swing.

³Time from deassertion until outputs are >200 mV

⁴INAB inputs

⁵The differential input clock must be running for the OE pin to work

Electrical Characteristics–Clock Input Parameters

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------------------|--------------------|---|-----------------------|-----|------|-------|-------|
| Input High Voltage - DIF_IN | V _{IHDIF} | Differential inputs (single-ended measurement) | 600 | 800 | 1150 | mV | 1 |
| Input Low Voltage - DIF_IN | V _{ILDIF} | Differential inputs (single-ended measurement) | V _{SS} - 300 | 0 | 300 | mV | 1 |
| Input Common Mode Voltage - DIF_IN | V _{COM} | Common Mode Input Voltage | 300 | | 1000 | mV | 1 |
| Input Amplitude - DIF_IN | V _{SWING} | Peak to Peak value | 300 | | 1450 | mV | 1 |
| Input Slew Rate - DIF_IN | dv/dt | Measured differentially | 1 | | 8 | V/ns | 1,2 |
| Input Leakage Current | I _{IN} | V _{IN} = V _{DD} , V _{IN} = GND | -5 | | 5 | uA | 1 |
| Input Duty Cycle | d _{in} | Measurement from differential waveform | 45 | | 55 | % | 1 |
| Input Jitter - Cycle to Cycle | J _{DIFin} | Differential Measurement | 0 | | 125 | ps | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

² Slew rate measured through +/-75mV window centered around differential zero.

Electrical Characteristics–DIF 0.7V Current Mode Differential Outputs

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|------------------------|---|------|------|------|-------|---------|
| Slew rate | T _{rf} | Scope averaging on | 1.5 | 2.9 | 4 | V/ns | 1, 2, 3 |
| Slew rate matching | ΔT _{rf} | Slew rate matching, Scope averaging on | | 14.4 | 20 | % | 1, 2, 4 |
| Voltage High | V _{High} | Statistical measurement on single-ended signal using oscilloscope math function. (Scope averaging on) | 660 | 761 | 850 | mV | 1 |
| Voltage Low | V _{Low} | | -150 | 0.6 | 150 | | 1 |
| Max Voltage | V _{max} | Measurement on single ended signal using absolute value. (Scope averaging off) | | 860 | 1150 | mV | 1 |
| Min Voltage | V _{min} | | -300 | -78 | | | 1 |
| V _{swing} | V _{swing} | Scope averaging off | 300 | 1531 | | mV | 1, 2 |
| Crossing Voltage (abs) | V _{cross_abs} | Scope averaging off | 250 | 354 | 550 | mV | 1, 5 |
| Crossing Voltage (var) | Δ-V _{cross} | Scope averaging off | | 36 | 140 | mV | 1, 6 |

¹ Guaranteed by design and characterization, not 100% tested in production. I_{REF} = VDD/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω (100Ω differential impedance).

² Measured from differential waveform

³ Slew rate is measured through the V_{swing} voltage range centered around differential 0V. This results in a +/-150mV window around differential 0V.

⁴ Matching applies to rising edge rate of Clock / falling edge rate of Clock#. It is measured in a +/-75mV window centered on the average cross point where Clock rising meets Clock# falling. The median cross point is used to calculate the voltage thresholds the oscilloscope uses for the edge rate calculations.

⁵ V_{cross} is defined as voltage where Clock = Clock# measured on a component test board and only applies to the differential rising edge (i.e. Clock rising and Clock# falling).

⁶ The total variation of all V_{cross} measurements in any particular system. Note that this is a subset of V_{cross_min/max} (V_{cross} absolute) allowed. The intent is to limit V_{cross} induced modulation by setting V_{cross_delta} to be smaller than V_{cross} absolute.

Electrical Characteristics–Current Consumption

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|--------------------------|----------------------|---|-----|-----|-----|-------|-------|
| Operating Supply Current | I _{DD3.3OP} | All outputs active @100MHz, C _L = 2pF; | | 80 | 85 | mA | 1 |
| Power Down Current | I _{DD3.3PD} | PD# pin low, input clock stopped | | 4 | 5 | mA | 1 |

¹ Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics–Output Duty Cycle, Jitter, and Skew Characteristics

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | NOTES |
|------------------------|----------------------|---------------------------------------|------|------|------|-------|-------|
| Duty Cycle | t _{DC} | When driven by 932SQ420 or equivalent | 45 | 49 | 55 | % | 1 |
| Duty Cycle Distortion | t _{DCD} | Measured differentially, @100MHz | -2 | 1.3 | 2 | % | 1,4 |
| Skew, Input to Output | t _{pdBYP} | V _T = 50% | 2500 | 3300 | 4500 | ps | 1 |
| Skew, Output to Output | t _{sk3} | V _T = 50% | | 37 | 50 | ps | 1 |
| Additive Jitter | t _{cyc-cyc} | Cycle to cycle Additive Jitter | | 1.1 | 10 | ps | 1,3 |

¹Guaranteed by design and characterization, not 100% tested in production.

²I_{REF} = V_{DD}/(3xR_R). For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

³Measured from differential waveform

⁴Duty cycle distortion is the difference in duty cycle between the output and the input clock when the device is operated in bypass mode.

Electrical Characteristics–PCIe Phase Jitter Parameter

TA = T_{COM} or T_{IND}; Supply Voltage VDD/VDDA = 3.3 V +/-5%, See Test Loads for Loading Conditions

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS | Notes |
|-----------------------|------------------------|--|-----|-----|-----|----------|-----------|
| Additive Phase Jitter | t _{jphPCIeG1} | PCIe Gen 1 | | 1 | 5 | ps (p-p) | 1,2,3,6 |
| | t _{jphPCIeG2} | PCIe Gen 2 Lo Band 10kHz < f < 1.5MHz | | 0.1 | 0.2 | ps (rms) | 1,2,5,6 |
| | | PCIe Gen 2 High Band 1.5MHz < f < Nyquist (50MHz) | | 0.1 | 0.2 | ps (rms) | 1,2,5,6 |
| | t _{jphPCIeG3} | PCIe Gen 3 (PLL BW of 2-4MHz, CDR = 10MHz) | | 0.1 | 0.2 | ps (rms) | 1,2,4,5,6 |

¹Applies to all outputs.

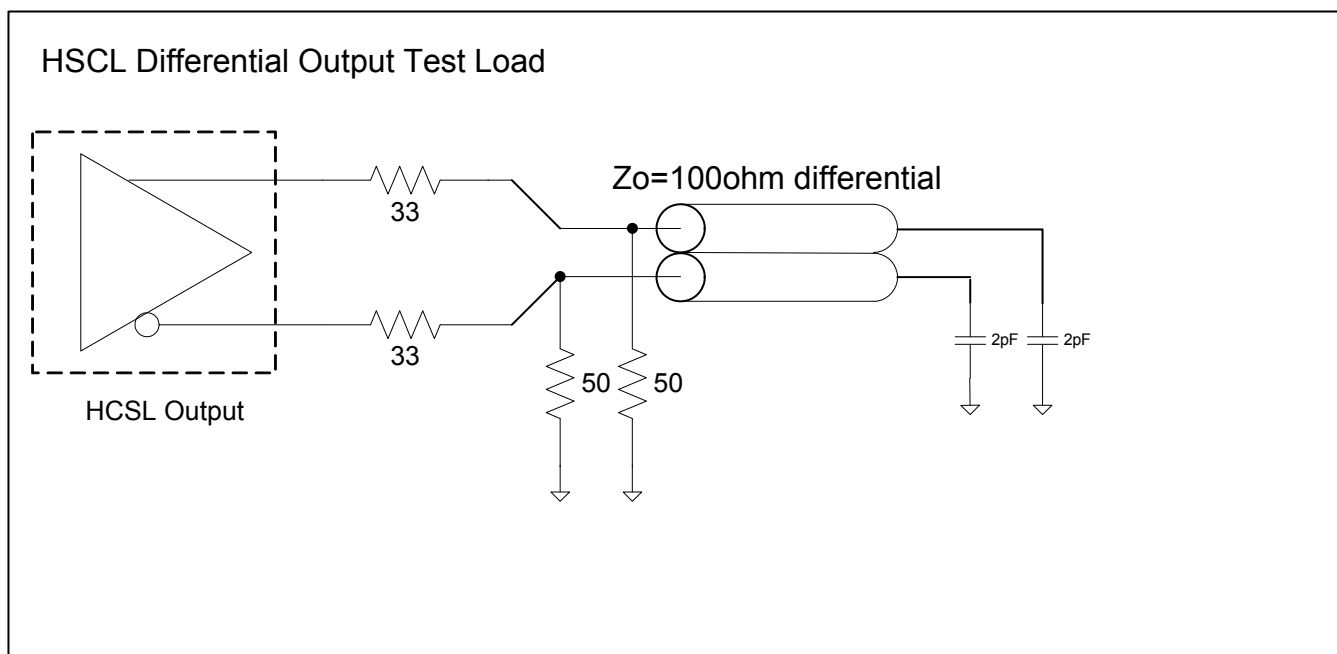
²See <http://www.pcisig.com> for complete specs

³Sample size of at least 100K cycles. This figures extrapolates to 108ps pk-pk @ 1M cycles for a BER of 1-12.

⁴Subject to final radification by PCI SIG.

⁵For RMS figures, additive jitter is calculated by solving the following equation: Additive jitter = SQRT[(total jitter)² - (input jitter)²]

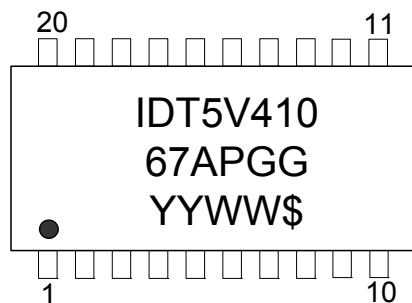
⁶Applies to 100MHz spread off and 0.5% down spread sources only.



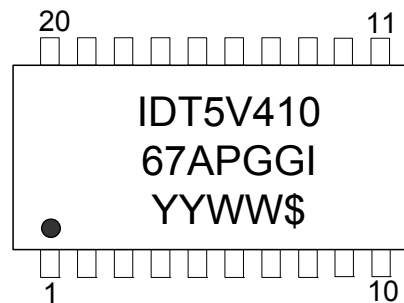
Thermal Characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units |
|--|---------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ_{JA} | Still air | | 93 | | °C/W |
| | θ_{JA} | 1 m/s air flow | | 78 | | °C/W |
| | θ_{JA} | 3 m/s air flow | | 65 | | °C/W |
| Thermal Resistance Junction to Case | θ_{JC} | | | 20 | | °C/W |

Marking Diagram



Marking Diagram (Industrial)

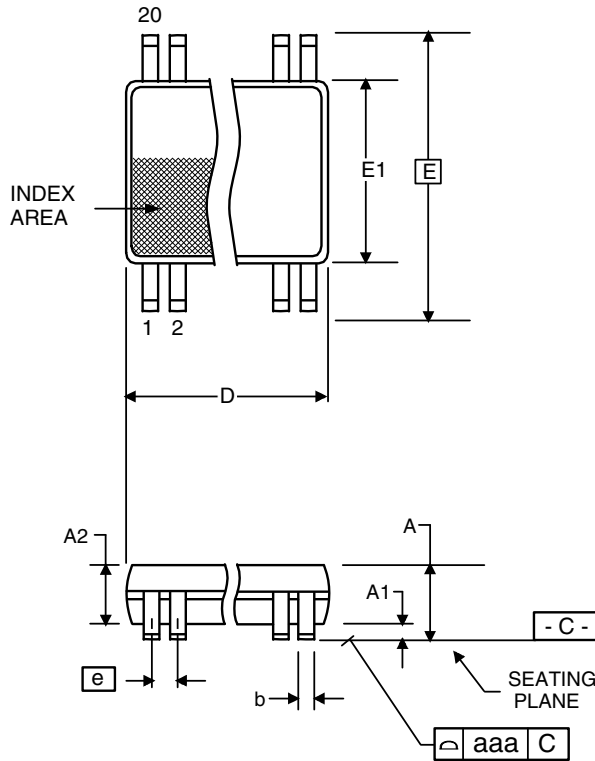


Notes:

1. \$ is the mark code.
2. YYWW is the last two digits of the year and week that the part was assembled.
3. "G" after the two-letter package code denotes RoHS compliant package.
4. "I" denotes industrial grade.
5. Bottom marking: country of origin if not USA.

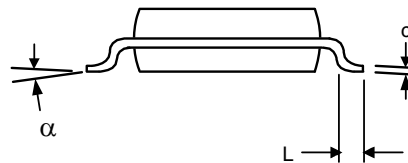
Package Outline and Package Dimensions (20-pin TSSOP, 173 Mil. Narrow Body)

Package dimensions are kept current with JEDEC Publication No. 95



| Symbol | Millimeters | | Inches* | |
|--------|-------------|------|--------------|-------|
| | Min | Max | Min | Max |
| A | | 1.20 | | 0.047 |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 |
| A2 | 0.80 | 1.05 | 0.032 | 0.041 |
| b | 0.19 | 0.30 | 0.007 | 0.012 |
| c | 0.09 | 0.20 | 0.0035 | 0.008 |
| D | 6.40 | 6.60 | 0.252 | 0.260 |
| E | 6.40 BASIC | | 0.252 BASIC | |
| E1 | 4.30 | 4.50 | 0.169 | 0.177 |
| e | 0.65 Basic | | 0.0256 Basic | |
| L | 0.45 | 0.75 | 0.018 | 0.030 |
| a | 0° | 8° | 0° | 8° |
| aaa | -- | 0.10 | -- | 0.004 |

*For reference only. Controlling dimensions in mm.



Ordering Information

| Part / Order Number | Shipping Packaging | Package | Temperature |
|---------------------|--------------------|--------------|--------------|
| 5V41067APGG | Tubes | 20-pin TSSOP | 0 to +70°C |
| 5V41067APGG8 | Tape and Reel | 20-pin TSSOP | 0 to +70°C |
| 5V41067APGGI | Tubes | 20-pin TSSOP | -40 to +85°C |
| 5V41067APGGI8 | Tape and Reel | 20-pin TSSOP | -40 to +85°C |

“G” after the two-letter package code are the Pb-Free configuration, RoHS compliant.

“A” is the device revision designer (will not correlate to the datasheet revision).

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Revision History

| Rev. | Originator | Issue Date | Description | Page # |
|------|------------|------------|--|----------|
| A | RDW | 1/7/2011 | Initial Release | |
| B | RDW | 1/25/2011 | 1. Corrected Pin 14 is corrected to be DIF_2 true, not complement 2. Added PD# latency (tSTAB) to electrical tables. 3. Input slew rate changed FROM 0.4V/ns MIN to 1.0V/ns MIN. Max value stays unchanged. 4. Output slew rate changed FROM 0.5V/ns – 2.0V/ns TO 1 V/ns – 4V/ns. 5. Output Disabled Current changed to Power Down Current. 6. Reference to Bypass mode removed, this part has no PLL and always operates in bypass mode. 7. Added footnote 5 to PCIE Phase Jitter Parameter Tables. | Various |
| C | RDW | 5/9/2011 | 1. Updated electrical characteristics and ordering information 2. Updated ordering information to indicate Rev A. | Various |
| D | RDW | 6/2/2011 | 1. Tightened additive phase jitter specifications 2. Added part marking information | 1, 9, 10 |
| E | RDW | 10/6/2011 | Release to final. | |
| F | RDW | 11/22/2011 | 1. Changed title to "2:1 PCIe GEN1/2/3 Clock Multiplexer" 2. Updated PCIe Phase Jitter table | Various |
| F | RDW | 6/7/2013 | Corrected typo in DS title. Was "2:1 PCIe."; now "2:4 PCIe." | Various |

IDT5V41067A

2:4 PCIE GEN1/2/3 CLOCK MULTIPLEXER

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