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3882 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0089-0101
Rev.1.01
Nov 14, 2005

GENERAL DESCRIPTION

The 3882 group is the 8-bit microcomputer based on the 740 family core technology.

The 3882 group is designed for Keyboard Controller for the note book PC.

FEATURES

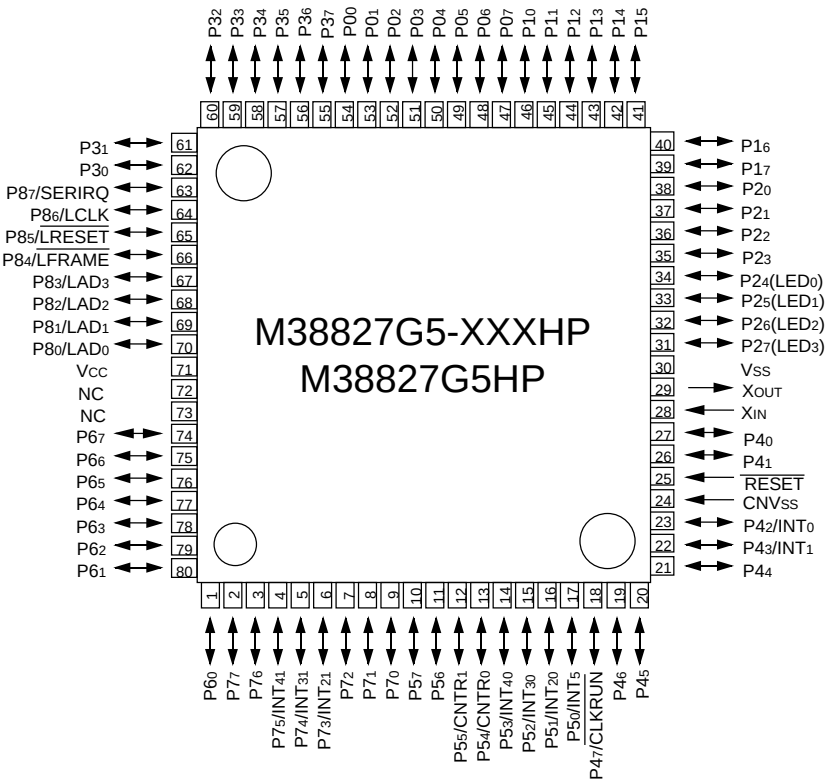
<Microcomputer mode>

- Basic machine-language instructions 71
- Minimum instruction execution time ..... 0.5 µs
  (at 8 MHz oscillation frequency)
- Memory size
  ROM ..... 20K bytes
  RAM ..... 1024 bytes
- Programmable input/output ports 72
- Software pull-up transistors 8
- Interrupts ..... 17 sources, 14 vectors
- Timers ..... 8-bit × 4
- Watchdog timer ..... 16-bit × 1
- LPC interface ..... 2 channels
- Serialized IRQ ..... 3 factors
- Clock generating circuit ..... Built-in 1 circuits
  (connect to external ceramic resonator)
- Power source voltage ..... 3.0 to 3.6 V
- Power dissipation
  In high-speed mode ..... 20 mW
  (at 8 MHz oscillation frequency, at 3.3 V power source voltage)
- Operating temperature range ..... –20 to 85°C

APPLICATION

Note book PC

PIN CONFIGURATION (TOP VIEW)



Package type : PLQP0080KB-A (80P6Q-A)

Fig. 1 Pin configuration

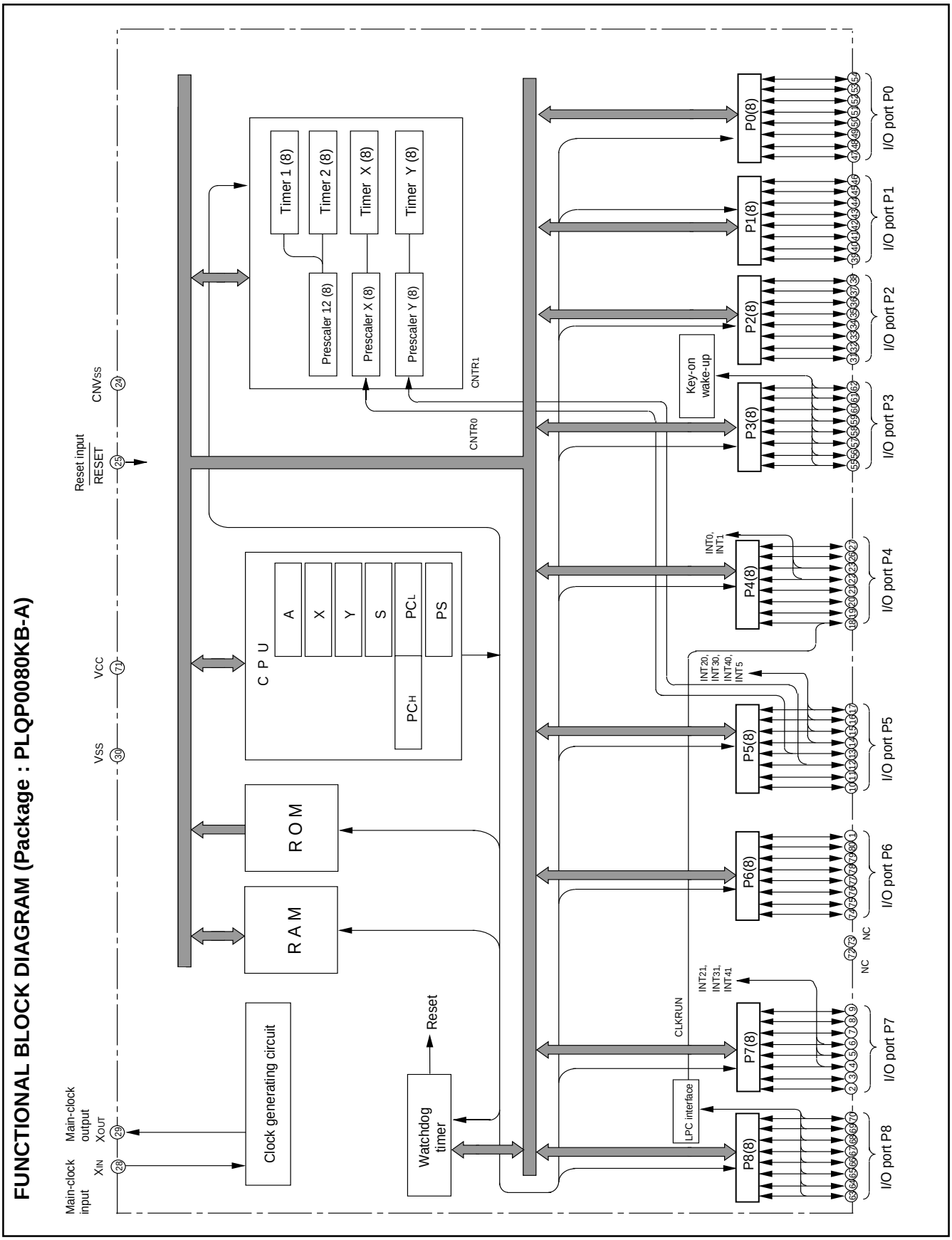


Fig. 2 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Functions	Function except a port function
V_{CC}, V_{SS}	Power source	•Apply voltage of 3.3 V ±10 % to Vcc, and 0 V to Vss.	
CNV_{SS}	CNV_{SS} input	•Connected to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active “L”.	
X_{IN}	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open.	
X_{OUT}	Clock output		
$P0_0$–$P0_7$	I/O port P0	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure or N-channel open-drain output structure.	
$P1_0$–$P1_7$	I/O port P1	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure or N-channel open-drain output structure.	
$P2_0$–$P2_7$	I/O port P2	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •$P2_4$ to $P2_7$ (4 bits) are enabled to output large current for LED drive.	
$P3_0$–$P3_7$	I/O port P3	•8-bit I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •These pins function as key-on wake-up . •These pins are enabled to control pull-up.	•Key-on wake-up input pins

Table 2 Pin description (2)

Pin	Name	Functions	Function except a port function
P40 P41	I/O port P4	•8-bit I/O port with the same function as port P0 <Input level> CMOS compatible input level <Output level> P40, P41 : CMOS 3-state output structure P42-P47 : CMOS 3-state output structure or N-channel open-drain output structure •Each pin level of P42 to P46 can be read even in output port mode.	
P42/INT0 P43/INT1			•Interrupt input pins
P44 P45 P46			
P47 /CLKRUN			•Serialized IRQ function pin
P50/INT5 P51/INT20 P52/INT30 P53/INT40	I/O port P5	•8-bit I/O port with the same function as port P0 •CMOS compatible input level •CMOS 3-state output structure	•Interrupt input pins
P54/CNTR0 P55/CNTR1			•Timer X, timer Y function pins
P56 P57			
P60–P67	I/O port P6	•8-bit I/O port with the same function as port P0 •CMOS compatible input level. •CMOS 3-state output structure.	
P70 P71 P72	I/O port P7	•8-bit CMOS I/O port with the same function as port P0 <Input level> P70–P75 : CMOS compatible input level or TTL compatible input level P76, P77 : CMOS compatible input level <Output structure> N-channel open-drain output structure •Each pin level of P70 to P75 can be read even in output port mode.	
P73/INT21 P74/INT31 P75/INT41			•Interrupt input pins
P76 P77			
P80/LAD0 P81/LAD1 P82/LAD2 P83/LAD3 P84/LFRAME P85/LRESET P86/LCLK	I/O port P8	•8-bit CMOS I/O port with the same function as port P0 •CMOS compatible input level. •CMOS 3-state output structure.	•LPC interface function pins
P87/SERIRQ			•Serialized IRQ function pin

PART NUMBERING

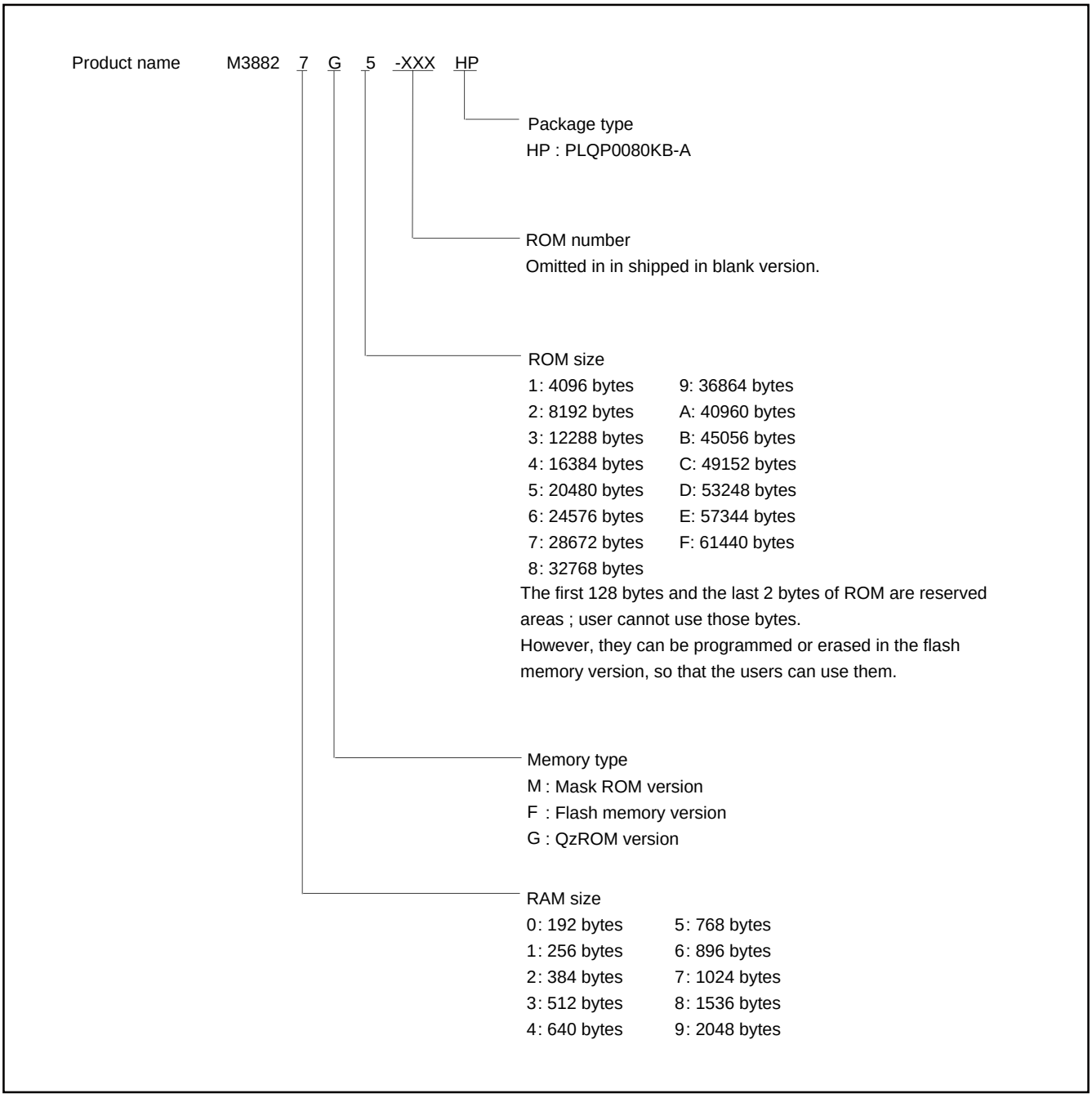


Fig. 3 Part numbering

GROUP EXPANSION

Renesas plans to expand the 3882 group as follows.

Memory Type

Support for QzROM version.

Memory Size

ROM size ..... 20 K bytes
RAM size ..... 1024 bytes

Packages

PLQP0080KB-A ..... 0.5 mm-pitch plastic molded LQFP

Memory Expansion

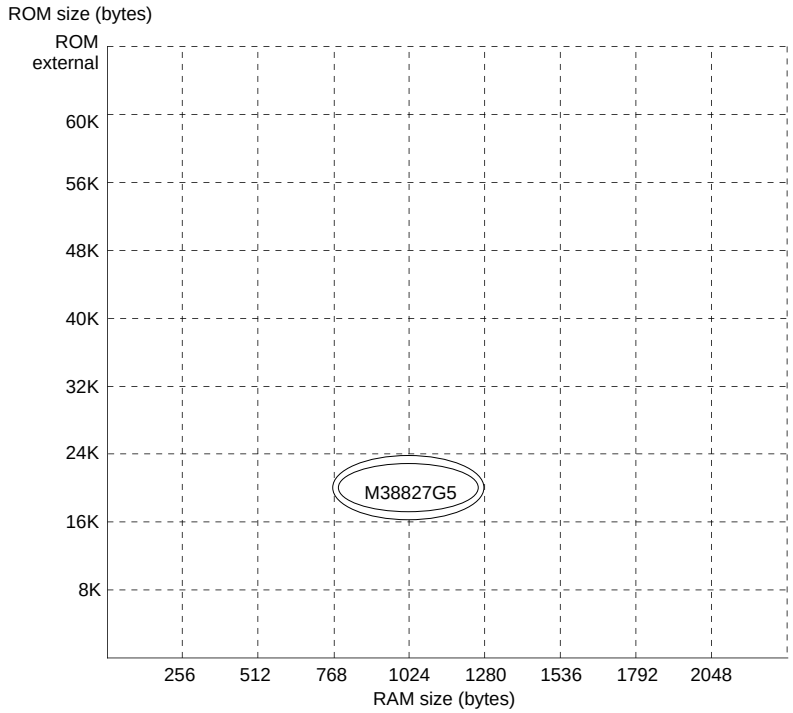


Fig. 4 Memory expansion plan

Table 3 Products plan list **As of Nov 2005**

Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38827G5-XXXHP	20480(20350)	1024	80P6Q-A	QzROM version (Programmed shipment) **(Note 1)**
M38827G5HP				QzROM version (blank) **(Note 2)**

Notes 1: This means a shipment of which User ROM has been programmed.
2: The user ROM area of a blank product is blank.

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3882 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.

Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

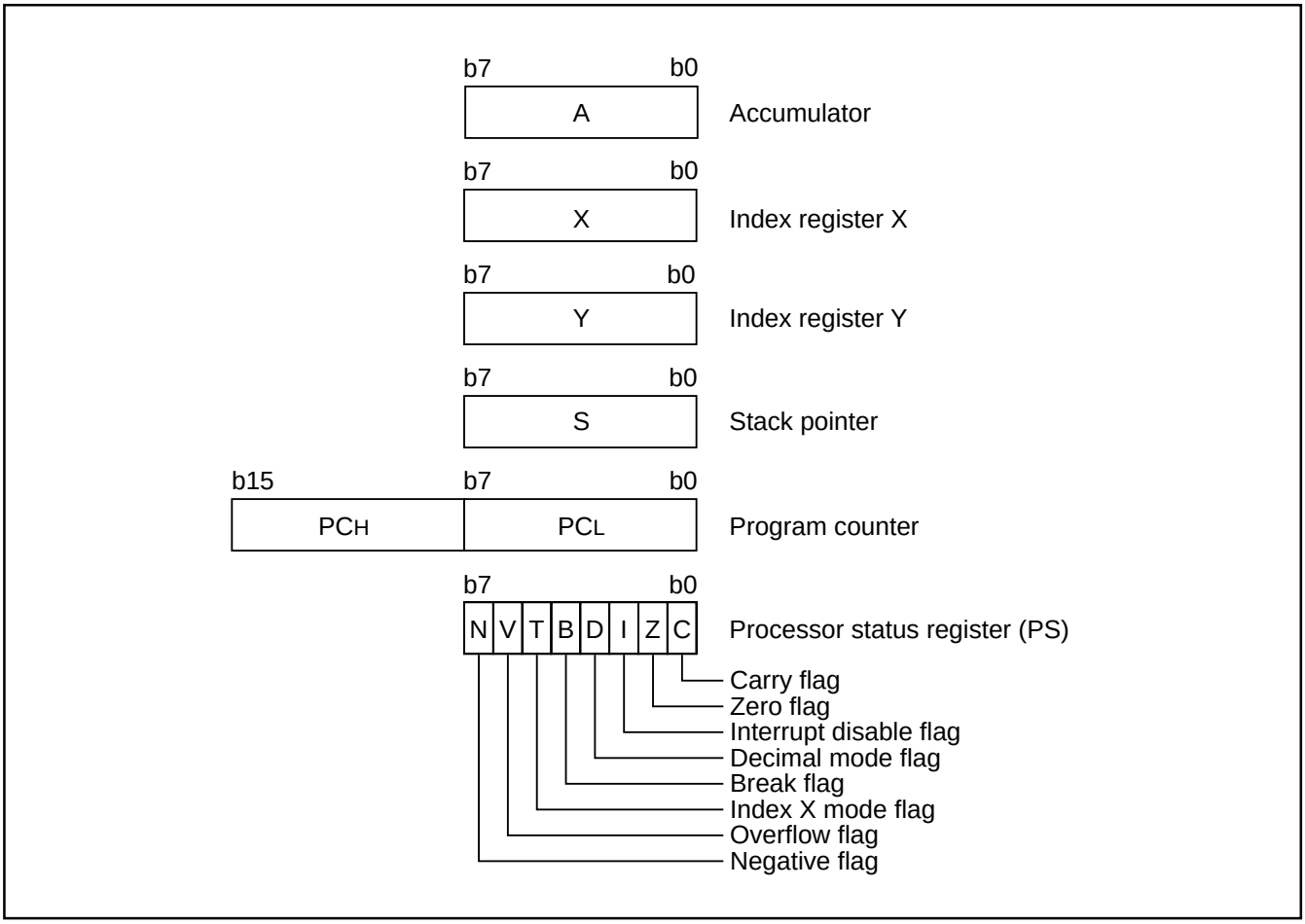


Fig. 5 740 Family CPU register structure

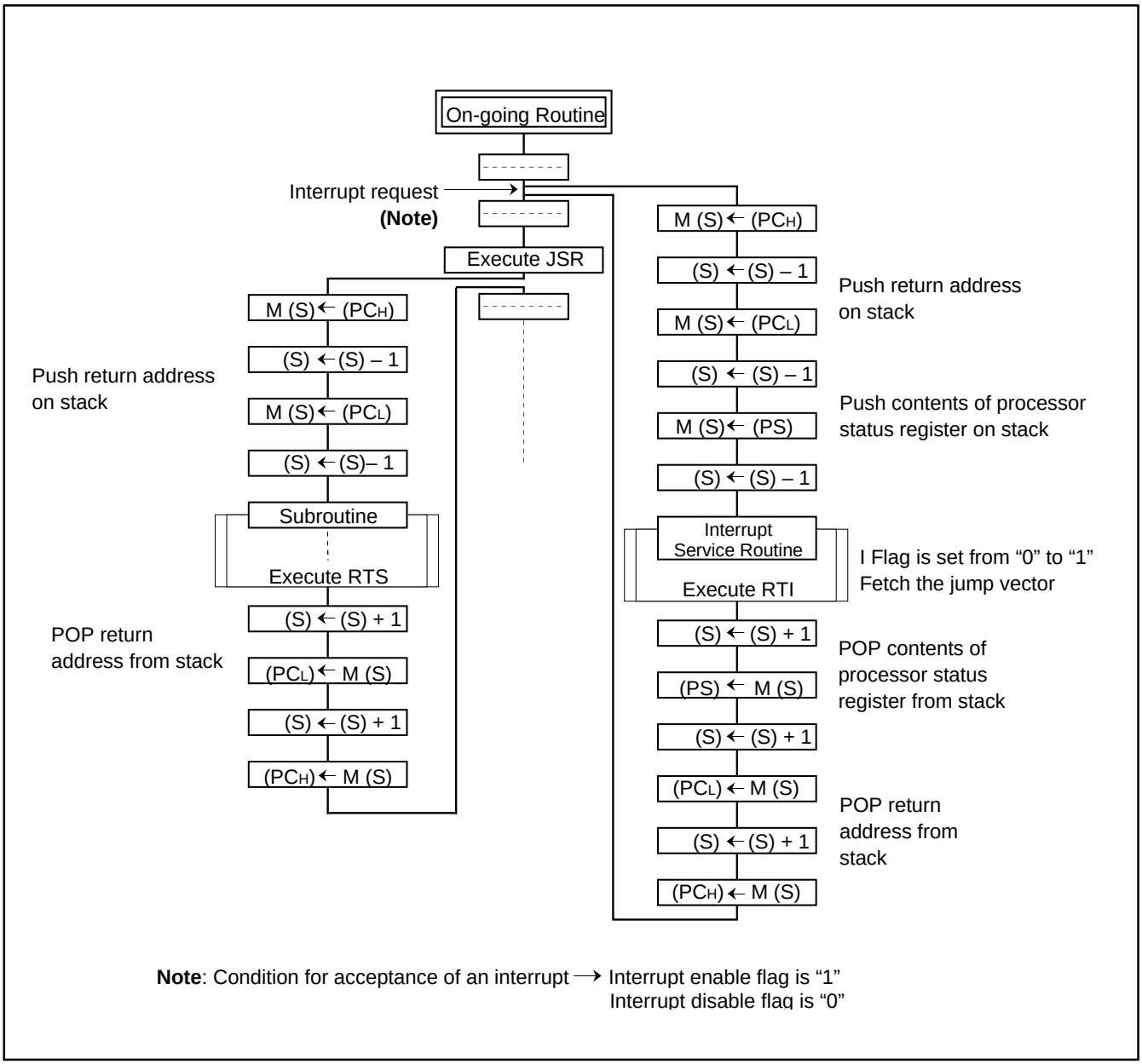


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is “0”, and cleared if the result is anything other than “0”.

•Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is “1”.

•Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”. Decimal correction is automatic in decimal mode. Only the ADC

•Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always “0”. When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to “1”.

•Bit 5: Index X mode flag (T)

When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.
The CPU mode register is allocated at address 003B16.

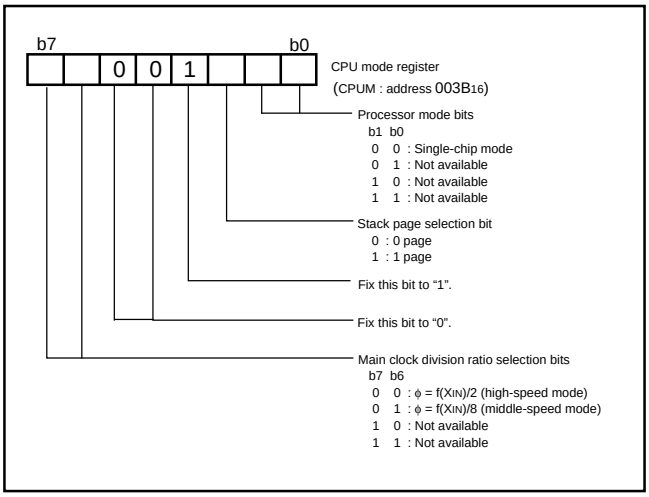


Fig. 7 Structure of CPU mode register

MEMORY

RAM
RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM
ROM is used for program code and data table storage.
The first 128 bytes and the last 2 bytes of ROM are reserved for device testing code and the rest is user area.

Zero Page
Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page
Access to this area with only 2 bytes is possible in the special page addressing mode.

Interrupt Vector Area
The interrupt vector area contains reset and interrupt vectors.

Special Function Register (SFR) Area
The special function register area contains the control registers such as I/O ports, timers, serial I/O, etc.

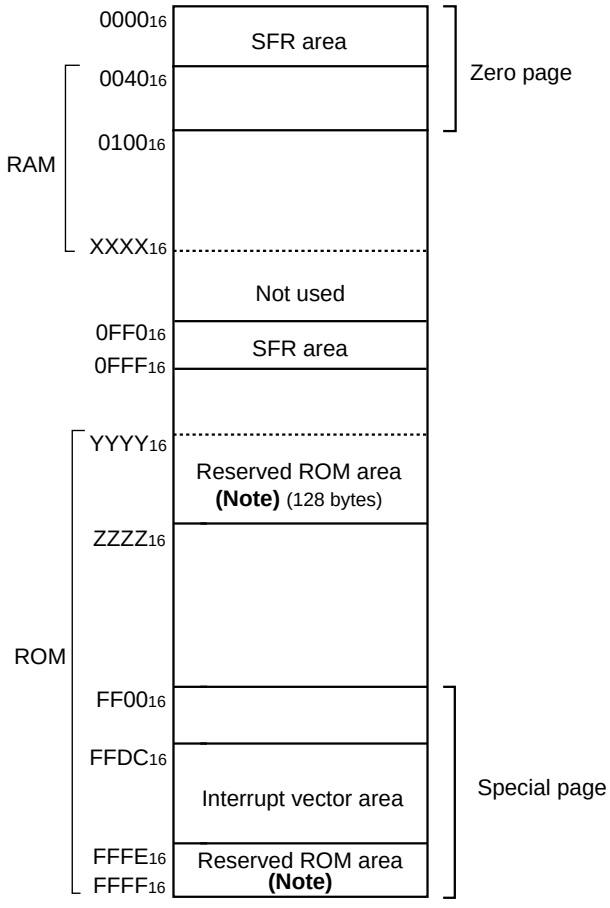
ROM Code Protect Address
"00_{16} " is written into ROM code protect address (other than the user ROM area) when selecting the protect bit write by using a serial programmer or selecting protect enabled for writing shipment by Renesas Technology corp..When "00_{16} " is set to the ROM code protect address,the protect function is enabled,so that reading or writing from/to QzROM is disabled by a serial programmer.
As for the QzROM product in blank, the ROM code is protected by selecting the protect bit write at ROM writing with a serial programmer.
As for the QzROM product shipped after writing,"00_{16} " (protect enabled) or "FF_{16} " (protect disabled) is written into the ROM code protect address when Renesas Technology corp. performs writing. The writing of "00_{16}" or "FF_{16} " can be selected as ROM option setup ("MASK option " written in the mask file converter) when ordering.

RAM area

RAM size (bytes)	Address $XXXX_{16}$
1024	$043F_{16}$

ROM area

ROM size (bytes)	Address $YYYY_{16}$	Address $ZZZZ_{16}$
20480	$B000_{16}$	$B080_{16}$



Notes: This area is reserved in the QzROM version.

Fig. 8 Memory map diagram

0000_{16}	Port P0 (P0)
0001_{16}	Port P0 direction register (P0D)
0002_{16}	Port P1 (P1)
0003_{16}	Port P1 direction register (P1D)
0004_{16}	Port P2 (P2)
0005_{16}	Port P2 direction register (P2D)
0006_{16}	Port P3 (P3)
0007_{16}	Port P3 direction register (P3D)
0008_{16}	Port P4 (P4)
0009_{16}	Port P4 direction register (P4D)
$000A_{16}$	Port P5 (P5)
$000B_{16}$	Port P5 direction register (P5D)
$000C_{16}$	Port P6 (P6)
$000D_{16}$	Port P6 direction register (P6D)
$000E_{16}$	Port P7 (P7)
$000F_{16}$	Port P7 direction register (P7D)
0010_{16}	Port P8 (P8)/Port P4 input register (P4I)
0011_{16}	Port P8 direction register (P8D)/Port P7 input register (P7I)
0012_{16}	
0013_{16}	
0014_{16}	
0015_{16}	
0016_{16}	
0017_{16}	
0018_{16}	
0019_{16}	
$001A_{16}$	
$001B_{16}$	
$001C_{16}$	
$001D_{16}$	Serialized IRQ control register (SERCON)
$001E_{16}$	Watchdog timer control register (WDTCON)
$001F_{16}$	Serialized IRQ request register (SERIRQ)

0020_{16}	Prescaler 12 (PRE12)
0021_{16}	Timer 1 (T1)
0022_{16}	Timer 2 (T2)
0023_{16}	Timer XY mode register (TM)
0024_{16}	Prescaler X (PREX)
0025_{16}	Timer X (TX)
0026_{16}	Prescaler Y (PREY)
0027_{16}	Timer Y (TY)
0028_{16}	Data bas buffer register 0 (DBB0)
0029_{16}	Data bas buffer status register 0 (DBBSTS0)
$002A_{16}$	LPC control register (LPCCON)
$002B_{16}$	Data bas buffer register 1 (DBB1)
$002C_{16}$	Data bas buffer status register 1 (DBBSTS1)
$002D_{16}$	
$002E_{16}$	Port control register 1 (PCTL1)
$002F_{16}$	Port control register 2 (PCTL2)
0030_{16}	
0031_{16}	
0032_{16}	
0033_{16}	
0034_{16}	
0035_{16}	
0036_{16}	
0037_{16}	
0038_{16}	
0039_{16}	Interrupt source selection register (INTSEL)
$003A_{16}$	Interrupt edge selection register (INTEDGE)
$003B_{16}$	CPU mode register (CPUM)
$003C_{16}$	Interrupt request register 1 (IREQ1)
$003D_{16}$	Interrupt request register 2 (IREQ2)
$003E_{16}$	Interrupt control register 1 (ICON1)
$003F_{16}$	Interrupt control register 2 (ICON2)

$0FF0_{16}$	LPC0 address register L (LPC0ADL)
$0FF1_{16}$	LPC0 address register H (LPC0ADH)
$0FF2_{16}$	LPC1 address register L (LPC1ADL)
$0FF3_{16}$	LPC1 address register H (LPC1ADH)

$0FF8_{16}$	Port P5 input register (P5I)
$0FF9_{16}$	Port control register 3 (PCTL3)

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

All I/O pins are programmable as input or output. All I/O ports have direction registers which specify the data direction of each pin like input/output. One bit in a direction register corresponds to one pin. Each pin can be set to be input or output port.

Writing "0" to the bit corresponding to the pin, that pin becomes an input mode. Writing "1" to the bit, that pin becomes an output mode.

When the data is read from the bit of the port register corresponding to the pin which is set to output, the value shows the port latch data, not the input level of the pin. When a pin set to input, the pin comes floating. In input port mode, writing the port register changes only the data of the port latch and the pin remains high impedance state.

When the P8 function selection bit of the port control register 2 is set to "1", reading from address 0010_{16} reads the port P4 register, and reading from address 0011_{16} reads the port P7 register.

Especially, the input level of $P4_2$ to $P4_6$ pins and $P7_0$ to $P7_5$ pins can be read regardless of the data of the direction registers in this case.

Table 6 I/O port function (1)

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
$P0_0$-$P0_7$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output or N-channel open-drain output		Port control register 1	(1)
$P1_0$-$P1_7$	Port P1					
$P2_0$-$P2_7$	Port P2		CMOS compatible input level CMOS 3-state output			(2)
$P3_0$-$P3_7$	Port P3			Key-on wake up input	Port control register 1	(3)
$P4_0$ $P4_1$	Port P4					(4)
$P4_2$/INT_0 $P4_3$/INT_1			CMOS compatible input level CMOS 3-state output or N-channel open-drain output	External interrupt input	Interrupt edge selection register Port control register 2	(5)
$P4_4$ $P4_5$ $P4_6$					Port control register 2	(6)
$P4_7$/$\overline{CLKRUN}$				Serialized IRQ function output	Serialized IRQ control register	(7)

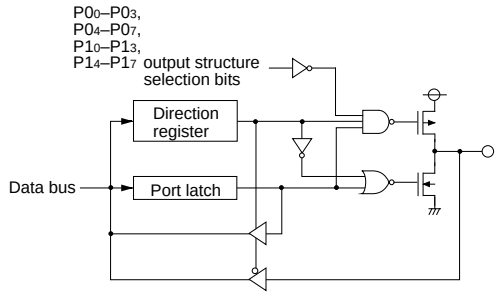
Table 7 I/O port function (2)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
P5$_0$/INT$_5$ P5$_1$/INT$_{20}$ P5$_2$/INT$_{30}$ P5$_3$/INT$_{40}$	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output or N-channel opendrain output	External interrupt input	Interrupt edge selection register Port control register 2 Port control register 3	(8)
P5$_4$/CNTR$_0$ P5$_5$/CNTR$_1$			CMOS compatible input level CMOS 3-state output	Timer X, timer Y function I/O	Timer XY mode register	(9)
P5$_6$ P5$_7$						(10)
P6$_0$– P6$_7$	Port P6					(10)
P7$_0$ P7$_1$ P7$_2$	Port P7		CMOS compatible input level or TTL input level Pure N-channel open-drain output		Port control register 2	(11)
P7$_3$/INT$_{21}$ P7$_4$/INT$_{31}$ P7$_5$/INT$_{41}$				External interrupt input	Interrupt edge selection register Port control register 2	(12)
P7$_6$ P7$_7$			CMOS compatible input level Pure N-channel open-drain output			(13)
P8$_0$/LAD$_0$ P8$_1$/LAD$_1$ P8$_2$/LAD$_2$ P8$_3$/LAD$_3$	Port P8		CMOS compatible input level CMOS 3-state output	LPC interface function I/O	Data bus buffer control register Port control register 2	(14)
P8$_4$/$\overline{\text{LFRAME}}$ P8$_5$/$\overline{\text{LRESET}}$ P8$_6$/LCLK						(15)
P8$_7$/ SERIRQ				Serialized IRQ function I/O		(16)

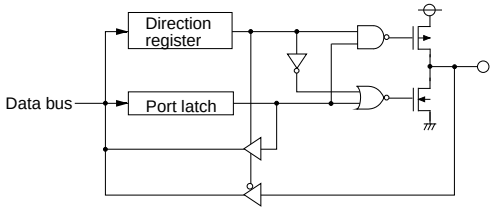
Notes1: For details usage of double-function ports as function I/O ports, refer to the applicable sections.

2: Make sure that the input level of each pin should be either 0 V or V_{CC} in STP mode.
When an input level is at an intermediate voltage level, the I_{CC} current will become large because of the input buffer gate.

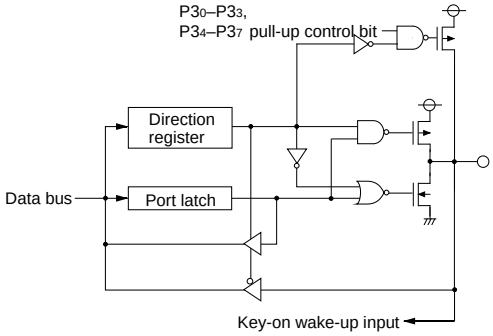
(1) Ports P0, P1



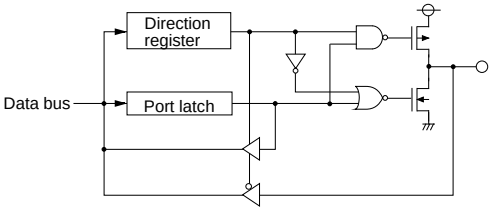
(2) Port P20–P27



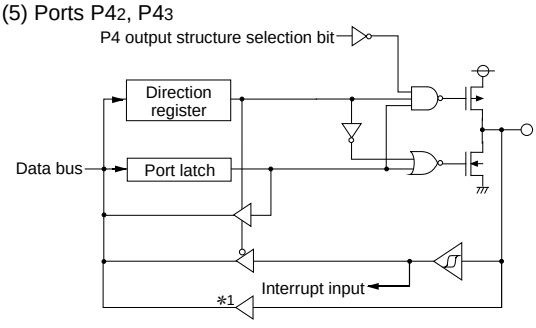
(3) Ports P30–P37



(4) Port P40, P41



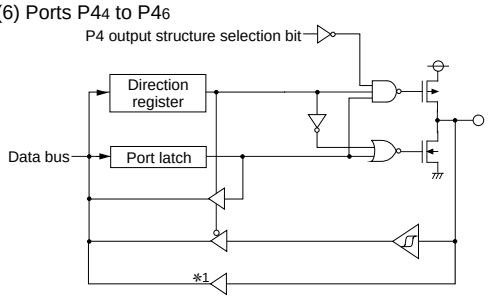
(5) Ports P42, P43



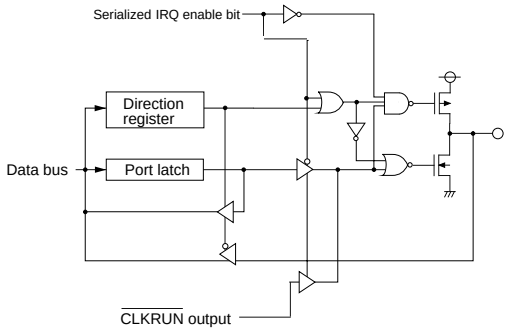
*1. Reading the port P8 register (address 001016) is switched to port P4 pin input level by the P8 function selection bit of the port control register 2 (PCTL2).

Fig. 10 Port block diagram (1)

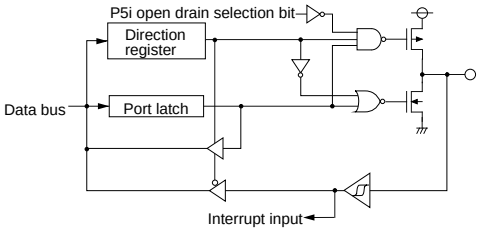
(6) Ports P44 to P46



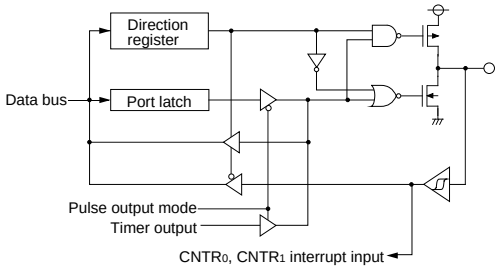
(7) Port P47



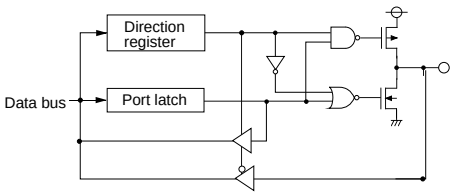
(8) Ports P50 to P53



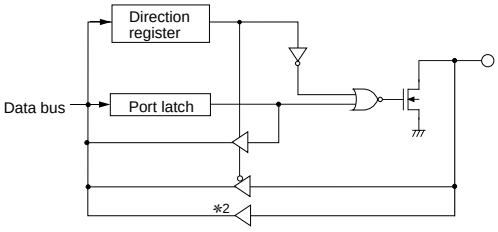
(9) Ports P54, P55



(10) Ports P56, P57, P6



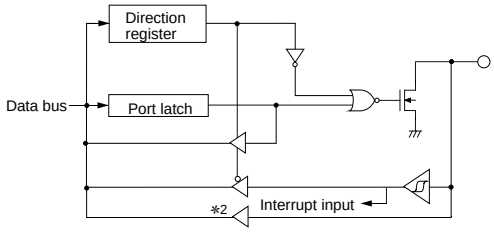
(11) Ports P70 to P72



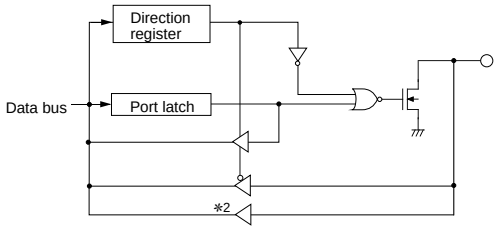
*1. Reading the port P8 register (address 001016) is switched to port P4 pin input level by the P8 function selection bit of the port control register 2 (PCTL2).
*2. Reading the port P8 direction register is switched to port P7 pin input level by the P8 function selection bit of the port control register 2 (PCTL2).

Fig. 11 Port block diagram (2)

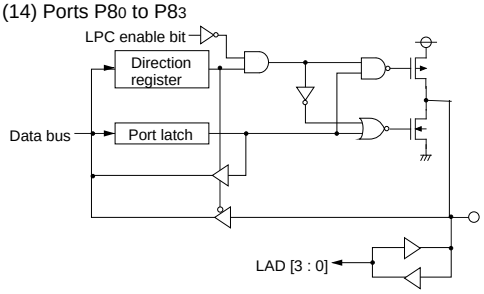
(12) Ports P7$_3$ to P7$_5$



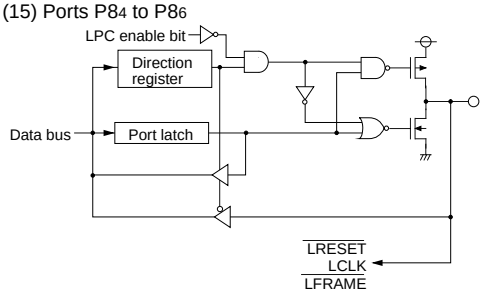
(13) Port P7$_6$, P7$_7$



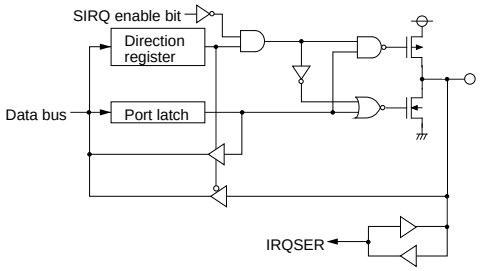
(14) Ports P8$_0$ to P8$_3$



(15) Ports P8$_4$ to P8$_6$



(16) Port P8$_7$



∗2. The input level can be switched between CMOS compatible input level and TTL level by the P7 input level selection bit of the port control register 2 (PCTL2).
Reading the port P8 direction register is switched to port P7 pin input level by the P8 function selection bit of the port control register 2 (PCTL2).

Fig. 12 Port block diagram (3)

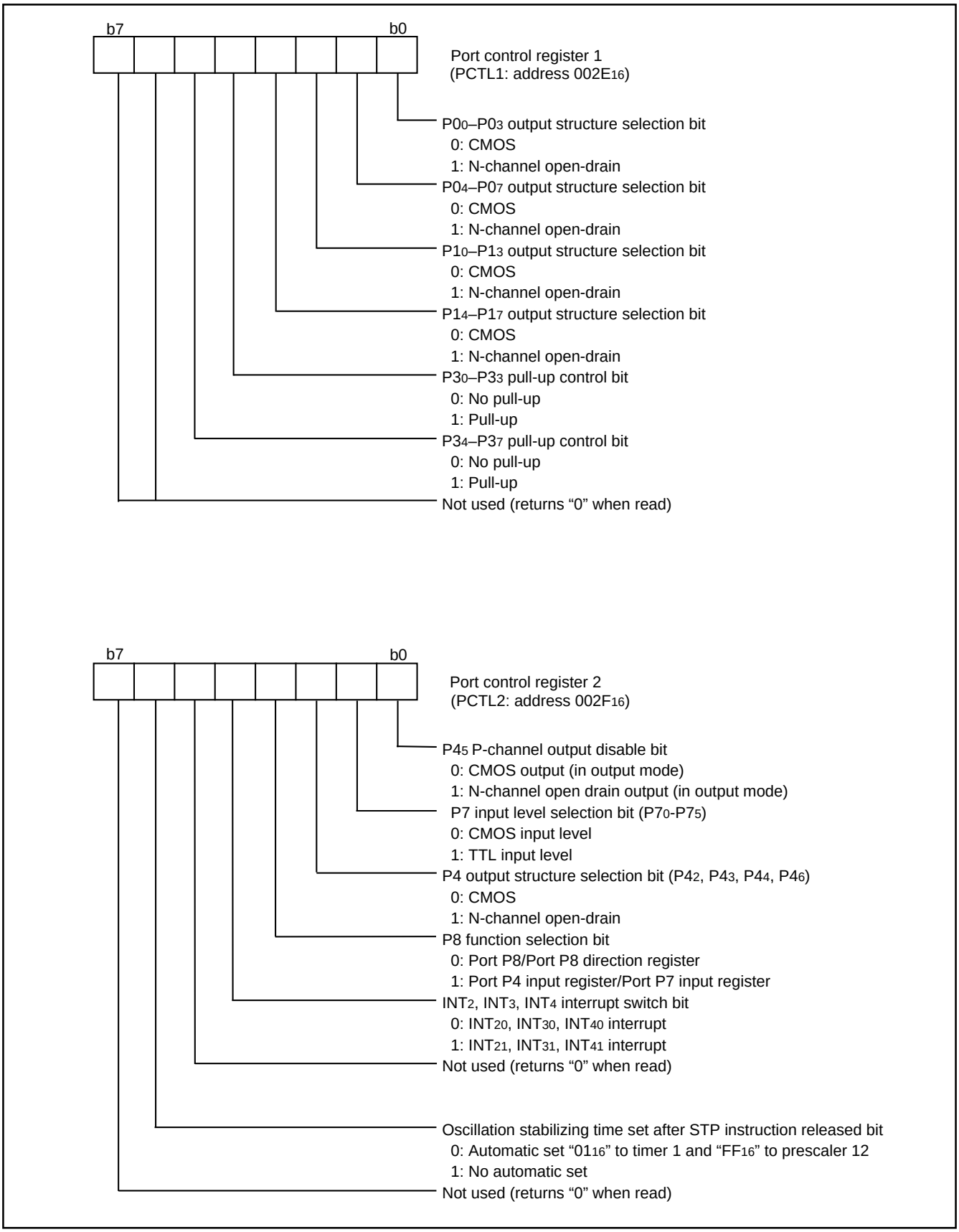


Fig. 13 Structure of port I/O related registers (1)

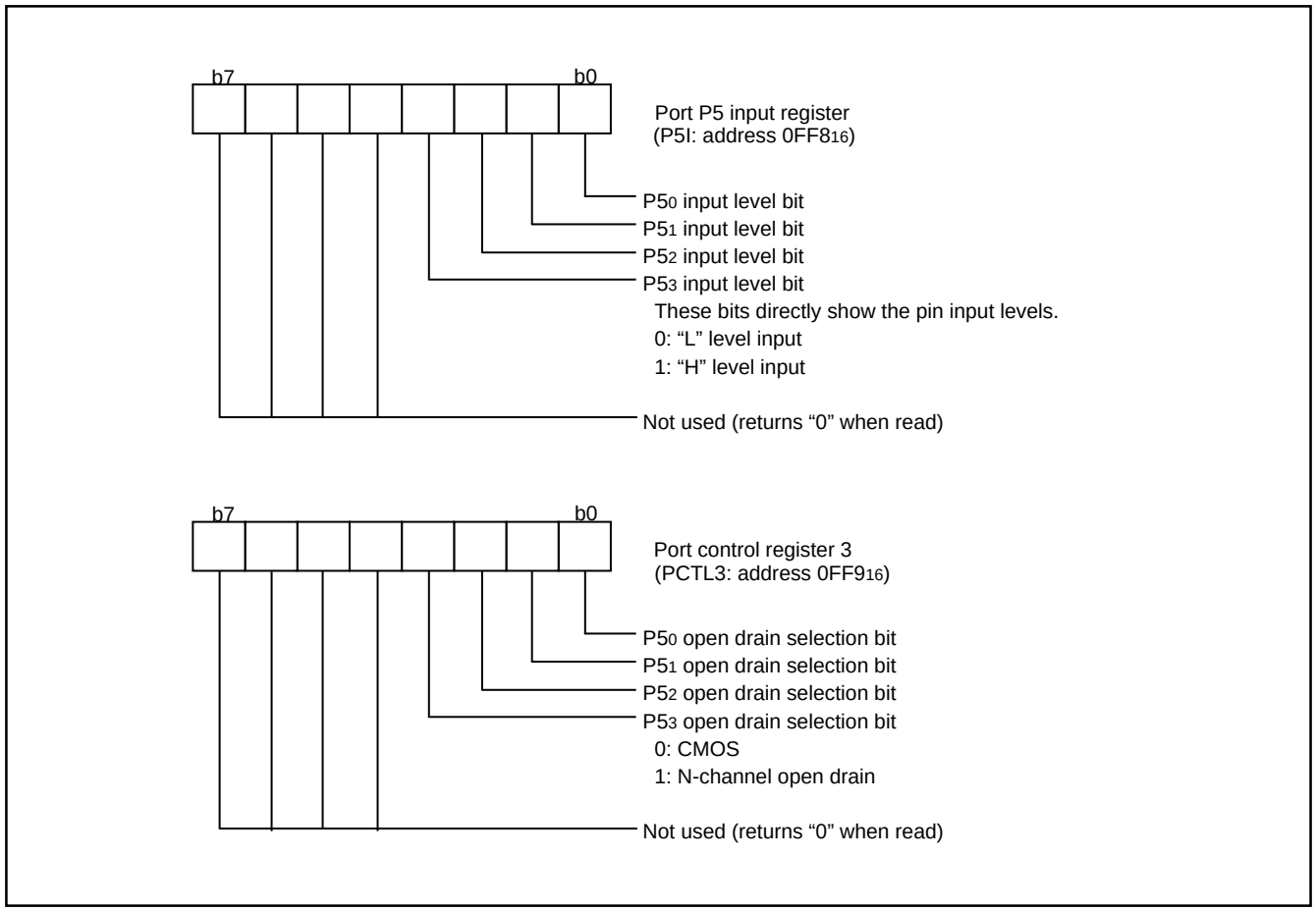


Fig. 14 Structure of port I/O related registers (2)

INTERRUPTS

Interrupts occur by 14 sources among 17 sources: ten external, six internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt caused by the BRK instruction. An interrupt occurs when both the corresponding interrupt request bit and interrupt enable bit are “1” and the interrupt disable flag is “0”.

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The BRK instruction interrupt cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.

When several interrupts occur at the same time, the interrupts are serviced according to the priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table and stored into the program counter.

Interrupt Source Selection

Any of the following interrupt sources can be selected by the interrupt source selection register (INTSEL).

1. INT_0 or Input buffer full
2. INT_1 or Output buffer empty
3. Timer 2 or INT_5
4. $CNTR_0$ or INT_0
5. $CNTR_1$ or INT_1

External Interrupt Pin Selection

The external interrupt sources of INT_2, INT_3, and INT_4 can be selected from either input pin from INT_{20}, INT_{30}, INT_{40} or input pin from INT_{21}, INT_{31}, INT_{41} by the INT_2, INT_3, INT_4 interrupt switch bit (bit 4 of PCTL2).

■ Notes

When setting the followings, the interrupt request bit may be set to “1”.

•When setting external interrupt active edge

Related register: Interrupt edge selection register (address $003A_{16}$); Timer XY mode register (address 0023_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Related register: Interrupt source selection register (address 0039_{16})

•When setting input pin of external interrupts INT_2, INT_3 and INT_4

Related register: INT_2, INT_3, INT_4 interrupt switch bit of Port control register 2 (bit 4 of address $002F_{16}$)

When not requiring the interrupt occurrence synchronized with these setting, take the following sequence.

(1) Set the corresponding interrupt enable bit to “0” (disabled).

(2) Set the active edge selection bit or the interrupt source selection bit to “1”.

(3) Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.

(4) Set the corresponding interrupt enable bit to “1” (enabled).

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
Input buffer full (IBF)				At input data bus buffer writing	
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Output buffer empty (OBE)				At output data bus buffer reading	
$\overline{\text{LRESET}}$	4	FFF716	FFF616	At falling edge of $\overline{\text{LRESET}}$ input	External interrupt
Timer X	5	FFF316	FFF216	At timer X underflow	
Timer Y	6	FFF116	FFF016	At timer Y underflow	
Timer 1	7	FFEF16	FFEE16	At timer 1 underflow	STP release timer underflow
Timer 2	8	FFED16	FFEC16	At timer 2 underflow	
INT5				At detection of either rising or falling edge of INT5 input	External interrupt (active edge selectable)
CNTR0	9	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
INT0				At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
CNTR1	10	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
INT1				At detection of either rising or falling edge of INT1 input	External interrupt (falling valid)
INT2	11	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
INT3	12	FFE316	FFE216	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
INT4	13	FFE116	FFE016	At detection of either rising or falling edge of INT4 input	External interrupt (active edge selectable)
Key-on wake-up	14	FFDF16	FFDE16	At falling of port P3 (at input) input logical level AND	External interrupt (falling valid)
BRK instruction	15	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset functions in the same way as an interrupt with the highest priority.

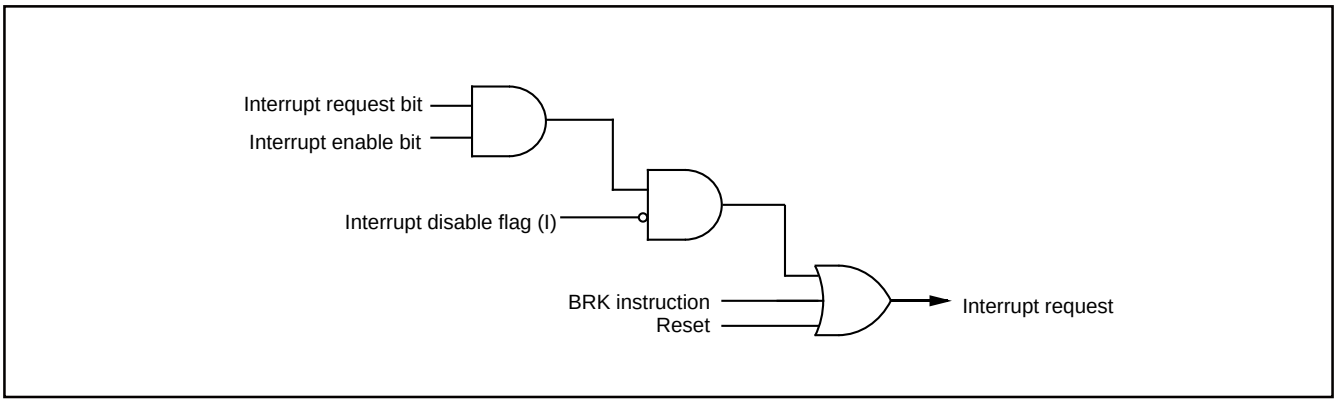


Fig. 15 Interrupt control

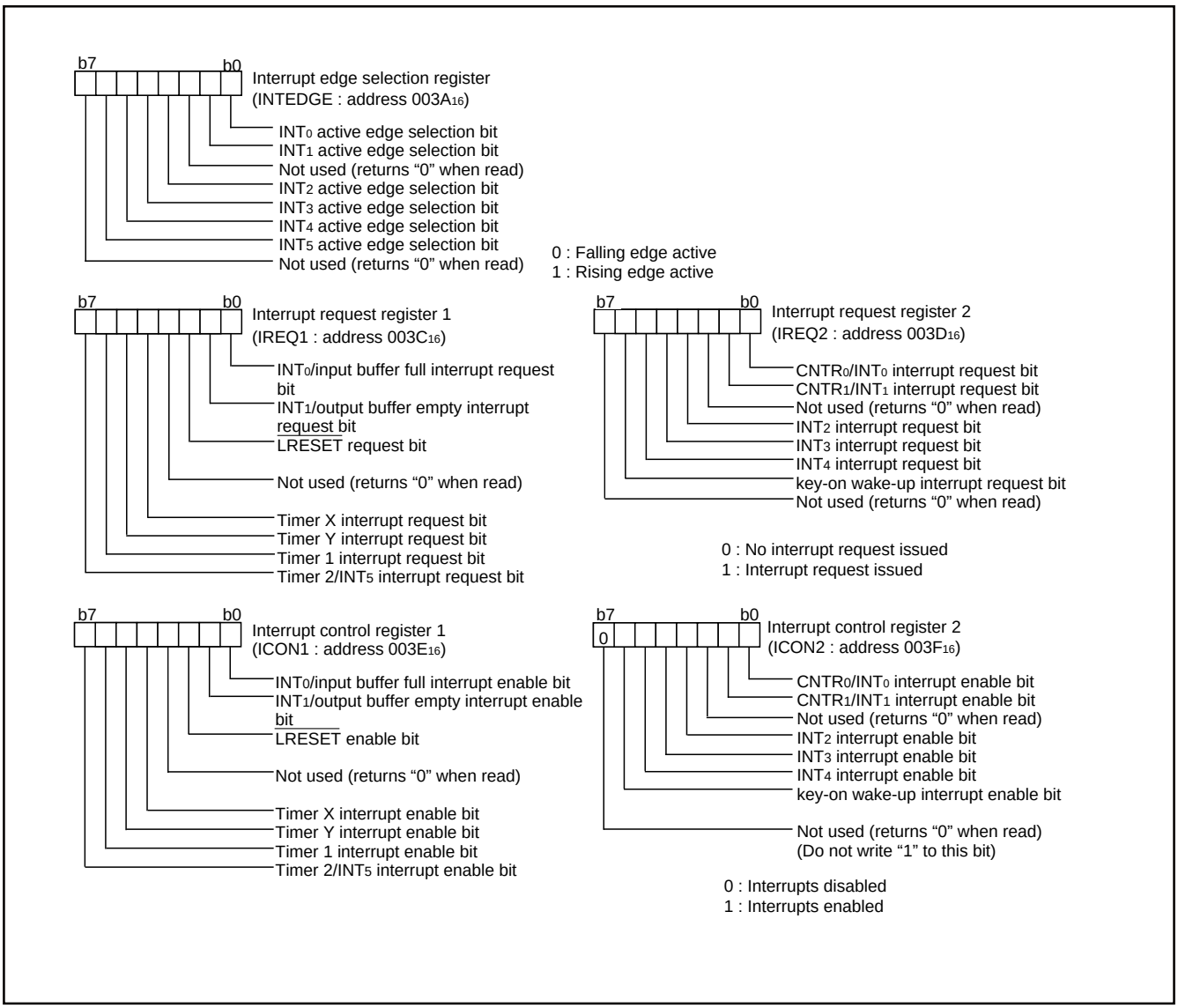


Fig. 16 Structure of interrupt-related registers (1)

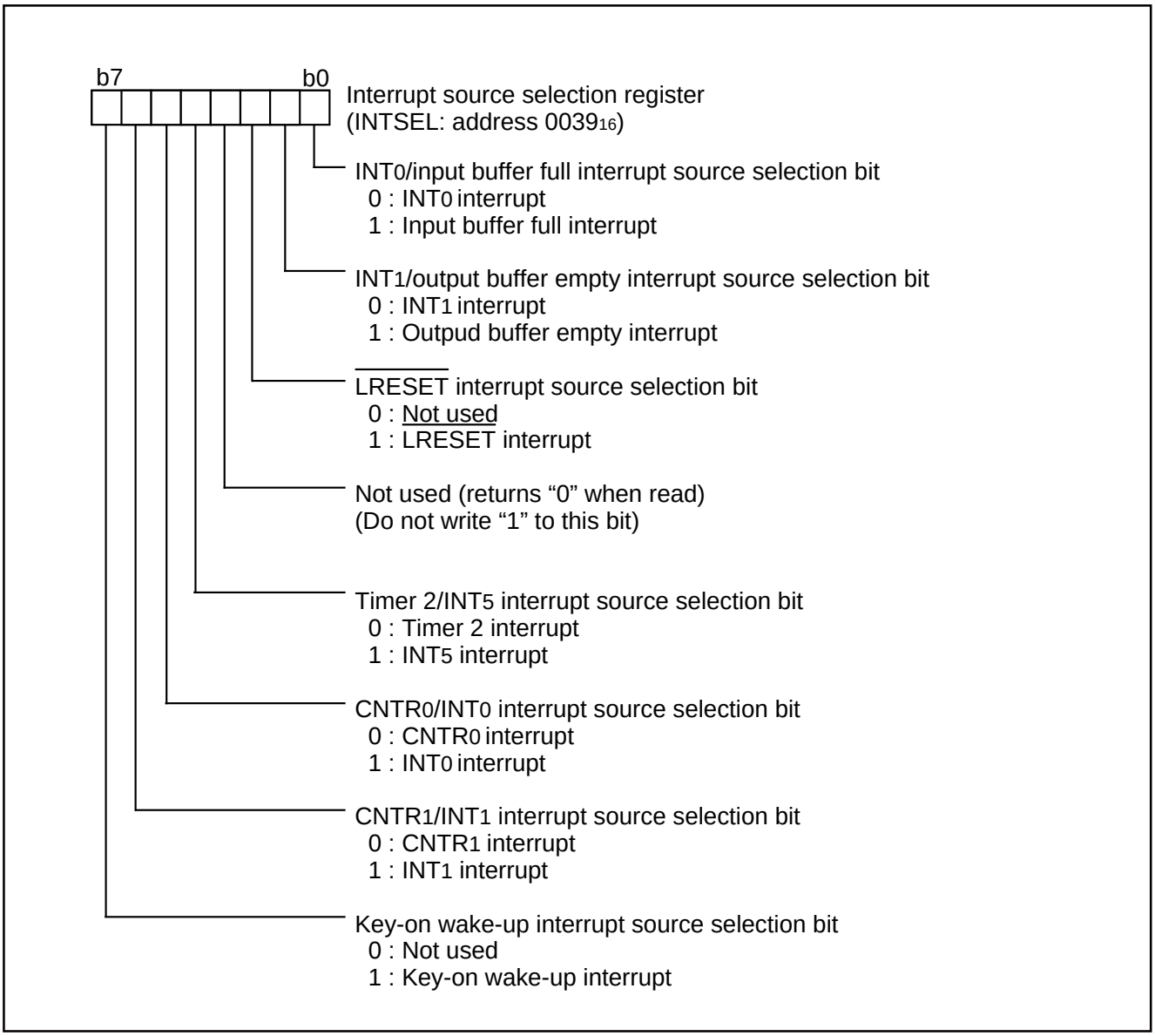


Fig. 17 Structure of interrupt-related registers (2)

Key Input Interrupt (Key-on Wake Up)

A Key input interrupt request is generated by applying “L” level to any pin of port P3 that have been set to input mode. In other words, it is generated when the logical AND of all port P3 input goes from “1” to “0”. An example of using a key input interrupt is shown in Figure 18, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports P3$_0$–P3$_3$.

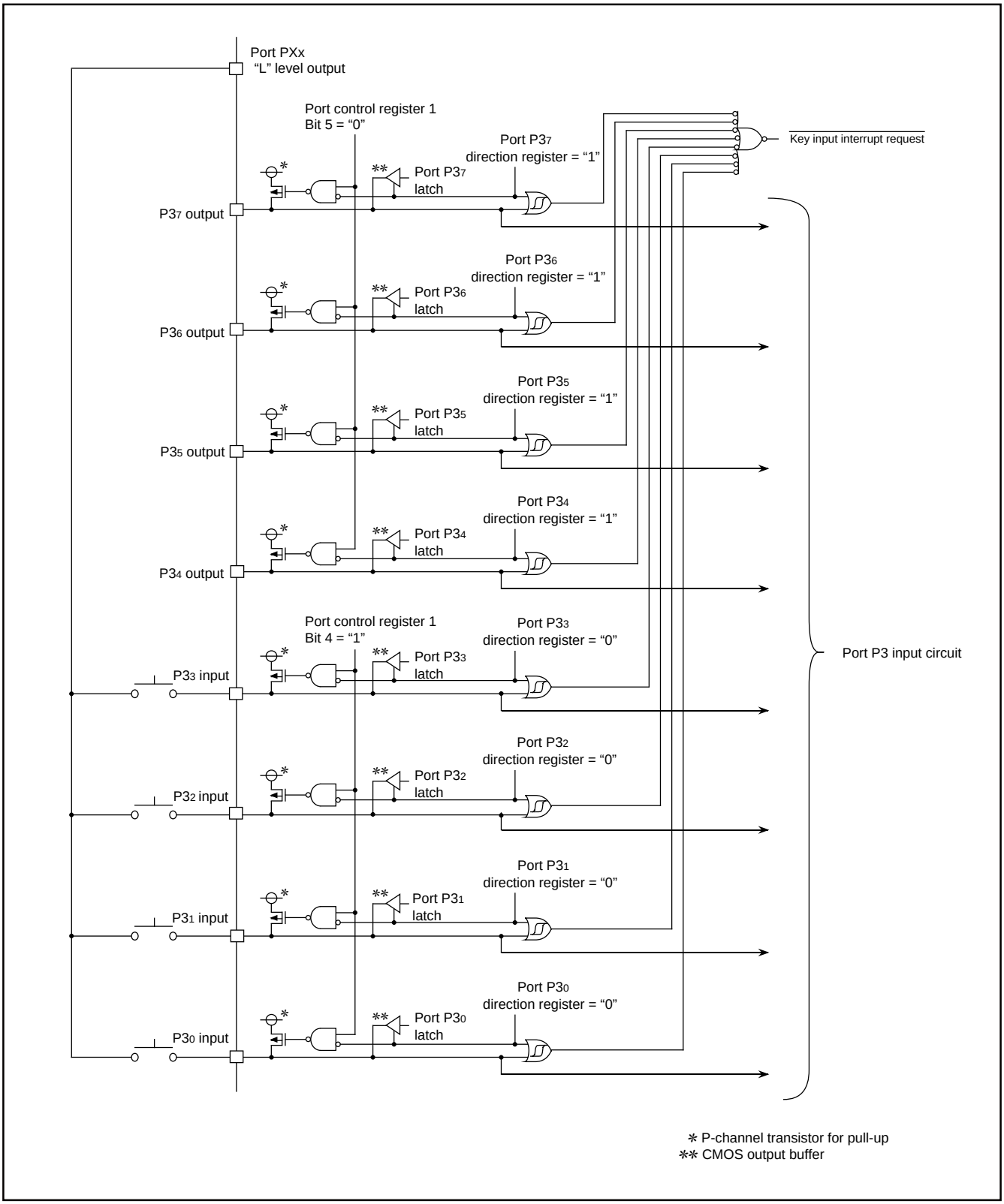


Fig. 18 Connection example when using key input interrupt and port P3 block diagram

TIMERS

The 3882 group has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are count down structure. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

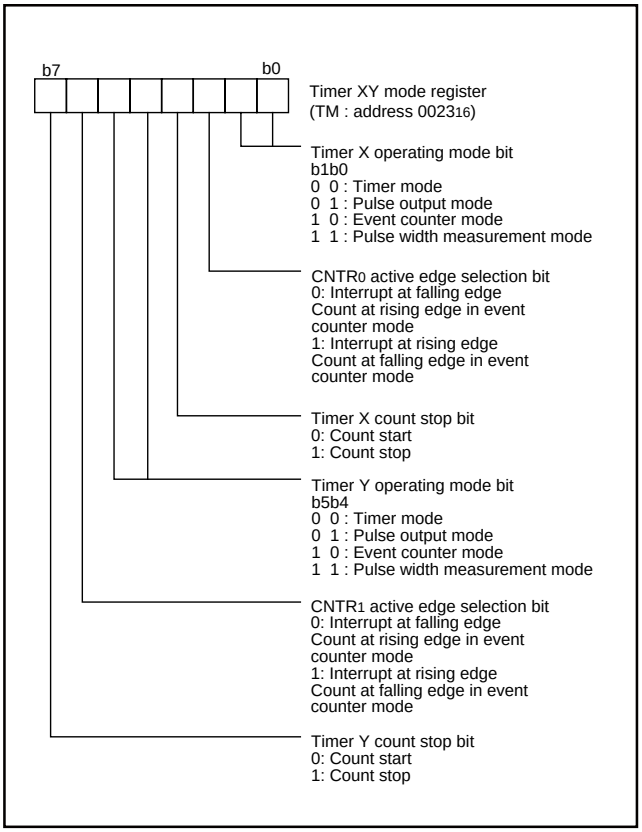


Fig. 19 Structure of timer XY mode register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency divided by 16. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts f(X_{IN})/16.

(2) Pulse Output Mode

Timer X (or timer Y) counts f(X_{IN})/16. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P5_4$ (or port $P5_5$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the rising edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the falling edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts f(X_{IN})/16 while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the timer counts while the $CNTR_0$ (or $CNTR_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer overflows.

The count source for timer Y in the timer mode or the pulse output mode can be selected from f(X_{IN})/16 by the timer Y count source selection bit of the port control register 2 (bit 5 of PCTL2).

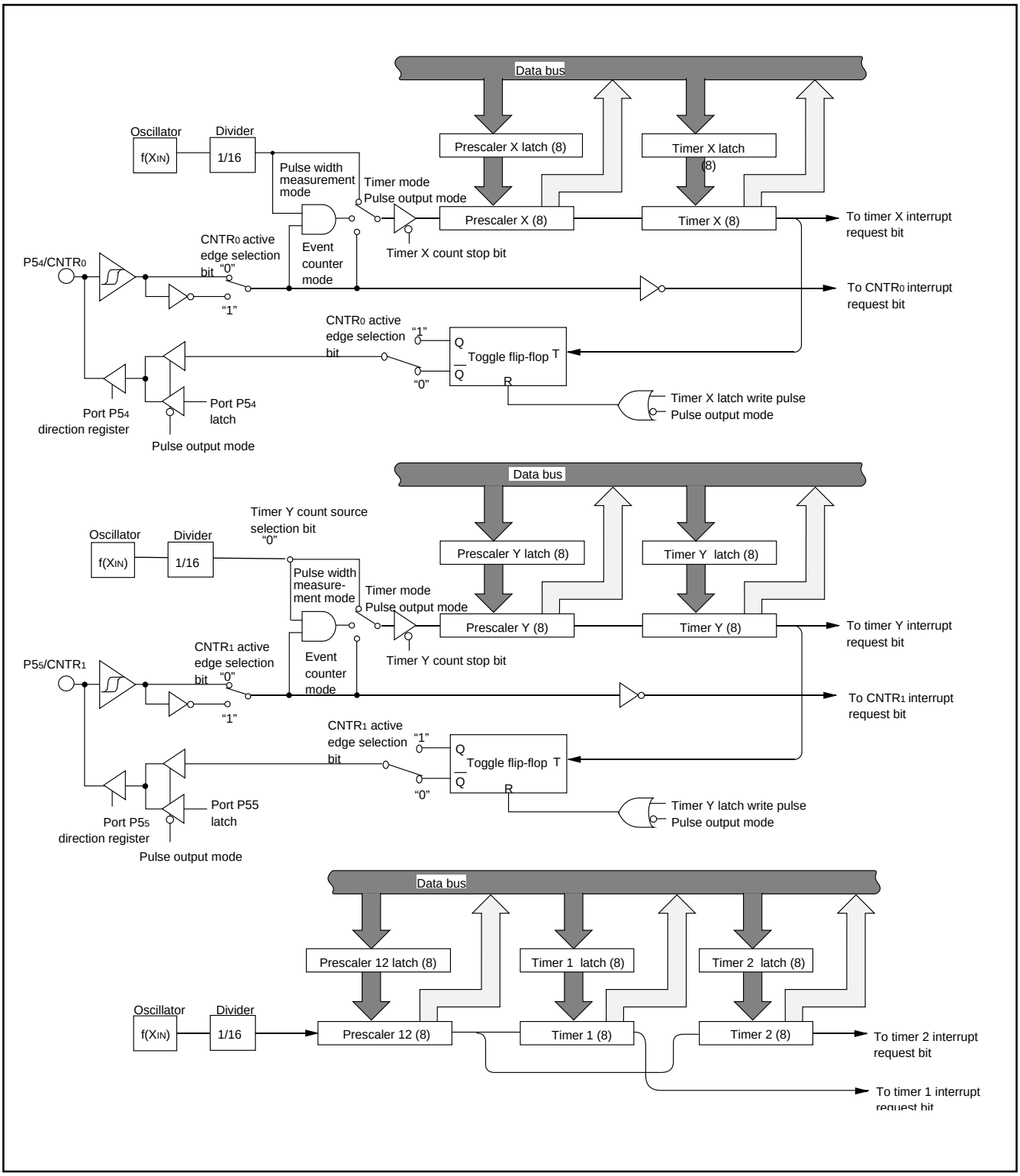


Fig. 20 Block diagram of timer X, timer Y, timer 1, and timer 2

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Initial Value of Watchdog Timer

At reset or writing to the watchdog timer control register (address 001E16), each of watchdog timer H and L is set to "FF16". Any instruction which generates a write signal such as the instructions of STA, LDM, CLB and others can be used to write. The data of bits 6 and 7 are only valid when writing to the watchdog timer control register. Each of watchdog timer is set to "FF16" regardless of the written data of bits 0 to 5.

Operation of Watchdog Timer

The watchdog timer stops at reset and starts to count down by writing to the watchdog timer control register. An internal reset occurs at an underflow of the watchdog timer H. The reset is released after waiting for a reset release time and the program is processed from the reset vector address. Accordingly, programming is usually performed so that writing to the watchdog timer control register may be started before an underflow of the watchdog timer H. If writing to the watchdog timer control register is not performed once, the watchdog timer does not function.

Bit 6 of Watchdog Timer Control Register

When bit 6 of the watchdog timer control register is "0", the MCU enters the stop mode by execution of STP instruction. Just after releasing the stop mode, the watchdog timer restarts counting (Note). When executing the WIT instruction, the watchdog timer does not stop.

When bit 6 is "1", execution of STP instruction causes an internal reset. When this bit is set to "1" once, it cannot be rewritten to "0" by program. Bit 6 is "0" at reset.

The necessary time after writing to the watchdog timer control register to an underflow of the watchdog timer H is shown as follows.

When bit 7 of the watchdog timer control register is "0":

131.072 ms at XIN = 8 MHz frequency.

When bit 7 of the watchdog timer control register is "1":

512 µs at XIN = 8 MHz frequency.

Note: The watchdog timer continues to count for waiting for a stop mode release time. Do not generate an underflow of the watchdog timer H during that time.

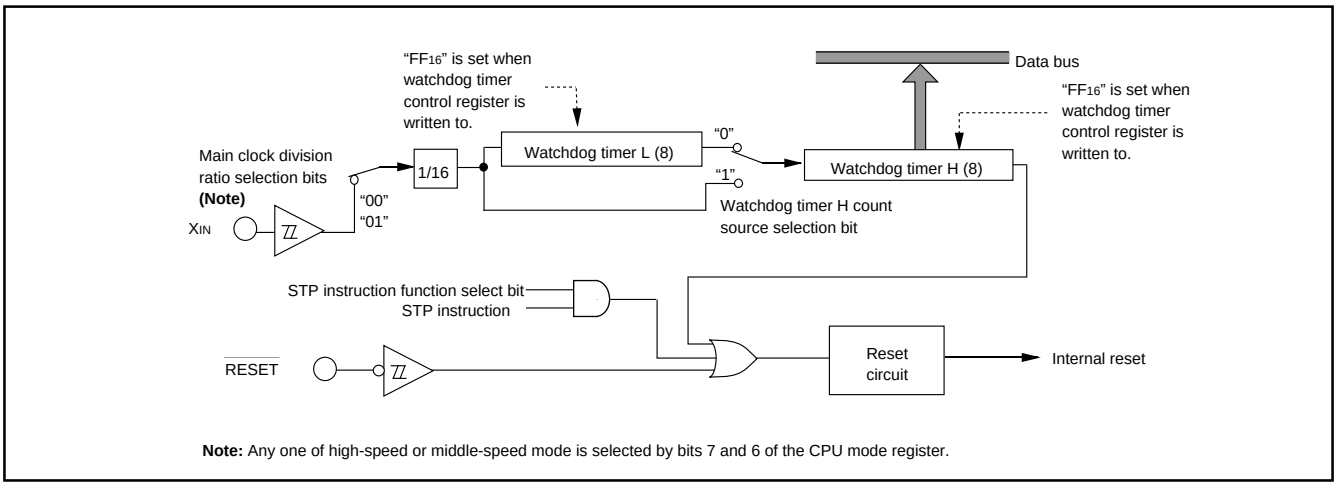


Fig. 21 Block diagram of Watchdog timer

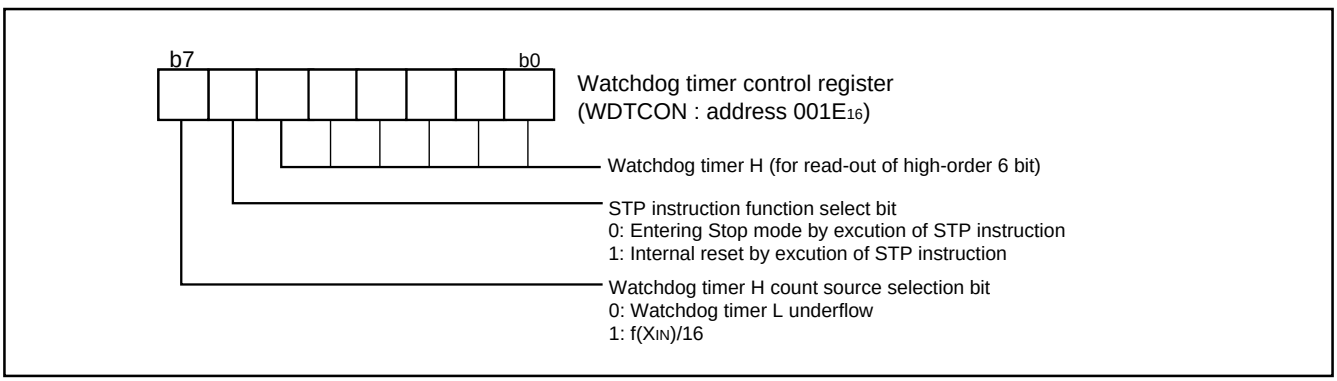


Fig. 22 Structure of Watchdog timer control register

LPC INTERFACE

LPC interface function is base on Low Pin Count (LPC) Interface Specification, Revision 1.0. The 3882 supports only I/O read cycle and
I/O write cycle. There are two channels of bus buffers to the host.
The functions of Input Data Bus Buffer, Output Data Bus Buffer and Data Bus Buffer Status Register are the same as that of the 8042, 3880 group, 3881 group,3886 group and 3885 group. It can be written in or read out from the host controller through LPC interface. LPC interface function block diagram is shown in Figure 23.
Functional input or output pins of LPC interface are shared with Port 8 ($P8_0$–$P8_6$). Setting the LPC interface enable bit (bit3 of LPCCON) to "1" enables LPC interface. Enabling channel i (i = 0, 1) of the data bus buffer is controlled by the data bus buffer i (i = 0, 1) enable bits (bit 4 or bit 5 of LPCCON).
The slave addresses of the data bus buffer channel i (i = 0, 1) are definable by setting LPCi (i = 0, 1) address register H/L (LPC0ADL, LPC0ADH, LPC1ADL, LPC1ADH). The bit 2 value of LPCi address register L is not decoded. This bit returns "0" when the internal CPU read. The bit 2 of slave address is latched to XA2i flag when the host controller writes the data.
The input buffer full (IBF) interrupt occurs when the host controller writes the data. The output buffer empty (OBE) interrupt is generated when the host controller reads out the data. The 3882 merges two input buffer full (IBF) interrupt requests and two output buffer empty (OBE) interrupt requests as shown in Figure 24.

Table 9 Function explanation of the control pin in LPC interface

Pin name	Input/ Output	Function
$P8_0$/LAD_0	I/O	These pins communicate address, control and data information between the host and the data bus buffer of the 3882.
$P8_1$/LAD_1	I/O	
$P8_2$/LAD_2	I/O	
$P8_3$/LAD_3	I/O	
$P8_4$/$\overline{LFRAME}$	I	Input the signal to indicate the start of new cycle and termination of abnormal communication cycles.
$P8_5$/$\overline{LRESET}$	I	Input the signal to reset the LPC interface function.
$P8_6$/LCLK	I	Input the LPC synchronous clock signal.

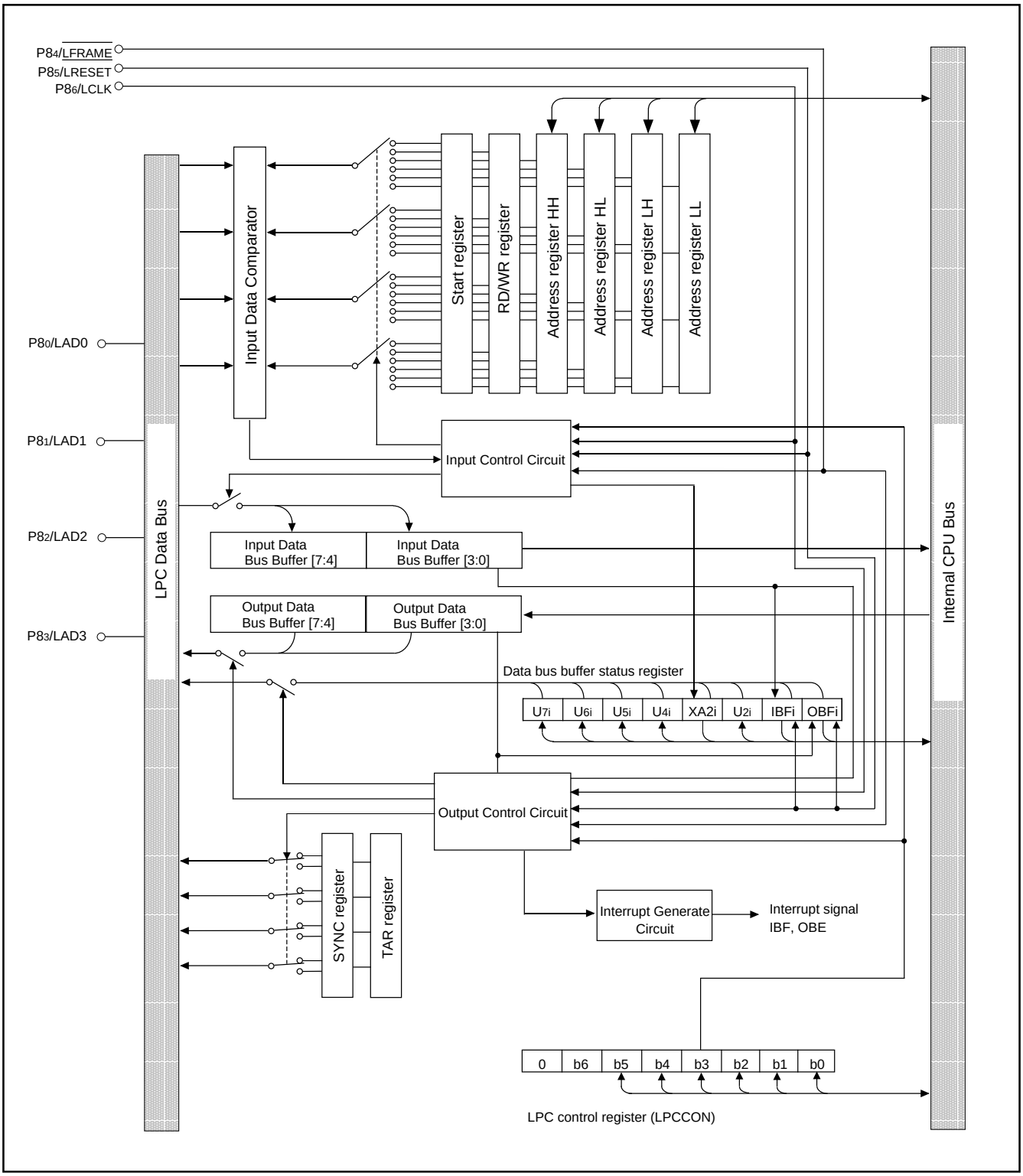


Fig. 23 Block diagram of LPC interface function (1ch)

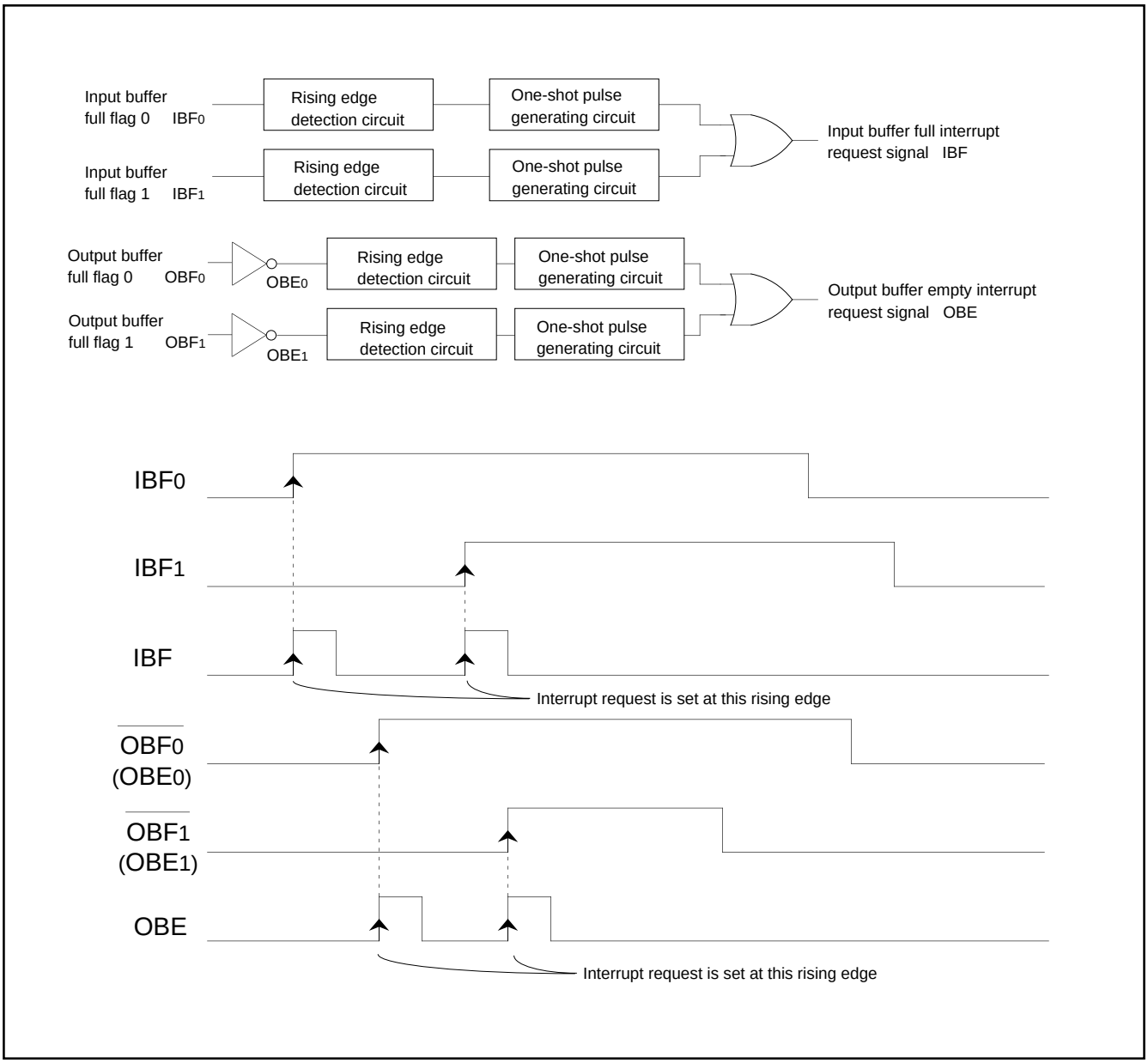


Fig. 24 Interrupt request circuit of data bus buffer

[LPC Control Register (LPCCON)] 002A16

• SYNC output select bit (SYNCSEL)
  "00": OK
  "01": LONG & OK
  "10": Err
  "11": LONG & Err
• LPC interface software reset bit (LPCSR)
  "0": Reset release (automatic)
  "1": Reset
• LPC interface enable bit (LPCBEN)
  "0": P80–P86 works as port
  "1": P80–P86 works as LPC interface
• Data bus buffer 0 enable bit (DBBEN0)
  "0": Data bus buffer 0 disable
  "1": Data bus buffer 0 enable
• Data bus buffer 1 enable bit (DBBEN1)
  "0": Data bus buffer 1 disable
  "1": Data bus buffer 1 enable

Bits 0 and 1 of the LPC control register (LPCCON) specify the SYNC code output.
Bit 2 of the LPC control register (LPCCON) enables the LPC interface to enter the reset state by software. When LPCSR is set to "1", LPC interface is initialized in the same manner as the external "L" input to $\overline{\text{LRESET}}$ pin (See Figure 30). Writing "0" to LPCSR the reset state will be released after 1.5 cycle of ϕ and this bit is cleared to "0".

[Data Bus Buffer Status Register i (i = 0, 1) (DBBSTS0, DBBSTS1)] 002916, 002C16

Bits 0, 1 and 3 are read-only bits and indicate the status of the data bus buffer. Bits 2, 4, 5, 6 and 7 are user definable flags which can be read and written by software. The data bus buffer status register can be read out by the host controller when bit 2 of the slave address (A2) is "1".

•Bit 0: Output buffer full flag i (OBFi)

This bit is set to "1" when a data is written into the output data bus buffer i and cleared to "0" when the host controller reads out the data from the output data bus buffer i.

•Bit 1: Input buffer full flag i (IBFi)

This bit is set to "1" when a data is written into the input data bus buffer i by the host controller, and cleared to "0" when the data is read out from the input data bus buffer i by the internal CPU.

•Bit 3: XA2 flag (XA2i)

The bit 2 of slave address is latched while a data is written into the input data bus buffer i.

[Input Data Bus Buffer i(i=0,1) (DBBIN0, DBBIN1)] 002816, 002B16

In I/O write cycle from the host controller, the data byte of the data phase is latched to DBBINi (i=0,1). The data of DBBINi can be read out form the data bus buffer registers (DBB0, DBB1) address in SFR area.

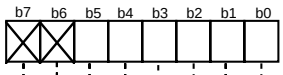
[Output Data Bus Buffer i (i = 0, 1) (DBBOUT0, DBBOUT1)] 002816, 002B16

Writing data to data bus buffer registers (DBB0 , DBB1) address from the internal CPU means writing to DBBOUTi (i = 0, 1). The data of DBBOUTi (i = 1, 0) is read out from the host controller when bit 2 of slave address (A2) is "0".

[LPCi address register H/L (LPC0ADL, LPC1ADL / LPC0ADH, LPC1ADH)] 0FF016 to 0FF316

The slave addresses of data bus buffer channel i(i=0,1) are definable by setting LPCi address registers H/L (LPC0ADL, LPC0ADH, LPC1ADL, LPC1ADH). These registers can be set and cleared any time. When the internal CPU reads LPCi address register L, the bit 2 (A2) is fixed to "0". The bit 2 of slave address (A2) is latched to XA2i flag when the host controller writes the data. The slave addresses, set in these registers, is used for comparing with the addresses from the host controller.

LPC control register

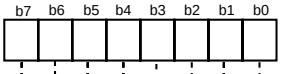


Symbol	Address	When reset
LPCCON	$002A_{16}$	00000000_2

Bit symbol	Bit name	Function	R	W
SYNCSEL	SYNC output select bit	00:OK 01:Long & OK 10:Err 11:Long & Err	○	○
LPCSR	LPC interface software reset bit	0 : Reset release(automatic) 1 : Reset	○	○
LPCEN	LPC interface enable bit	0 : $P8_0$ to P86 as port 1 : LPC interface enable	○	○
DBBEN0	Data bus buffer 0 enable bit	0 : Data bus buffer 0 disable 1 : Data bus buffer 0 enable	○	○
DBBEN1	Data bus buffer 1 enable bit	0 : Data bus buffer 1 disable 1 : Data bus buffer 1 enable	○	○
Cannot write to this bit. Returns "0"when read.				

Fig. 25 LPC control register

Data bus buffer status register i (i = 0, 1)

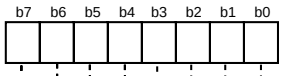


Symbol	Address	When reset
DBBSTS0	0029_{16}	00000000_2
DBBSTS1	$002C_{16}$	00000000_2

Bit symbol	Bit name	Function	R	W
OBFi	Output buffer full flag	0 : Buffer empty 1 : Buffer full	○	×
IBFi	Input buffer full flag	0 : Buffer empty 1 : Buffer full	○	×
U2i	User definable flag	This flag can be freely defined by user.	○	○
XA2i	XA2i flag	This flag indicates the A2 status when IBFi flag is set.	○	×
U4i	User definable flag	This flag can be freely defined by user.	○	○
U5i			○	○
U6i			○	○
U7i			○	○

Fig. 26 Data bus buffer control register

LPCi address register L (i=0,1) **(Note2)**

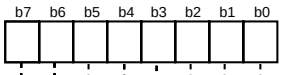


Symbol	Address	When reset
LPC0ADL	0FF0$_2$	00000000$_2$
LPC1ADL	0FF2$_2$	00000000$_2$

Bit symbol	Bit name	R	W
LPCSAD0	Slave address bit 0	○	○
LPCSAD1	Slave address bit 1	○	○
LPCSAD2	Slave address bit 2 **(Note 1)**	○	×
LPCSAD3	Slave address bit 3	○	○
LPCSAD4	Slave address bit 4	○	○
LPCSAD5	Slave address bit 5	○	○
LPCSAD6	Slave address bit 6	○	○
LPCSAD7	Slave address bit 7	○	○

Notes 1: Always returnes “0” when read , even if writing “1” to this bit.
2: Do not set the same 16-bit slave address to both channel 0 and channel 1.

LPCi address register H (i=0,1)



Symbol	Address	When reset
LPC0ADH	0FF1$_2$	00000000$_2$
LPC1ADH	0FF3$_2$	00000000$_2$

Bit symbol	Bit name	R	W
LPCSAD8	Slave address bit 8	○	○
LPCSAD9	Slave address bit 9	○	○
LPCSAD10	Slave address bit 10	○	○
LPCSAD11	Slave address bit 11	○	○
LPCSAD12	Slave address bit 12	○	○
LPCSAD13	Slave address bit 13	○	○
LPCSAD14	Slave address bit 14	○	○
LPCSAD15	Slave address bit 15	○	○

Fig. 27 LPC related registers

Basic Operation of LPC Interface

Set up steps for LPC interface is as below.

•Set the LPC interface enable bit (bit3 of LPCCON) to “1”.

•Choose which data bus buffer channel use.

•Set the data bus buffer i enable bit (i = 0, 1) (bit 4 or 5 of LPCCON) to “1”.

•Set the slave address to LPCi address register L and H (i = 0, 1) (LPC0ADL, LPC0ADH, LPC1ADL, LPC1ADH).

(1) Example of I/O write cycle

The I/O write cycle timing is shown in Figure 28. The standard transfer cycle number of I/O write cycle is 13. The communication starts from the falling edge of $\overline{\text{LFRAME}}$.

The data on LAD [3:0] is monitored at every rising edge of LCLK.

• 1st clock: The last clock when $\overline{\text{LFRAME}}$ is “Low”. The host send “0000_2” on LAD [3:0] for communication start.

• 2nd clock: $\overline{\text{LFRAME}}$ is “High”. The host send “$001X_2$” on LAD [3:0] to inform the cycle type as I/O write.

• From 3rd clock to 6th clock : In these four cycles , the host sends 16-bit slave address. The 3882 compares it with the LPCi address register H and L (i = 0, 1).

  3rd clock: The slave address bit [15:12].

  4th clock: The slave address bit [11:8].

  5th clock: The slave address bit [7:4].

  6th clock: The slave address bit [3:0].

• 7th clock and 8th clock are used for one data byte transfer. The data is written to the input data bus buffer (DBBINi, i = 0, 1)

  7th clock: The host sends the data bit [3:0].

  8th clock: The host sends the data bit [7:4].

• 9th clock and 10th clock are for turning the communication direction from the host→the peripheral to the slave→the host.

  9th clock: The host outputs “1111_2” on LAD [3:0].

  10th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

• 11th clock: The 3882 outputs “0000_2” (SYNC OK) to LAD [3:0] for acknowledgment.

• 12th clock: The 3882 outputs “1111_2” to LAD [3:0]. In this timing the address bit 2 is latched to XA2i (bit3 of DBBSTSi), IBFi (bit 1 of DBBSTSi) is set to “1” and IBF interrupt signal is generated.

• 13th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

(2) Example for I/O read cycle

The I/O read cycle timing is shown in Figure 29. The standard transfer cycle number of I/O read cycle is 13. The data on LAD [3:0] is monitored at every rising edge of LCLK. The communication starts from the falling edge of $\overline{\text{LFRAME}}$.

•1st clock: The last clock when $\overline{\text{LFRAME}}$ is “Low”. The host sends “0000_2” on LAD [3:0] for communication start.

•2nd clock: $\overline{\text{LFRAME}}$ is “High”. The host sends “$000X_2$” on LAD [3:0] to inform the cycle type as I/O read.

• From 3rd clock to 6th clock: In these four cycles , the host sends 16-bit slave address. The 3882 compares it with the LPCi address register H or L (i = 0, 1).

  3rd clock: The slave address bit [15:12].

  4th clock: The slave address bit [11:8].

  5th clock: The slave address bit [7:4].

  6th clock: The slave address bit [3:0].

• 7thclock and 8thclock are used for turning the communication direction from the host→the peripheral to the peripheral→the host.

  7th clock: The host outputs “1111_2” on LAD [3:0].

  8th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

• 9th clock: The 3882 outputs “0000_2” (SYNC OK) to LAD [3:0] for acknowledgment.

• 10th clock and 11th clock are used for one data byte transfer from the output data bus buffer i (DBBOUTi) or data bus buffer status register i (DBBSTSi).

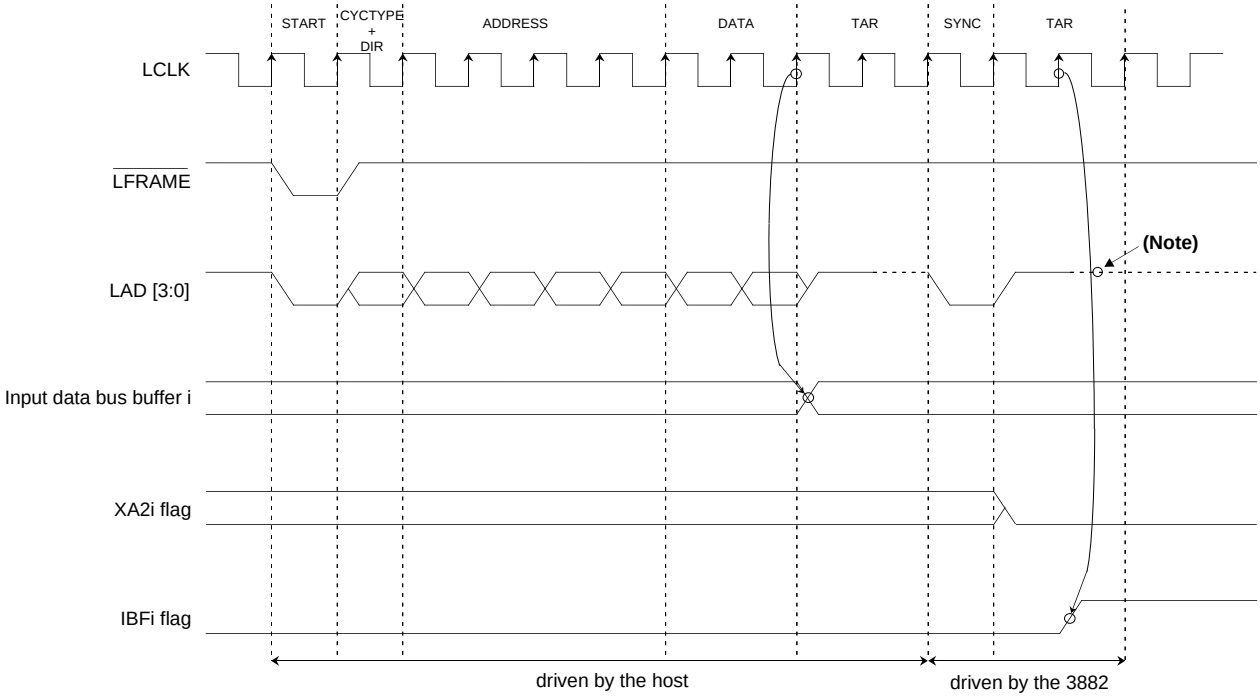
  10th clock: The 3882 sends the data bit [3:0].

  11th clock: The 3882 sends the data bit [7:4].

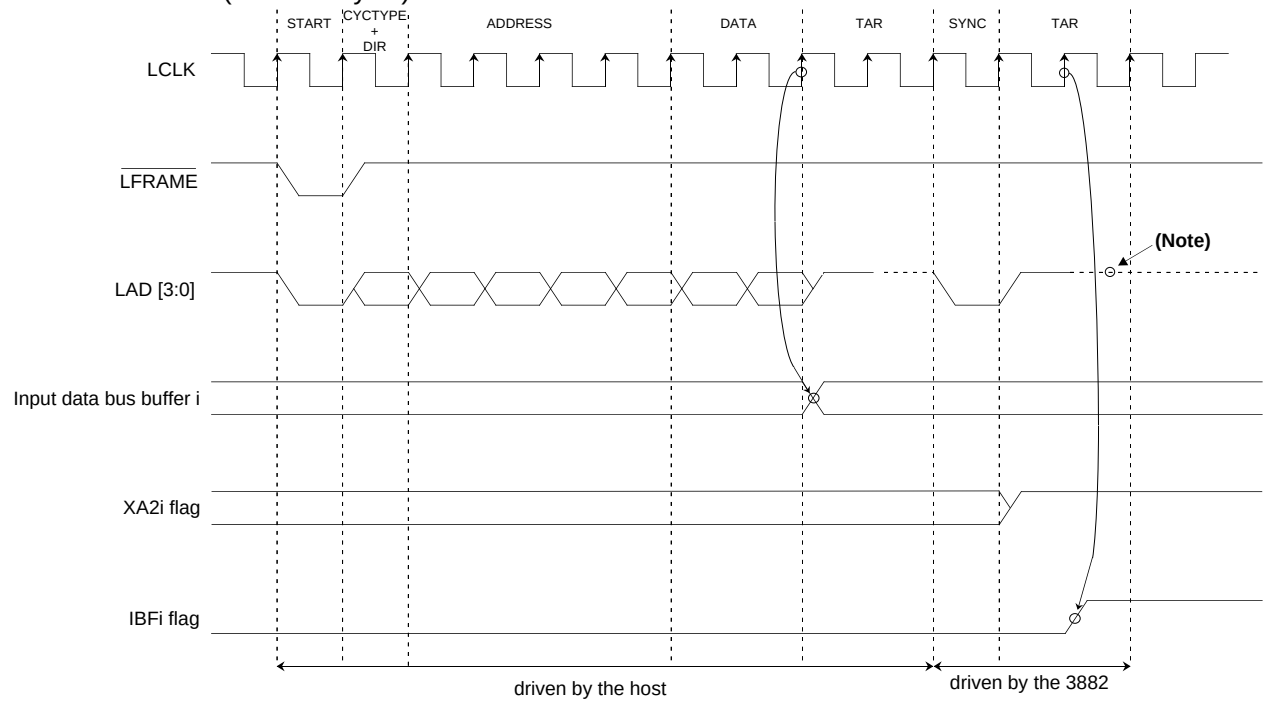
• 12th clock: The 3882 outputs “1111_2” to LAD [3:0]. In this timing OBFi (bit 2 of DBBSTSi) is cleared to “0” and OBE interrupt signal is generated.

• 13th clock: The LAD [3:0] is set to tri-state by the host to turn the communication direction.

● Data write (I/O write cycle)

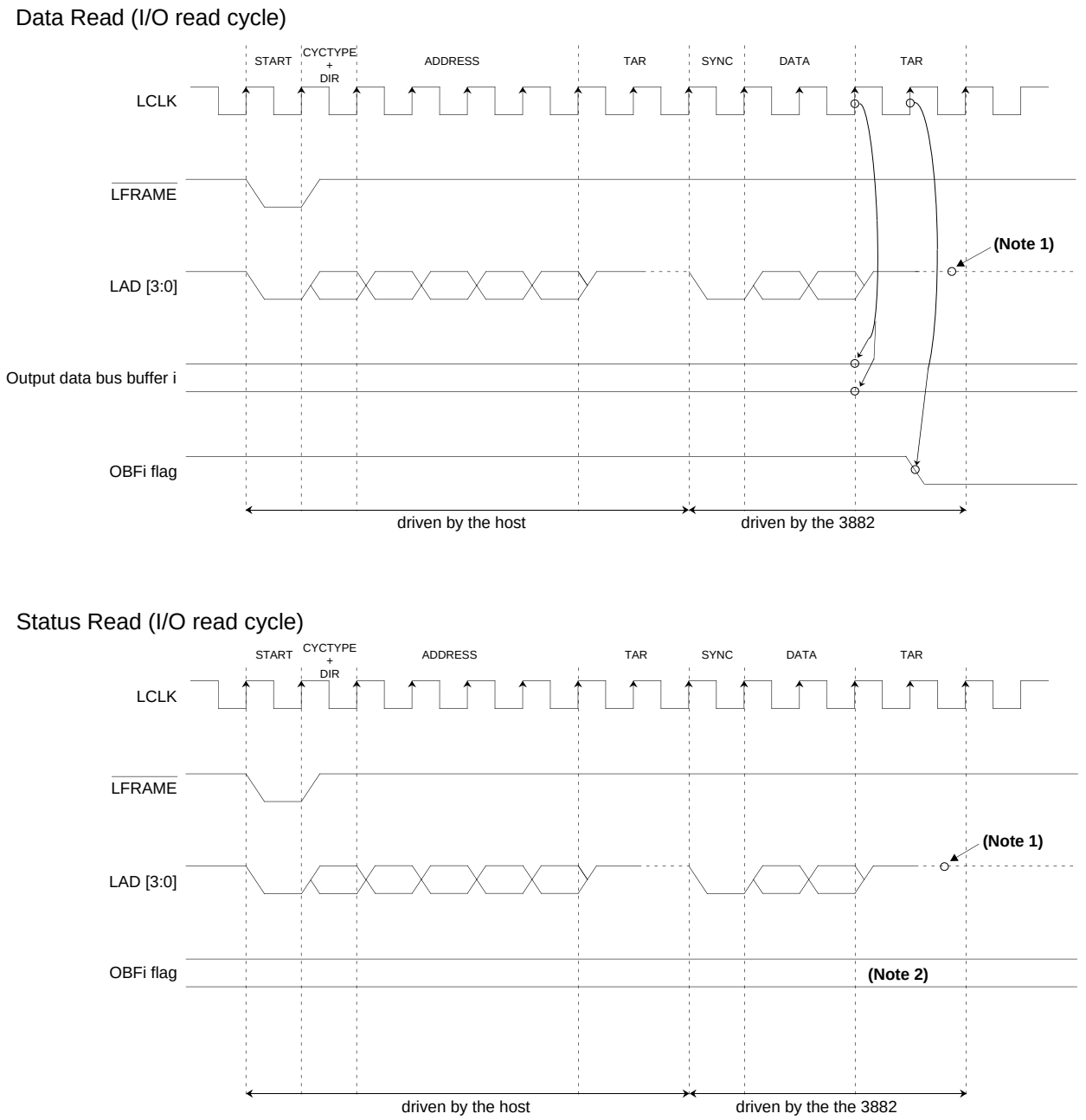


● Command write (I/O write cycle)



Note: LAD_0 to LAD_3 pins remain tri-state after transfer

Fig. 28 Data and command write timing



Notes: 1: LAD_0 to LAD_3 pins remain tri-state after transfer completion.
2: OBFi flag does not change.

Fig. 29 Data and status read timing

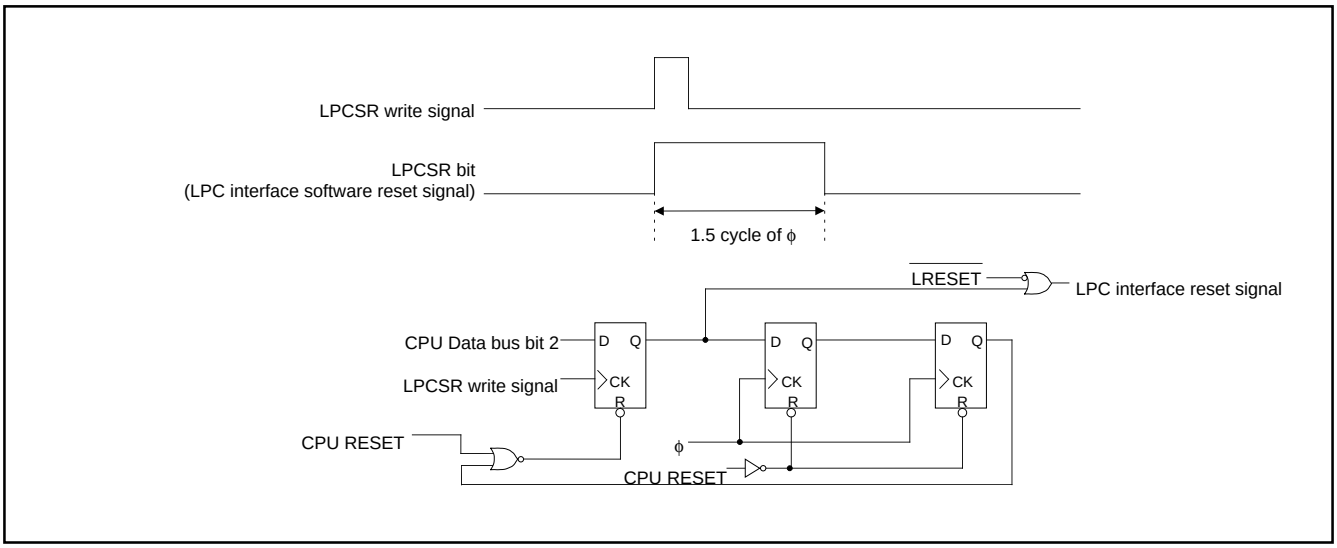


Fig. 30 Reset timing and block

Table 10 Reset conditions of LPC interface function

	Pin name / Internal register	$\overline{\text{LRESET}}$ = “L”	Note
Pin	P80/LAD0	Tri-state	
	P81/LAD1		
	P82/LAD2		
	P83/LAD3		
	P84/$\overline{\text{LFRAME}}$	Input	
	P85/$\overline{\text{LRESET}}$	LPC bus interface function	
	P86/LCLK	Input	
Internal register	Input data bus buffer registeri	Keep same value before $\overline{\text{LRESET}}$ goes “L”.	
	Output data bus buffer registeri		
	Uxi flag 7, 6, 5, 4, 2		
	XA2i flag	Initialization to “0”.	
	IBFi flag	Initialization to “0”.	There is possibility to generate IBF interrupt request.
	OBFi flag	Initialization to “0”.	There is possibility to generate OBE interrupt request.
	LPCi address register	Keep same value before $\overline{\text{LRESET}}$ goes “L”.	
	LPCCON		

SERIALIZED INTERRUPT

The serialized IRQ circuit communicates the interrupt status to the host controller based on the Serialized IRQ Support for PCI System, Version 6.0.
Table 11 shows the summary of serialized interrupt of 3882.

Table 11 Smmary of serialized IRQ function

Item	Function
The factors of serialized IRQ	The numbers of serialized IRQ factor that can output simultaneously are 3. • Channel 0 (IRQ1,IRQ2) ① Setting Software IRQi (i = 1, 12) request bit (bits 0, 1 of SERIRQ) to “1”. ② The “1” of OBF0 and Hardware IRQi (i=1, 12) request bit (bits 3, 4 of SERCON) to “1”. • Channel 1 (IRQx ; user selectable) ① Setting the IRQx request bit (bit 7 of SERIRQ) to “1”. ② The “1” of OBF1 and Hardware IRQx request bit to “1”.
The number of frame	• Channel 0 (IRQ1, IRQ12) ① Setting Software IRQ1 request bit (bit 0 of SERIRQ) to “1” or detecting “1” of OBF0 with “1” of Hardware IRQ1 request bit (bit 4 of SERCON) selects IRQ1 Frame . ② Setting IRQ12 Software request bit (bit 1 of SERIRQ) to “1” or detecting “1” of OBF0 with “1” of Hardware IRQ1 request bit (bit 4 of SERCON) selects IRQ12 Frame. • Channel 1 (IRQx ; user selectable) Setting IRQx frame select bit (bit 2-6 of SERIRQ) selects IRQ 1–15 frame or extend frame 0–10.
Operation clock	Synchronized with LCLK (Max. 33 MHz).
Clock restart	LPC clock restart enable bit (bit 1 of SERCON) enables restart owing to “L” output of $\overline{\text{CLKRUN}}$ with the interrupt when the LPC clock has stopped or slowed down.
Clock stop inhibition	LPC clock stop inhibition bit (bit 2 of SERCON) enables the inhibition of clock stop control during the IRQSER cycle when the clock tends to stop or slow down.

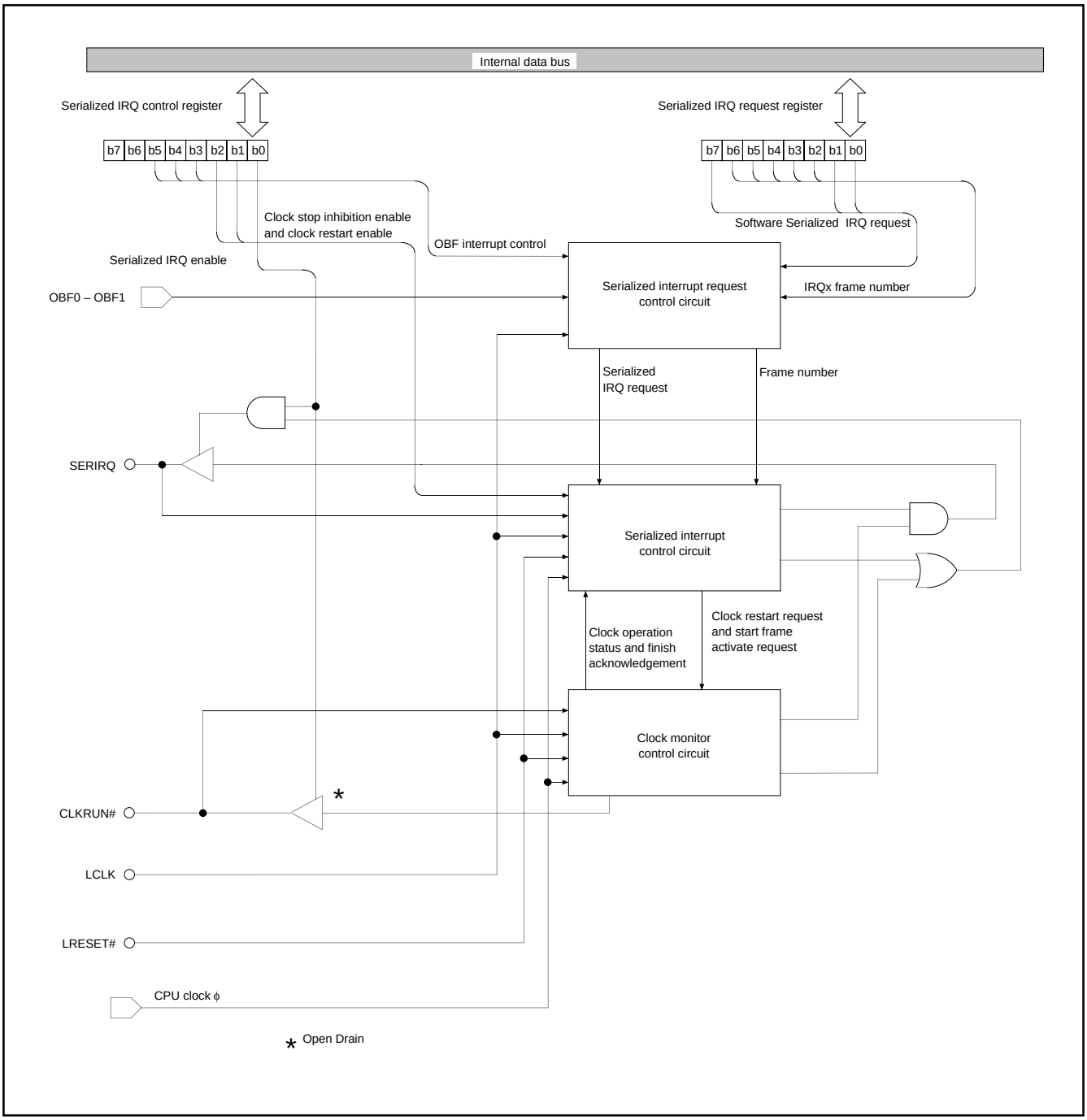


Fig. 31 Block diagram of serialized interrupt

Register Explanation

The serialized IRQ function is configured and controlled by the serialized IRQ request register (SERIRQ) and the serialized IRQ control register (SERCON).

[Serialized IRQ control register (SERCON)] 001D16

Bit 0 : Serialized IRQ enable bit (SIRQEN)

This bit enables/disables the serialized IRQ interface. When this bit is “1”, use of serialized IRQ is enabled. Then P87 functions as IRQ/Data line (SERIRQ) and P47 functions as CLKRUN.
Output structure of CLKRUN pin becomes N-channel open drain.

Bit 1 : LPC clock restart enable bit (RUNEN)

Setting this bit to “1” enables clock restart with “L” output of CLKRUN.

Bit 2 : LPC clock stop inhibition bit (SUPEN)

Setting this bit to “1” makes CLKRUN output change to “L” for inhibiting the clock stop.

Bit 3 : Hardware IRQ1 request bit (SEIR1)

When this bit is “1”, OBF0 status is directly connected to the IRQ1 frame.

Bit 4 : Hardware IRQ12 request bit (SEIR12)

When this bit is “1”, OBF0 status is directly connected to IRQ12 frame.

Bit 5 : Hardware IRQx request bit (SEIRx)

When this bit is “1”, OBF1 status is directly connected to the IRQx frame.

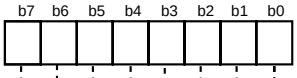
Bit 6 : IRQ1/IRQ12 disable bit (SCH0EN)

This bit controls whether the serialized IRQ channel 0 transfers the IRQ1 and IRQ12 frame to the host or not.

Bit 7 : IRQx output polarity bit (SCH1POL)

This bit selects IRx frame output level.

Serialized IRQ control register



Symbol	Address	When reset
SERCON	001D16	00000000₂

Bit symbol	Bit name	Function	R	W
SIRQEN	Serialized IRQ enable bit	0 : Serialized IRQ disable 1 : Serialized IRQ enable	○	○
RUNEN	LPC clock restart enable bit	0 : Clock restart disable 1 : Clock restart enable	○	○
SUPEN	LPC clock stop inhibition bit	0 : Stop inhibition control disable 1 : Stop inhibition control enable	○	○
SEIR1	Hardware IRQ1 request bit	0 : No IRQ1 request 1 : OBF0 synchronized IRQ1 request	○	○
SEIR12	Hardware IRQ12 request bit	0 : No IRQ12 request 1 : OBF0 synchronized IRQ12 request	○	○
SEIRx	Hardware IRQx request bit	0 : No IRQx request 1 : OBF1 synchronized IRQx request	○	○
SCH0EN	IRQ1/IRQ12 disable bit	0 : IRQ1/IRQ12 output enable 1 : IRQ1/IRQ12 output disable	○	○
SCH1POL	IRQx output polarity bit	0 : -Request Hiz-Hiz-Hiz -No request L-H-Hiz 1 : -Request L-H-Hiz -No request Hiz-Hiz-Hiz	○	○

Fig. 32 Configuration of serialized IRQ control register

[Serialized IRQ request register (SERIRQ)] 001F16

The interrupt source is definable by this register.

Bit 0 : Software IRQ1 request bit (IR1)

SERIRQ line shows IR1 value at the sample phase of IRQ1 frame, when the SCH0EN is “1”.

Bit 1 : Software IRQ12 request bit (IR12)

SERIRQ line shows IR12 value at the sample phase of IRQ12 frame, when the SCH0EN is “1”.

Bits 2-6 : IRQx frame select bits (ISi, i = 0–4)

These bits select the active IRQ frame of serial IRQ channel 1. When these bit are “000002”, the serial IRQ channel 1 is disabled.

Bit 7 : Software IRQx request bit (IRx)

SERIRQ line shows IRx value at the sample phase of IRQx frame which is selected by bits 2 to 6 of SERIRQ. Output level is selectable by the IRQx output polarity bit (SCH1POL).

Serialized IRQ request register

b7 b6 b5 b4 b3 b2 b1 b0

Symbol: SERIRQ — Address: 001F16 — When reset: 000000002

Bit symbol	Bit name	Function	R	W
IR1	Software IRQ1 request bit	0: No IRQ1 request 1: IRQ1 request	○	○
IR12	Software IRQ12 request bit	0: No IRQ12 request 1: IRQ12 request	○	○
IS0	IRQx frame select bit	b6b5b4b3b2 0 0 0 0 0 : Disable serial IRQ channel 1 0 0 0 0 1 : IRQ1 Frame 0 0 0 1 0 : IRQ2 Frame 0 0 0 1 1 : IRQ3 Frame 0 0 1 0 0 : IRQ4 Frame 0 0 1 0 1 : IRQ5 Frame 0 0 1 1 0 : IRQ6 Frame 0 0 1 1 1 : IRQ7 Frame 0 1 0 0 0 : IRQ8 Frame 0 1 0 0 1 : IRQ9 Frame 0 1 0 1 0 : IRQ10 Frame 0 1 0 1 1 : IRQ11 Frame 0 1 1 0 0 : IRQ12 Frame 0 1 1 0 1 : IRQ13 Frame 0 1 1 1 0 : IRQ14 Frame 0 1 1 1 1 : IRQ15 Frame 1 0 0 0 0 : Do not select 1 0 0 0 1 : Do not select 1 0 0 1 0 : Do not select 1 0 0 1 1 : Do not select 1 0 1 0 0 : Do not select 1 0 1 0 1 : Extend Frame 0 1 0 1 1 0 : Extend Frame 1 1 0 1 1 1 : Extend Frame 2 1 1 0 0 0 : Extend Frame 3 1 1 0 0 1 : Extend Frame 4 1 1 0 1 0 : Extend Frame 5 1 1 0 1 1 : Extend Frame 6 1 1 1 0 0 : Extend Frame 7 1 1 1 0 1 : Extend Frame 8 1 1 1 1 0 : Extend Frame 9 1 1 1 1 1 : Extend Frame 10	○	○
IS1			○	○
IS2			○	○
IS3			○	○
IS4			○	○
IRx	Software IRQx request bit	0: No IRQx request 1: IRQx request	○	○

Fig. 33 Structure of serialized IRQ request register

Operation of Serialized IRQ

A cycle operation of serialized IRQ starts with Start Frame and finishes with Stop Frame. There are two modes of operation : Continuous (Idle) mode and Quiet (Active) mode. The next operation mode is determined by monitoring the stop frame pulse width.

●Timing of serialized IRQ cycle

Figure 54 shows the timing diagram of serialized IRQ cycle.

(1) Start Frame

The Start Frame is detected when the SERIRQ line remains “L” in 4 to 8 clocks.

(2) IRQ/Data Frame

Each IRQ/Data Frame is three clocks. When the IRQi (i = 0, 1, x) request is “0”, then the SERIRQ line is driven to “L” during the Sample phase (1st clock) of the corresponding IRQ/Data frame, to “H” during the Recovery phase (2nd clock), to tri-state during the Turn-around phase (3rd clock). When the IRQi request is “1”, then the SERIRQ line is tri-state in all phases (3 clocks period).

(3) Stop Frame

The Stop Frame is detected when the SERIRQ line remains “L” in 2 or 3 clocks. The next operation mode is Quiet mode when the pulse width of “L” is 2 clocks. The next operation mode is the Continuous mode when the pulse width is 3 clocks.

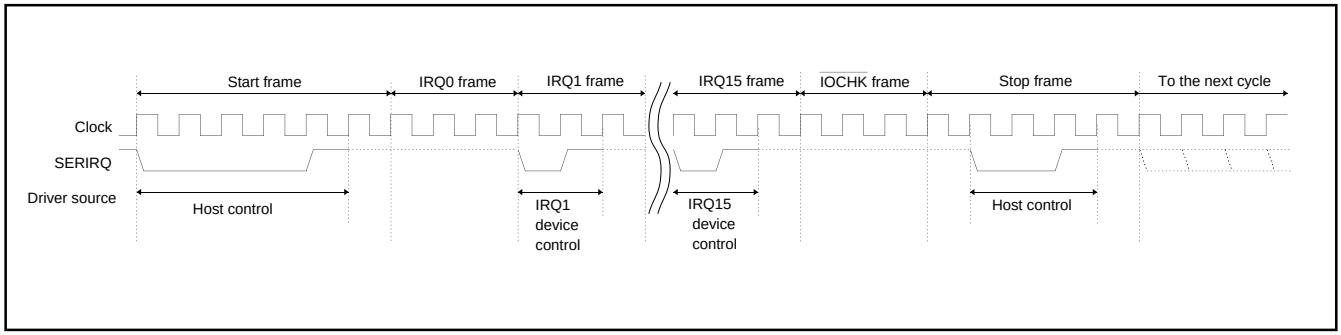


Fig. 34 Timing diagram of serialized IRQ cycle

Operation Mode

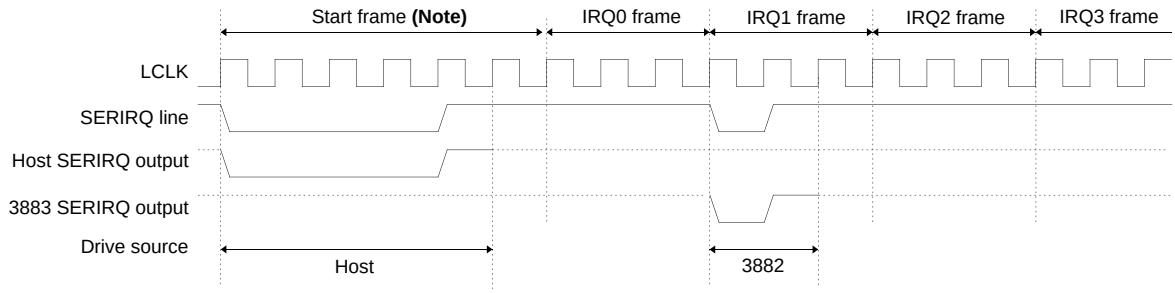
Figure 35 shows the timing of continuous mode; Figure 36 shows that of Quiet mode.

(1) Continuous mode

Serialized IRQ cycles starts in Continuous mode after CPU reset in the case of $\overline{\text{LRESET}}$ = "L" and the previous stop frame being 3 clocks.

After receiving the start frame; the IRQ1 Frame, IRQ12 Frame or IRQx frame is asserted.

Note : If the pulse width of "L" is less than 4 clocks, or 9 clocks or more; the start frame is not detected and the next start (the falling edge of SERIRQ) is waited.



Note: The start frame count is 4 clocks as exemple.

Fig. 35 Timing diagram of Continuous mode

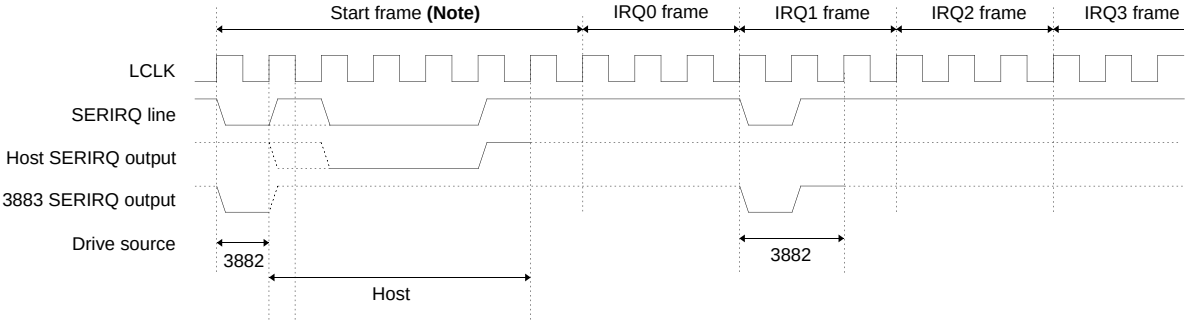
(2) Quiet mode

At clock stop, clock slow down or the pulse width of the last stop frame being 2 clocks, it is the Quiet mode.

In this mode the 3882 drives the SERIRQ line to "L" in the 1st clock. After that the host drives the rest start frame (Note). The IRQ1 frame, IRQ12 frame or IRQx frame is asserted.

Note: When the sum of pulse width of "L" driven by the 3882 in the 1st clock and driven by the host in the rest clocks is within 4 to 8-clock cycles, the start frame is detected.

If the sum of pulse width of "L" is less than 4 clocks, or 9 clocks or more; the start frame is not detected and the next start (the falling edge of SERIRQ) is waited.



Note: The start frame count is 4 clocks as exemple

Fig. 36 Timing diagram of Quiet mode

Clock Restart/Stop Inhibition Request

Asserting the CLKRUN signal can request the host to restart for clocks stopped or slowed down, or maintain the clock tending to stop or slow down.

Figure 37 shows the timing diagram of clock restart request; Figure 38 shows an example of timing of clock stop inhibition request.

(1) Clock restart operation

In case the LPC clock restart enable bit (bit 1 of SERCON) is “1” and the CLKRUN (BUS) is “H”, when the serialized interrupt request occurs, the 3882 drives CLKRUN to “L” for requesting the PCI clock generator to restart the LCLK if the clock is slowed down or stopped.

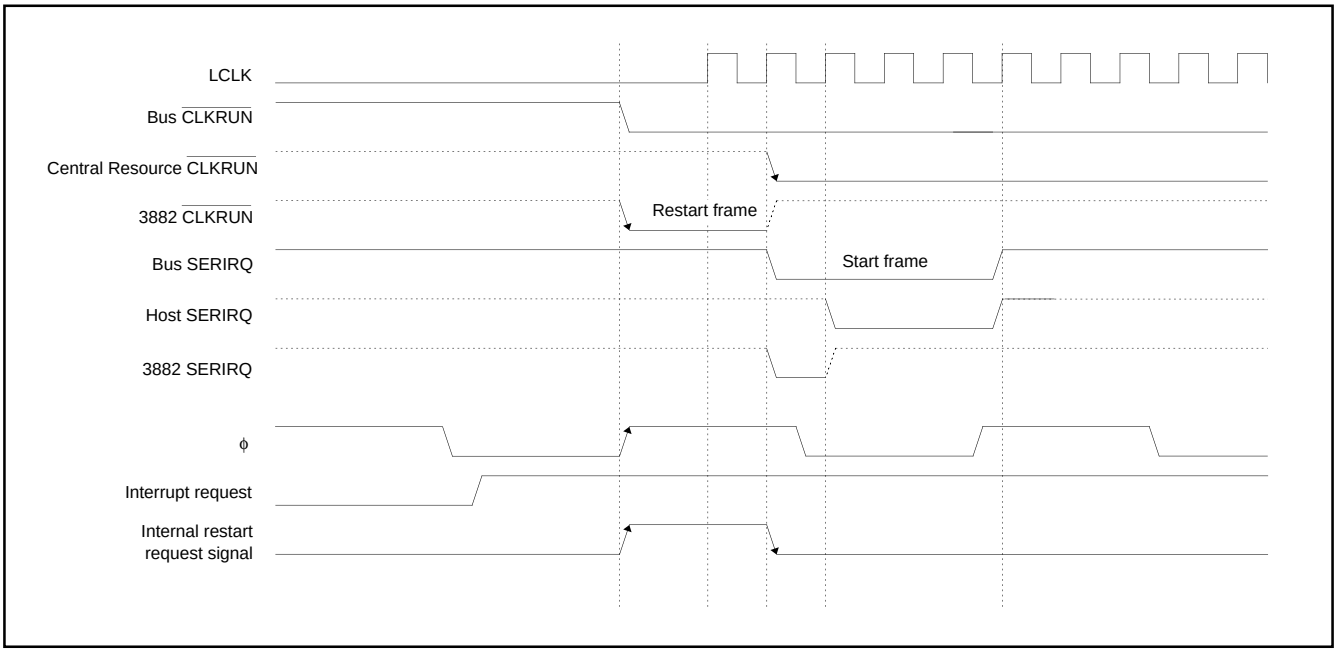


Fig. 37 Timing diagram of clock restart request

(2) Clock stop inhibition request

In case the LPC clock stop inhibition bit (bit 2 of SERCON) is “1” and the serialized interrupt request is held, if the LCLK tends to stop, the 3882 drives CLKRUN to “L” for requesting the PCI clock generator not to stop LCLK.

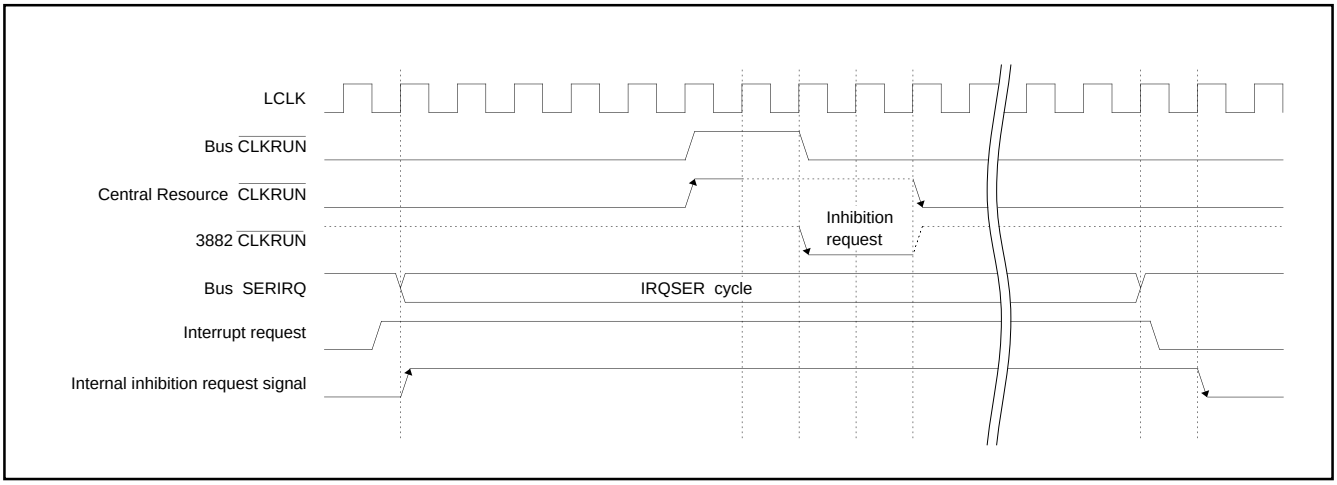


Fig. 38 Timing diagram of clock stop inhibition request

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an “L” level for 16 X_{IN} cycle or more. (When the power source voltage should be between 3.3V ± 0.3V and the oscillation should be stable.) Then the $\overline{\text{RESET}}$ pin set to “H”, the reset state is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.6 V for V_{CC} of 3.0 V.

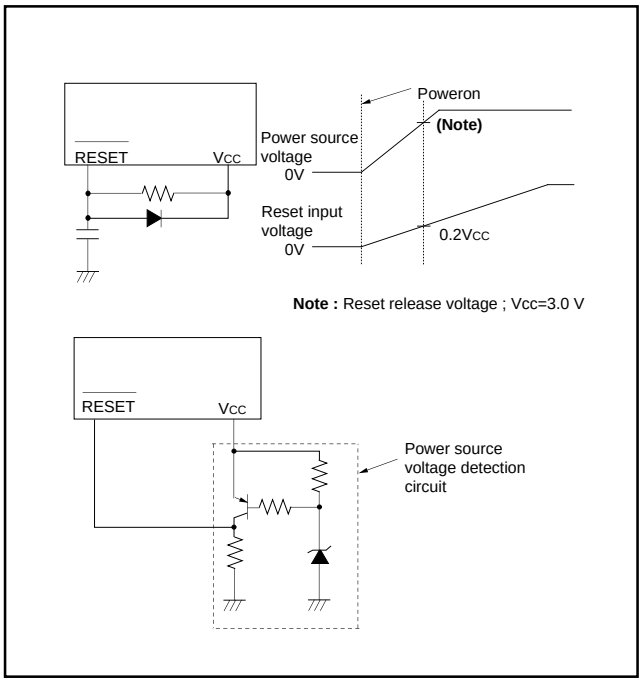


Fig. 39 Reset circuit example

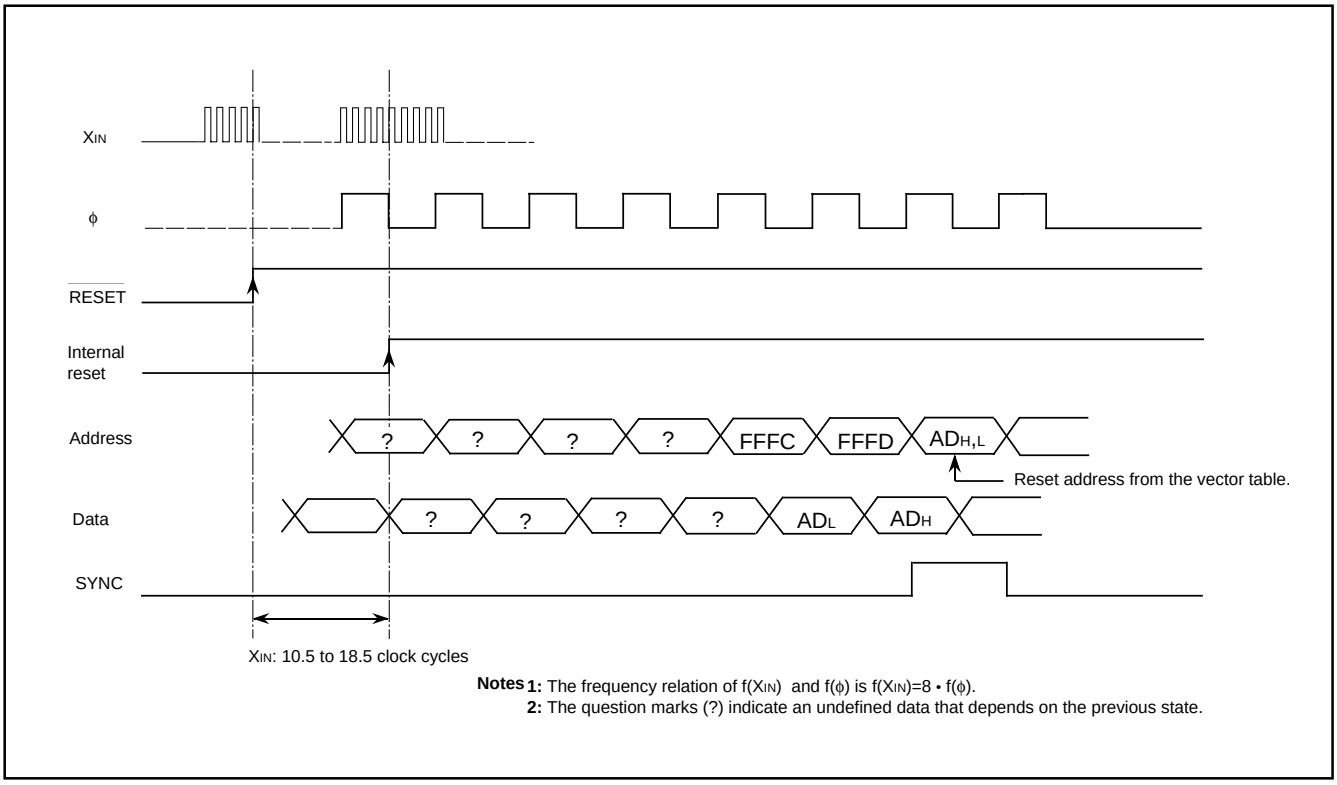


Fig. 40 Reset sequence

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Port P5 (P5)	$000A_{16}$	00_{16}
(12)	Port P5 direction register (P5D)	$000B_{16}$	00_{16}
(13)	Port P6 (P6)	$000C_{16}$	00_{16}
(14)	Port P6 direction register (P6D)	$000D_{16}$	00_{16}
(15)	Port P7 (P7)	$000E_{16}$	00_{16}
(16)	Port P7 direction register (P7D)	$000F_{16}$	00_{16}
(17)	Port P8 (P8)	0010_{16}	00_{16}
(18)	Port P8 direction register (P8D)	0011_{16}	00_{16}
(19)	Serialized IRQ control register (SERCON)	$001D_{16}$	00_{16}
(20)	Watchdog timer control register (WDTCON)	$001E_{16}$	0 0 1 1 1 1 1 1
(21)	Serialized IRQ request register (SERIRQ)	$001F_{16}$	X X X X X X X X
(22)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(23)	Timer 1 (T1)	0021_{16}	01_{16}
(24)	Timer 2 (T2)	0022_{16}	FF_{16}
(25)	Timer XY mode register (TM)	0023_{16}	00_{16}
(26)	Prescaler X (PREX)	0024_{16}	FF_{16}
(27)	Timer X (TX)	0025_{16}	FF_{16}
(28)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(29)	Timer Y (TY)	0027_{16}	FF_{16}
(30)	Data bus buffer register 0 (DBB0)	0028_{16}	X X X X X X X X
(31)	Data bus buffer status register 0 (DBBSTS0)	0029_{16}	00_{16}
(32)	LPC control register (LPCCON)	$002A_{16}$	00_{16}
(33)	Data bus buffer register 1 (DBB1)	$002B_{16}$	X X X X X X X X
(34)	Data bus buffer status register 1 (DBBSTS1)	$002C_{16}$	00_{16}
(35)	Port control register 1 (PCTL1)	$002E_{16}$	00_{16}
(36)	Port control register 2 (PCTL2)	$002F_{16}$	00_{16}
(37)	Interrupt source selection register (INTSEL)	0039_{16}	00_{16}
(38)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(39)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(40)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(41)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(42)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(43)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(44)	LPC0 address register L (LPC0ADL)	$0FF0_{16}$	00_{16}
(45)	LPC0 address register H (LPC0ADH)	$0FF1_{16}$	00_{16}
(46)	LPC1 address register L (LPC1ADL)	$0FF2_{16}$	00_{16}
(47)	LPC1 address register H (LPC1ADH)	$0FF3_{16}$	00_{16}
(48)	Port P5 input register (P5I)	$0FF8_{16}$	00_{16}
(49)	Port control register 3 (PCTL3)	$0FF9_{16}$	00_{16}
(50)	Processor status register	(PS)	X X X X X 1 X X
(51)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 41 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3882 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.)

Immediately after power on, only the XIN oscillation circuit starts oscillating.

Frequency Control
(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

■Note

If you switch the mode between middle/high-speed ,stabilize XIN oscillations.

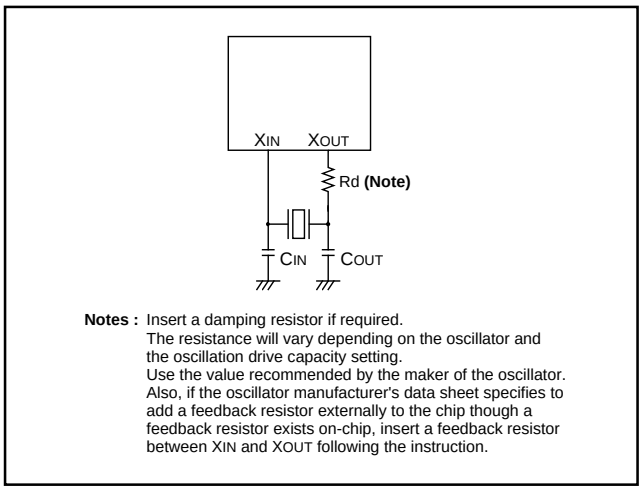
Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN oscillators stop. When the oscillation stabilizing time set after STP instruction released bit is "0," the prescaler 12 is set to "FF16" and timer 1 is set to "0116". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

XIN divided by 16 is input to the prescaler 12 as count source, and the output of the prescaler 12 is connected to timer 1. Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. Therefore make sure not to set the timer 1 interrupt request bit to "1" before the STP instruction stops the oscillator. When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.



Notes : Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies to add a feedback resistor externally to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 42 Ceramic resonator circuit

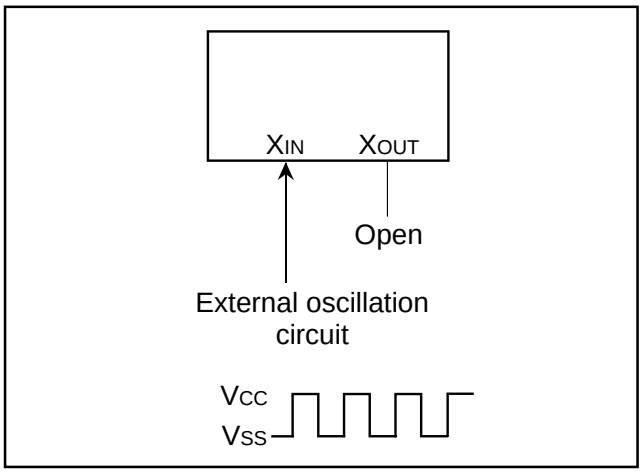
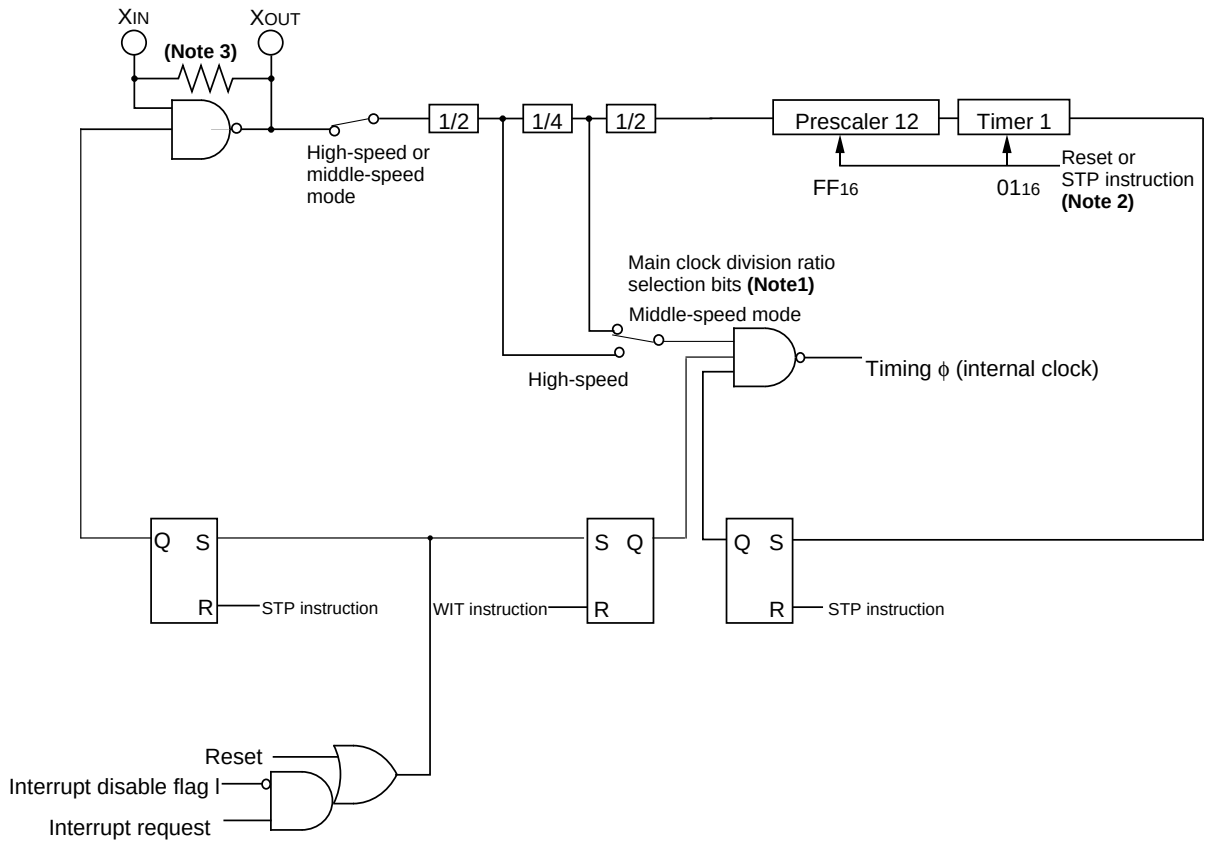
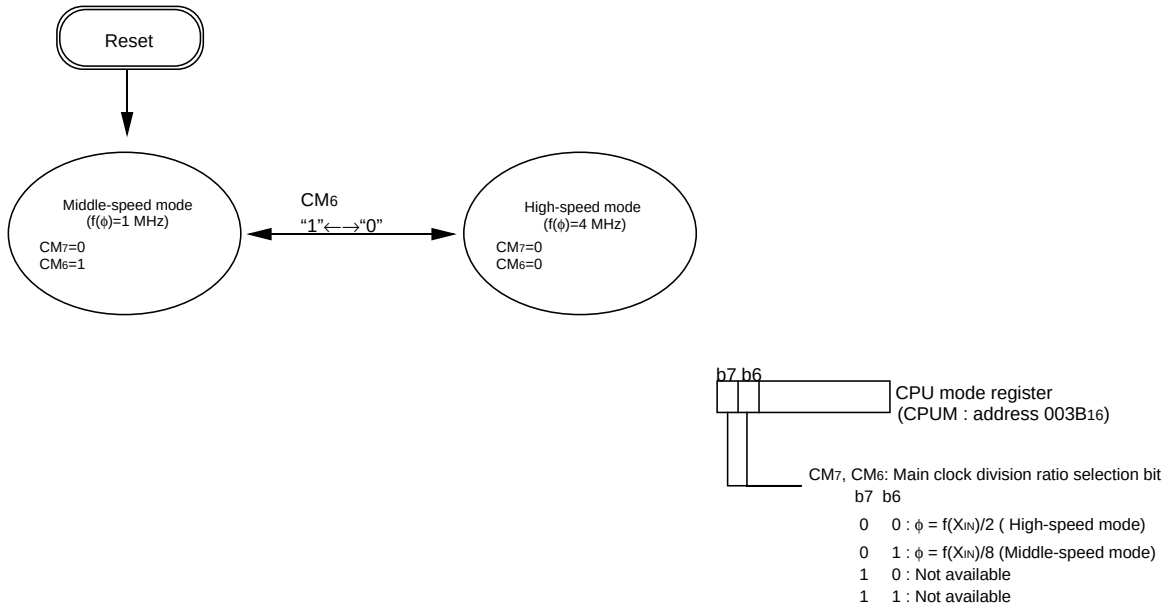


Fig. 43 External clock input circuit



Notes 1: Either high-speed ,or middle-speed is selected by bits 7 and 6 of the CPU mode register.
2: f(X_{IN})/16 is supplied as the count source to the Prescaler 12 at reset. When exciting STP instruction, the count source does not change either f(X_{IN}))/16 after releasing stop mode. Oscillation stabilizing time is not fixed "$01FF_{16}$" when the bit 6 of PCTL2 is "1".
3: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig. 44 System clock generating circuit block diagram (Single-chip mode)



Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3 : Timer operates in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs by connecting prescaler 12 and Timer 1 in middle/high-speed mode.
5 : The example assumes that 8 MHz is being applied to the X_{IN} pin . ϕ indicates the internal clock.

Fig. 45 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock ϕ is twice of the X_{IN} period in high-speed mode.

Reserved Area, Reserved Bit

Do not write any data to the reserved area in the SFR area and thespecial page. (Do not change the contents after reset.)

CPU Mode Register

Be sure to fix bit 3 of the CPU mode register (address $003B_{16}$) to “1”.

NOTES ON USAGE

Termination of Unused Pins
Be sure to perform the termination of unused pins.

Handling of Power Source Pins
In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (V_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF–0.1 µF is recommended.

Power Source Voltage
When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.
In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Product shipped in blank
As for the product shipped in blank, Renesas does not perform the writing test to user ROM area after the assembly process though the QzROM writing test is performed enough before the assembly process. Therefore, a writing error of approx.0.1 %may occur.
Moreover, please note the contact of cables and foreign bodies on a socket, etc. because a writing environment may cause some writing errors.

Overvoltage
Take care that overvoltage is not applied. Overvoltage may cause the QzROM contents rewriting. Take care especially at turning on the power.

QzROM Version
Connect the CNV$_{SS}$/(V_{PP}) pin the shortest possible to the GND pattern which is supplied to the V_{SS} pin of the microcomputer.
In addition connecting an approximately 5 k Ω resistor in series to the GND could improve noise immunity. In this case as well as the above mention, connect the pin the shortest possible to the GND pattern which is supplied to the V_{SS} pin of the microcomputer.

•Reason

The CNV$_{SS}$/(V_{PP}) pin is the power source input pin for the built-in QzROM. When programming in the QzROM, the impedance of the V_{PP} pin is low to allow the electric current for writing to flow into the built-in QzROM. Because of this, noise can enter easily.If noise enters the CNV$_{SS}$/(V_{PP}) pin, abnormal instruction codes or data are read from the QzROM, which may cause a program runaway.

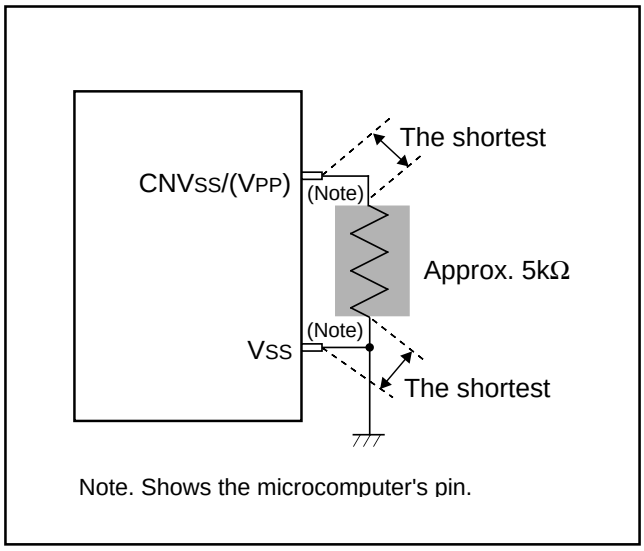


Fig. 46 Wiring for the CNV$_{SS}$/(V_{PP}) pin

NOTES ON QzROM
Notes On QzROM Writing Orders
When ordering the QzROM product shipped after writing, submit the mask file (extension : .msk) which is made by the mask file converter MM.
Be sure to set the ROM option (“MASK option“ written in the mask file converter) setup when making the mask file by using the mask file converter MM.

Notes On ROM Code Protect (QzROM product shipped after writing)
As for the QzROM product shipped after writing, the ROM code protect is specified according to the ROM option setup data in the mask file which is submitted at ordering. The ROM option setup data in the mask file is “00_{16}” for protect enabled or “FF_{16}” for protect disabled. Therefore, the contents of the ROM code protect address (other than the user ROM area)of the QzROM product shipped after writing is “00_{16}” or “FF_{16}”.
Note that the mask file which has nothing at the ROM option data or has the data other than “00_{16}” and “FF_{16}” can not be accepted.

DATA REQUIRED FOR QzROM WRITING ORDERS
The following are necessary when ordering a QzROM product shipped after writing:
1.QzROM Writing Confirmation Form*
2.Mark Specification Form*
3.ROM data.....Mask file
*For the QzROM writing confirmation form and the mark specification form, refer to the “Renesas Technology Corp.” Homepage (http://www.renesas.com/homepage.jsp).
Note that we cannot deal with special font marking (customer's trademark etc.) in QzROM microcomputer.

ELECTRICAL CHARACTERISTICS

Table 12 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltages	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 4.6	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, $\overline{RESET}$, X_{IN}, CNV_{SS}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P7_0$–$P7_7$		–0.3 to 5.8	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage $P7_0$–$P7_7$		0.3 to 5.8	V
P_d	Power dissipation	Ta = 25°C	500	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

Table 13 Recommended operating conditions
(V_{CC} = 3.3 V ± 0.3V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage		3.0	3.3	3.6	V
V_{SS}	Power source voltage			0		V
V_{IH}	“H” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$, $\overline{RESET}$, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage	$P7_0$–$P7_7$	0.8V_{CC}		5.5	V
V_{IH}	“H” input voltage (when TTL input level is selected)	$P7_0$–$P7_5$	2.0		5.5	V
V_{IH}	“H” input voltage	X_{IN}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, $\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	“L” input voltage (when TTL input level is selected)	$P7_0$–$P7_5$	0		0.8	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V

Table 14 Recommended operating conditions
(V_{CC} = 3.3 V ± 0.3V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			–80	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$			–80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P2_4$–$P2_7$			80	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			–40	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$			–40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P2_4$–$P2_7$			40	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	$P4_0$–$P4_7$,$P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 15 Recommended operating conditions
(V_{CC} = 3.3 V ± 0.3V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note 1)**			–10	mA
$I_{OL(peak)}$	"L" peak output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ **(Note 1)**			10	mA
$I_{OL(peak)}$	"L" peak output current	$P2_4$–$P2_7$ **(Note 1)**			20	mA
$I_{OH(avg)}$	"H" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note 2)**			–5	mA
$I_{OL(avg)}$	"L" average output current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ **(Note 2)**			5	mA
$I_{OL(avg)}$	"L" peak output current	$P2_4$–$P2_7$ **(Note 2)**			15	mA
$f(X_{IN})$	Main clock input oscillation frequency **(Note 3)**				8	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50%.

Table 16 Electrical characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P8_0$–$P8_7$ **(Note)**	I_{OH} = –5 mA	V_{CC}–1.0			V
V_{OL}	"L" output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	I_{OL} = 5 mA			1.0	V
		I_{OL} = 1.6 mA			0.4	V
V_{T+}–V_{T-}	Hysteresis $CNTR_0$, $CNTR_1$, INT_0, INT_1 INT_{20}–INT_{40}, INT_{21}–INT_{41}, INT_5 $P3_0$–$P3_7$, $\overline{\text{LRESET}}$ $\overline{\text{LFRAME}}$, LCLK, SERIRQ			0.4		V
I_{IH}	"H" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ $\overline{\text{RESET}}$, CNV_{SS}	V_I = V_{CC} (Pin floating. Pull-up transistors "off")			5.0	µA
I_{IH}	"H" input current X_{IN}	V_I = V_{CC}		3		µA
I_{IL}	"L" input current $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$ $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$ $P6_0$–$P6_7$, $P7_0$–$P7_7$, $P8_0$–$P8_7$ $\overline{\text{RESET}}$,CNV_{SS}	V_I = V_{SS} (Pin floating. Pull-up transistors "off")			–5.0	µA
I_{IL}	"L" input current X_{IN}	V_I = V_{SS}		–3	–100	µA
I_{IL}	"L" input current $P3_0$–$P3_7$ (at Pull-up)	V_I = V_{SS}	–13	–50	3.6	µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0			V

Note: $P0_0$–$P0_3$ are measured when the $P0_0$–$P0_3$ output structure selection bit (bit 0 of PCTL1) is "0".
$P0_4$–$P0_7$ are measured when the $P0_4$–$P0_7$ output structure selection bit (bit 1 of PCTL1) is "0".
$P1_0$–$P1_3$ are measured when the $P1_0$–$P1_3$ output structure selection bit (bit 2 of PCTL1) is "0".
$P1_4$–$P1_7$ are measured when the $P1_4$–$P1_7$ output structure selection bit (bit 3 of PCTL1) is "0".
$P4_2$, $P4_3$, $P4_4$, and $P4_6$ are measured when the P4 output structure selection bit (bit 2 of PCTL2) is "0".

Table 17 Electrical characteristics
(V_{CC} = 3.3 V ± 0.3V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 8 MHz Output transistors “off”			1.5	5	mA
		High-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) Output transistors “off”			0.5	2	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz Output transistors “off”			0.7	3	mA
		Middle-speed mode $f(X_{IN})$ = 8 MHz (in WIT state) Output transistors “off”			0.4	1.5	mA
		Additional current when LPC I/F functions LCLK = 33 MHz			1.5		mA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

Table 18 Timing requirements
(Vcc = 3.3 V ± 0.3V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
tw($\overline{\text{RESET}}$)	Reset input “L” pulse width	16			tc(XIN)
tc(XIN)	Main clock input cycle time	125			ns
twH(XIN)	Main clock input “H” pulse width	50			ns
twL(XIN)	Main clock input “L” pulse width	50			ns
tc(CNTR)	CNTR0, CNTR1 input cycle time	200			ns
twH(CNTR)	CNTR0, CNTR1 input “H” pulse width	80			ns
twL(CNTR)	CNTR0, CNTR1 input “L” pulse width	80			ns
twH(INT)	INT0, INT1, INT20, INT30, INT40, INT21, INT31, INT41 input “H” pulse width	80			ns
twL(INT)	INT0, INT1, INT20, INT30, INT40, INT21, INT31, INT41 input “L” pulse width	80			ns

Table 19 Switching characteristics
(Vcc = 3.3 V ± 0.3V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
tr (CMOS)	CMOS output rising time **(Note 1)**	Fig. 46		10	30	ns
tf (CMOS)	CMOS output falling time **(Note 1)**			10	30	ns

Notes 1: The XOUT pin is excluded.

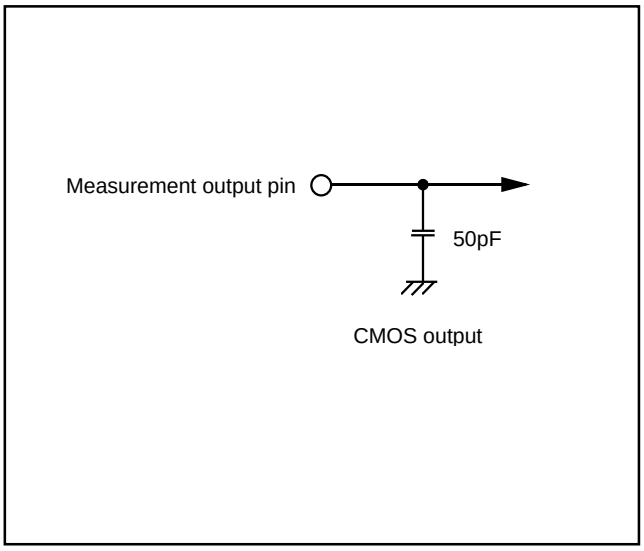


Fig. 47 Circuit for measuring output switching characteristics

Timing diagram

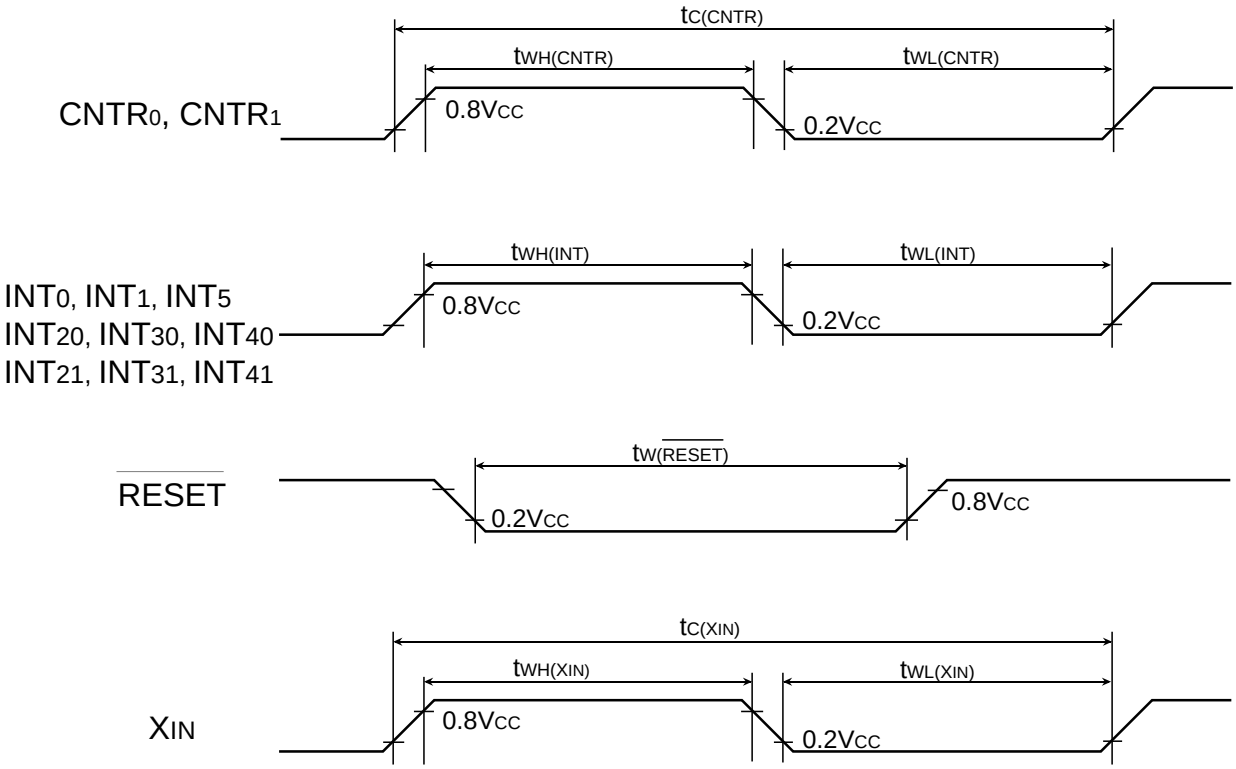


Fig. 48 Timing diagram

Table 20 Timing requirements and switching characteristics
(Vcc = 3.3 V ± 0.3V, Vss = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$t_{C(CLK)}$	LCLK clock input cycle time		30			ns
$t_{WH(CLK)}$	LCLK clock input “H” pulse width		11			ns
$t_{WL(CLK)}$	LCLK clock input “L” pulse width		11			ns
$t_{su(D-C)}$	input set up time	LAD_3 to LAD_0,	13			ns
		SERIRQ, $\overline{CLKRUN}$, $\overline{LFRAME}$	7			
$t_{h(C-D)}$	input hold time	LAD_3 to LAD_0, $\overline{CLKRUN}$, $\overline{LFRAME}$	0			ns
		SERIRQ,	2			
$t_{V(C-D)}$	LAD_3 to LAD_0, SERIRQ, $\overline{CLKRUN}$ valid delay time		2		15	ns
$t_{off(A-F)}$	LAD_3 to LAD_0,SERIRQ,$\overline{CLKRUN}$ floating output delay time				28	ns

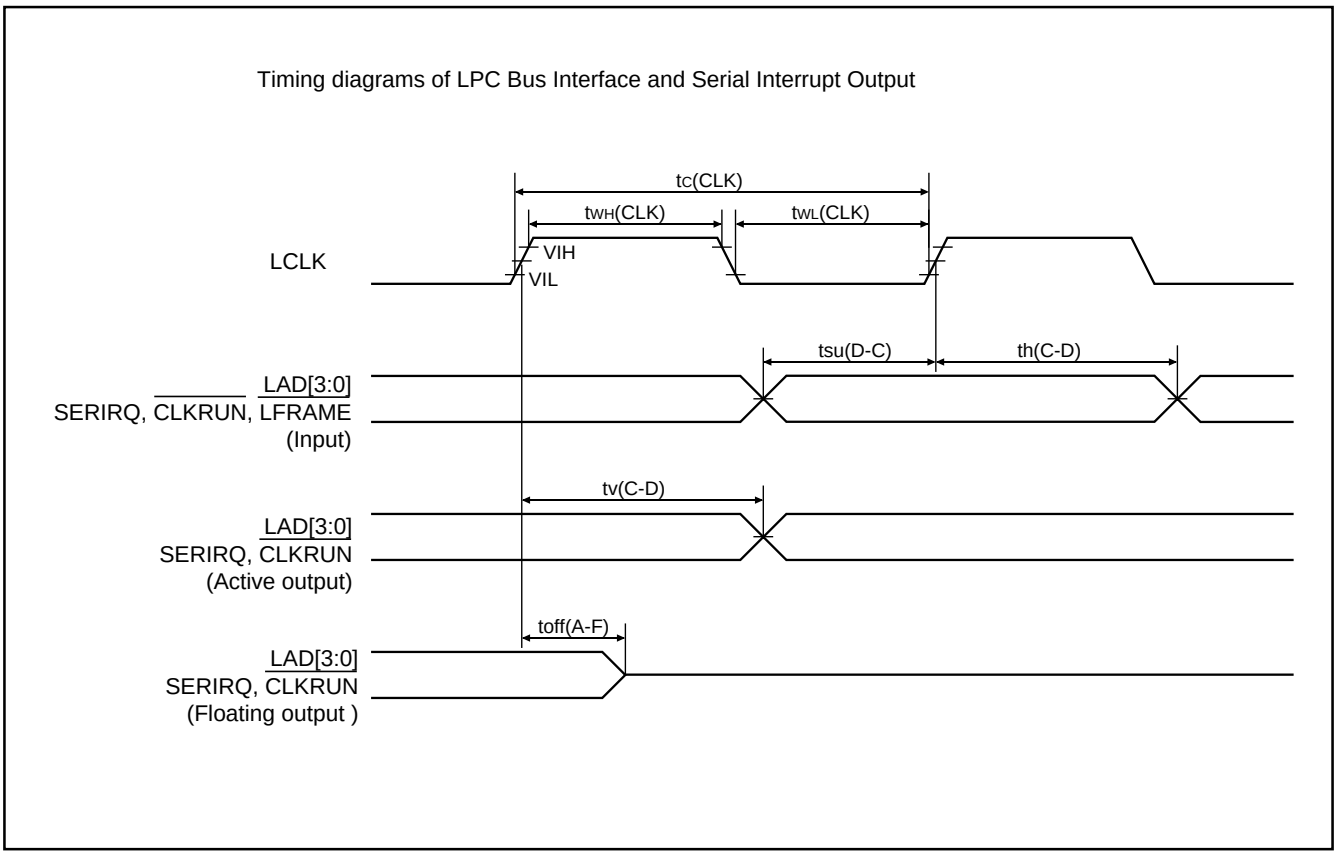
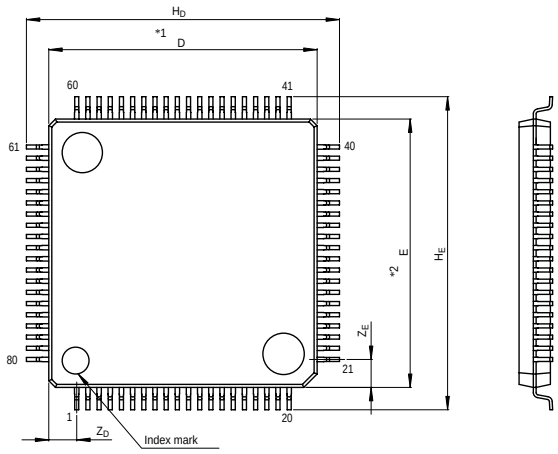
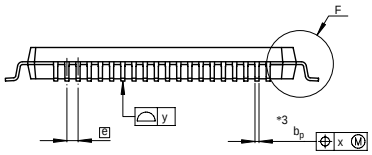


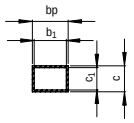
Fig. 49 Timing diagram of LPC Interface and Serialized IRQ

PACKAGE OUTLINE

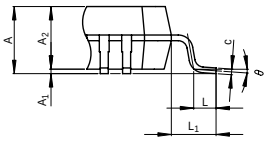
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

REVISION HISTORY	3882 Group Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Oct 29, 2004	–	First edition issued
1.01	Nov 14, 2005	1 1-2,5-6 3 5 6 11 14 16 27 47 48 50 51 52 55 60	Power dissipation is revised. 1.5 mA → 20mW Package name of 80P6Q-A is revised. 80P6Q-A → PLQP0080KB-A Table 1 is partly revised. Fig.3 is partly revised. Table 3 is partly added. Note of Table 2 is added. ROM Code Protect Address is added. Table 7 is partly revised. Note 2 of Fig.11 is added. • WATCHDOG TIMER is revised. • Fig.21 and Fig.22 are partly revised. • CLOCK GENERATING CIRCUIT is partly revised. • Fig.42 is partly revised. Note 3 of Fig.44 is added. Reserved Area, Reserved Bit and CPU Mode Register are added. The following are added; -Termination of Unused Pins -Product shipped in blank -Overvoltage -QzROM Version -Fig.46 Wiring for the CNVSS/(VPP) pin -Notes On QzROM Writing Orders -Notes On ROM Code Protect -DATA REQUIRED FOR QzROM WRITING ORDERS Table 12 is partly revised. Table 17 is partly revised. PACKAGE OUTLINE of 80P6Q-A is revised.

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