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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.) Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

3807 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

DESCRIPTION

The 3807 group is a 8-bit microcomputer based on the 740 family core technology.

The 3807 group has two serial I/Os, an A-D converter, a D-A converter, a real time output port function, a watchdog timer, and an analog comparator, which are available for a system controller which controls motors of office equipment and household appliances.

The various microcomputers in the 3807 group include variations of internal memory size and packaging. For details, refer to the section on part numbering.

For details on availability of microcomputers in the 3807 group, refer to the section on group expansion.

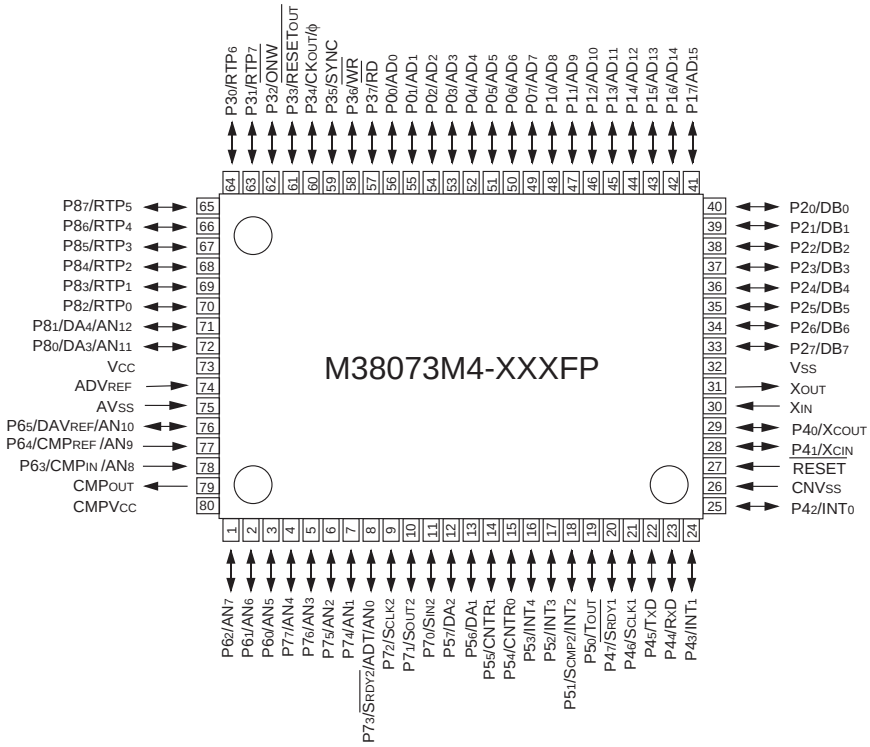
FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time ..... 0.5 μs (at 8 MHz oscillation frequency)
- Memory size .....
  - ROM ..... 8 to 60 K bytes
  - RAM ..... 384 to 2048 bytes
- Programmable input/output ports 68
- Software pull-up resistors (Ports P0 to P2) 24
- Input ports (Ports $P6_3$ and $P6_4$) 2
- Interrupts ..... 20 sources, 16 vectors
- Timers X, Y ..... 16-bit × 2
- Timers A, B (for real time output port function) ..... 16-bit × 2
- Timers 1–3 ..... 8-bit × 3
- Serial I/O1 (UART or Clock-synchronized) ..... 8-bit × 1
- Serial I/O2 (Clock-synchronized) ..... 8-bit × 1
- A-D converter ..... 8-bit × 13 channels
- D-A converter ..... 8-bit × 4 channels
- Watchdog timer ..... 16-bit × 1
- Analog comparator ..... 1 channel
- 2 Clock generating circuit
  - Main clock (X_{IN}–X_{OUT}) ..... Internal feedback resistor
  - Sub-clock (X_{CIN}–X_{COUT}) ..... Without internal feedback resistor
  - (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  - In high-speed mode ..... 4.0 to 5.5 V (at 8 MHz oscillation frequency and high-speed selected)
  - In middle-speed mode ..... 2.7 to 5.5 V (at 8 MHz oscillation frequency and middle-speed selected)
  - In low-speed mode ..... 2.7 to 5.5 V (at 32 kHz oscillation frequency and low-speed selected)
- Power dissipation
  - In high-speed mode ..... 34 m W (at 8 MHz oscillation frequency, at 5 V power source voltage)
  - In low-speed mode ..... 60 µW (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Memory expansion ..... possible
- Operating temperature range ..... –20 to 85 °C

APPLICATION

LBP engine control, PPC, FAX, office equipment, household appliances, consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : 80P6N-A
80-pin plastic-molded QFP

Fig. 1. Pin configuration of M38073M4-XXXFP

FUNCTIONAL BLOCK

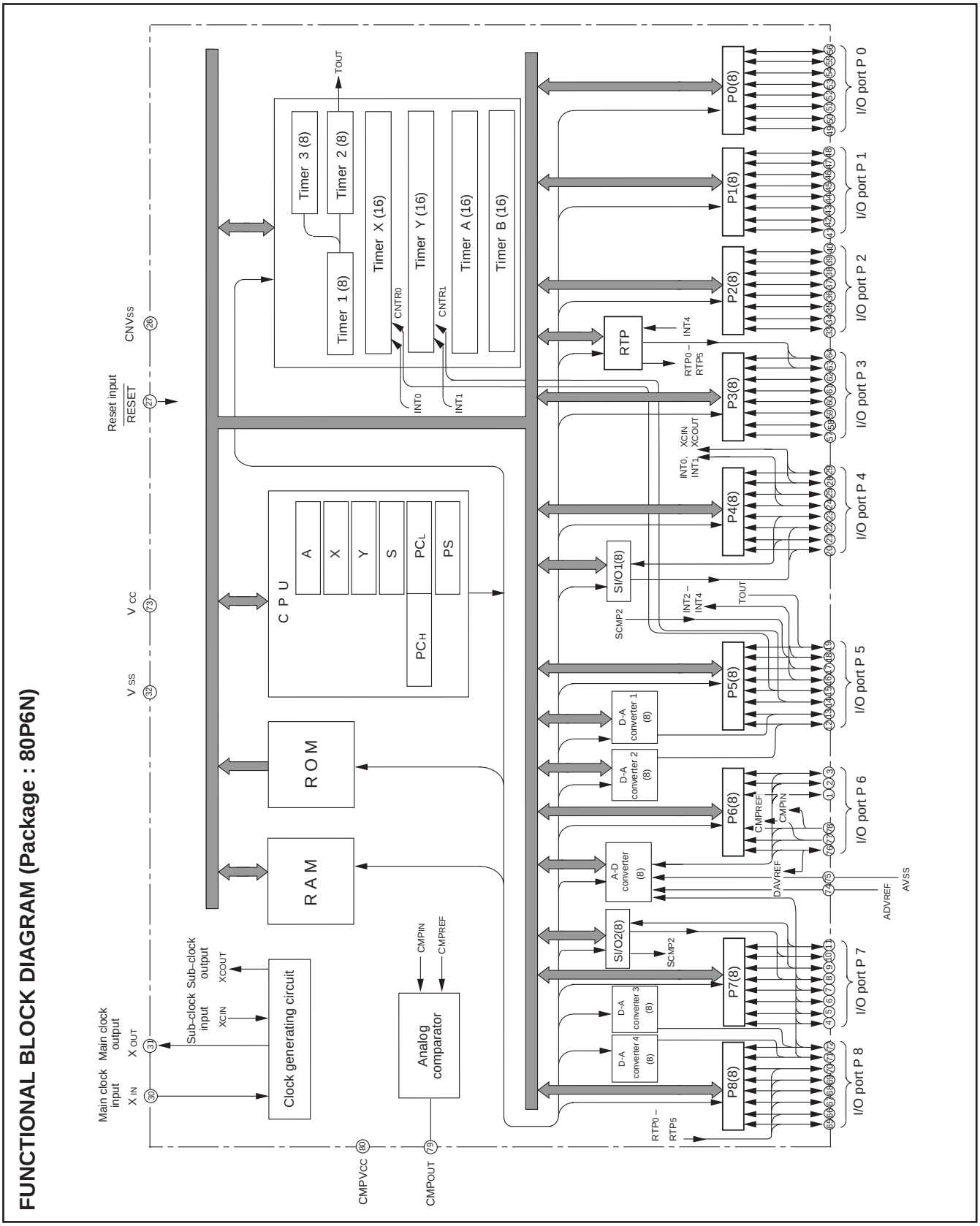


Fig. 2. Functional block diagram

PIN DESCRIPTION

Table. 1. Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC}, V_{SS}	Power source	• Apply voltage of 2.7–5.5 V to V_{CC}, and 0 V to V_{SS}.	
CMPV_{CC}	Analog comparator power source	• Power source input pin for an analog comparator	
CNV$_{SS}$	CNV$_{SS}$	• This pin controls the operation mode of the chip. • Normally connected to V_{SS}. • If this pin is connected to V_{CC}, the internal ROM is inhibited and external memory is accessed.	
ADV$_{REF}$	Analog reference voltage	• Reference voltage input pin for A-D converter.	
AV$_{SS}$	Analog power source	• Analog power source input pin for A-D and D-A converter and an analog comparator • Connect to V_{SS}.	
CMP$_{OUT}$	Analog comparator output	• Output pin for an analog comparator	
$\overline{RESET}$	Reset input	• Reset input pin for active “L”	
X_{IN}	Clock input	• Input and output signals for the internal clock generating circuit. • Connect a ceramic resonator or quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency.	
X_{OUT}	Clock output	• If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. • The clock is used as the oscillating source of system clock.	
$P0_0$–$P0_7$	I/O port P0	• 8-bit CMOS I/O port	
$P1_0$–$P1_7$	I/O port P1	• I/O direction register allows each pin to be individually programmed as either input or output.	
$P2_0$–$P2_7$	I/O port P2	• At reset this port is set to input mode. • In modes other than single-chip, these pins are used as address, data bus I/O pins. • CMOS compatible input level • CMOS 3-state output structure • Port P2 can be switched CMOS or TTL input level.	
$P3_0$/RTP$_6$, $P3_1$/RTP$_7$	I/O port P3	• 8-bit CMOS I/O port • I/O direction register allows each pin to be individually programmed as either input or output.	• Real time port function pins
$P3_4$/CK$_{OUT}$,		• At reset this port is set to input mode.	• Clock output function pin
$P3_2$, $P3_3$, $P3_5$–$P3_7$		• In modes other than single-chip, these pins are used as control bus I/O pins. • CMOS compatible input level • CMOS 3-state output structure • Port $P3_2$ can be switched CMOS or TTL input level.	
$P4_0$/X_{COUT}, $P4_1$/X_{CIN}	I/O port P4	• 8-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level	• Sub-clock generating I/O pins(connect a resonator)
$P4_2$/INT$_0$, $P4_3$/INT$_1$		• CMOS 3-state output structures	• Interrupt input pins • Timer X, Timer Y function pins (INT$_0$, INT$_1$)
$P4_4$/R$_X$D, $P4_5$/T$_X$D, $P4_6$/S$_{CLK1}$, $P4_7$/$\overline{S_{RDY1}}$			• Serial I/O1 function pins
$P5_0$/T$_{OUT}$	I/O port P5	• 8-bit CMOS I/O port with the same function as port P0	• Timer 2 output pin
$P5_1$/S$_{CMP2}$/ INT$_2$		• CMOS compatible input level • CMOS 3-state output structure	• Interrupt input pin • Serial I/O2 function pin
$P5_2$/INT$_3$, $P5_3$/INT$_4$			• Interrupt input pin • Real time port function pin(INT$_4$)
$P5_4$/CNTR$_0$, $P5_5$/CNTR$_1$			• Timer X, Timer Y function pins
$P5_6$/DA$_1$, $P5_7$/DA$_2$			• D-A conversion output pins

Table. 2. Pin description (2)

Pin	Name	Function	Function except a port function
$P6_0/AN_5$–$P6_2/AN_7$	I/O port P6	• 3-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structure	• A-D conversion output pins
$P6_3/CMP_{IN}$/AN_8	Input port P6	• 2-bit CMOS input port • CMOS compatible input level	• Analog comparator input pin • A-D conversion input pin
$P6_4/CMP_{REF}$/AN_9			• Reference voltage input pin for analog comparator • A-D conversion input pin
$P6_5/DAV_{REF}$/AN_{10}	I/O port P6	• 1-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structure	• D-A conversion power source input pin • A-D conversion input pin
$P7_0/S_{IN2}$, $P7_1/S_{OUT2}$, $P7_2/S_{CLK2}$	I/O port P7	• 8-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structures	• Serial I/O2 function pins
$P7_3/S_{RDY2}$/ADT/AN_0			• Serial I/O2 function pin • A-D conversion input pin • A-D trigger input pin
$P7_4/AN_1$–$P7_7/AN_4$			• A-D conversion input pin
$P8_0/DA_3$/AN_{11}, $P8_1/DA_4$/AN_{12},	I/O port P8	• 8-bit CMOS I/O port with the same function as port P0 • CMOS compatible input level • CMOS 3-state output structures	• D-A conversion output pin • A-D conversion input pin
$P8_2/RTP_0$–$P8_7/RTP_5$			• Realtime port function pins

PART NUMBERING

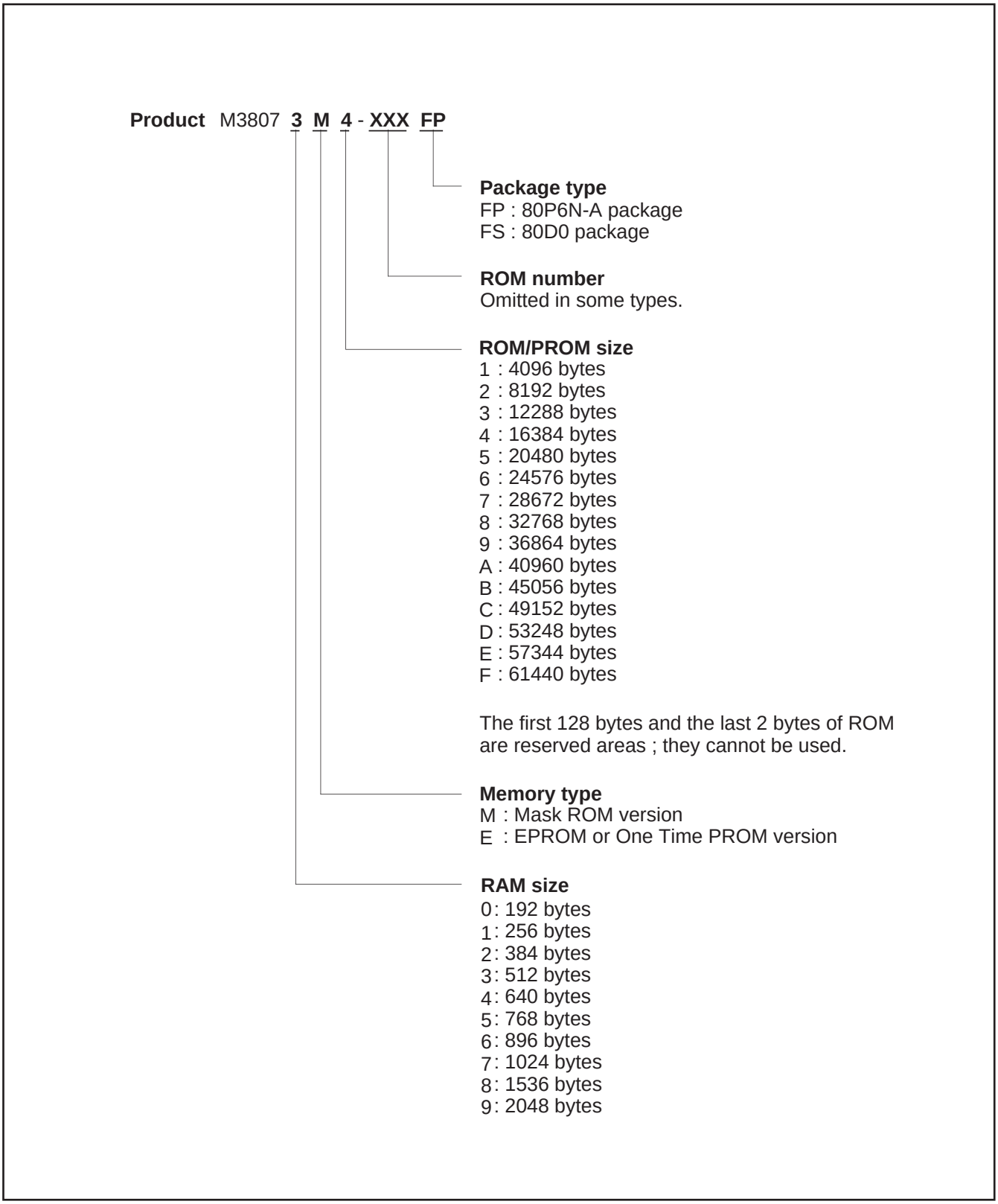


Fig. 3. Part numbering

GROUP EXPANSION

Mitsubishi plans to expand the 3807 group as follows:

Memory Type

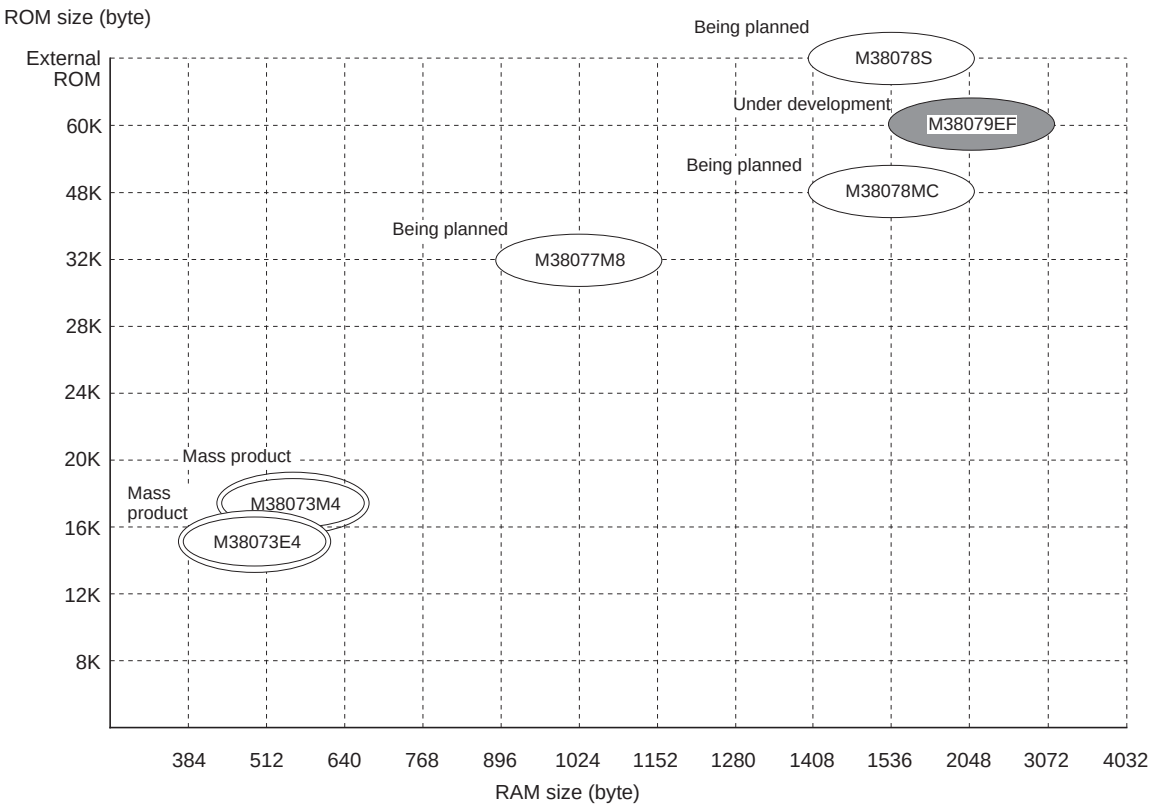
Support for Mask ROM, One Time PROM and EPROM versions.

Memory Size

ROM/PROM size ..... 8K to 60K bytes
RAM size ..... 384 to 2048 bytes

Package

80P6N-A ..... 0.8 mm-pitch plastic molded QFP
80D0 ..... 0.8 mm-pitch ceramic LCC (EPROM version)



Note : Products under development or planning : the development schedule and specifications may be revised without notice.

Fig. 4. Memory expansion plan

Currently supported products are listed below.

Table 3. List of supported products

As of May 1996

Product	(P) ROM size (bytes) ROM size for User ()	RAM size (bytes)	Package	Remarks
M38073M4-XXXFP	16384 (16254)	512	80P6N-A	Mask ROM version
M38073E4-XXXFP				One Time PROM version
M38073E4FP				One Time PROM version (blank)
M38073E4FS			80D0	EPROM version

RENESAS
Renesas Technology Corp.

FUNCTIONAL DESCRIPTION

Central Processing Unit (CPU)

The 3807 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 <Software> User´s Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:

The FST and SLW instructions cannot be used.

The MUL, DIV, WIT and STP instruction can be used.

The central processing unit (CPU) has the six registers.

CPU Mode Register

The CPU mode register contains the stack page selection bit and processor mode bits. The CPU mode register is allocated at address $003B_{16}$.

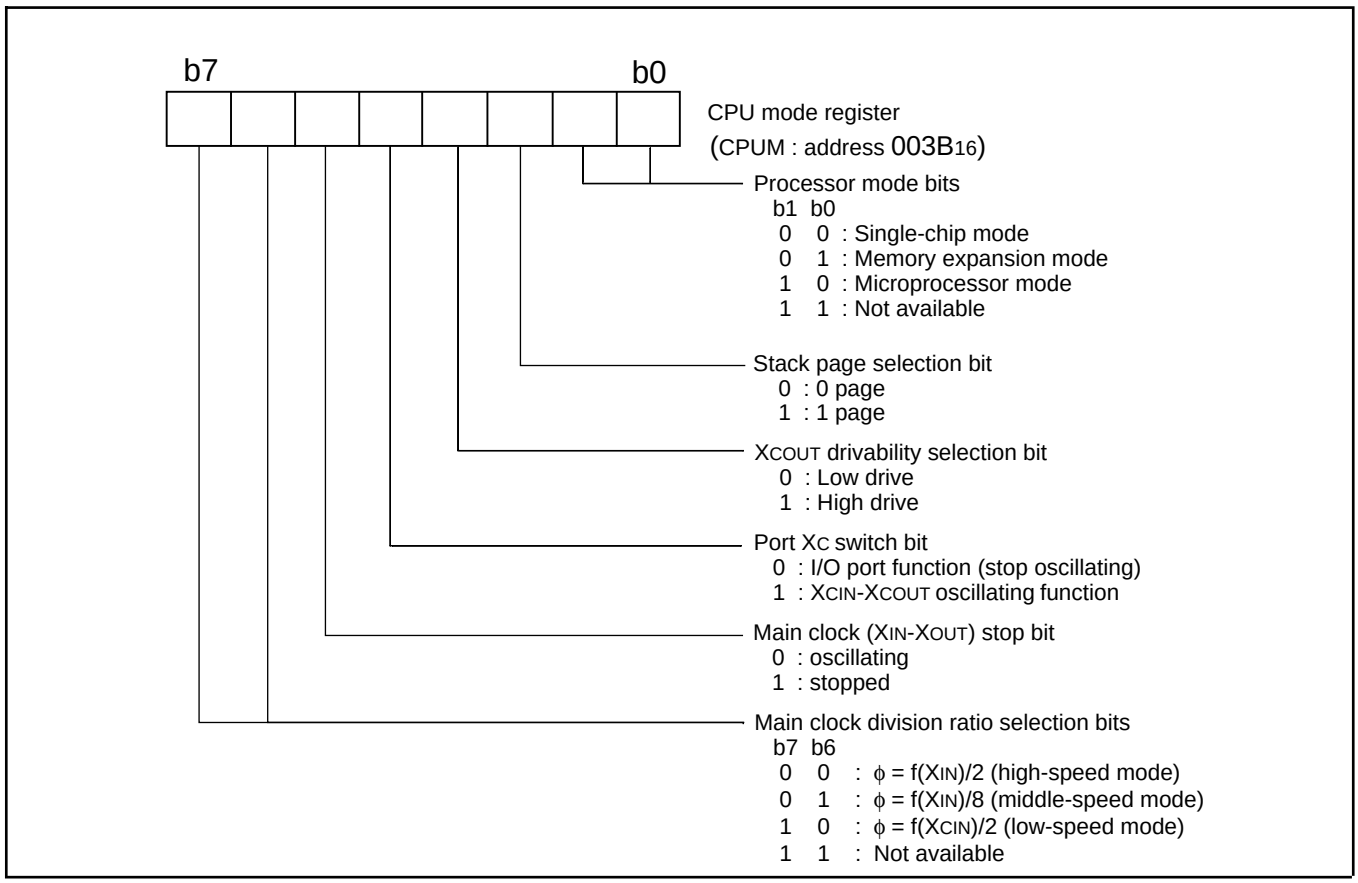


Fig. 5. Structure of CPU mode register

Memory
Special function register (SFR) area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the reset is user area for storing programs.

Interrupt vector area

The interrupt vector area contains reset and interrupt vectors.

Zero page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM capacity (byte)	Address XXXX16
192	$00FF_{16}$
256	$013F_{16}$
384	$01BF_{16}$
512	$023F_{16}$
640	$02BF_{16}$
768	$033F_{16}$
896	$03BF_{16}$
1024	$043F_{16}$
1536	$063F_{16}$
2048	$083F_{16}$

ROM area

ROM capacity (byte)	Address YYYY16	Address ZZZZ16
4096	$F000_{16}$	$F080_{16}$
8192	$E000_{16}$	$E080_{16}$
12288	$D000_{16}$	$D080_{16}$
16384	$C000_{16}$	$C080_{16}$
20480	$B000_{16}$	$B080_{16}$
24576	$A000_{16}$	$A080_{16}$
28672	9000_{16}	9080_{16}
32768	8000_{16}	8080_{16}
36864	7000_{16}	7080_{16}
40960	6000_{16}	6080_{16}
45056	5000_{16}	5080_{16}
49152	4000_{16}	4080_{16}
53248	3000_{16}	3080_{16}
57344	2000_{16}	2080_{16}
61440	1000_{16}	1080_{16}

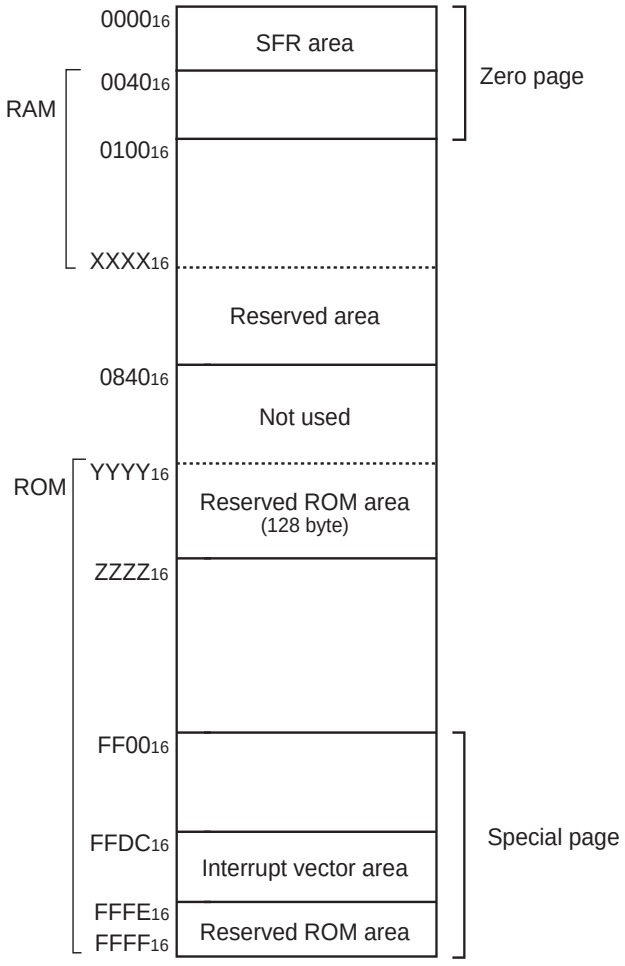


Fig. 6. Memory map diagram

0000_{16}	Port P0 (P0)	0020_{16}	Timer X (low-order) (TXL)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer X (high-order) (TXH)
0002_{16}	Port P1 (P1)	0022_{16}	Timer Y (low-order) (TYL)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer Y (high-order) (TYH)
0004_{16}	Port P2 (P2)	0024_{16}	Timer 1 (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 (T2)
0006_{16}	Port P3 (P3)	0026_{16}	Timer 3 (T3)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer X mode register (TXM)
0008_{16}	Port P4 (P4)	0028_{16}	Timer Y mode register (TYM)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 123 mode register (T123M)
$000A_{16}$	Port P5 (P5)	$002A_{16}$	Real time port register (RTP)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	Real time port control register 0 (RTPCON0)
$000C_{16}$	Port P6 (P6)	$002C_{16}$	Real time port control register 1 (RTPCON1)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	Real time port control register 2 (RTPCON2)
$000E_{16}$	Port P7 (P7)	$002E_{16}$	Real time port control register 3 (RTPCON3)
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	Timer A (low-order) (TAL)
0010_{16}	Port P8 (P8)	0030_{16}	Timer A (high-order) (TAH)
0011_{16}	Port P8 direction register (P8D)	0031_{16}	Timer B (low-order) (TBL)
0012_{16}		0032_{16}	Timer B (high-order) (TBH)
0013_{16}		0033_{16}	D-A control register (DACON)
0014_{16}	Timer XY control register (TXYCON)	0034_{16}	A-D control register (ADCON)
0015_{16}	Port P2P3 control register (P2P3C)	0035_{16}	A-D conversion register (AD)
0016_{16}	Pull-up control register (PULL)	0036_{16}	D-A1 conversion register (DA1)
0017_{16}	Watchdog timer control register (WDTCON)	0037_{16}	D-A2 conversion register (DA2)
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	D-A3 conversion register (DA3)
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	D-A4 conversion register (DA4)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$	Serial I/O2 control register 1 (SIO2CON1)	$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$	Serial I/O2 control register 2 (SIO2CON2)	$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2(ICON2)

Fig. 7. Memory map of special function register (SFR)

I/O Ports

[Direction Registers] PiD

The 3807 group has 68 programmable I/O pins arranged in nine individual I/O ports (P0—P5, P60—P62, P65 and P7—P8). The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, each pin can be set to be input port or output port. When "0" is written to the bit corresponding to a pin, that pin becomes an input pin. When "1" is written to that pin, that pin becomes an output pin. If data is read from a pin set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input (the bit corresponding to that pin must be set to "0") are floating and the value of that pin can be written to. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

[Pull-up Control Register] PULL

Ports P0, P1 and P2 have built-in programmable pull-up resistors. The pull-up resistors are valid only in the case that the each control bit is set to "1" and the corresponding port direction registers are set to input mode.

(1) CMOS/TTL input level selection

Either CMOS input level or TTL input level can be selected as an input level for ports P20 to P27 and P32. The input level is selected by P2·P32 input level selection bit (b7) of the port P2P3 control register (address 001516). When the bit is set to "0", CMOS input level is selected. When the bit is set to "1", the TTL input level is selected. After this bit is re-set, its initial value depends on the state of the CNVss pin. When the CNVss pin is connected to Vss, the initial value becomes "0". When the CNVss pin is connected to Vcc, the initial value becomes "1".

(2) Notes on STP instruction execution

Make sure that the input level at each pin is either 0V or to Vcc during execution of the STP instruction. When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

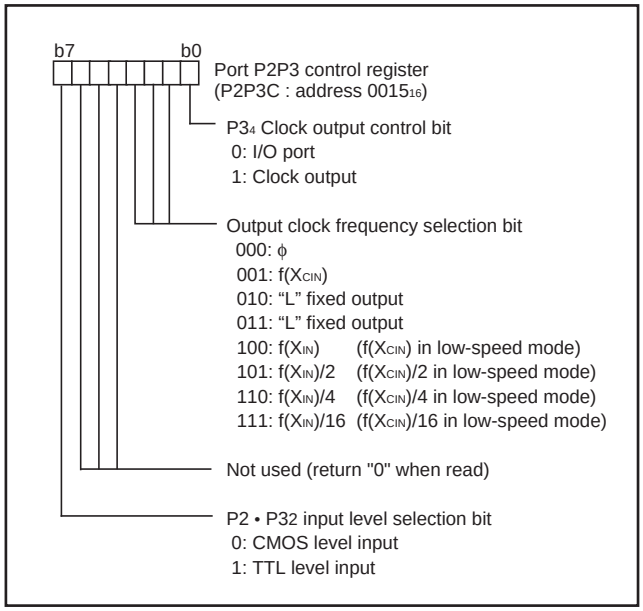


Fig. 8. Structure of Port P2P3 control register

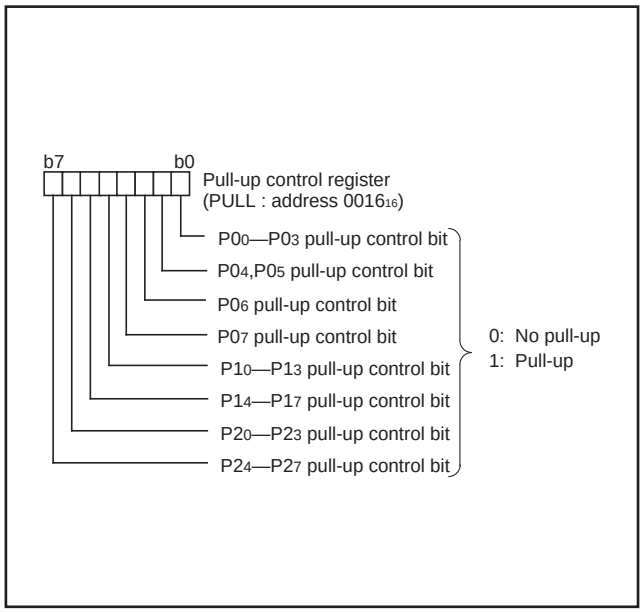


Fig. 9. Structure of Pull-up control register

Table. 4. List of I/O port functions (1)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
$P0_0$–$P0_7$	Port P0	Input/output, individual bits	CMOS compatible input level	Address low-order byte output	CPU mode register	(1)
$P1_0$–$P1_7$	Port P1		CMOS 3-state output	Address high-order byte output	Pull-up control register	
$P2_0$–$P2_7$	Port P2		CMOS/TTL input level CMOS 3-state output	Data bus I/O	CPU mode register Pull-up control register Port P2P3 control register	
$P3_0$/RTP_6, $P3_1$/RTP_7	Port P3		CMOS compatible input level CMOS 3-state output	Real time port output	CPU mode register Real time port control register	(2)
$P3_2$			CMOS/TTL input level CMOS 3-state output	Control signal input	CPU mode register Port P2P3 control register	(3)
$P3_3$			CMOS compatible input level CMOS 3-state output	Control signal output	CPU mode register	
$P3_4$/CK_{OUT}				Clock output, ϕ output	CPU mode register Port P2P3 control register	(4)
$P3_5$–$P3_7$				Control signal I/O	CPU mode register	(3)
$P4_0$/X_{COUT}, $P4_1$/X_{CIN}	Port P4			Sub-clock generating circuit	CPU mode register	(5) (6)
$P4_2$/INT_0, $P4_3$/INT_1				External interrupt input Timer X, Timer Y function input	Interrupt edge selection register	(7)
$P4_4$/R_XD, $P4_5$/T_XD, $P4_6$/S_{CLK1}, $P4_7$/S_{RDY1}				Serial I/O1 function I/O	Serial I/O1 control register UART control register	(8) (9) (10) (11)
$P5_0$/T_{OUT}	Port P5			Timer 2 output	Timer 123 mode register	(12)
$P5_1$/S_{CMP2}/ INT_2				External interrupt input Serial I/O2 function I/O	Interrupt edge selection register Serial I/O2 control register	(22)
$P5_2$/INT_3, $P5_3$/INT_4				External interrupt input Real time port trigger input (INT_4)	Interrupt edge selection register	(7)
$P5_4$/$CNTR_0$				Timer X, Timer Y function I/O	Timer X mode register	(13)
$P5_5$/$CNTR_1$					Timer Y mode register	
$P5_6$/DA_1, $P5_7$/DA_2				D-A conversion output	D-A control register	(14)
$P6_0$/AN_5— $P6_2$/AN_7	Port P6			A-D conversion input	A-D control register	(15)
$P6_3$/CMP_{IN}/ AN_8		Input	CMOS compatible input level	Analog comparator input pin A-D conversion input	A-D control register	(16)
$P6_4$/CMP_{REF}/ AN_9				Analog comparator reference voltage input pin A-D conversion input		
$P6_5$/DAV_{REF}/ AN_{10}		Input/output, individual bits	CMOS compatible input level CMOS 3-state output	D-A converter power source input A-D conversion input	A-D control register	(17)
$P7_0$/S_{IN2}, $P7_1$/S_{OUT2}, $P7_2$/S_{CLK2}	Port P7			Serial I/O2 function I/O	Serial I/O2 control register	(18) (19) (20)
$P7_3$/S_{RDY2}/ ADT/AN_0				Serial I/O2 function I/O A-D trigger input A-D conversion input	Serial I/O2 control register A-D control register	(21)
$P7_4$/AN_1— $P7_7$/AN_4				A-D conversion input	A-D control register	(15)

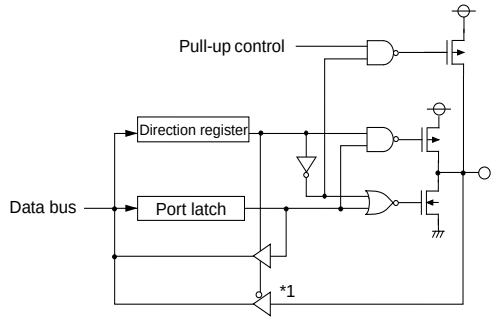
Table. 5. List of I/O port functions (2)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Ref.No.
$P8_0/DA_3/AN_{11}$ $P8_1/DA_4/AN_{12}$	Port P8	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	D-A conversion output A-D conversion input	D-A control register A-D control register	(14)
$P8_2/RTP_0$— $P8_7/RTP_5$				Real time port output	Real time port control register	(23)

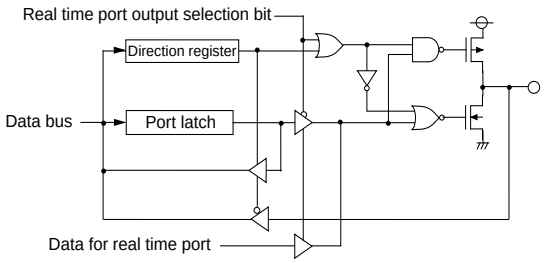
Note1 : For details of the functions of ports P0 to P3 in modes other than single-chip mode, and how to use double-function ports as function I/O ports, refer to the applicable sections.

2 : Make sure that the input level at each pin is either 0 V or Vcc during execution of the STP instruction.
When an input level is at an intermediate potential, a current will flow from Vcc to Vss through the input-stage gate.

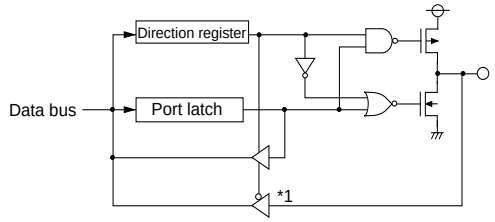
(1) Ports P0—P2



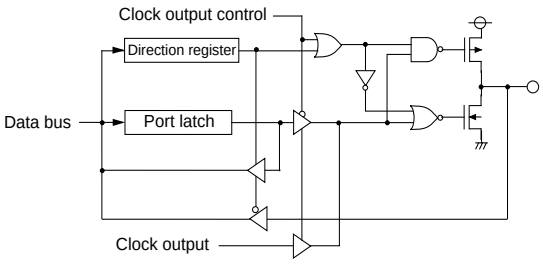
(2) Ports P3$_0$,P3$_1$



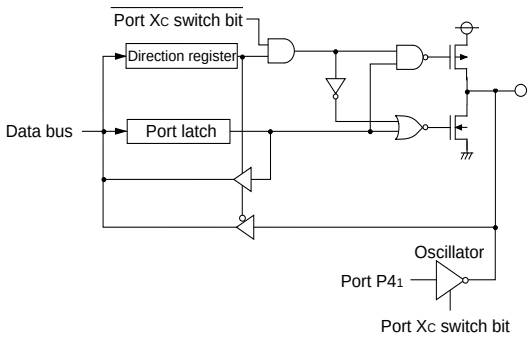
(3) Ports P3$_2$,P3$_3$,P3$_5$—P3$_7$



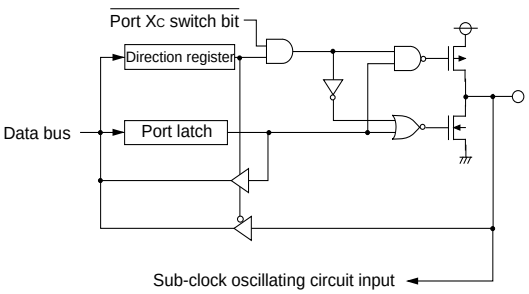
(4) Port P3$_4$



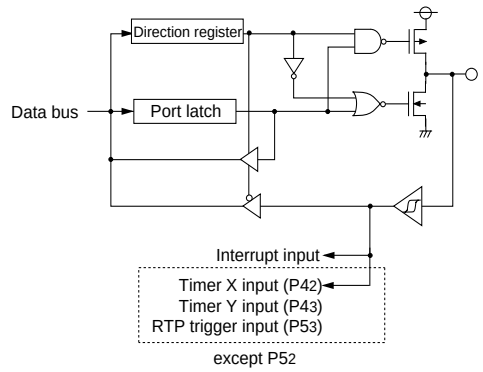
(5) Port P4$_0$



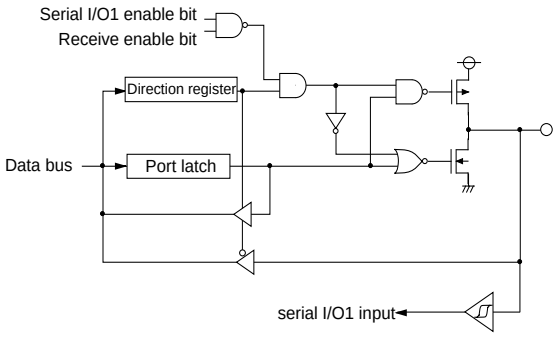
(6) Port P4$_1$



(7) Ports P4$_2$,P4$_3$,P5$_2$,P5$_3$



(8) Port P4$_4$



*1 Either CMOS input level or TTL input level can be selected as an input level for ports P2$_0$ to P2$_7$ and P3$_2$ by P2•P3$_2$ input level selection bit.

Fig. 10. Port block diagram (1)

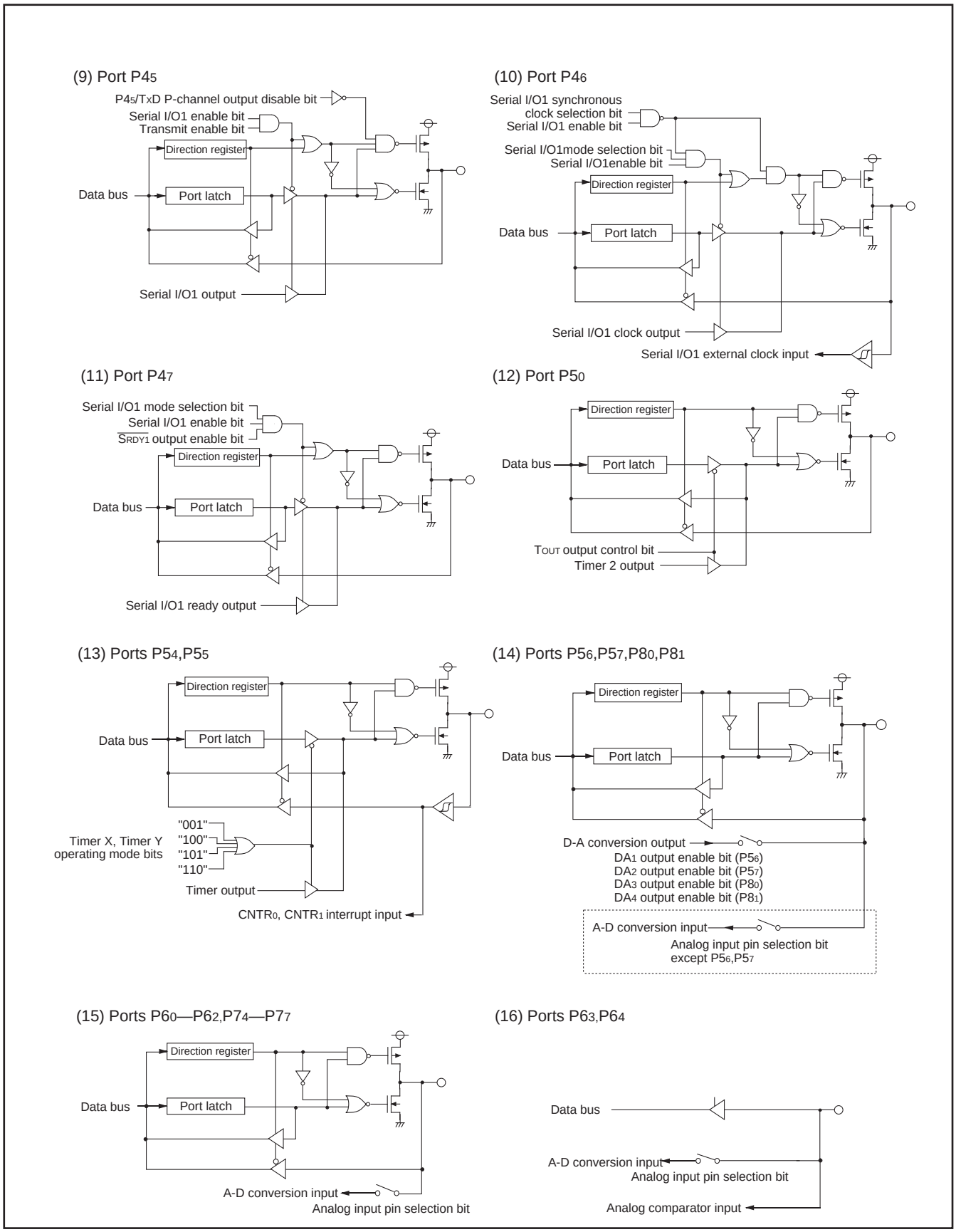
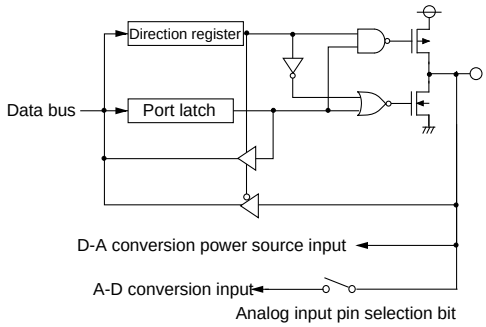
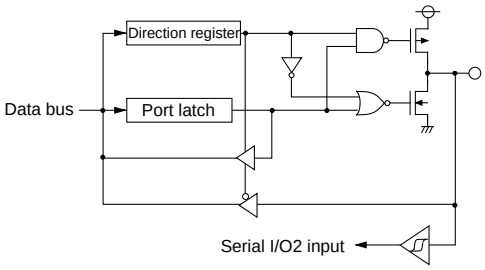


Fig. 11. Port block diagram (2)

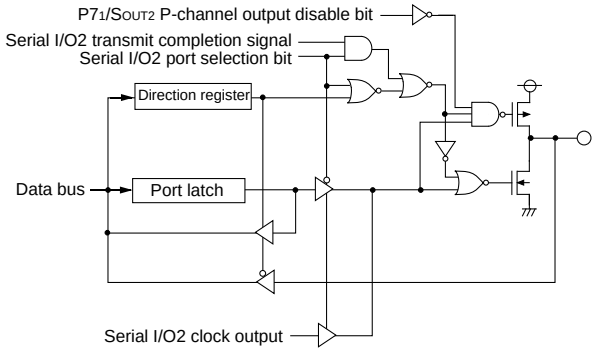
(17) Port P6$_5$



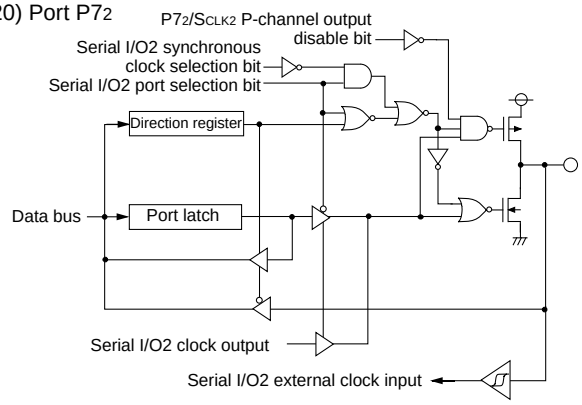
(18) Port P7$_0$



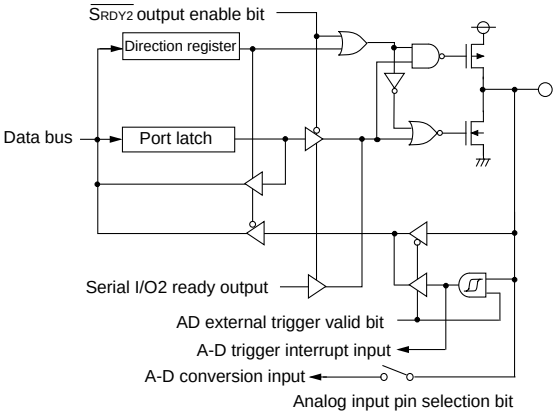
(19) Port P7$_1$



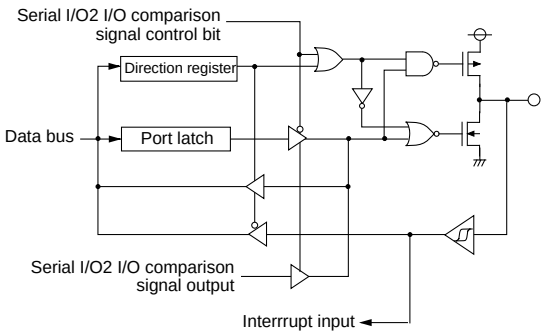
(20) Port P7$_2$



(21) Port P7$_3$



(22) Port P5$_1$



(23) Ports P8$_2$—P8$_7$

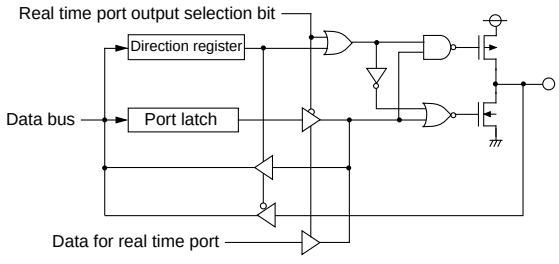


Fig. 12. Port block diagram (3)

Interrupts

Interrupts occur by twenty sources: eight external, eleven internal, and one software.

(1) Interrupt Control

Each interrupt except the BRK instruction interrupt have both an interrupt request bit and an interrupt enable bit, and is controlled by the interrupt disable flag. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0". Interrupt enable bits can be set or cleared by software. Interrupt request bits can be cleared by software, but cannot be set by software. The BRK instruction interrupt and reset cannot be disabled with any flag or bit. The I flag disables all interrupts except the BRK instruction interrupt and reset. If several interrupts requests occurs at the same time the interrupt with highest priority is accepted first.

(2) Interrupt Operation

Upon acceptance of an interrupt the following operations are automatically performed:

1. The processing being executed is stopped.
2. The contents of the program counter and processor status register are automatically pushed onto the stack
3. Concurrently with the push operation, the interrupt jump destination address is read from the vector table into the program counter.
4. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.

■Notes on Use

When the active edge of an external interrupt (INT_0—INT_4, $CNTR_0$ or $CNTR_1$) is set or the timer /INT interrupt source and the ADT/ A-D conversion interrupt source are changed, the corresponding interrupt request bit may also be set. Therefore, please take following sequence:

(1) Disable the external interrupt which is selected.
(2) Change the active edge in interrupt edge selection register (in case of $CNTR_0$: Timer X mode register ; in case of $CNTR_1$: Timer Y mode register).
(3) Clear the set interrupt request bit to "0."
(4) Enable the external interrupt which is selected.

Table. 6. Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses (Note 1)		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD16	FFFC16	At reset	Non-maskable
INT0	2	FFFB16	FFFA16	At detection of either rising or falling edge of INT0 input	External interrupt (active edge selectable)
INT1	3	FFF916	FFF816	At detection of either rising or falling edge of INT1 input	External interrupt (active edge selectable)
Serial I/O1 receive	4	FFF716	FFF616	At completion of serial I/O1 data receive	Valid when serial I/O1 is selected
Serial I/O1 transmit	5	FFF516	FFF416	At completion of serial I/O1 data transmit shift or when transmit buffer is empty	Valid when serial I/O1 is selected
Timer X	6	FFF316	FFF216	At timer X underflow	
Timer Y	7	FFF116	FFF016	At timer Y underflow	
INT3	8	FFEF16	FFEE16	At detection of either rising or falling edge of INT3 input	External interrupt (active edge selectable)
					Valid when INT3 interrupt is selected
Timer 2				At timer 2 underflow	Valid when timer 2 interrupt is selected
INT4	9	FFED16	FFEC16	At detection of either rising or falling edge of INT4 input	External interrupt (active edge selectable)
					Valid when INT4 interrupt is selected
Timer 3				At timer 3 underflow	Valid when timer 3 interrupt is selected
CNTR0	10	FFEB16	FFEA16	At detection of either rising or falling edge of CNTR0 input	External interrupt (active edge selectable)
CNTR1	11	FFE916	FFE816	At detection of either rising or falling edge of CNTR1 input	External interrupt (active edge selectable)
Serial I/O2	12	FFE716	FFE616	At completion of serial I/O2 data transmit and receive	Valid when serial I/O2 is selected
INT2	13	FFE516	FFE416	At detection of either rising or falling edge of INT2 input	External interrupt (active edge selectable)
					Valid when INT2 interrupt is selected
Timer 1				At timer 1 underflow	Valid when timer 1 interrupt is selected
Timer A	14	FFE316	FFE216	At timer A underflow	
Timer B	15	FFE116	FFE016	At timer B underflow	
A-D conversion	16	FFDF16	FFDE16	At completion of A-D conversion	Valid when A-D interrupt is selected
ADT				At falling edge of ADT input	External interrupt(valid at falling) Valid when ADT interrupt is selected and when A-D external trigger is selected.
BRK instruction	17	FFDD16	FFDC16	At BRK instruction execution	Non-maskable software interrupt

Note1 : Vector addresses contain interrupt jump destination addresses.

2 : Reset function in the same way as an interrupt with the highest priority.

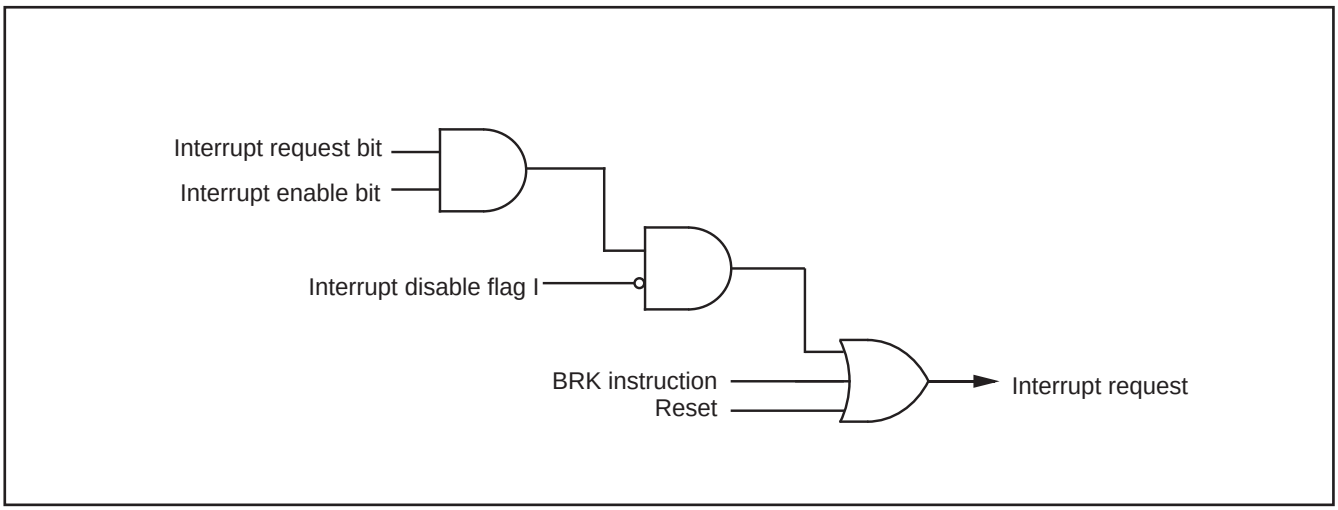


Fig. 13. Interrupt control

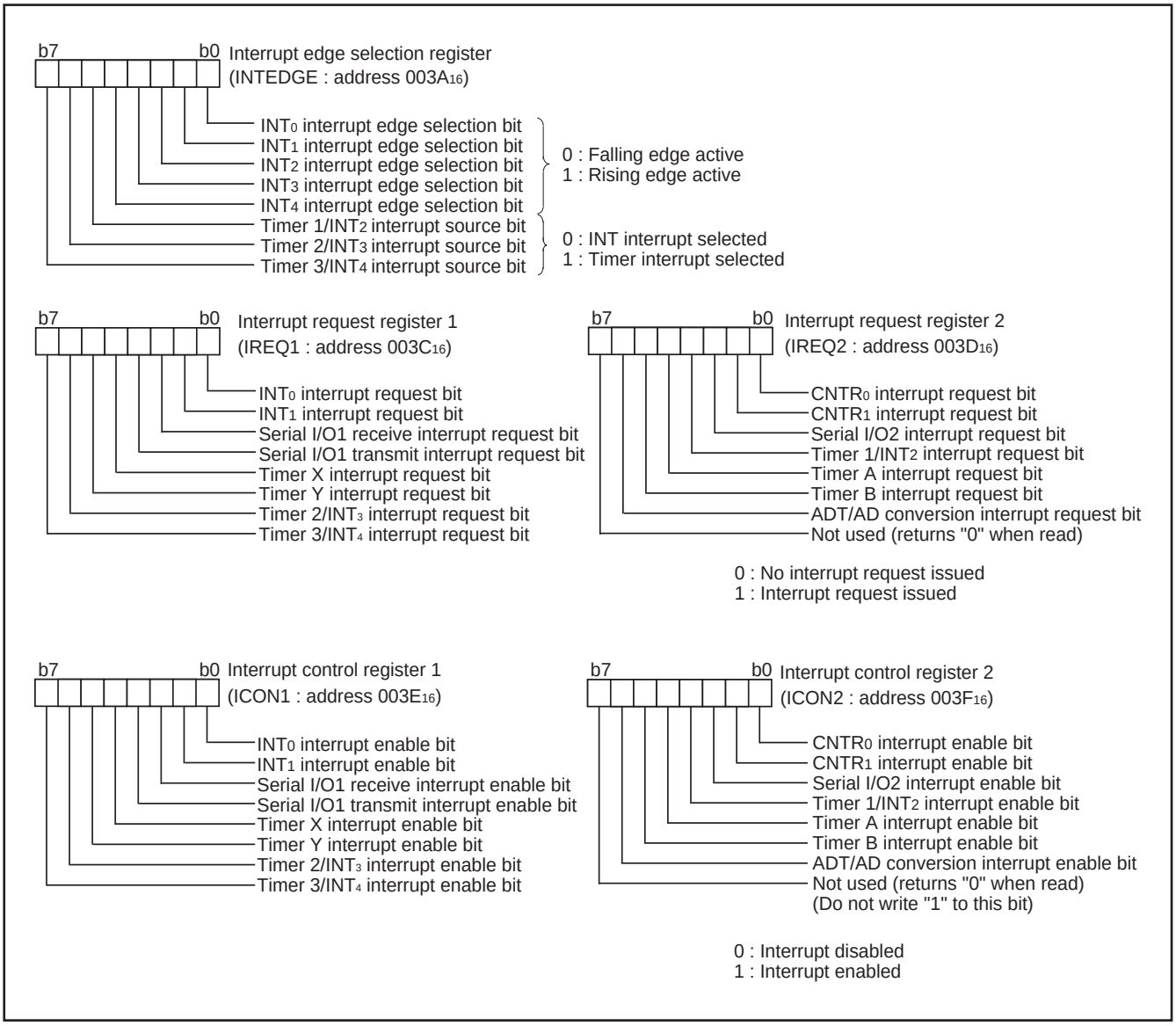


Fig. 14. Structure of Interrupt-related registers

Timers

The 3807 group has seven timers : four 16-bit timers (Timer X, Timer Y, Timer A, and Timer B) and three 8-bit timers (Timer 1, Timer 2, and Timer 3).

All timers are down-counters. When the timer reaches either "00$_{16}$" or "0000$_{16}$", an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1."

Read and write operation on 16-bit timer must be performed for both high- and low-order bytes. When reading a 16-bit timer, read from the high-order byte first. When writing to 16-bit timer, write to the low-order byte first. The 16-bit timer cannot perform the correct operation when reading during write operation, or when writing during read operation.

Timers A and B are real time output port timers. For details, refer to the section "Real time output port".

●Timer X, Timer Y

Timer X and Y are independent 16-bit timers which can select enable seven different operation modes each by the setting of their mode registers. The related registers of timer X and Y are listed below. The following register abbreviations are used:

- Timer XY control register (TXYCON: address 0014$_{16}$)
- Port P4 direction register (P4D: address 0009$_{16}$)
- Port P5 direction register (P5D: address 000B$_{16}$)
- Timer X (low-order) (TXL: address 0020$_{16}$)
- Timer X (high-order) (TXH: address 0021$_{16}$)
- Timer Y (low-order) (TYL: address 0022$_{16}$)
- Timer Y (high-order) (TYH: address 0023$_{16}$)
- Timer X mode register (TXM: address 0027$_{16}$)
- Timer Y mode register (TYM: address 0028$_{16}$)
- Interrupt edge selection register (INTEDGE: address 003A$_{16}$)
- Interrupt request register 1 (IREQ1: address 003C$_{16}$)
- Interrupt request register 2 (IREQ2: address 003D$_{16}$)
- Interrupt control register 1 (ICON1: address 003E$_{16}$)
- Interrupt control register 2 (ICON2: address 003F$_{16}$)

For details, refer to the structures of each register.

The following is an explanation of the seven modes:

(1) Timer • event counter mode

①Timer mode

- Mode selection

  This mode can be selected by setting "000" to the following bits.

  Timer X operating mode bit (bits 2 to 0) of TXM

  Timer Y operating mode bit (bits 2 to 0) of TYM
- Count source selection

  In high- or middle-speed mode, f(X$_{IN}$)/2, f(X$_{IN}$)/16, or f(X$_{CIN}$) can be selected as the count source.

  In low-speed mode the count source is f(X$_{CIN}$).

  A count source is selected by the following bit.

  Timer X count source selection bit (bits 7 and 6) of TXM

  Timer Y count source selection bit (bits 7 and 6) of TYM
- Interrupt

  When an underflow is generated, the corresponding timer X interrupt request bit (b4) or timer Y interrupt request bit (b5) of IREQ1 is set to "1".
- Explanation of operation

  After reset release, timer X stop control bit (b0) and timer Y stop control bit (b1) of TXYCON are set to "1"and the timer stops. During timer stop, a timer value written to the timer X or timer Y is set by writing data to the corresponding timer latch and timer at the same time. The timer operation is started by setting the bits 0 or 1 of TXYCON to "0". When the timer reaches "0000$_{16}$", an underflow occurs with the next count pulse. Then the contents of the timer latch is reloaded into the timer and the timer continues down-counting. For changing a timer value during count operation, a latch value must be changed by writing data only to the corresponding latch first. Then the timer is reloaded with the new latch value at the next underflow.

②Event counter mode

- Mode selection

  This mode can be selected by the following sequence.

  1. Set "000" to the timer X operating mode bit (bits 2 to 0) of TXM, or to the timer Y operating mode bit (bits 2 to 0) of TYM.
  2. Select an input signal from the CNTR$_0$ pin (in case of timer X ; set "11" to bits 7 and 6 of TXM), or from the CNTR$_1$ pin (in case of timer Y ; set "11" to bits 7 and 6 of TYM) as a count source.

  The valid edge for the count operation is selected by the CNTR$_0$/CNTR$_1$ active edge switch bit (b5) of TXM or TYM: if set to "0", counting starts with the rising edge or if set to "1", counting starts with the falling edge.
- Interrupt

  The interrupt generation at underflow is the same as already explained for the timer mode.
- Explanation of operation

  The operation is the same as already explained for the timer mode. In this mode, the double-function port of CNTR$_0$/CNTR$_1$ pin must be set to input.

Figure 19 shows the timing chart for the timer • event counter mode.

(2) Pulse output mode

- Mode selection

  This mode can be selected by setting "001" to the following bits.

  Timer X operating mode bit (bits 2 to 0) of TXM

  Timer Y operating mode bit (bits 2 to 0) of TYM
- Count source selection

  In high- or middle-speed mode, f(X$_{IN}$)/2, f(X$_{IN}$)/16, or f(X$_{CIN}$) can be selected as the count source.

  In low-speed mode the count source is f(X$_{CIN}$).
- Interrupt

  The interrupt generation at underflow is the same as already explained for the timer mode.
- Explanation of operation

  Counting operation is the same as in timer mode. Moreover the pulse which is inverted each time the timer underflows is output from CNTR$_0$/CNTR$_1$ pin. When the CNTR$_0$/CNTR$_1$ active edge switch bit (b5) of TXM or TYM is "0", output starts with "H" level. When set to "1", output starts with "L" level.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin to output in this mode.

[During timer operation stop]

The output from $CNTR_0$/$CNTR_1$ pin is initialized to the level set through $CNTR_0$/$CNTR_1$ active edge switch bit.

[During timer operation enabled]

When the value of the $CNTR_0$/$CNTR_1$ active edge switch bit is written over, the output level of $CNTR_0$/$CNTR_1$ pin is inverted.

Figure 20 shows the timing chart of the pulse output mode.

(3) Pulse period measurement mode

• Mode selection

This mode can be selected by setting "010" to the following bits.

Timer X operating mode bit (bits 2 to 0) of TXM

Timer Y operating mode bit (bits 2 to 0) of TYM

• Count source selection

In high- or middle-speed mode, f(X_{IN})/2 or f(X_{IN})/16 can be selected as the count source.

In low-speed mode the count source is f(X_{CIN}).

• Interrupt

The interrupt generation at underflow is the same as already explained for the timer mode. Bits 0 or 1 of IREQ2 is set to "1" synchronously to pulse period measurement completion.

• Explanation of operation

[During timer operation stop]

Select the count source. Next, select the interval of the pulse periods to be measured. When bit 5 of the TXM or TYM is set to "0", the timer counts during the interval of one falling edge of $CNTR_0$/$CNTR_1$ pin input until the next falling edge of input. If bits 5 are set to "1", the timer counts during the interval of one rising edge until the next rising edge.

[During timer operation enabled]

The pulse period measurement starts by setting bit 0 or 1 of TXYCON to "0" and the timer counts down from the value that was set to the timer before the start of measurement. When a valid edge of measurement start/stop is detected, the 1's complement of the timer value is written to the timer latch and "$FFFF_{16}$" is set to the timer. Furthermore when the timer underflows, a timer X/Y interrupt request occurs and "$FFFF_{16}$" is set to the timer. The measured value is held until the next measurement completion.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin to input in this mode.

A read-out of timer value is impossible in this mode. The timer is written to only during timer stop (no measurement of pulse periods). Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operations during measurement.

The timer is set to "$FFFF_{16}$" when the timer either underflows or a valid edge of pulse period measurement is detected. Due to that, the timer value at the start of measurement depends on the timer value before the start of measurement.

Figure 19 shows the timing chart of the pulse period measurement mode.

(4) Pulse width measurement mode

• Mode selection

This mode can be selected by setting "011" to the following bits.

Timer X operating mode bit (bits 2 to 0) of TXM

Timer Y operating mode bit (bits 2 to 0) of TYM

• Count source selection

In high- or middle-speed mode, f(X_{IN})/2 or f(X_{IN})/16 can be selected as the count source.

In low-speed mode the count source is f(X_{CIN}).

• Interrupt

The interrupt generation at underflow is the same as already explained for the timer mode. Bit 0 or 1 of IREQ2 is set to "1" synchronously to pulse width measurement completion.

• Explanation of operation

[During timer operation stop]

Select the count source. Next, select the interval of the pulse widths to be measured. When bit 5 of TXM or TYM is set to "1", the timer counts during the interval of one falling edge of $CNTR_0$/$CNTR_1$ pin input until the next rising edge of input ("L" interval). If bit 5 is set to "0", the timer counts during the interval of one rising edge until the next falling edge ("H" interval).

[During timer operation enabled]

The pulse width measurement starts by setting bit 0 or 1 of TXYCON to "0" and the timer counts down from the value that was set to the timer before the start of measurement. When a valid edge of measurement completion is detected, the 1's complement of the timer value is written to the timer latch and "$FFFF_{16}$" is set to the timer. Furthermore when the timer underflows, a timer X/Y interrupt request occurs and "$FFFF_{16}$" is set to the timer. The measured value is held until the next measurement completion.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin to input in this mode.

A read-out of timer value is impossible in this mode. The timer is written to only during timer stop (no measurement of pulse widths). Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operations during measurement.

The timer value is set to "$FFFF_{16}$" when the timer either underflows or a valid edge of pulse widths measurement is detected. Due to that, the timer value at the start of measurement depends on the timer value before the start of measurement.

Figure 20 shows the timing chart of the pulse width measurement mode.

(5) Programmable waveform generation mode

• Mode selection

This mode can be selected by setting "100" to the following bits.

Timer X operating mode bit (bits 2 to 0) of TXM

Timer Y operating mode bit (bits 2 to 0) of TYM

• Count source selection

In high- or middle-speed mode, f(X_{IN})/2, f(X_{IN})/16, or f(X_{CIN}) can be selected as the count source.

In low-speed mode the count source is f(X_{CIN}).

• Interrupt

The interrupt generation at underflow is the same as already

explained for the timer mode.

• Explanation of operation

Counting operation is the same as in timer mode. Moreover the timer outputs the data set in the corresponding output level latch (bit 4 of TXM or TYM) to $CNTR_0$/$CNTR_1$ pin each time the timer underflows. After the timer underflows, the generation of optional waveform from $CNTR_0$/$CNTR_1$ pin is possible through a change of values in the output level latch and timer latch.

■Precautions

Set the double-function port of $CNTR_0$/$CNTR_1$ pin to output in this mode.

Figure 23 shows the timing chart of the programmable waveform generation mode.

(6) Programmable one-shot generating mode

• Mode selection

This mode can be selected by setting "101" to the following bits.

Timer X operating mode bit (bits 2 to 0) of TXM
Timer Y operating mode bit (bits 2 to 0) of TYM

• Count source selection

In high- or middle-speed mode, f(X_{IN})/2 or f(X_{IN})/16 can be selected as the count source.

• Interrupt

The interrupt generation at underflow is the same as already explained for the timer mode. The one-shot generating trigger condition must be set to the INT_0 interrupt edge selection bit (b0) and INT_1 interrupt edge selection bit (b1) of INTEDGE. Setting these bits to "0" causes the interrupt request being triggered by a falling edge, setting them to "1" causes the interrupt request being triggered by a rising edge. The INT_0 interrupt request bit (b0) and INT_1 interrupt request bit (b1) of IREQ1 are set to "1" by detecting the active edge of the INT pin.

• Explanation of operation

For a "H" one-shot pulse, set bit 5 of TXM, TYM to "0".

[During timer operation stop]

The output level of $CNTR_0$/$CNTR_1$ pin is initialized to "L" at mode selection. Set the one-shot pulse width to TXH, TXL, TYH, TYL. A trigger generation during timer stop (input signal to INT_0/INT_1 pin) is invalid.

[During timer operation enabled]

When a trigger generation is detected, "H" is output, and at underflow "L" is output from $CNTR_0$/$CNTR_1$ pin.

For a "L" one-shot pulse set bit 5 of TXM, TYM to "1".

[During timer operation stop]

The output level of $CNTR_0$/$CNTR_1$ pin is initialized to "H" at mode selection. Set the one-shot pulse width to TXH, TXL, TYH, TYL. A trigger generation during timer stop (input signal to INT_0/INT_1 pin) is invalid.

[During timer operation enabled]

When a trigger generation is detected, "L" is output, and at underflow "H" is output from $CNTR_0$/$CNTR_1$ pin.

■Precautions

• Set the double-function port of $CNTR_0$/$CNTR_1$ pin to output and the double-function port of INT_0/INT_1 pin to input in this mode.

• This mode is unused in low-speed mode.

• During one-shot generation permission or one-shot generation the output level from $CNTR_0$/$CNTR_1$ pin changes if the value of the $CNTR_0$/$CNTR_1$ active edge switch bit is inverted.

Figure 24 shows the timing chart of the programmable one-shot generating mode.

(7) PWM mode

• Mode selection

This mode can be selected by setting "110" to the following bits.

Timer X operating mode bit (bits 2 to 0) of TXM
Timer Y operating mode bit (bits 2 to 0) of TYM

• Count source selection

In high- or middle-speed mode, f(X_{IN})/2 or f(X_{IN})/16 can be selected as the count source.

• Interrupt

With a rising edge of $CNTR_0$/$CNTR_1$ output, the timer X interrupt request bit (b4) and timer Y interrupt request bit (b5) of IREQ1 are set to "1".

• Explanation of operation

PWM waveform is output from $CNTR_0$ pin (in case of timer X) or from $CNTR_1$ pin (in case of timer Y).

The "H" interval of PWM waveform is determined by the setting value m (m=0 to 255) of TXH and TYH and the "L" interval of PWM waveform is determined by the setting value n (n=0 to 255) of TXL and TYL.

The PWM cycles are:

PWM cycle time = (m+n)·ts
PWM duty = m/(m+n)
where: ts: period of timer X/timer Y count source

[During count operation stop]

When a timer value is set to TXL, TXH, TYL, TYH by writing data to timer and timer latch at the same time. When setting this value, the output of $CNTR_0$/$CNTR_1$ pin is initialized to the "H" level.

[During count operation enabled]

By setting the bit 0 or 1 of TXYCON to "0", an "H" interval of TXH or TYH is output first, and after that a "L" level interval of TXL or TYL are output next. These operations are repeated continuously. The PWM output is changed after the underflow by setting a timer value, which is set by writing data to the timer latch only, to TXL, TXH, TYL, TYH.

■Precautions

• Set the double-function port of $CNTR_0$/$CNTR_1$ pin to output in this mode.

• This mode is unused in low-speed mode.

• When the PWM "H" interval is set to "00_{16}", PWM output is "L".

• When the PWM "L" interval is set to "00_{16}", PWM output is "H".

• When the PWM "H" interval and "L" interval are set to "00_{16}", PWM output is "L".

• When a PWM "H" interval or "L" interval is set to "00_{16}" at least for a short time, timer X/timer Y interrupt request does not occur.

• When the value set to the timer latch is "00_{16}", the value is undefined since the timer counts down by dummy count operation.

Figure 23 shows the timing chart of the PWM mode.

■Precautions regarding all modes

• Timer X, timer Y writing control

One of the following operation is selected by bit 3 of TXM or TYM for timer X or timer Y.

Writing data to the corresponding latch and timer at the same time

Writing data to only corresponding latch

When the operation "writing data to only corresponding latch" is selected, the value is set to the timer latch by writing a value to timer X/Y address and a timer is renewed at the next underflow. After releasing a reset, "writing the corresponding latch and timer at the same time" is selected. When a value is written to timer X/Y address, a value is set to a timer and a timer latch at the same time. When "writing data to only corresponding latch" is selected, if writing to a reload latch and an underflow are performed at the same timing, the timer value is undefined.

• Timer X, timer Y read control

In pulse period measurement mode and pulse width measurement mode the timer value cannot be read-out. In all other modes read-out operations without effect to count operations/stops are possible. However, the timer latch value cannot be read-out.

• Precautions regarding the $CNTR_0$/$CNTR_1$ active edge switch bit and the INT_0/INT_1 interrupt edge selection bit:

The $CNTR_0$/$CNTR_1$ active edge switch bit and the INT_0/INT_1 interrupt edge selection bit settings have an effect also on each interrupt active edge.

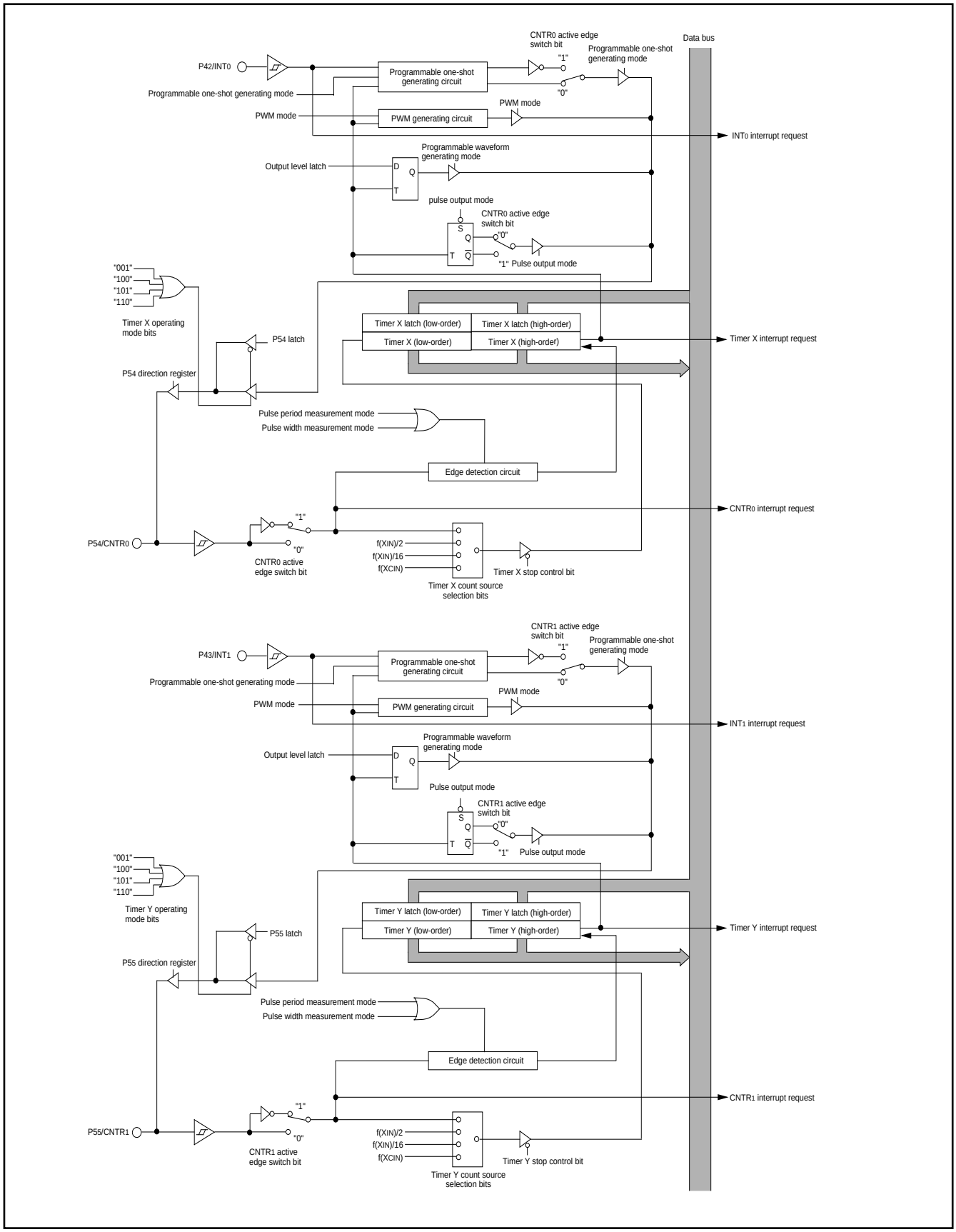


Fig. 15. Block diagram of Timer X and Timer Y

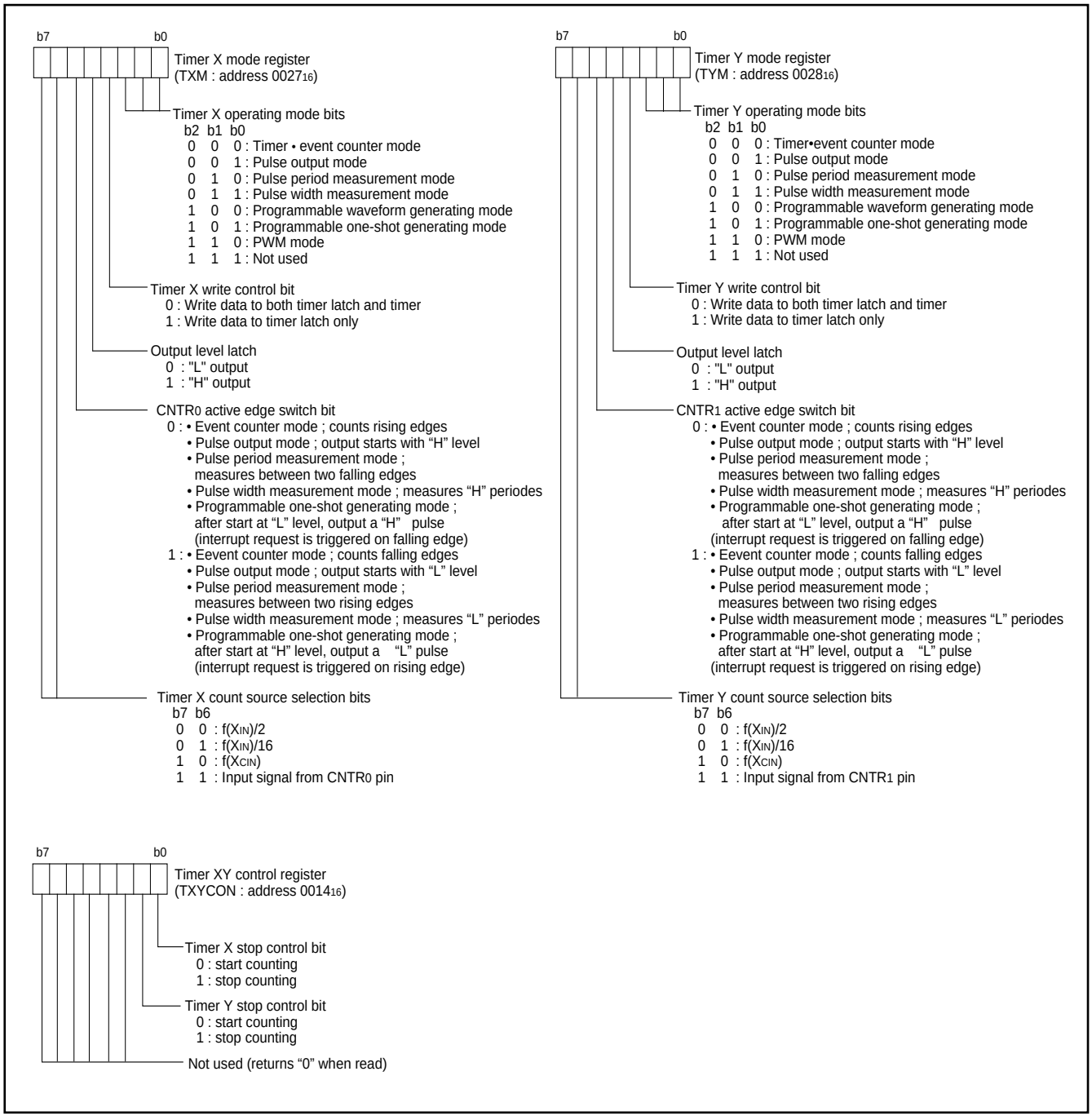
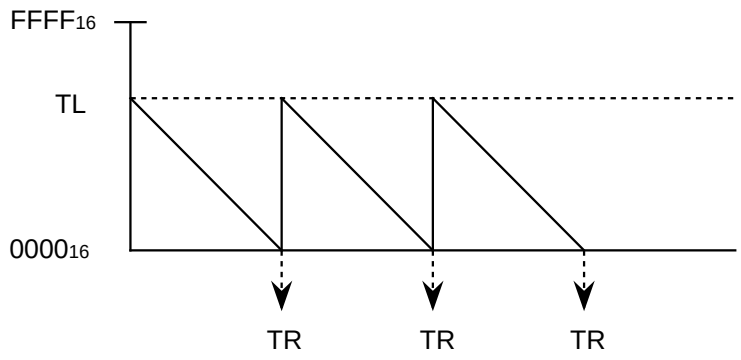
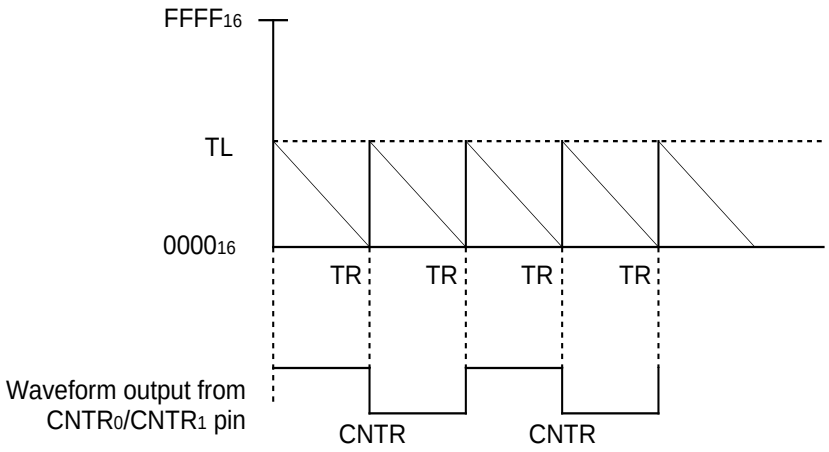


Fig. 16. Structure of Timer X mode register, Timer Y mode register, and Timer XY control register



TL: A value set to a timer latch
TR: Timer interrupt request

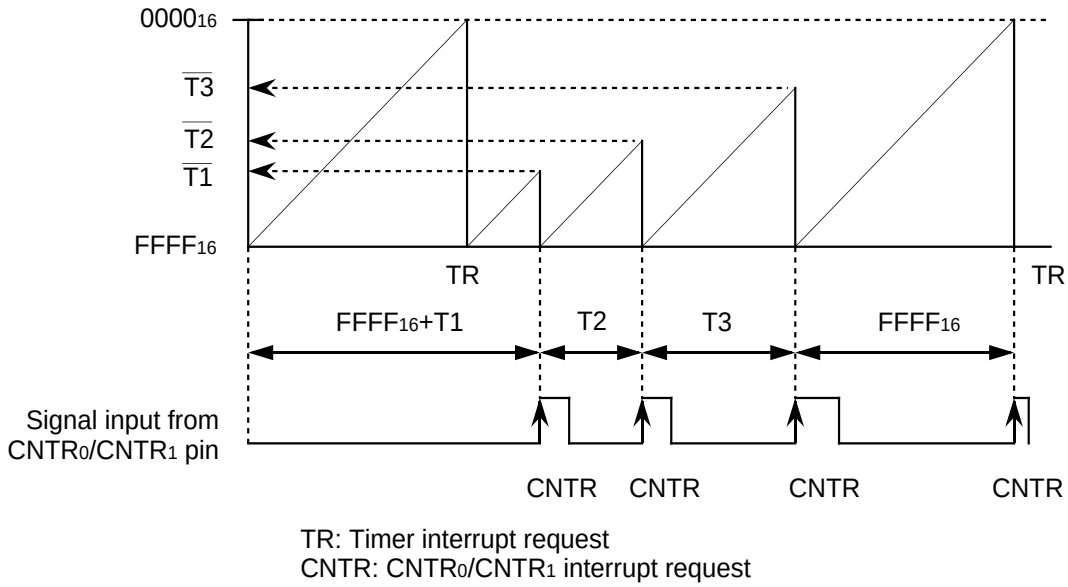
Fig. 17. Timing chart of Timer•Event counter mode



TL: A value set to a timer latch
TR: Timer interrupt request
CNTR: $CNTR_0/CNTR_1$ interrupt request

This example's condition:
$CNTR_0/CNTR_1$ active edge switch bit "0":
⇒ output starts with "H" level, interrupt at falling edge

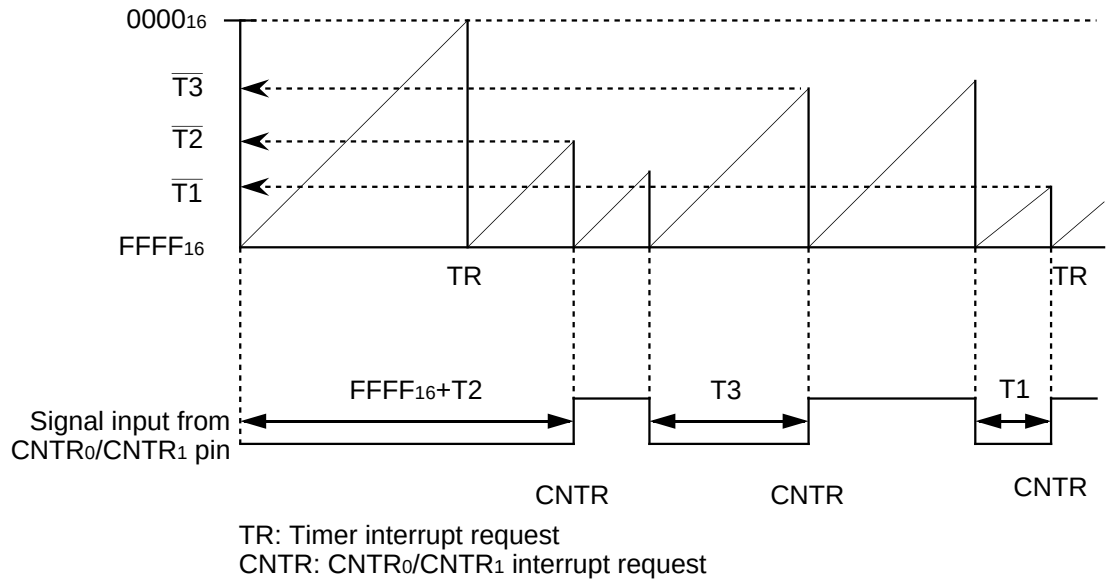
Fig. 18. Timing chart of Pulse output mode



TR: Timer interrupt request
CNTR: $CNTR_0/CNTR_1$ interrupt request

This example's condition:
$CNTR_0/CNTR_1$ active edge switch bit set to "1"
⇒ measure from rising edge to rising edge; interrupt at rising edge

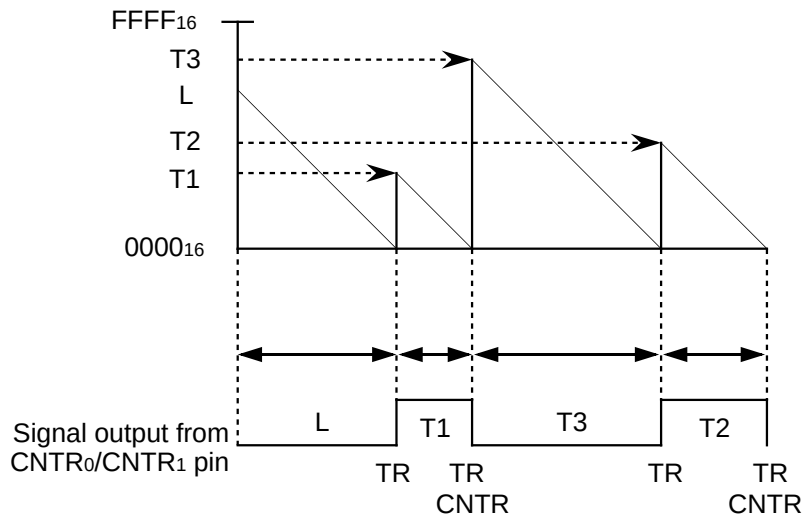
Fig. 19 Timing chart of Pulse period measurement mode



TR: Timer interrupt request
CNTR: $CNTR_0/CNTR_1$ interrupt request

This example's condition:
$CNTR_0/CNTR_1$ active edge switch bit set to "1"
⇒ measure "L" width; interrupt at rising edge

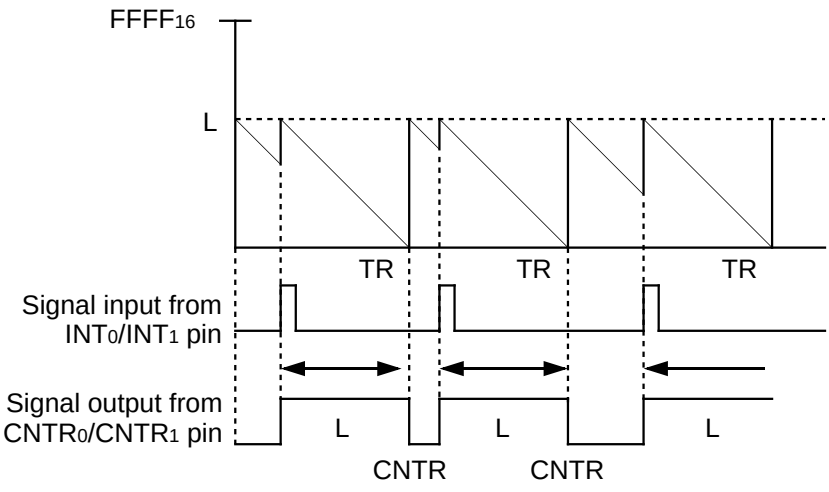
Fig. 20. Timing chart of Pulse width measurement mode



L: Initial value of timer
TR: Timer interrupt request
CNTR: $CNTR_0/CNTR_1$ interrupt request

This example's condition:
$CNTR_0/CNTR_1$ active edge switch bit set to "0"
⇒ output starts with "L" level; interrupt at falling edge

Fig. 21. Timing chart of Programmable waveform generating mode



L: One-shot pulse width; timer latch value
TR: timer interrupt request
CNTR: $CNTR_0/CNTR_1$ interrupt request

This example's condition:
$CNTR_0/CNTR_1$ active edge switch bit set to "0"
⇒ output a "H" pulse; interrupt at falling edge

Fig. 22. Timing chart of Programmable one-shot generating mode

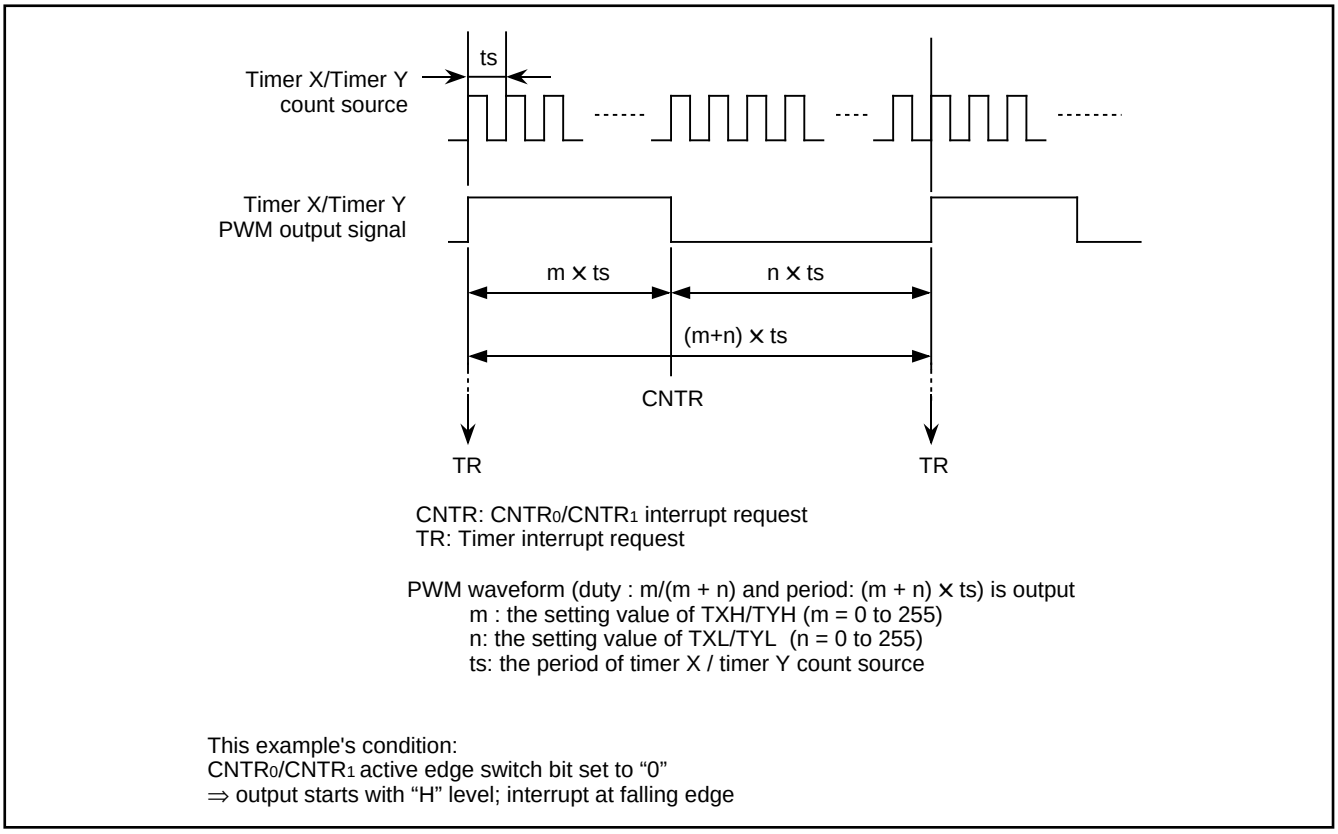


Fig. 23. Timing chart of PWM mode

●Timer 1, Timer 2, Timer 3

Timer 1 to 3 are 8-bit timers for which the count source can be selected through timer 123 mode register.

(1) Timer 2 write control

Timer 2 write control bit (b2) of timer 123 mode register allows to select whether a value written to timer 2 is written to timer latch and timer synchronously or to the timer latch only.

If only the timer latch is written to, the value is set only to the reload-latch by writing a value to the timer address at that time. The content of timer is reloaded with the next underflow. Usually writing operation to the timer latch and timer synchronously is selected. And a value is written to the timer latch and timer synchronously when a value is written to the timer address.

If only the timer latch is written to, it may occur that the value set to the counter is not constant, when the timing with which the reload-latch is written to and the underflow timing is nearly the same.

(2) Timer 2 output control

When timer 2 output (T_{OUT}) is enabled, inverted signals are output from T_{OUT} pin each time timer 2 has underflow. For this reason, set the double-function port of T_{OUT} pin to output mode.

■Precautions on timers 1 to 3

When the count source for timer 1 to 3 is switched, it may occur that short pulses are generated in count signals and that the timer count value shows big changes. When timer 1 output is selected as timer 2 or timer 3 count source, short pulses are generated to signals output from timer 1 through writing timer 1. Due to that, the count values for timer 2 and 3 may change very often.

Therefore, when the count sources for timer 1 to 3 are set, set the values in order starting from timer 1.

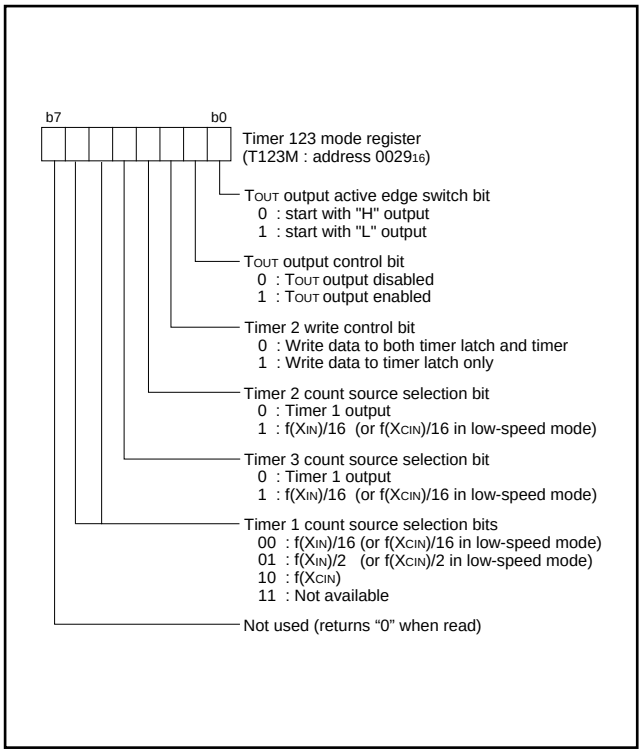


Fig. 24. Structure of Timer 123 mode register

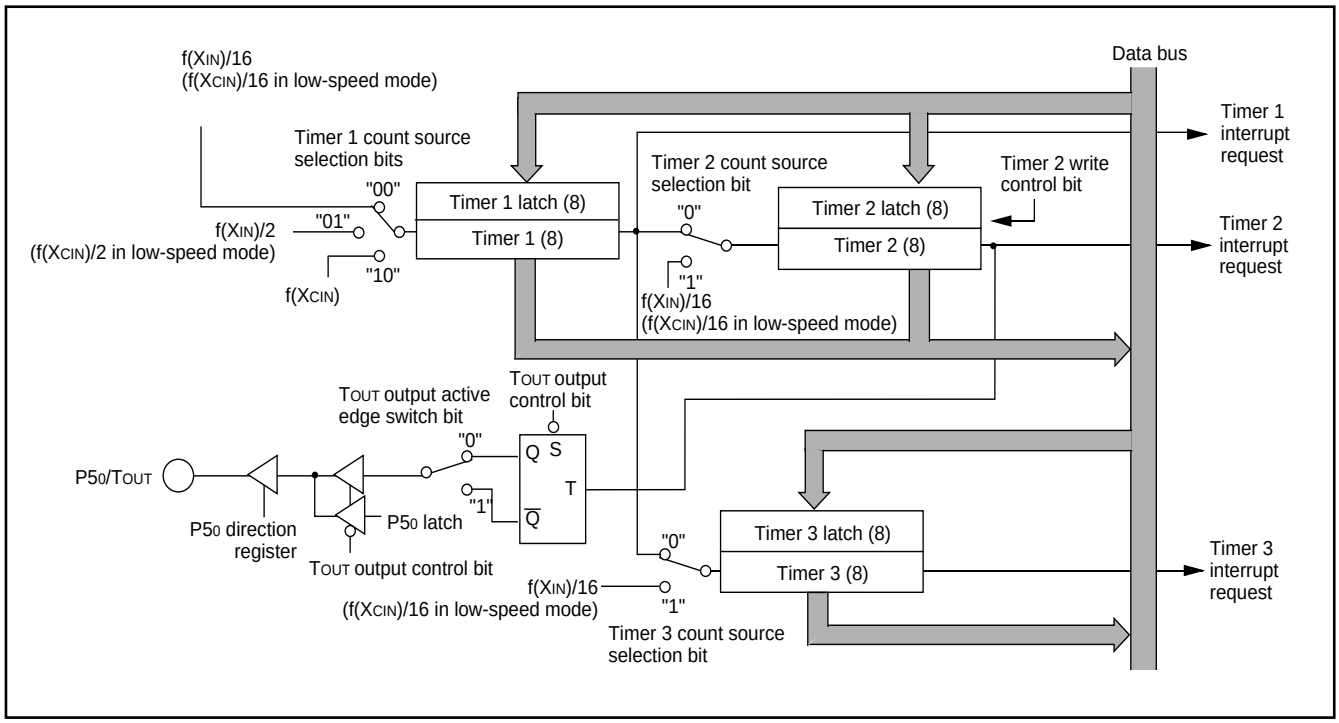


Fig. 25. Block diagram of Timer

●Real time output port

The 3807 group has two on-chip sets of real time output ports (RTP). The two sets of real time output ports consist of two 16-bit timers A and B and eight 8-bit real time port registers. Synchronous to the reloading of timers A and B, the real time port register values are output from ports $P8_2$ to $P8_7$, $P3_0$ and $P3_1$. The real time port registers consist of 8-bit register 0 to 7. Each port with its corresponding bits is shown in figure 26.

Timer A and timer B have each two 16-bit timer latches. Figure 26 shows the real time port block diagram and figure 27 and 28 show the structure of the real time port control registers 0 to 3.

There are four operating modes for real time ports which are: 8 repeated load mode, 6 repeated load mode, 5 repeated load mode and one-shot pulse generating mode. Each operating mode can be set for timer A and timer B separately. However, switch modes during timer count stop.

(1) 8 repeated load mode

The output operation for each value of the real time port registers 7 to 0 is performed repeatedly in association with an alternate underflow of the corresponding timer latch 1 or 0. The real time port output pointer changes in sequence as a cycle of 8 repeated load operations as "7, 6, 5, 4, 3, 2, 1, 0, 7, 6, 5, 4, 3, 2, 1, 0, 7, 6, 5, ..."

The initial value at the generation of a start trigger can be specified by setting a value in the output pointer. Figure 29 shows a timing chart of 8 repeated load mode.

(2) 6 repeated load mode

The output operation for each value of real time port registers 5 to 0 is performed repeatedly in association with an alternate underflow of the corresponding timer latch 1 to 0. The real time port output pointer changes in sequence as a cycle of 6 repeated load operations as "5, 4, 3, 2, 1, 0, 5, 4, 3, 2, 1, 0, 5, 4, ..."

The initial value at the generation of a start trigger can be specified by setting a value in the output pointer. Figure 30 shows a timing chart of the 6 repeated load mode.

(3) 5 repeated load mode

The output operation for each value of real time port registers 4 to 0 is performed repeatedly in association with an alternate underflow of the corresponding timer latch 1 or 0. The real time port output pointer changes in sequence as a cycle of 5 repeated load operations as "4, 3, 2, 1, 0, 4, 3, 2, 1, 0, 4, 3, 2, 1, ..." The initial value at the generation of a start trigger can be specified by setting a value in the output pointer. Figure 31 shows a timing chart of the 5 repeated load mode.

(4) One-shot pulse generation mode

The output operation for each value of real time port registers 2 to 0 is performed only once in association with trigger generation and an underflow of timer latch 1 or 0. After a trigger is generated, the value of real time port register 1 is output from the real time output port and the output pointer value becomes "000_2". At each underflow of the timer, the each value of real time port registers 0 and 2 is output in ascending sequence, then the operation is completed.

After completion of the operation, the value of real time port register 2 is continuously output from the real time output port and the output pointer value continues to be "001_2" until the next start trigger is generated. In this condition, the real time port function is in the wait status.

When this mode is selected, the pointer value is not changed by writing a value into the output pointer. If external trigger is specified as trigger selection when this mode is selected, a rising and falling double edge trigger is generated regardless of the contents of the INT_4 interrupt source bit (b7) of the interrupt edge selection register.

Figure 32 shows a timing chart of the one-shot pulse generation mode.

(5) Selection of timer interrupt mode

The timer is a count-down system. The contents of the timer latch are reloaded by the count pulse subsequent to the moment when the contents of the counter becomes "0000_{16}". At the same time, the interrupt request bit corresponding to each timer is set to "1." The interrupt request corresponding to the value of the real time port output pointer can also be controlled. For controlling the interrupt request bit, refer to the item pertaining to the timer interrupt mode selection bit of the real time port control register 1,2 shown in figure 27 and 28.

(6) Switch of timer count source

The timer A and the timer B can select the system clock ϕ divided by 2 or 16 as a count source with the timer A, B count source selection bit (b0) of real time port control register 0.

[Timer latches]

Each of the timer A and the timer B has two 16-bit timer latches. Data is written into the 8 low-order bits and the 8 high-order bits in this order. When the high-order side has been written, the next latch is automatically specified. The writing pointer changes in sequence as "1, 0, 1, 0, 1, ..." The timer latch to be written first can be specified by setting the timer writing pointer. Data is not written directly into the timer A and the timer B. When reading the contents of the timer, the count value at that point of time is read. Read the high-order side first and then the low-order side. The low-order side value is read with the same timing as that for the high-order side value and held at the timer read latch. The data held state is released by reading the low-order side. At a reload operation of the timer A or the timer B. Timer latch 1 is reloaded as the initial value after a trigger is generated. After that, the timer latch is reloaded in sequence as "0, 1, 0, 1, ..." The timer latch value cannot be read out.

[Start trigger]

The operation of the real time port is started by a start trigger. When a start trigger is generated, the value of the real time port register specified by the output pointer (the value of real time port register 1 in the one-shot pulse generation mode) is output from the real time output port.

The value of timer latch 1 is reloaded into the timer A or the timer B and the timer count A, B source stop bit is released, so that the timer count is started.

After that, when the timer underflows, data is transferred from the real port register to the real time output port.

As a start trigger, either internal trigger or external trigger can be selected by the timer A start trigger selection bit (b2) or timer B start trigger selection bit (b5) of real time port control register 0.

When the internal trigger is selected, a start trigger is generated by an input signal of the INT_4 pin. The start trigger becomes a falling edge when the INT_4 interrupt edge selection bit is "0" and a rising edge when this bit is "1".
When the external trigger is selected in the one-shot pulse generation mode, the start trigger becomes a rising/falling double edge trigger regardless of the contents of the INT_4 interrupt edge selection bit.

[Real time port registers] RTP
The data to be output to real time ports is written into 8 real time port registers 0 to 7. The correspondence between each bit of real time port registers and each port output is as follows :

$P3_1$: bit 7 of real time port registers 7 to 0
$P3_0$: bit 6 of real time port registers 7 to 0
$P8_7$: bit 5 of real time port registers 7 to 0
$P8_6$: bit 4 of real time port registers 7 to 0
$P8_5$: bit 3 of real time port registers 7 to 0
$P8_4$: bit 2 of real time port registers 7 to 0
$P8_3$: bit 1 of real time port registers 7 to 0
$P8_2$: bit 0 of real time port registers 7 to 0

It can be selected for each bit by real time port control register 3 whether the output of each port is to be used as an ordinary I/O port or a real time port output.

[Real time port data pointer]
It can be optionally specified by the real time port data pointers A or B and the real time port data pointer A or B switching bit in which real time port register the output data is to be set or form which real time port register the data output is to be started.
When writing output data into the real time port register, set the real time port data pointer A, B switch bit to "0" (select the R/W pointer) and also write a value into the 3 bits of the real time port data pointers A, B. With this, the real time port register for writing will be specified. After that, when a value is written into the real time port register (address $002A_{16}$), the data is written into the specified real time port register and also the R/W pointer value is automatically decreased by 1. Then writing data is enabled into the next real time port register.
A value of "000_2" to "111_2" can be set int the R/W pointer regardless of the operating mode specified by the timer A, B operating mode selection bit, and the R/W pointer value is automatically decreased by 1 by writing data into the real time port register. However, when a value becomes "000_2", the R/W pointer value is decreased by 1 in the numeral range of stages to be used in each operating mode unless the R/W pointer is set again at the subsequent write operation to the real time port register. When "111_2 (=7)" is set in the R/W pointer, the R/W pointer operation in each selected mode is as follows :

•During 8 repeated load mode 7→6→5→4→3→2→1→0→7→6→5...
•During 6 repeated load mode 7→6→5→4→3→2→1→0→5→4→3...
•During 5 repeated load mode 7→6→5→4→3→2→1→0→4→3→2....
•During one-shot pulse generation mode
7→6→5→4→3→2→1→0→2→1→0....

When reading the real time port register, set the real time port data pointer A, B switch bit to "0" (select the R/W pointer) and also writing a value into the 3 bits of the real time port data pointer A, B to specify the real time port register for reading. After that, the value of the specified real time port register can be read by reading the real time port register (address $002A_{16}$). In this care, however, the R/W pointer value is not counted down automatically. Accordingly, to read another real time port register, rewrite the R/W pointer beforehand.
To specify a read port register to be output to the real time output port, set the real time port data pointer A, B switch bit to "1" (select an output pointer) and also set a value in the 3 bits of the real time port data pointer A or B.
When a start trigger is generated, data is output beginning with the real time port register set in the output pointer and the output pointer value is automatically decreased by 1.
At each underflow of the timer A or timer B, the output pointer value is automatically decreased by 1. Regarding the case of the one-shot pulse generation mode, however, refer to the item pertaining to the one-shot pulse generation mode.
When the real time port data pointer A to B has been read, only the output pointer can be read.

■Notes regarding all modes
•When the trigger is generated again during timer count operation, the operation is started from the beginning. In this case, put an interval of 3 cycles or more between the generation of a trigger and the generation of the next trigger, If the generation of the next trigger occurs almost concurrently with the underflow timing of the timer, the next real time output may not be performed normally.
•To stop the timer count after generation of a start trigger, write "1" in the timer A, B count source stop bit of real time port control register 0 at an interval of 3 cycles or more of the timer count source.
•To change the contents of the real time port data pointer A, B switch bit, the real time port data pointer must be specified simultaneously. Therefore, use the LDM/STA instruction instead of the SEB/CLB instruction.
•If the timer A, B count source stop bit is changed ("1"→"0") by a start trigger between the read operation and the write operation of a read-modify-write instruction such as the SEB instruction which is used in real time port control register 0, the timer count will stop, having an effect on the real time output.
An maximum interval of 2 cycles of the count source is required before the timer A, B count source stop bit is cleared to "0" which indicates the count operation state after a start trigger is generated regardless of whether the start trigger is an internal trigger or an external trigger.
Accordingly, do not use the read-modify-write instruction for real time port control register 0 in this period. If a write operation for real time port control register 0 with any purpose other than stopping the timer count is performed concurrently with the generation of a start trigger, be sure to use such an instruction for writing "0" into the timer A, B count source stop bit as the LDM/STA instruction.
Even if "0" is written into the timer A, B count source stop bit, the timer count remains in the stop state without change.
•When the timing for writing to the high-order side reload latch is almost equal to the underflow timing, an undesirable value may be set in the timer A or timer B.
•If the real time output port is selected by real time port control register 3 after resetting, "L" is output from this pin until a start trigger is generated.

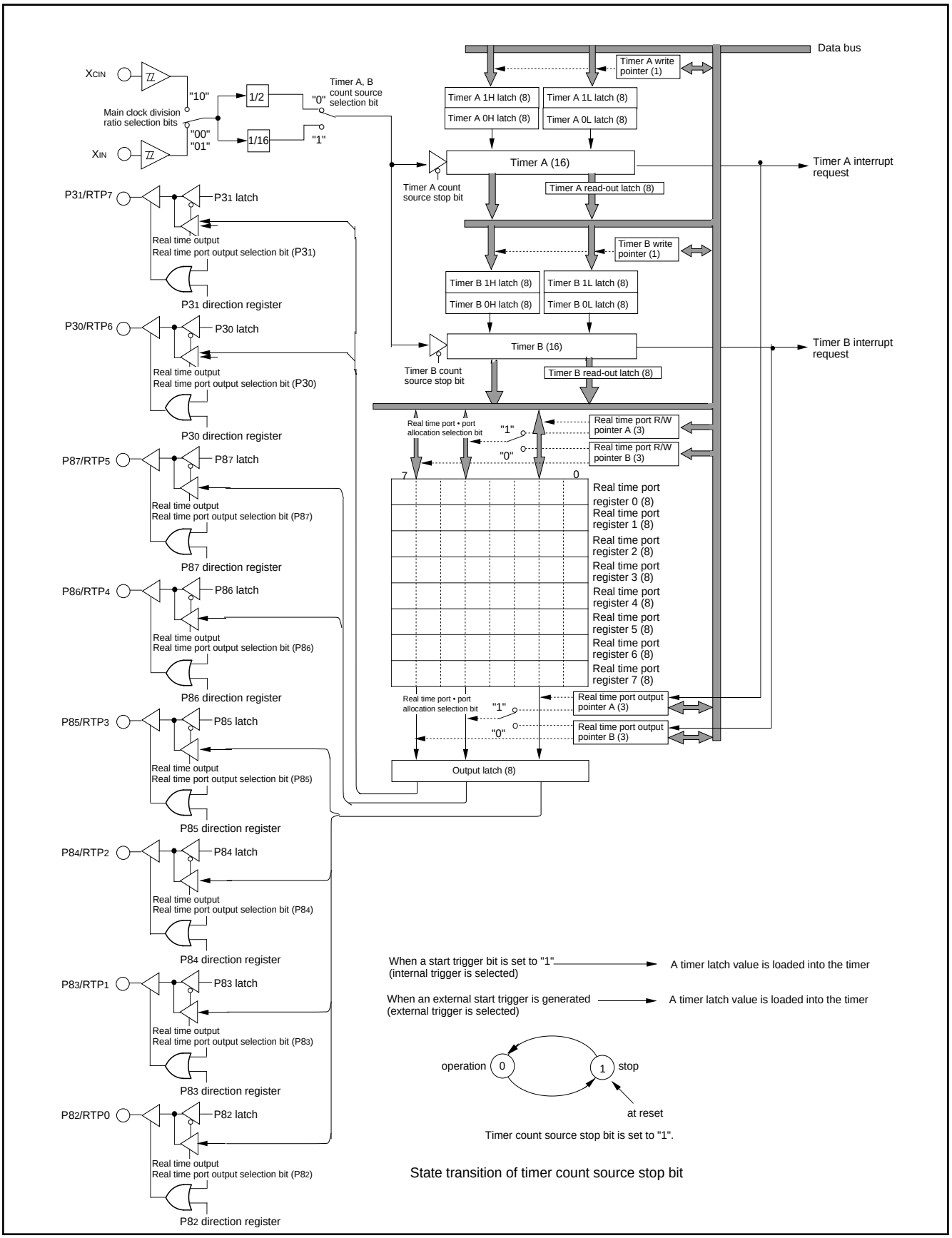


Fig. 26. Block diagram of Real time output port

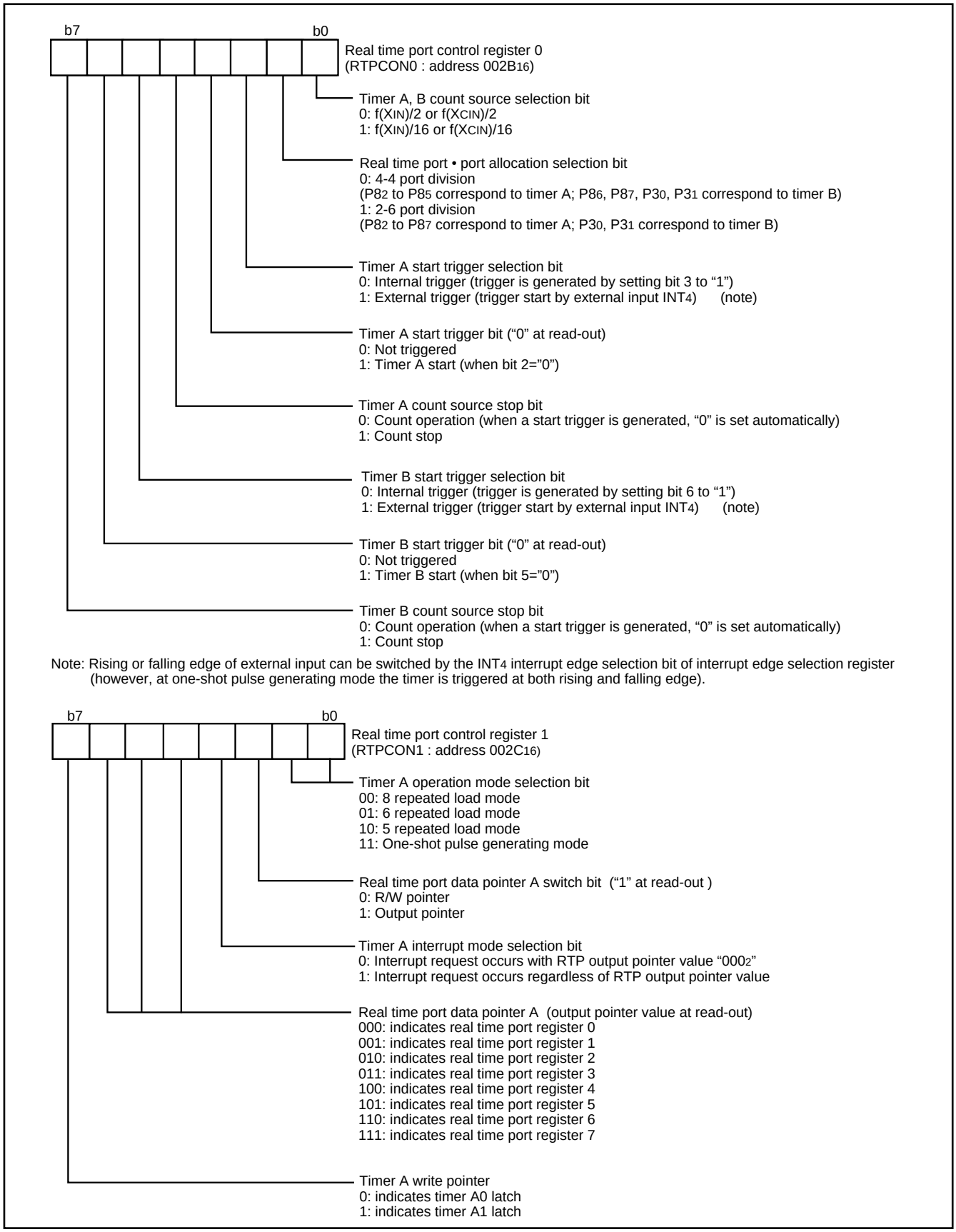


Fig. 27. Structure of Real time output port related register (1)

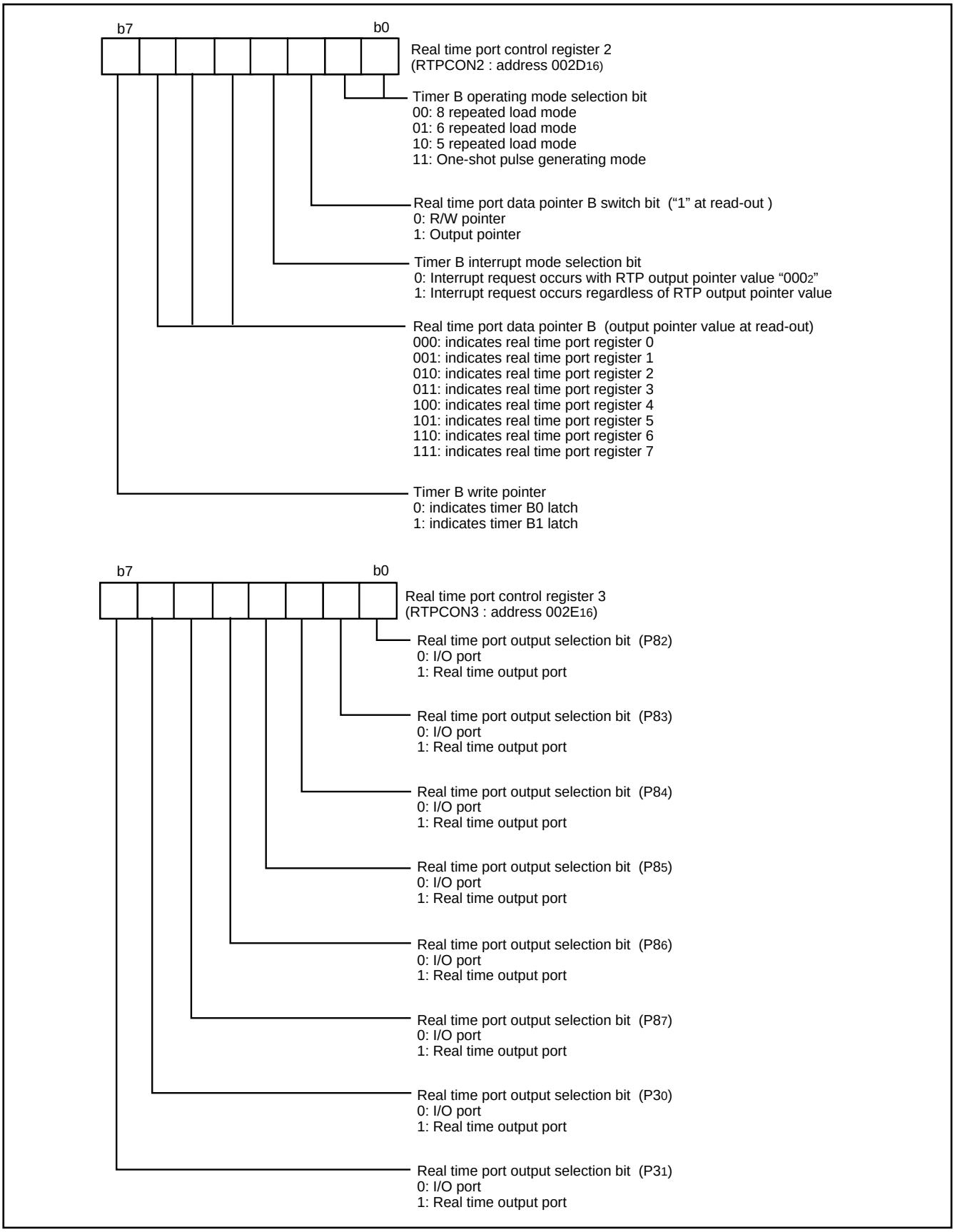


Fig. 28 Structure of Real time output port related register (2)

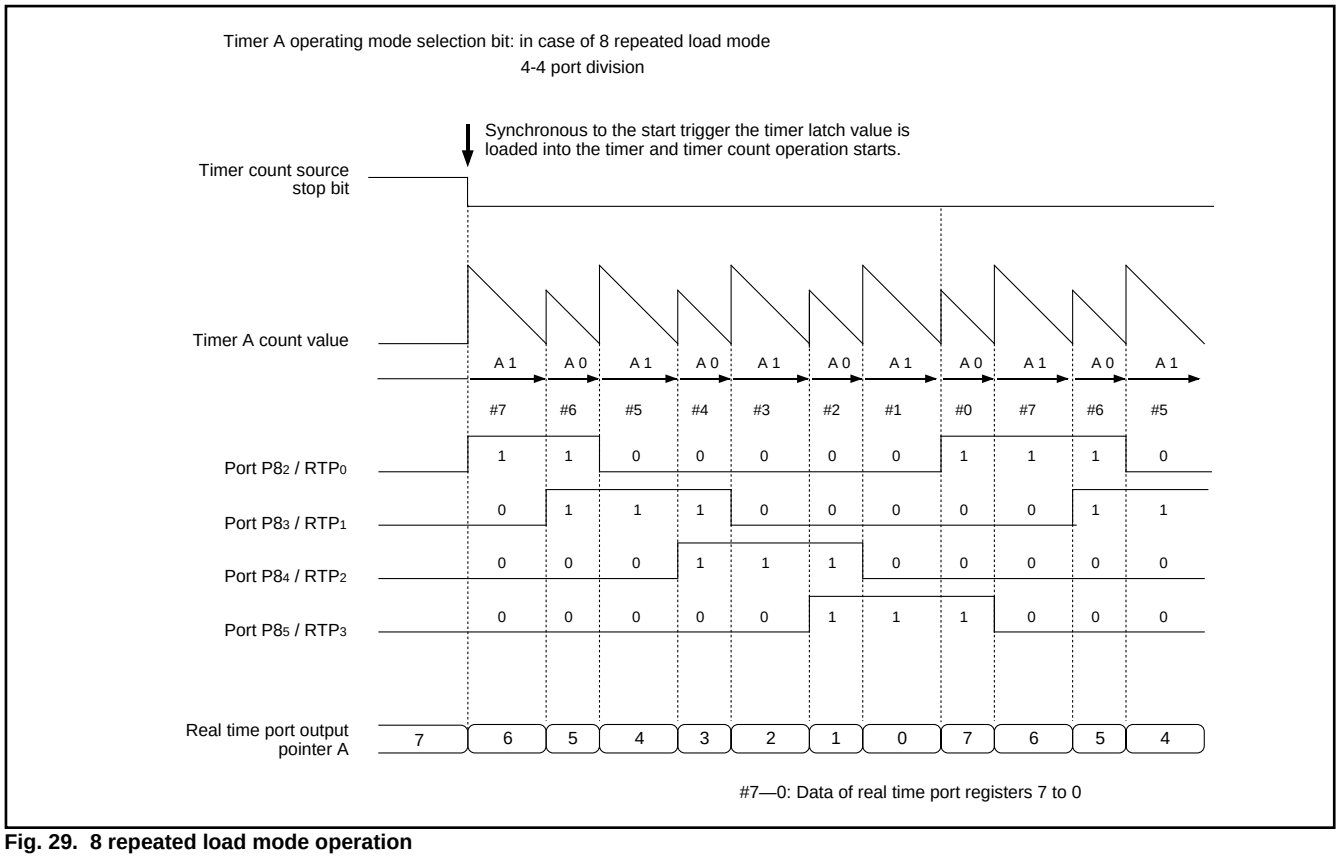


Fig. 29. 8 repeated load mode operation

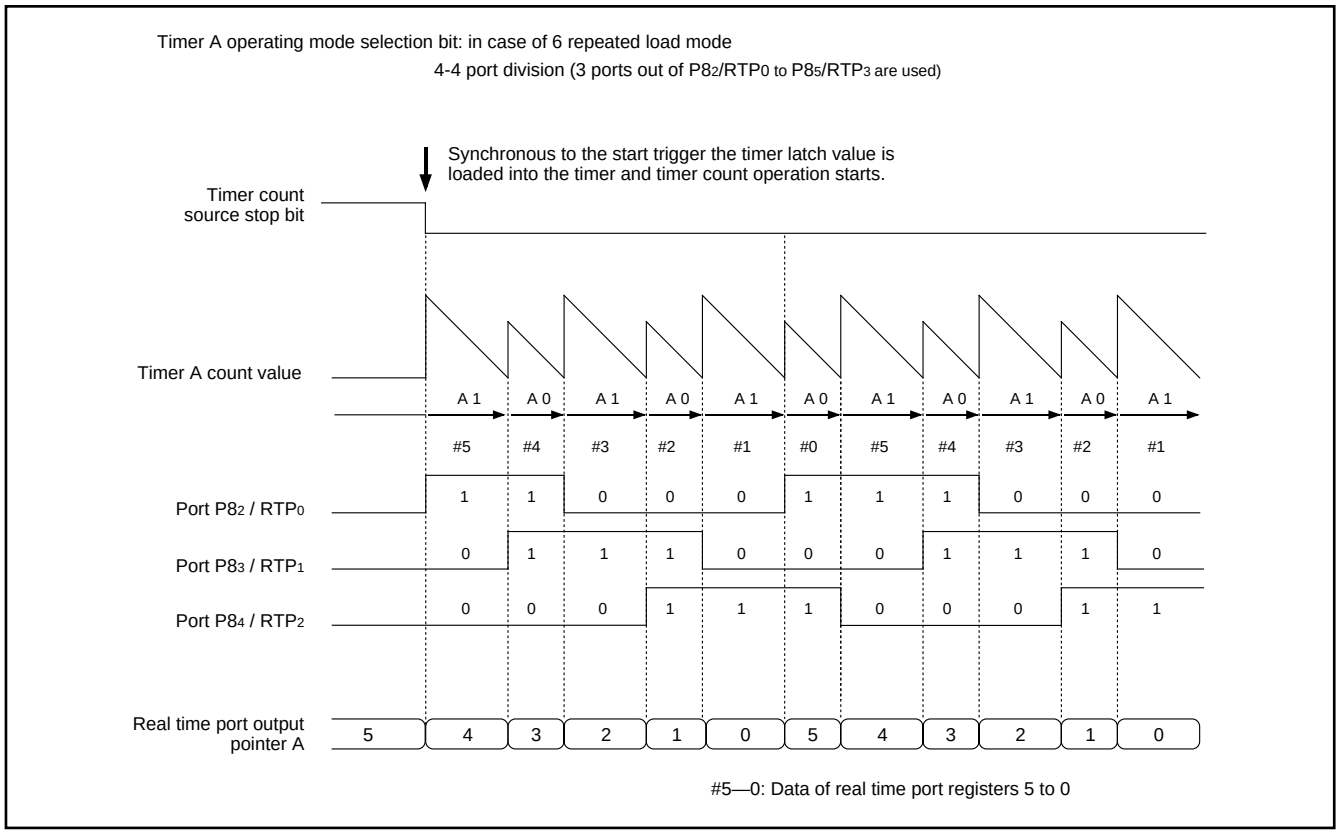


Fig. 30. 6 repeated load mode operation

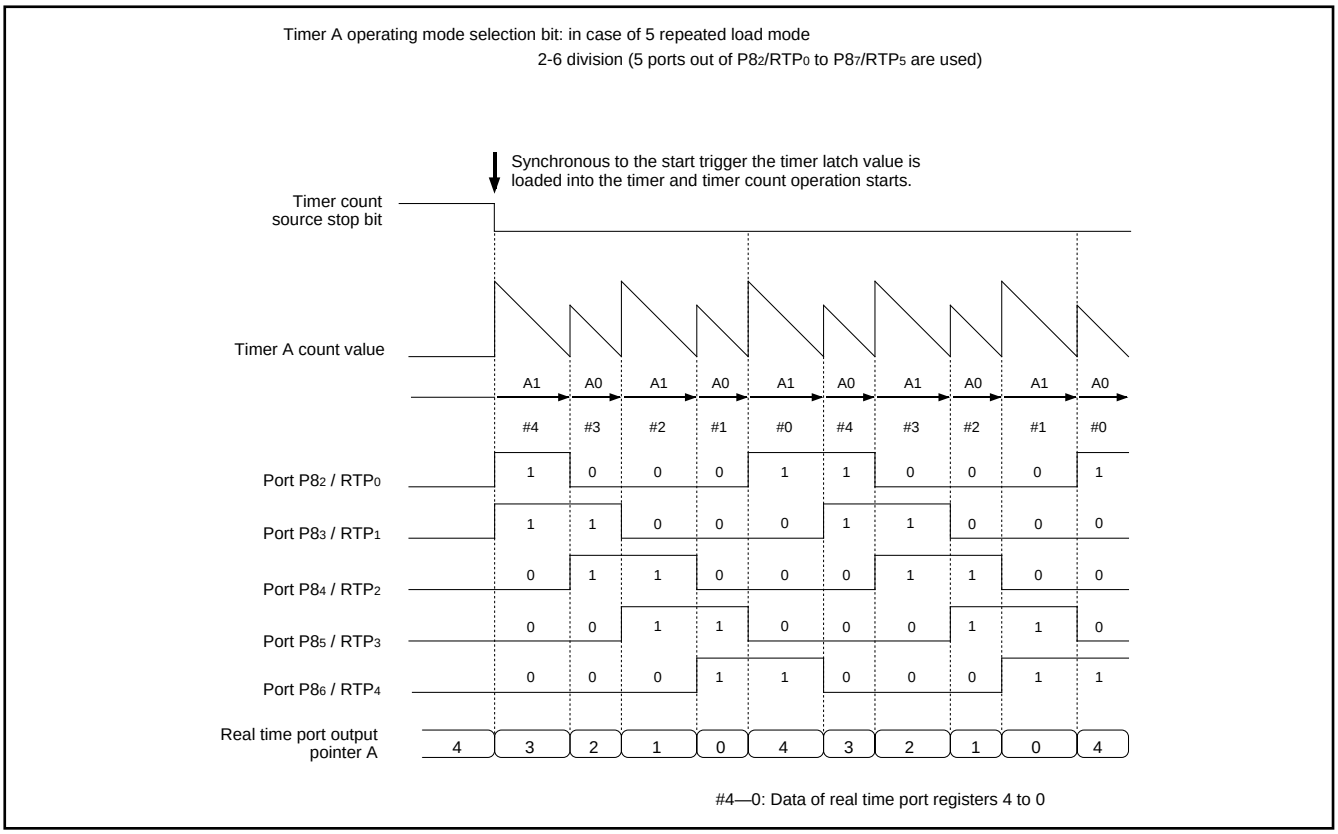


Fig. 31. 5 repeated load mode operation

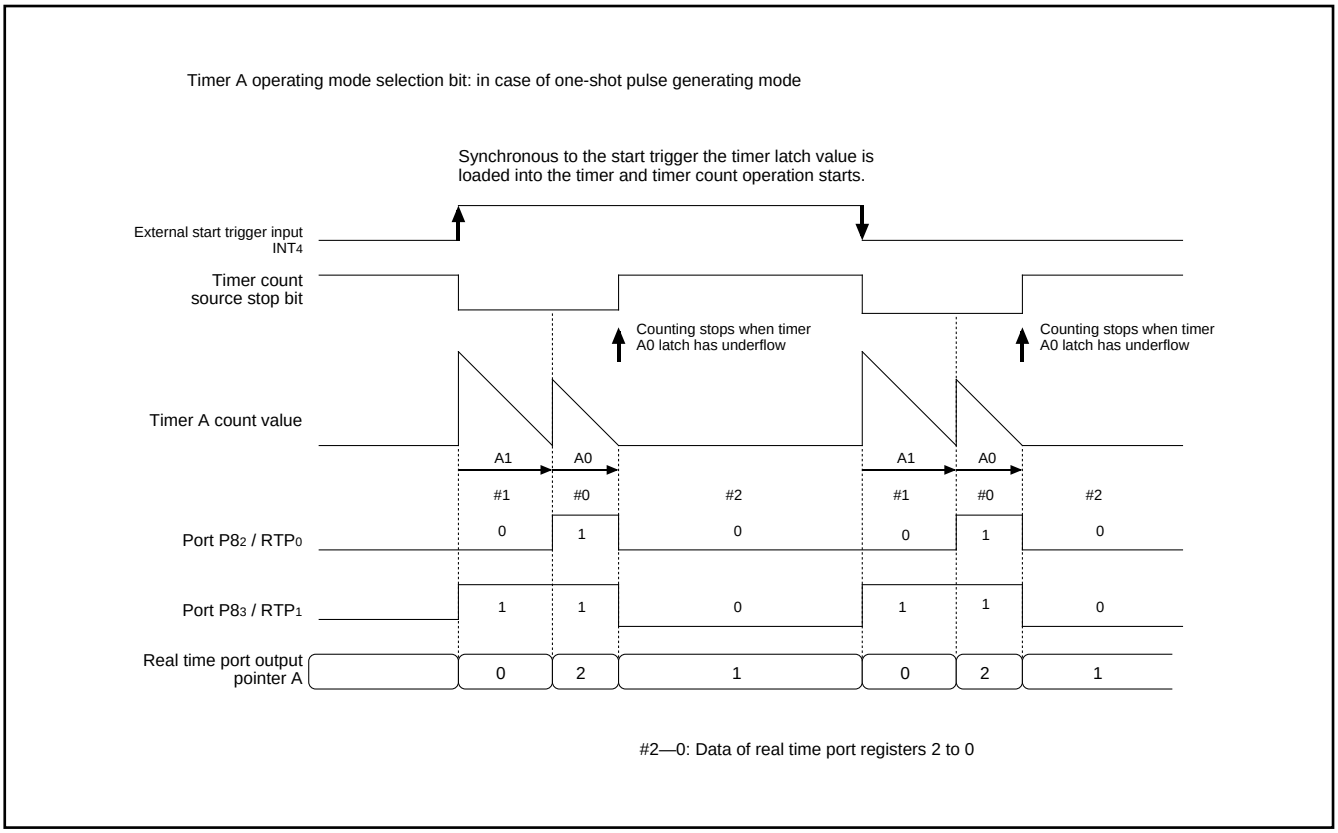


Fig. 32. One-shot pulse generating mode operation

Serial I/O

●Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation during Serial I/O1 operation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to "1." For clock synchronous serial I/O, the transmitter and the receiver must use the same clock for serial I/O1 operation. If an internal clock is used, transmit/receive is started by a write signal to the Transmit/Receive buffer register (TB/RB) (address:0018_{16}).

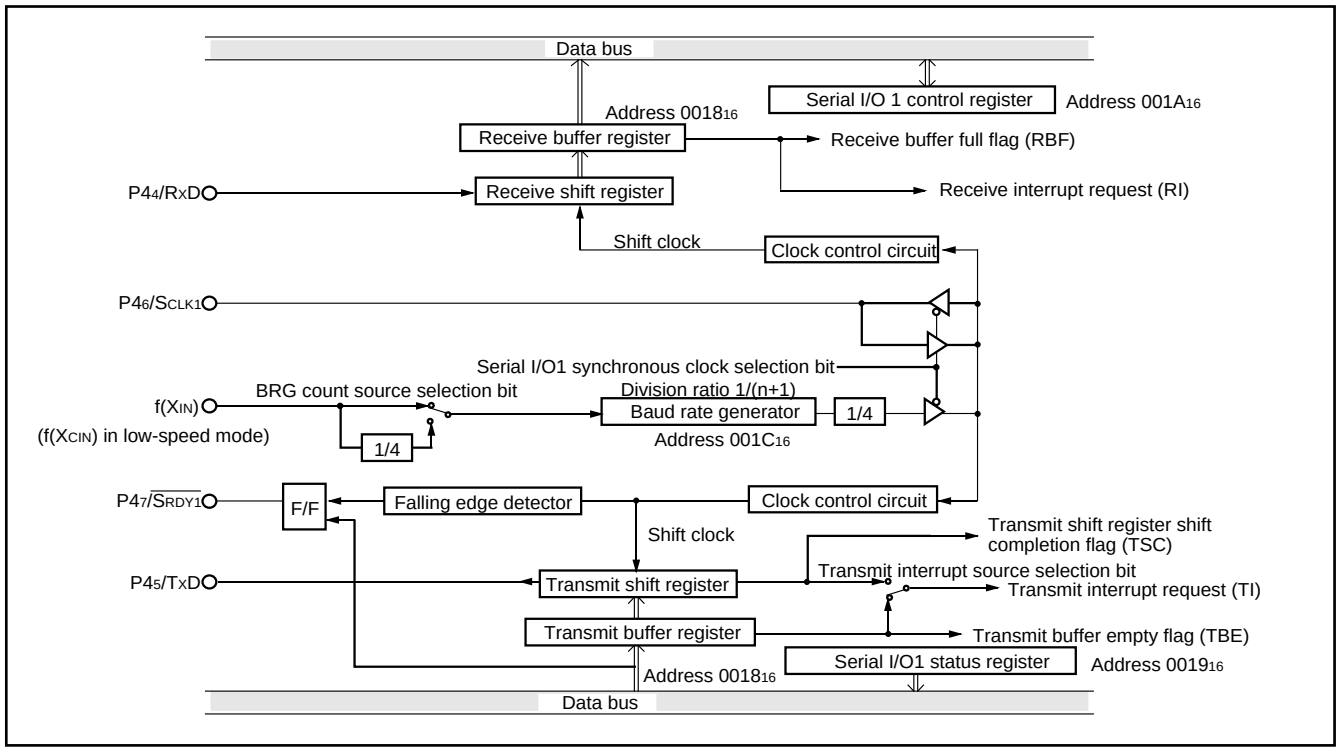
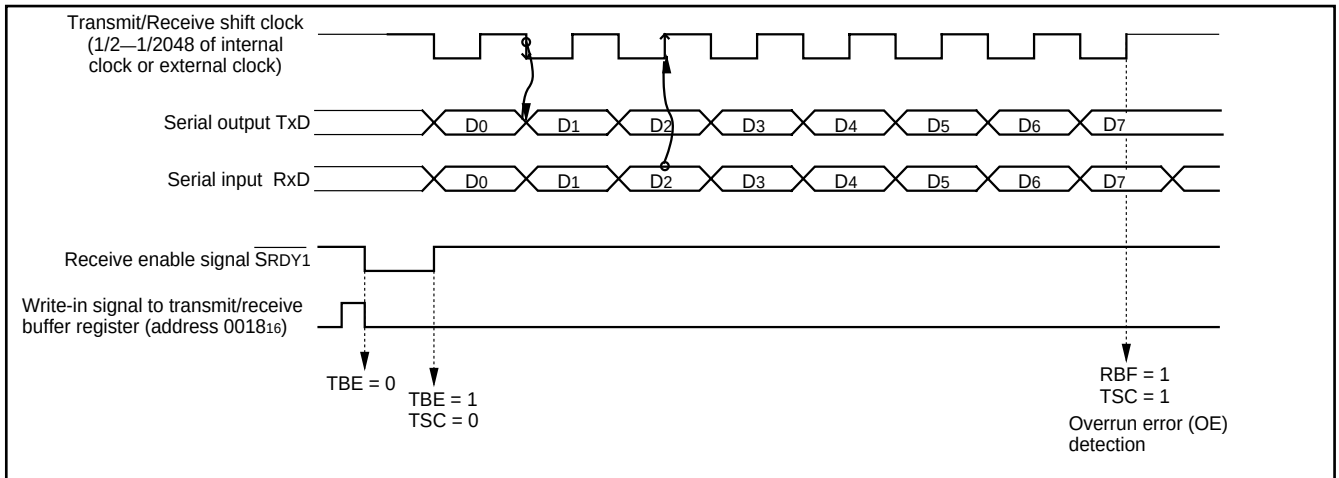


Fig. 33. Block diagram of clock synchronous serial I/O1



Notes 1 : The transmit interrupt (TI) can be selected to occur either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
2 : If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.
3 : The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 34. Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Asynchronous serial I/O1 mode (UART) can be selected by clearing the Serial I/O1 mode selection bit (b6) of the Serial I/O1 control register to "0." Eight serial data transfer formats can be selected and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer (the two buffers have the same address in memory). Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer. The transmit buffer can also hold the next data to be transmitted, and the receive buffer can hold a character while the next character is being received.

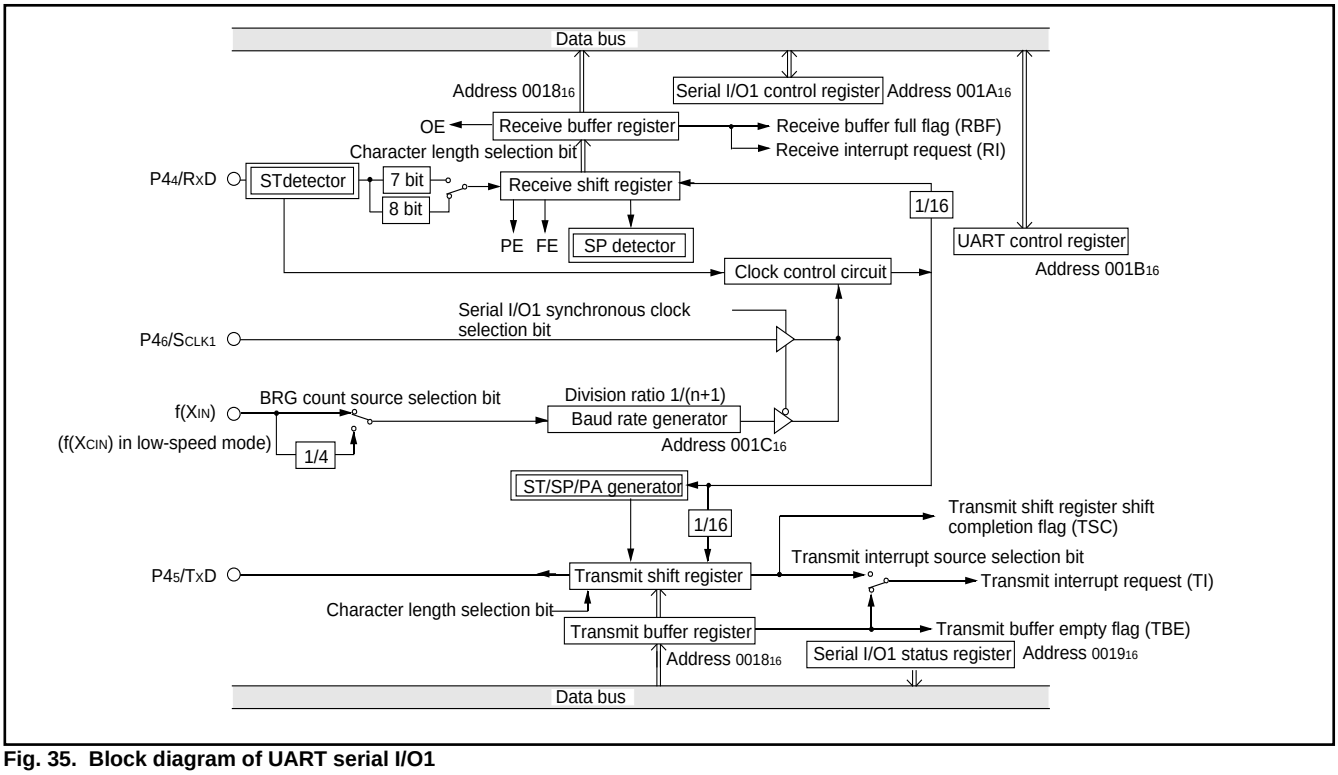
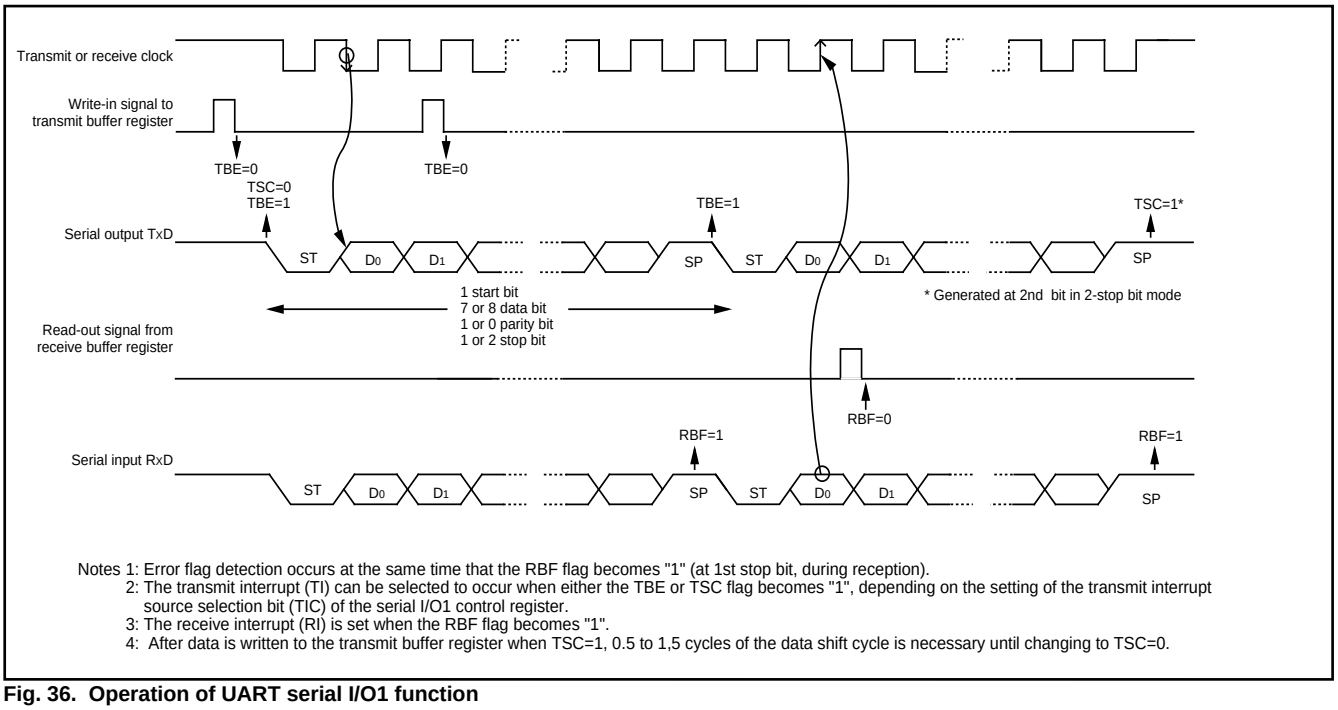


Fig. 35. Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes "1" (at 1st stop bit, during reception).
2: The transmit interrupt (TI) can be selected to occur when either the TBE or TSC flag becomes "1", depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes "1".
4: After data is written to the transmit buffer register when TSC=1, 0.5 to 1,5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 36. Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register] TB/RB (0018_{16})

The transmit buffer and the receive buffer are located in the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Serial I/O 1 Status Register] SIO1STS (0019_{16})

The read-only serial I/O1 status register consists of seven flags (b0 to b6) which indicate the operating status of the serial I/O1 function and various errors. Three of the flags (b4 to b6) are only valid in UART mode. The receive buffer full flag (b1) is cleared to "0" when the receive buffer is read.

The error detection is performed at the same time data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A writing to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (b3 to b6, respectively). Writing "0" to the serial I/O1 enable bit (SIOE : b7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

All bits of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (b4) of the serial I/O1 control register has been set to "1", the transmit shift register shift completion flag (b2) and the transmit buffer empty flag (b0) become "1."

[Serial I/O1 Control Register] SIO1CON ($001A_{16}$)

The serial I/O1 control register contains eight control bits for serial I/O1 functions.

[UART Control Register] UARTCON ($001B_{16}$)

The UART control register consists of four control bits (b0 to b3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer. One bit in this register (b4) is always valid and sets the output structure of the $P4_5$/TxD pin.

[Baud Rate Generator] BRG ($001C_{16}$)

The baud rate generator determines the baud rate for serial transfer. With the 8-bit counter having a reload register the baud rate generator divides the frequency of the count source by 1/(n+1), where n is the value written to the baud rate generator.

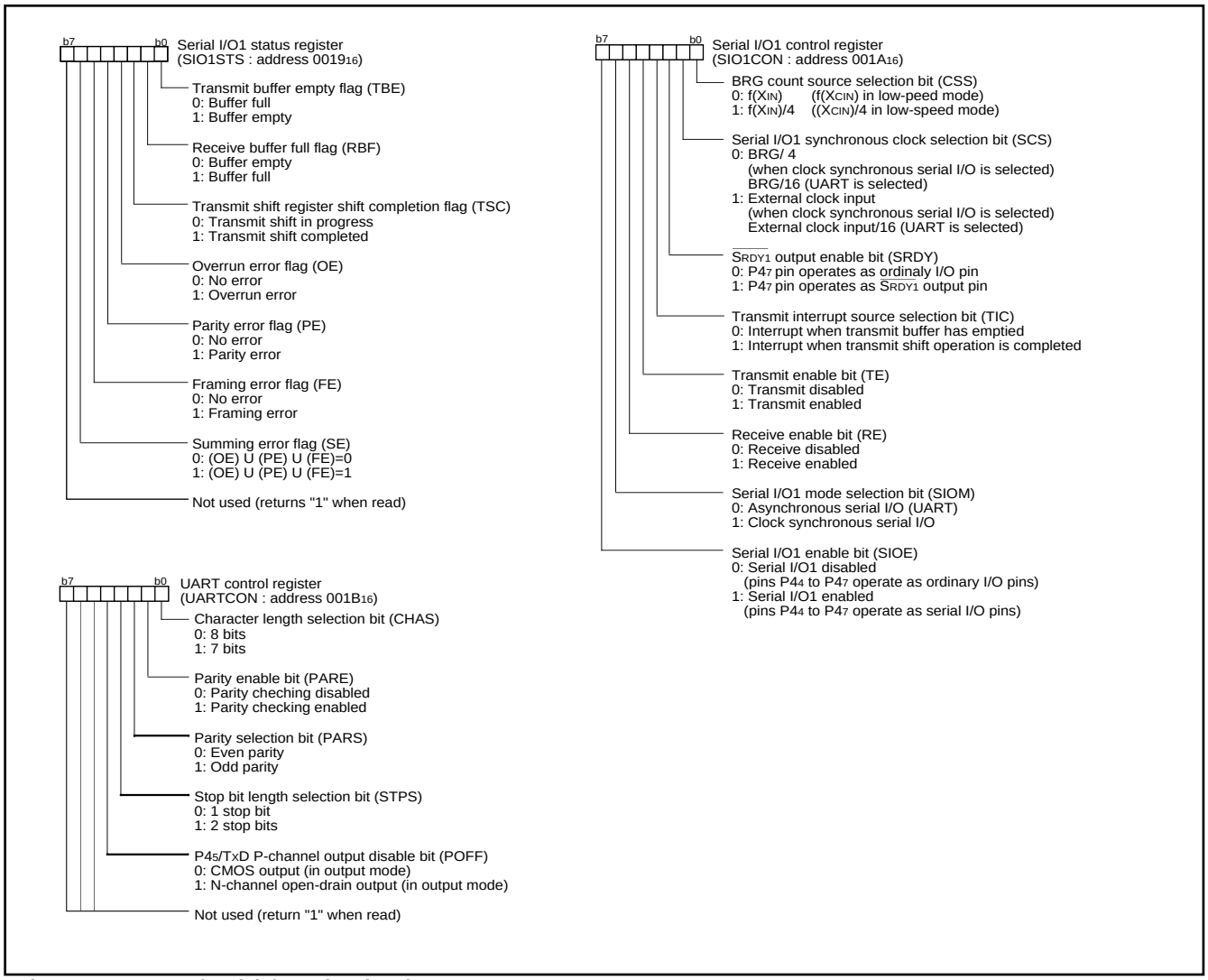


Fig. 37. Structure of serial I/O1 related register

●Serial I/O2

The serial I/O2 can be operated only as the clock synchronous type. As a synchronous clock for serial transfer, either internal clock or external clock can be selected by the serial I/O2 synchronous clock selection bit (b6) of serial I/O2 control register 1.

The internal clock incorporates a dedicated divider and permits selecting 6 types of clock by the internal synchronous clock selection bit (b2, b1, b0) of serial I/O2 control register 1.

Regarding S_{OUT2} and S_{CLK2} being output pins, either CMOS output format or N-channel open-drain output format can be selected by the $P7_1/S_{OUT2}$, $P7_2/S_{CLK2}$ P-channel output disable bit (b7) of serial I/O2 control register 1.

When the internal clock has been selected, a transfer starts by a write signal to the serial I/O2 register (address $001F_{16}$). After completion of data transfer, the level of the S_{OUT2} pin goes to high impedance automatically but bit 7 of the serial I/O2 control register 2 is not set to "1" automatically.

When the external clock has been selected, the contents of the serial I/O2 register is continuously sifted while transfer clocks are input. Accordingly, control the clock externally. Note that the S_{OUT2} pin does not go to high impedance after completion of data transfer.

To cause the S_{OUT2} pin to go to high impedance in the case where the external clock is selected, set bit 7 of the serial I/O2 control register 2 to "1" when S_{CLK2} is "H" after completion of data transfer. After the next data transfer is started (the transfer clock falls), bit 7 of the serial I/O2 control register 2 is set to "0" and the S_{OUT2} pin is put into the active state.

Regardless of the internal clock to external clock, the interrupt request bit is set after the number of bits (1 to 8 bits) selected by the optional transfer bit is transferred. In case of a fractional number of bits less than 8 bits as the last data, the received data to be stored in the serial I/O2 register becomes a fractional number of bits close to MSB if the transfer direction selection bit of serial I/O2 control register 1 is LSB first, or a fractional number of bits close to LSB if the said bit is MSB first. For the remaining bits, the previously received data is shifted.

At transmit operation using the clock synchronous serial I/O, the S_{CMP2} signal can be output by comparing the state of the transmit pin S_{OUT2} with the state of the receive pin S_{IN2} in synchronization with a rise of the transfer clock. If the output level of the S_{OUT2} pin is equal to the input level to the S_{IN2} pin, "L" is output from the S_{CMP2} pin. If not, "H" is output. At this time, an INT_2 interrupt request can also be generated. Select a valid edge by bit 2 of the interrupt edge selection register (address $003A_{16}$).

[Serial I/O2 Control Registers 1, 2] SIO2CON1 / SIO2CON2

The serial I/O2 control registers 1 and 2 are containing various selection bits for serial I/O2 control as shown in Figure 40.

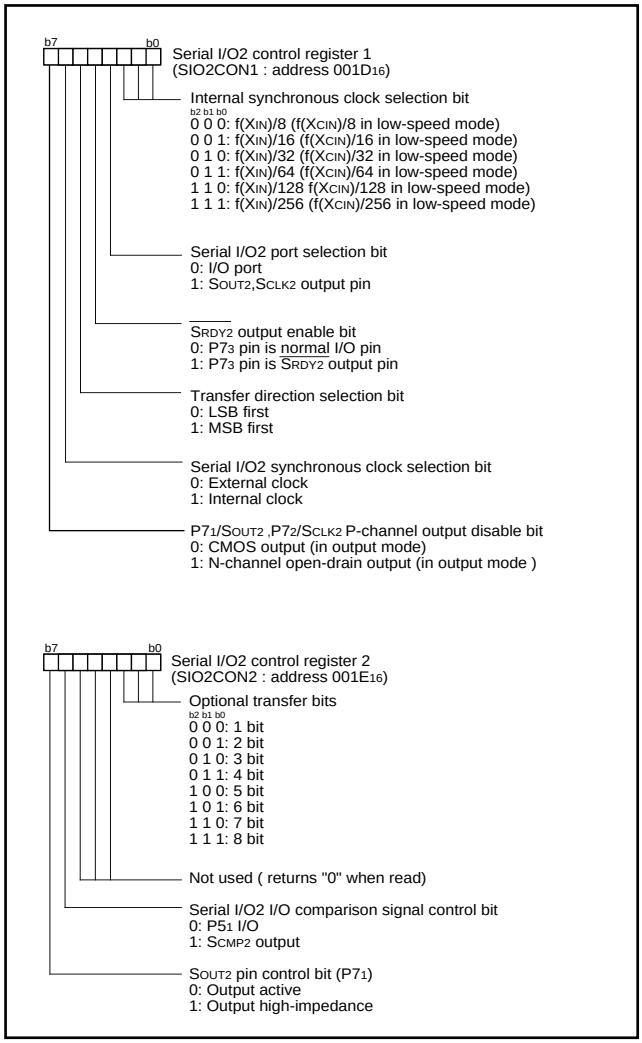
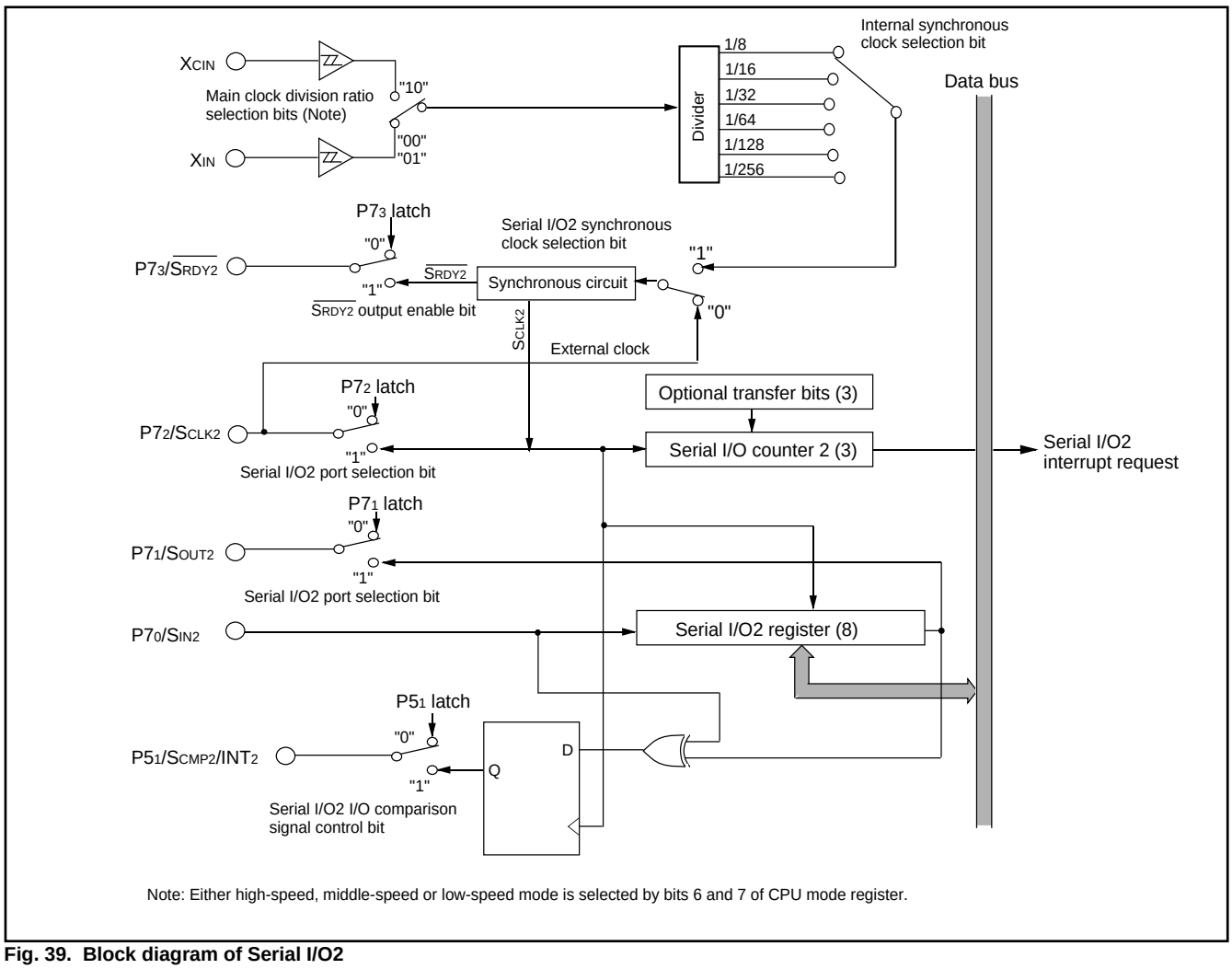
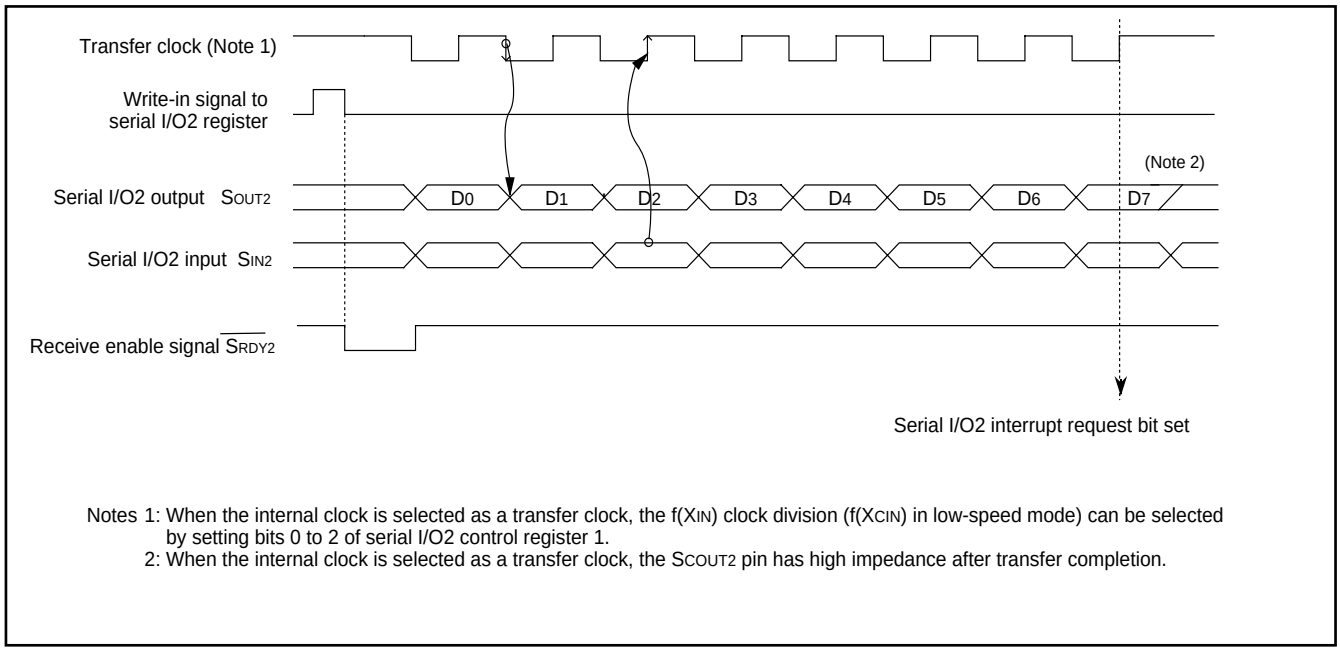


Fig. 38 Structure of Serial I/O2 control registers 1, 2



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 6 and 7 of CPU mode register.

Fig. 39. Block diagram of Serial I/O2



Notes 1: When the internal clock is selected as a transfer clock, the f(XIN) clock division (f(XCIN) in low-speed mode) can be selected by setting bits 0 to 2 of serial I/O2 control register 1.
2: When the internal clock is selected as a transfer clock, the SCOUT2 pin has high impedance after transfer completion.

Fig. 40. Timing chart of Serial I/O2

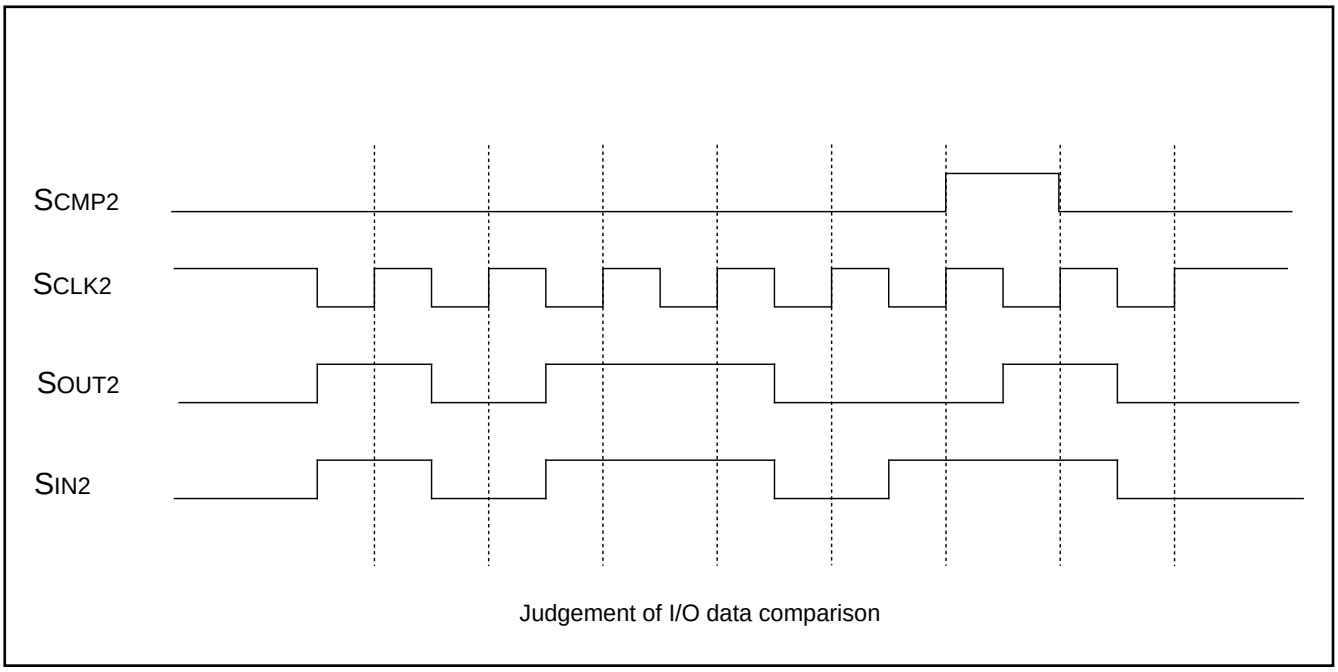


Fig. 41 SCMP2 output operation

A-D Converter

[A-D Conversion Register] AD (address 0035$_{16}$)

The A-D conversion register is a read-only register that contains the result of an A-D conversion. When reading this register during an A-D conversion, the previous conversion result is read.

[A-D Control Register] ADCON

The A-D control register controls the A-D conversion process. Bits 0 to 3 of this register select specific analog input pins. Bit 4 signals the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion, then changes to "1" when the A-D conversion is completed. Writing "0" to this bit starts the A-D conversion. When bit 6, which is the AD external trigger valid bit, is set to "1", this bit enables A-D conversion at a falling edge of an ADT input. Set ports which is also used as ADT pins to input when using an A-D external trigger. Bit 5 is the ADV$_{REF}$ input switch bit. Writing "1" to this bit, this bit always causes ADV$_{REF}$ connection. Writing "0" to this bit causes ADV$_{REF}$ connection only during A-D conversion and cut off when A-D conversion is completed.

[Comparison Voltage Generator]

The comparison voltage generator divides the voltage between AV$_{SS}$ and ADV$_{REF}$ by 256, and outputs the divided voltages.

[Channel Selector]

The channel selector selects one of the input ports AN$_{12}$ to AN$_0$ and inputs it to the comparator.

[Comparator and Control Circuit]

The comparator and control circuit compares an analog input voltage with the comparison voltage and stores the result in the A-D conversion register. When an A-D conversion is completed, the control circuit sets the AD conversion completion bit and the AD conversion interrupt request bit to "1."

Note that the comparator is constructed linked to a capacitor, so set f(X$_{IN}$) to at least 500kHz during A-D conversion. Use a CPU system clock dividing the main clock X$_{IN}$ as the internal clock ϕ.

■Note

When the A-D external trigger is invalidated by the AD external trigger valid bit, any interrupt request is not generated at a fall of the ADT input. When the AD external trigger valid bit is set to "1" beforehand, A-D conversion is not started by writing "0" into the AD conversion completion bit and "0" is not written into the AD conversion completion bit. Do not set "0" in the AD conversion completion bit concurrently with the timing at which the AD external trigger valid bit is rewritten. Put an interval of at least 50 cycles to more of the internal clock ϕ between a start of A-D conversion and the next start of A-D conversion.

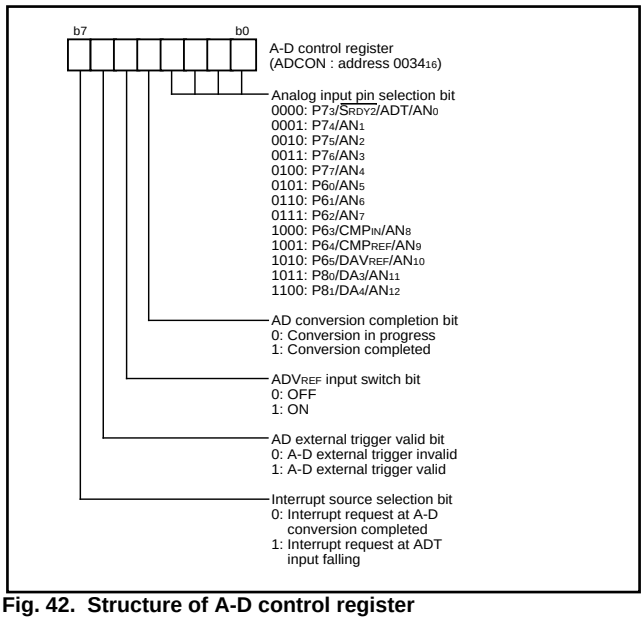


Fig. 42. Structure of A-D control register

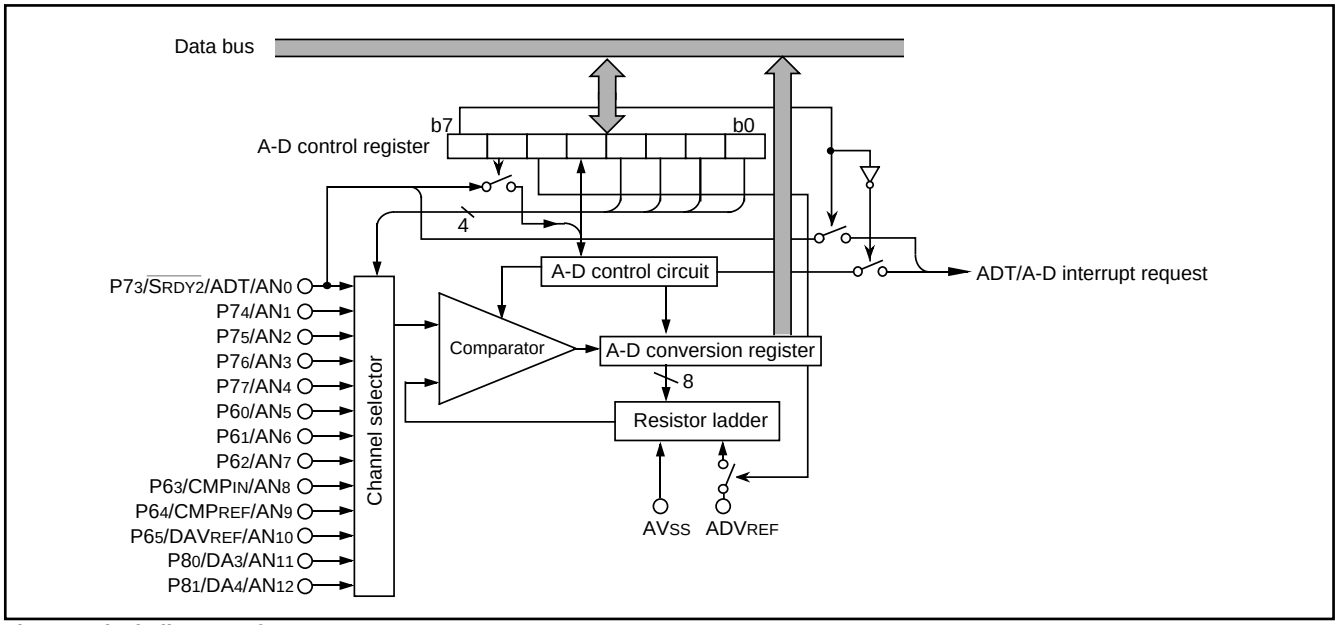


Fig. 43. Block diagram of A-D converter

D-A Converter

The 3807 group has an on-chip D-A converter with 8-bit resolution and 4 channels (DAi (i=1—4)). The D-A converter is performed by setting the value in the D-A conversion register. The result of D-A converter is output from DAi pin by setting the DAi output enable bits to "1." When using the D-A converter, the corresponding port direction register bit ($P6_5/DAV_{REF}/AN_{10}$, $P5_6/DA_1$, $P5_7/DA_2$, $P8_0/DA_3/AN_{11}$, $P8_1/DA_4/AN_{12}$) should be set to "0" (input status).

The output analog voltage V is determined by the value n (base 10) in the D-A conversion register as follows:

$V = DAV_{REF} \times n/256$ (n=0 to 255)

Where DAV_{REF} is the reference voltage.

At reset, the D-A conversion registers are cleared to "00_{16}", the DAi output enable bits are cleared to "0", and DAi pin is set to input (high impedance). The DA output is not buffered, so connect an external buffer when driving a low-impedance load.

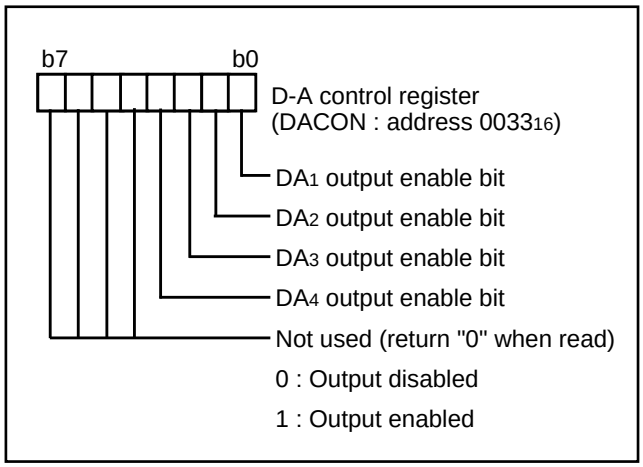


Fig. 44. Structure of D-A control register

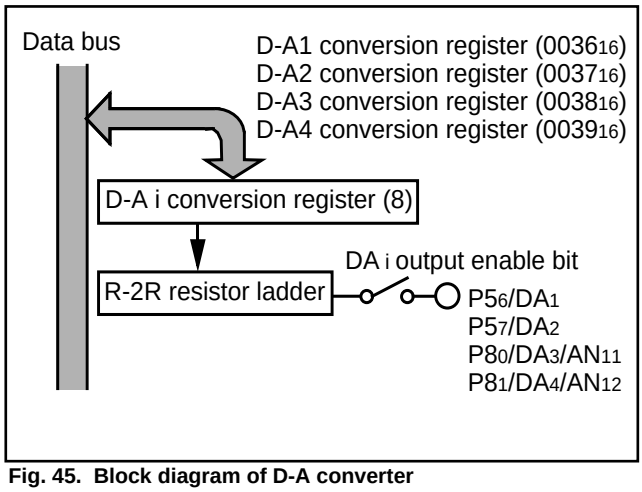


Fig. 45. Block diagram of D-A converter

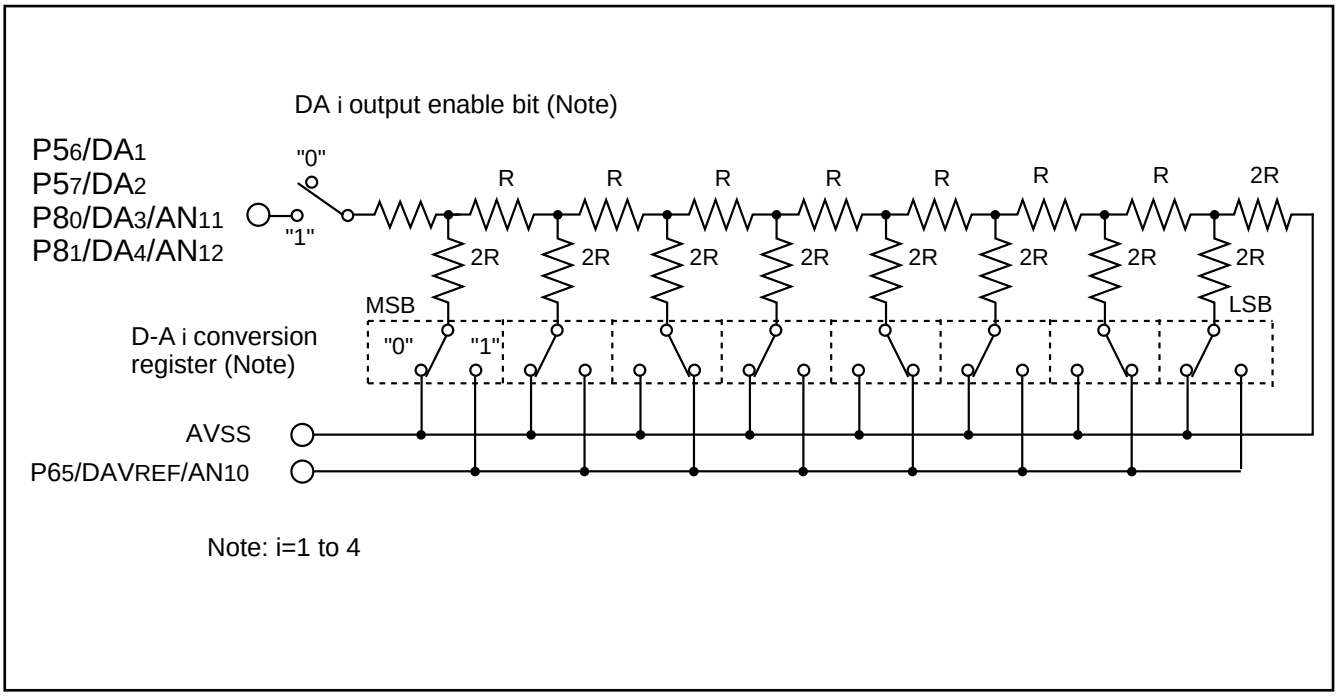


Fig. 46. Equivalent connection circuit of D-A converter

Analog Comparator

An analog comparator circuit which is independent of peripheral circuits in the microcomputer is incorporated (**Note**).
An analog comparator outputs the result of comparison with an input voltage of CMP_{REF} pin which is specified as a reference voltage and an input voltage of CMP_{IN} pin to CMP_{OUT} pin. The result is "1" when the input voltage to port CMP_{IN} is higher than the voltage applied to port CMP_{REF} and "0" when the voltage is lower.
Because the analog comparator consists of an analog MOS circuit, set the input voltage to the CMP_{IN} pin and the CMP_{REF} pin within the following range :

V_{SS} +1.2 V to $CMPV_{CC}$–0.5V

■Note

The analog comparator circuit is separated from the MCU internal peripheral circuit in the microcomputer. Accordingly, even if the microcomputer runs away, the analog comparator is still in operation. For this reason, the analog comparator can be used for safety circuit design.

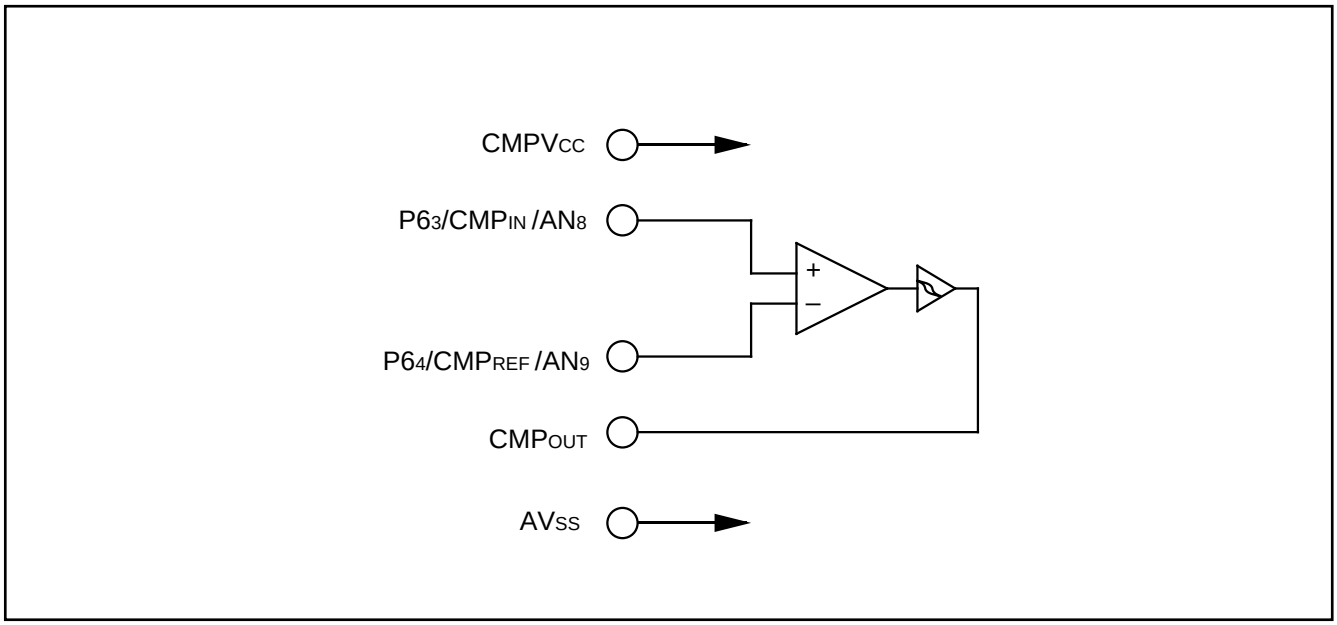


Fig. 47. Block diagram of Analog comparator

Watchdog Timer

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and a 8-bit watchdog timer H.

●Standard operation of watchdog timer

When any data is not written into the watchdog timer control register (address 0017_{16}) after resetting, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0017_{16}) and an internal resetting takes place at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0017_{16}) may be started before an underflow. When the watchdog timer control register (address 0017_{16}) is read, the values of the 6 high-order bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

(1) Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0017_{16}), each watchdog timer H and L is set to "FF_{16}."

(2) Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0017_{16}) permits selecting a watchdog timer H count source. When this bit is set to "0", the count source becomes the underflow signal of watchdog timer L. The detection time is set then to f(X_{IN})=131.072 ms at 8 MHz frequency and f(X_{CIN})=32.768 s at 32 kHz frequency.

When this bit is set to "1", the count source becomes the signal divided by 16 for f(X_{IN}) (or f(X_{CIN})). The detection time in this case is set to f(X_{IN})=512 µs at 8 MHz frequency and f(X_{CIN})=128 ms at 32 KHz frequency. This bit is cleared to "0" after resetting.

(3) Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0017_{16}) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is "0", the STP instruction is enabled.

When this bit is "1", the STP instruction is disabled.

Once the STP instruction is executed, an internal resetting takes place.

When this bit is set to "1", it cannot be rewritten to "0" by program.

This bit is cleared to "0" after resetting.

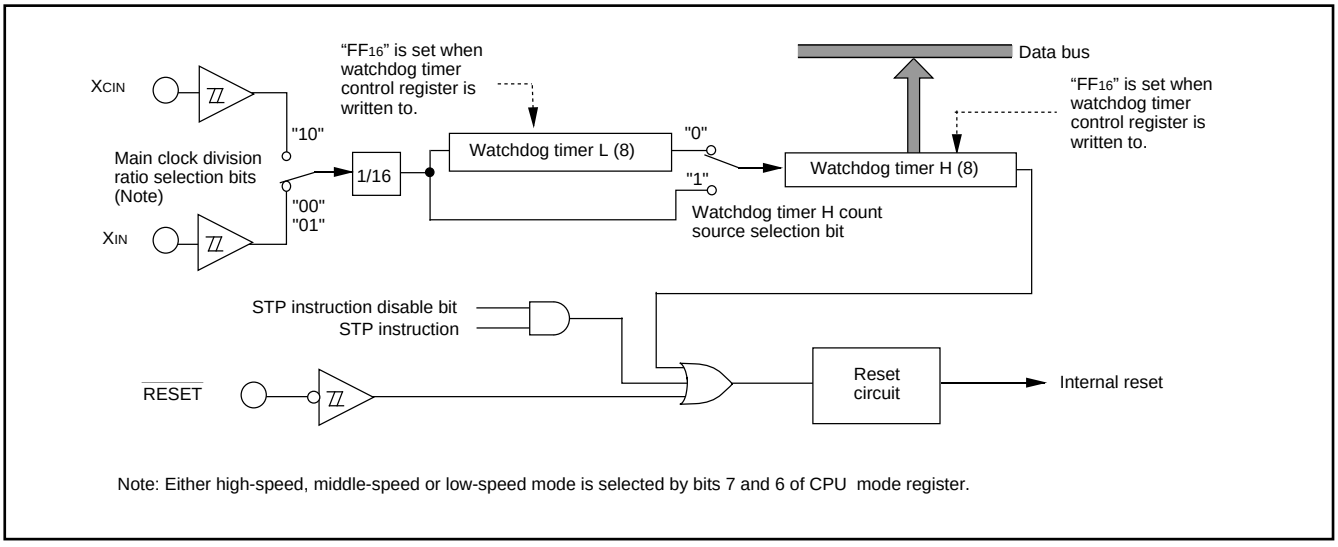


Fig. 48. Block diagram of Watchdog timer

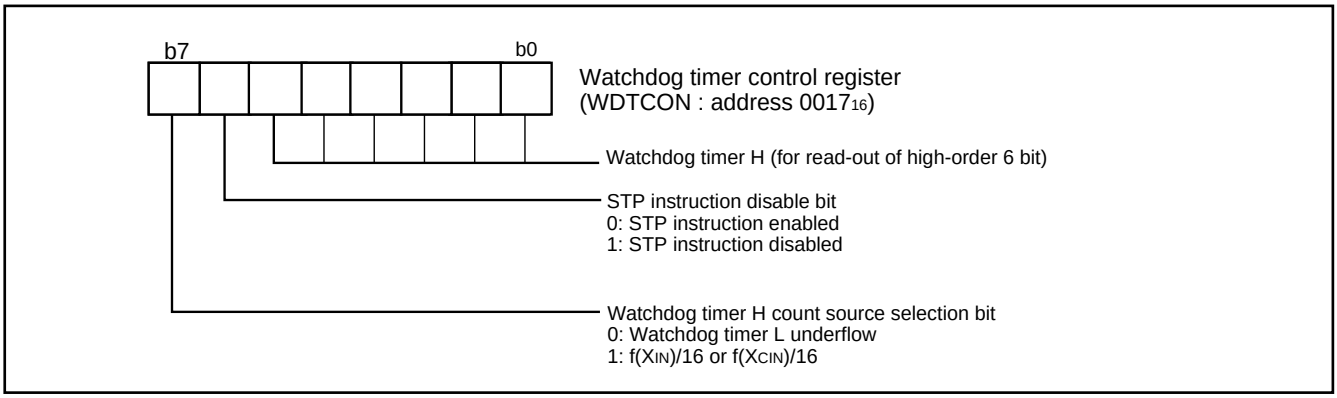


Fig. 49. Structure of Watchdog timer control register

Clock output function

The internal clock ϕ can be output from I/O port P3$_4$. Control of I/O ports and clock output function can be performed by port P2P3 control register (address 0015$_{16}$).

(1) I/O ports or clock output function selection

The P3$_4$ clock output control bit (b0) of port P2P3 control register selects the I/O port or clock output function. When clock output function is selected, the clock is output regardless of the port P3$_4$ direction register settings.

Directly after bit 0 is written to, the port or clock output is switched synchronous to a falling edge of clock frequency selected by the output clock frequency selection bit. When memory expansion mode or microprocessor mode is selected in CPU mode register (b1, b0), clock output is selected on regardless of P3$_4$ clock output control bit settings or port P3$_4$ direction register settings.

(2) Selection of output clock frequency

The output clock frequency selection bits (b3, b2, b1) of port P2P3 control register select the output clock frequency.

The output waveform when f(X$_{IN}$) or f(X$_{CIN}$) is selected, depends on X$_{IN}$ or X$_{CIN}$ input waveform however; all other output waveform settings have a duty cycle of 50%.

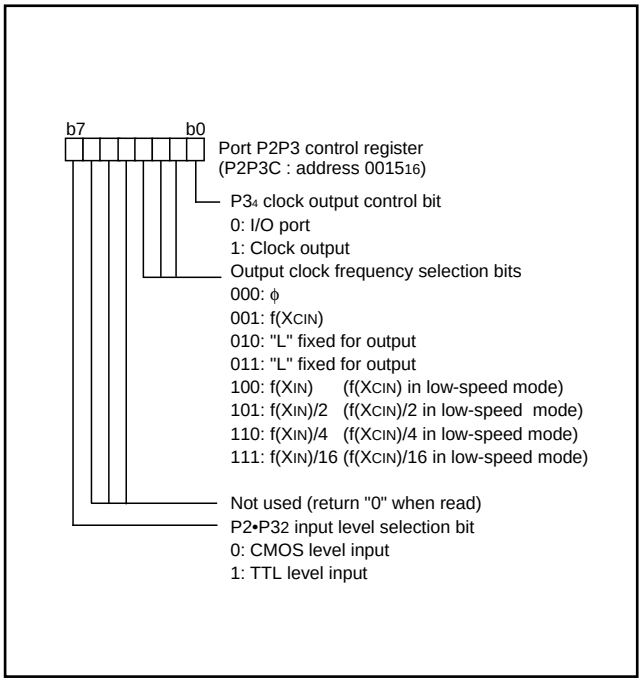
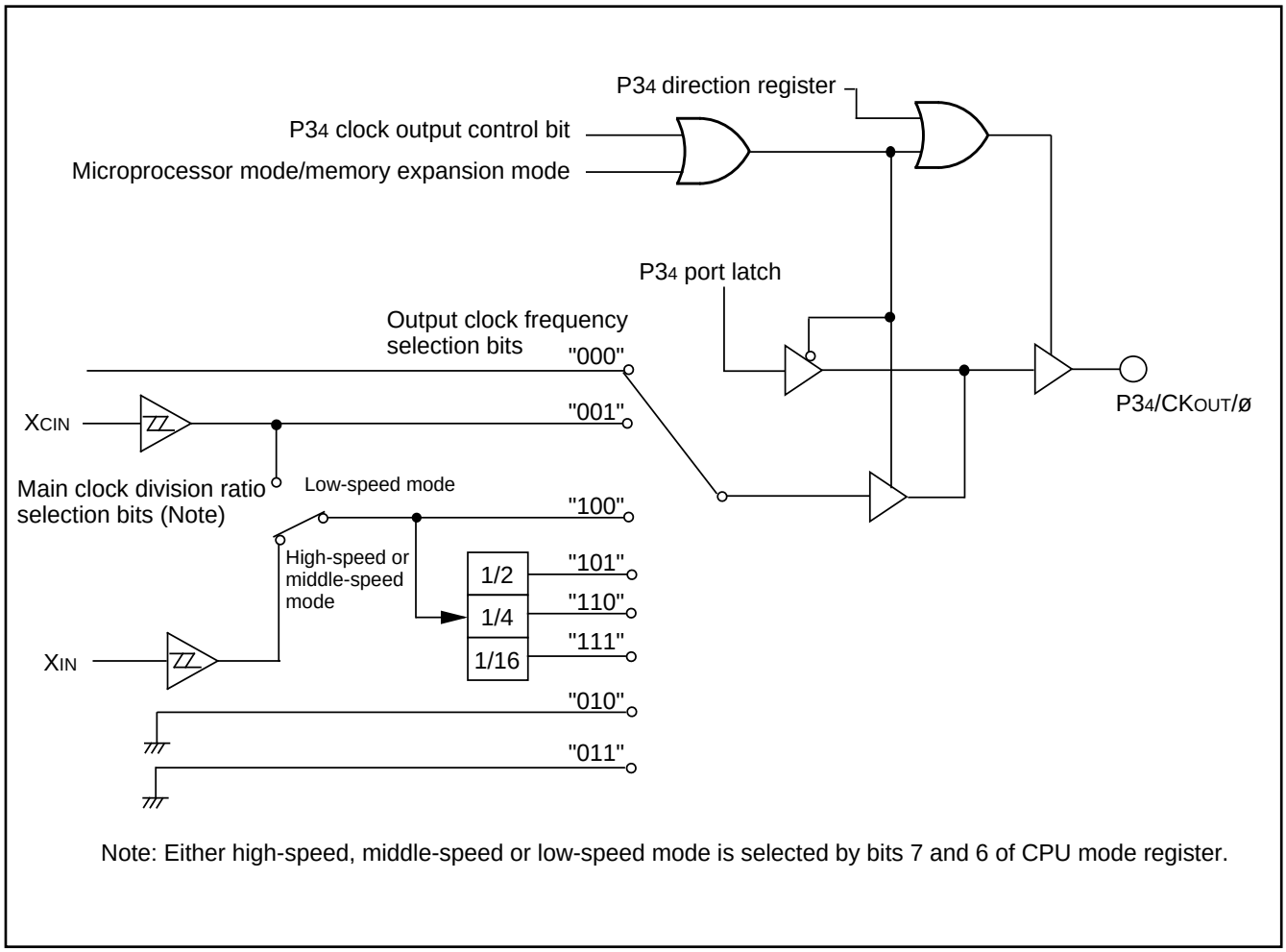


Fig. 50. Structure of Port P2P3 control register



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of CPU mode register.

Fig. 51. Block diagram of Clock output function

Reset Circuit

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 2 μs or more. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.7 V and 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address contained in address FFFD_{16} (high-order byte) and address FFFC_{16} (low-order byte). Make sure that the reset input voltage is less than 0.54 V for V_{CC} of 2.7 V.

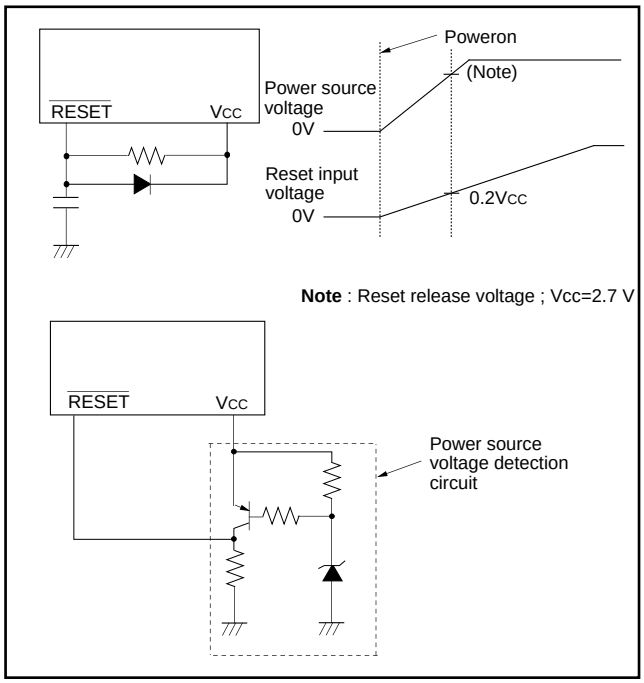


Fig. 52. Reset circuit example

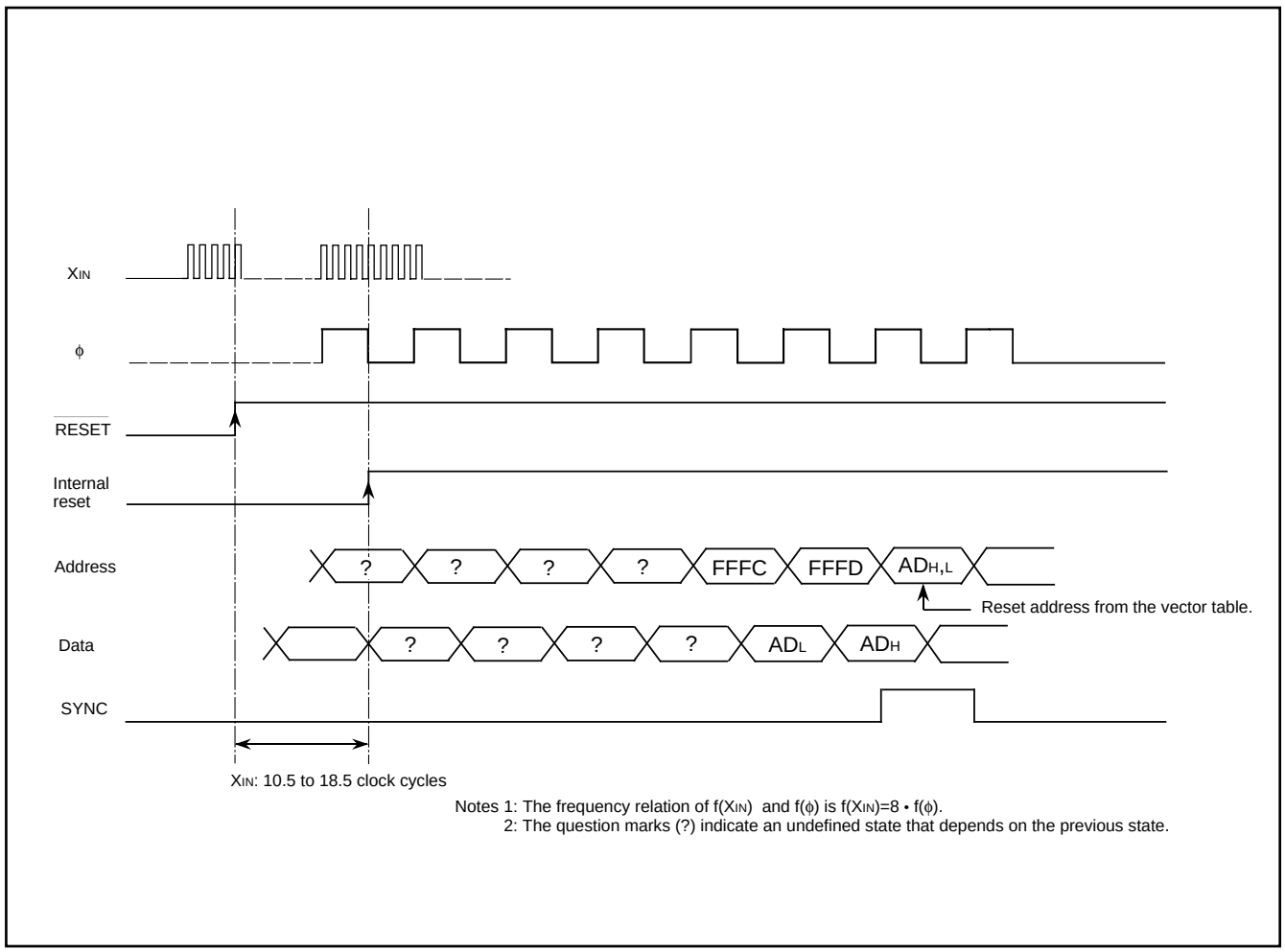


Fig. 53. Reset sequence

	Address	Register contents
(1) Port P0	0000_{16}	00_{16}
(2) Port P0 direction register	0001_{16}	00_{16}
(3) Port P1	0002_{16}	00_{16}
(4) Port P1 direction register	0003_{16}	00_{16}
(5) Port P2	0004_{16}	00_{16}
(6) Port P2 direction register	0005_{16}	00_{16}
(7) Port P3	0006_{16}	00_{16}
(8) Port P3 direction register	0007_{16}	00_{16}
(9) Port P4	0008_{16}	00_{16}
(10) Port P4 direction register	0009_{16}	00_{16}
(11) Port P5	$000A_{16}$	00_{16}
(12) Port P5 direction register	$000B_{16}$	00_{16}
(13) Port P6	$000C_{16}$	00_{16}
(14) Port P6 direction register	$000D_{16}$	00_{16}
(15) Port P7	$000E_{16}$	00_{16}
(16) Port P7 direction register	$000F_{16}$	00_{16}
(17) Port P8	0010_{16}	00_{16}
(18) Port P8 direction register	0011_{16}	00_{16}
(19) Timer XY control register	0014_{16}	0 0 0 0 0 0 1 1
(20) Port P2P3 control register	0015_{16}	* 0 0 0 0 0 0 0
(21) Pull-up control register	0016_{16}	00_{16}
(22) Watchdog timer control register	0017_{16}	0 0 1 1 1 1 1 1
(23) Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 0
(24) Serial I/O1 control register	$001A_{16}$	00_{16}
(25) UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(26) Serial I/O2 control register 1	$001D_{16}$	00_{16}
(27) Serial I/O2 control register 2	$001E_{16}$	0 0 0 0 0 1 1 1
(28) Timer X (low-order)	0020_{16}	FF_{16}
(29) Timer X (high-order)	0021_{16}	FF_{16}
(30) Timer Y (low-order)	0022_{16}	FF_{16}
(31) Timer Y (high-order)	0023_{16}	FF_{16}
(32) Timer 1	0024_{16}	FF_{16}
(33) Timer 2	0025_{16}	01_{16}

	Address	Register contents
(34) Timer 3	0026_{16}	FF_{16}
(35) Timer X mode register	0027_{16}	00_{16}
(36) Timer Y mode register	0028_{16}	00_{16}
(37) Timer 123 mode register	0029_{16}	00_{16}
(38) Real time port register 0—7	$002A_{16}$	00_{16}
(39) Real time port control register 0	$002B_{16}$	1 0 0 1 0 0 0 0
(40) Real time port control register 1	$002C_{16}$	1 – – – 0 0 0 0
R/W pointer		– 1 1 1 – – – –
Output pointer		– 1 1 1 – – – –
(41) Real time port control register 2	$002D_{16}$	1 – – – 0 0 0 0
R/W pointer		– 1 1 1 – – – –
Output pointer		– 1 1 1 – – – –
(42) Real time port control register 3	$002E_{16}$	00_{16}
(43) Timer A (low-order)	$002F_{16}$	FF_{16}
(44) Timer A (high-order)	0030_{16}	FF_{16}
(45) Timer B (low-order)	0031_{16}	FF_{16}
(46) Timer B (high-order)	0032_{16}	FF_{16}
(47) D-A control register	0033_{16}	00_{16}
(48) A-D control register	0034_{16}	0 0 0 1 0 0 0 0
(49) D-A1 conversion register	0036_{16}	00_{16}
(50) D-A2 conversion register	0037_{16}	00_{16}
(51) D-A3 conversion register	0038_{16}	00_{16}
(52) D-A4 conversion register	0039_{16}	00_{16}
(53) Interrupt edge selection register	$003A_{16}$	00_{16}
(54) CPU mode register	$003B_{16}$	0 1 0 0 1 0 * 0
(55) Interrupt request register 1	$003C_{16}$	00_{16}
(56) Interrupt request register 2	$003D_{16}$	00_{16}
(57) Interrupt control register 1	$003E_{16}$	00_{16}
(58) Interrupt control register 2	$003F_{16}$	00_{16}
(59) Processor status register	(PS)	X X X X X 1 X X
(60) Program counter	(PC_H)	$FFFD_{16}$ contents
	(PC_L)	$FFFC_{16}$ contents

* The initial values depend on level of port CNV_{SS}.

X: Not fixed

Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 54. Internal status at reset

Clock Generating Circuit

The 3807 group has two built-in oscillation circuits. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

●Frequency control

(1) Middle-speed mode

The internal clock ϕ is the frequency of XIN divided by 8. After reset, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of XIN.

(3) Low-speed mode

The internal clock ϕ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3f(XCIN).

(4) Low power consumption mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1." When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set enough time for oscillation to stabilize.

By clearing furthermore the XCOUT drivability selection bit (b3) of CPU mode register to "0", low power consumption operation of less than 55 µA (VCC=3 V, XCIN=32 kHz) can be realized by reducing the drivability between XCIN and XCOUT. At reset or during STP instruction execution this bit is set to "1" and a reduced drivability that has an easy oscillation start is set. The sub-clock XCIN-XCOUT oscillating circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

●Oscillation control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and XIN and XCIN oscillators stop. Timer 1 is set to "FF16" and timer 2 is set to "0116."

Either XIN or XCIN divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2. The bits of the timer 123 mode register except timer 3 count source selection bit (b4) are cleared to "0". Set the timer 2/INT3 interrupt source bit to "1" and timer 1/INT2 as well as timer 2/INT3 interrupt enable bit to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize. The internal clock ϕ is supplied for the first time, when timer 2 underflows. Therefore make sure not to set the timer 2/INT3 interrupt request bit to "1" before the STP instruction stops the oscillator. When the oscillator is restarted by reset apply "L" level to port $\overline{\text{RESET}}$ until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level. The states of XIN and XCIN are the same as the state before executing the WIT instruction. The internal clock restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

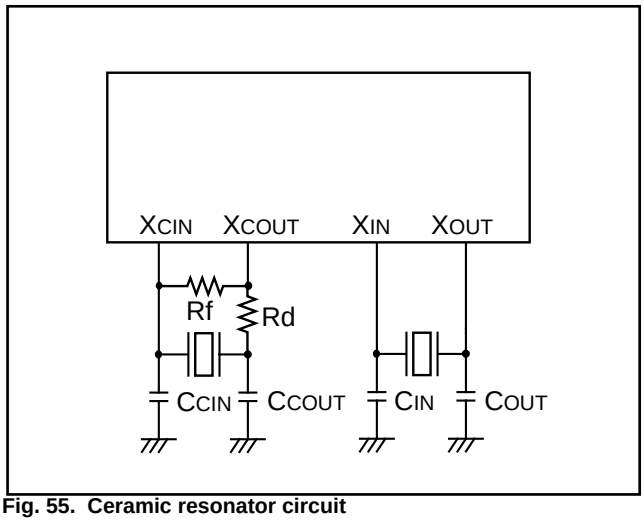


Fig. 55. Ceramic resonator circuit

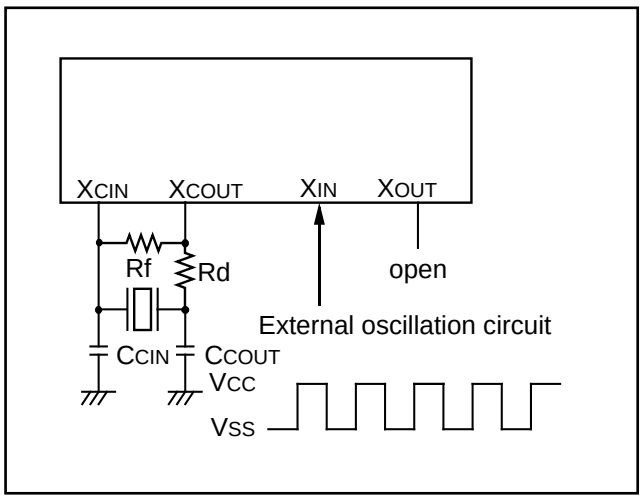
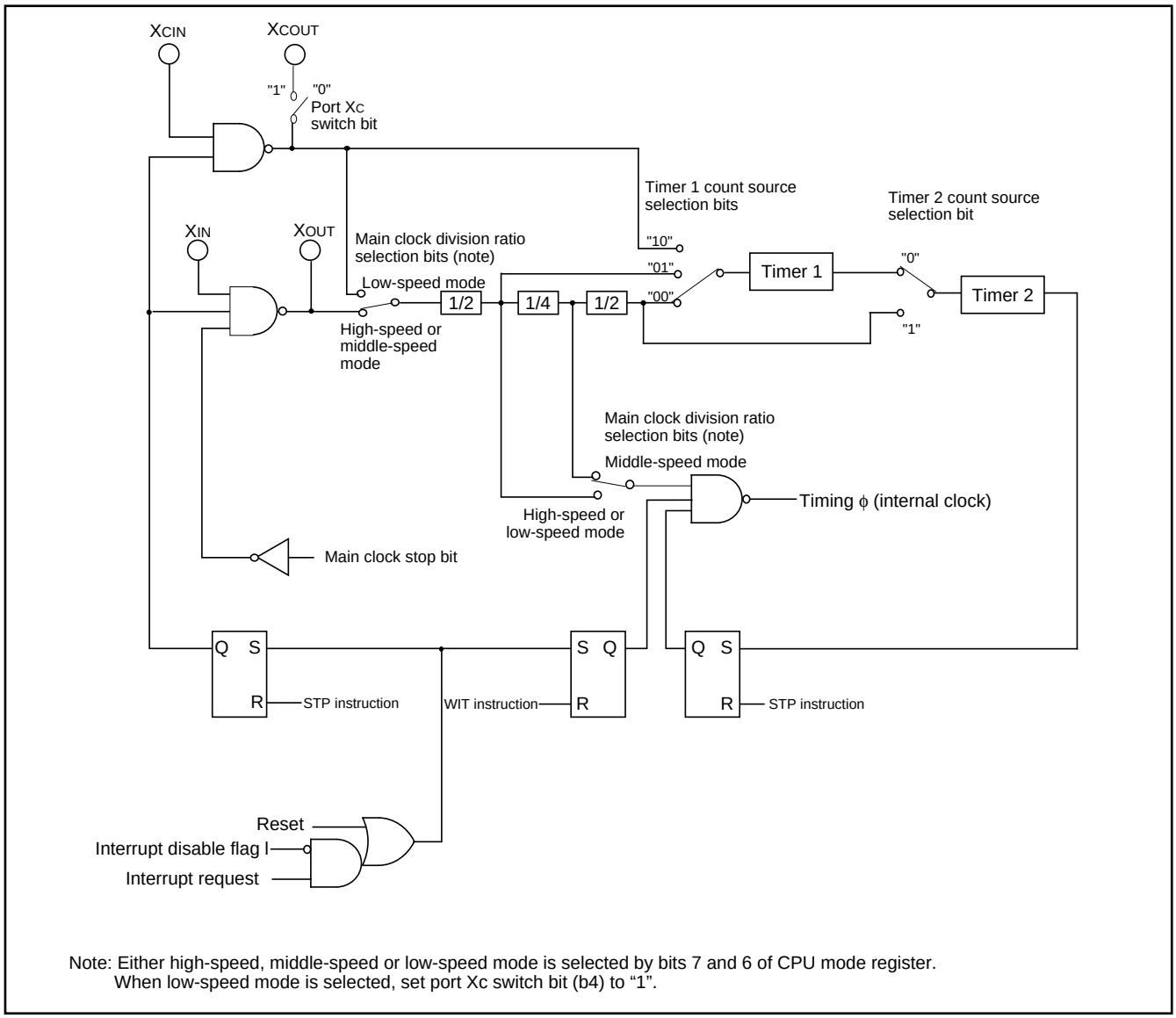
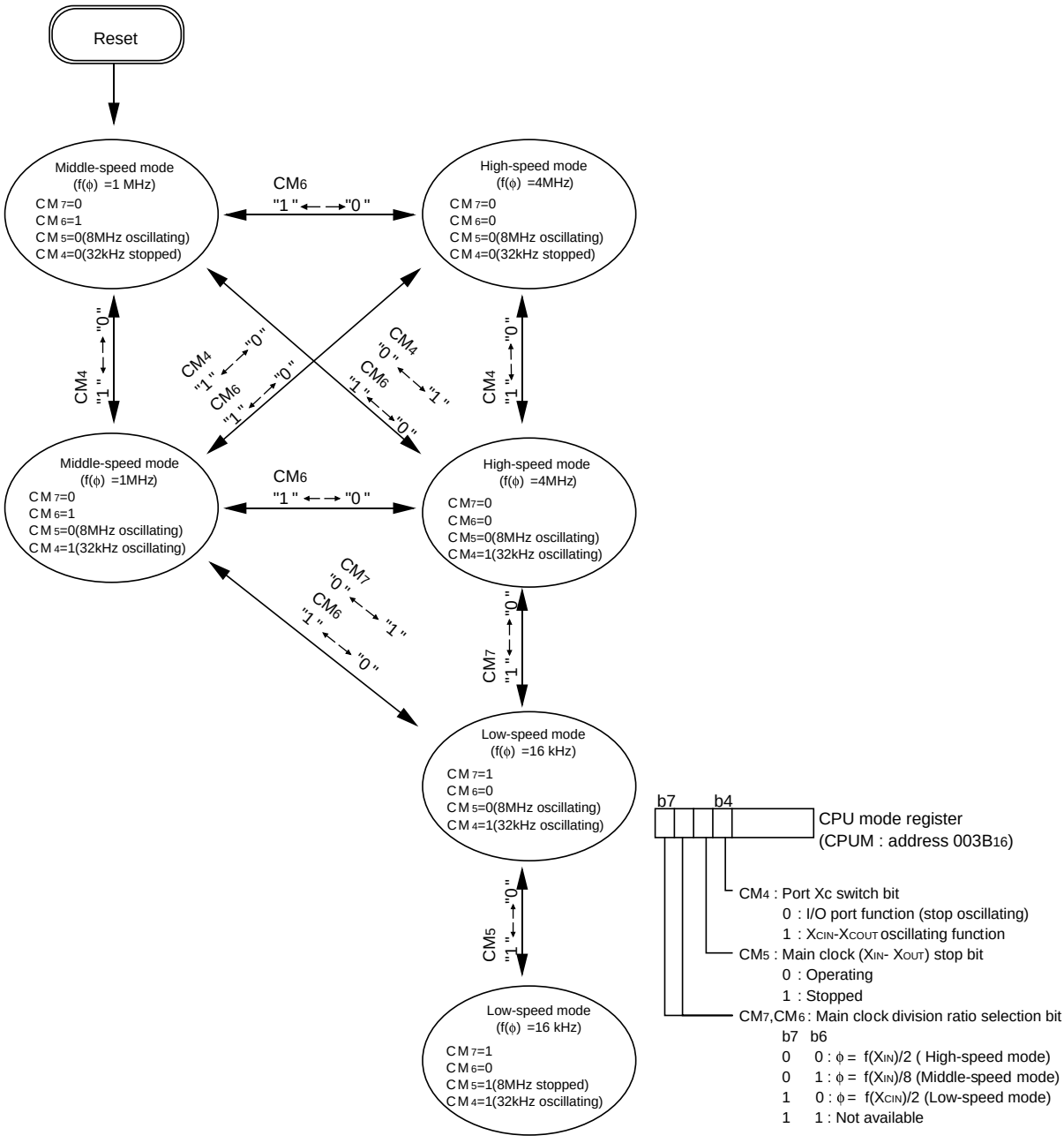


Fig. 56. External clock input circuit



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of CPU mode register.
When low-speed mode is selected, set port Xc switch bit (b4) to “1”.

Fig. 57. System clock generating circuit block diagram (Single-chip mode)



Note 1:Switch the mode by the allows shown between the mode blocks. (Do not switch between the mode directly without an allow.)
2:The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3:Timer operates in the wait mode.
4:When the stop mode is ended, a delay of approximately 1 ms occurs by Timer 1 and Timer 2 in middle/high-speen mode.
5:When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 and Timer 2 in low-speed mode.
6:Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.
7:The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. ϕ indicates the internal clock.

Fig. 58. State transitions of system clock

Processor Mode

Single-chip mode, memory expansion mode, and microprocessor mode can be selected by changing the contents of the processor mode bits (CM_0 and CM_1 : b1 and b0 of address $003B_{16}$). In memory expansion mode and microprocessor mode, memory can be expanded externally through ports P0 to P3. In these modes, ports P0 to P3 lose their I/O port functions and become bus pins.

Table. 7. Port functions in memory expansion mode and microprocessor mode

Port Name	Function
Port P0	Outputs 8-bits low-order byte of address.
Port P1	Outputs 8-bits high-order byte of address.
Port P2	Operates as I/O pins for data D_7 to D_0 (including instruction code)
Port P3	$P3_0$ and $P3_1$ function only as output pins (except that the port latch cannot be read). $P3_2$ is the $\overline{ONW}$ input pin. $P3_3$ is the $REST_{OUT}$ output pin. (**Note**) $P3_4$ is the ϕ output pin. $P3_5$ is the SYNC output pin. $P3_6$ is the $\overline{WR}$ output pin, and $P3_7$ is the $\overline{RD}$ output pin.

Note : If CNV_{SS} is connected to V_{SS}, the microcomputer goes to single-chip mode after a reset, so this pin cannot be used as the $RESET_{OUT}$ output pin.

(1) Single-chip mode

Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{SS}.

(2) Memory expansion mode

Select this mode by setting the processor mode bits (b1, b0) to "01" in software with CNV_{SS} connected to V_{SS}. This mode enables external memory expansion while maintaining the validity of the internal ROM. However, some I/O devices will not support the memory expansion mode. Internal ROM will take precedence over external memory if addresses conflict.

(3) Microprocessor mode

Select this mode by resetting the microcomputer with CNV_{SS} connected to V_{CC}, or by setting the processor mode bits to "10" in software with CNV_{SS} connected to V_{SS}. In microprocessor mode, the internal ROM is no longer valid and external memory must be used.

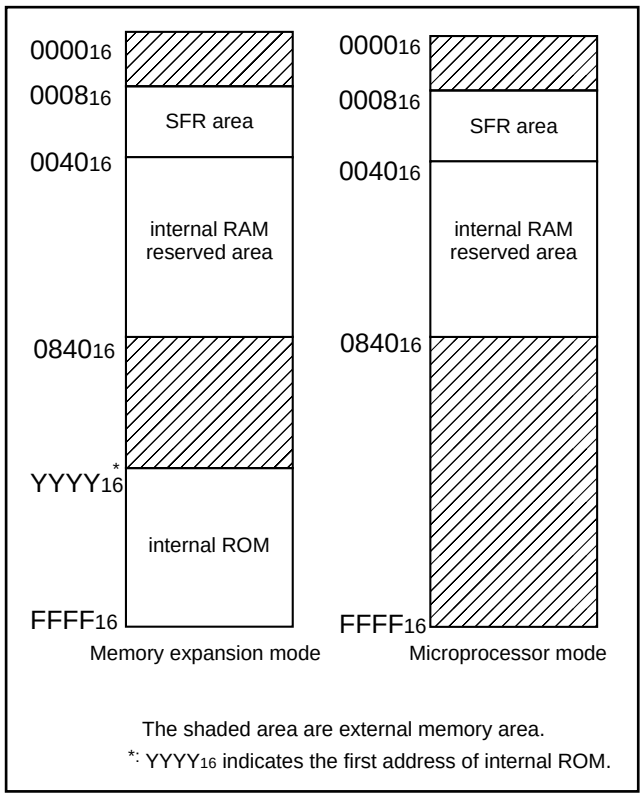


Fig. 59. Memory maps in various processor modes

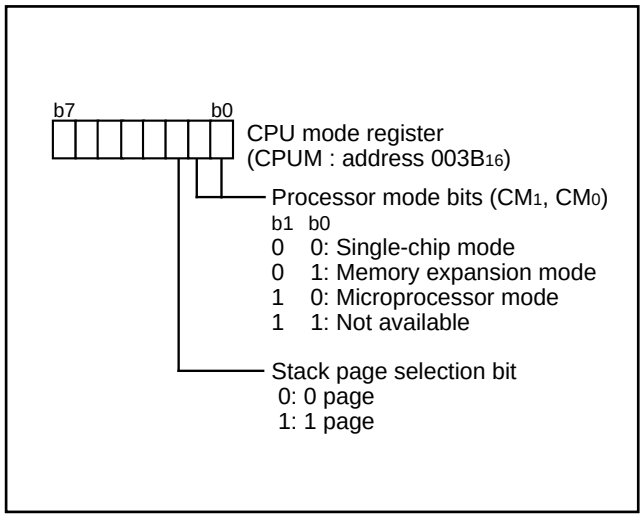
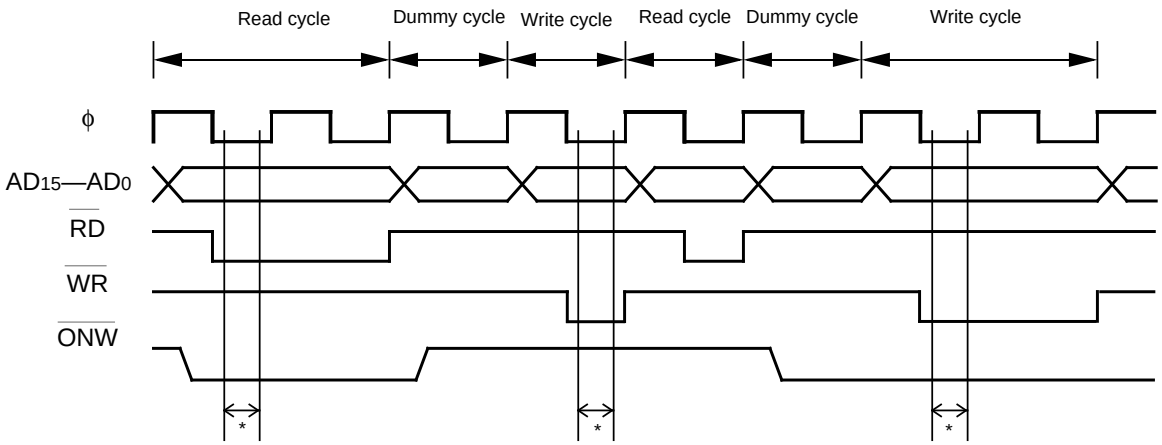


Fig. 60. Structure of CPU mode register

Bus control at memory expansion

The 3807 group has a built-in $\overline{ONW}$ function to facilitate access to external (expanded) memory and I/O devices in memory expansion mode or microprocessor mode.

If an "L" level signal is input to port P3$_2$/$\overline{ONW}$ when the CPU is in a read or write state, the corresponding read or write cycle is extended by one cycle of ϕ. During this extended period, the $\overline{RD}$ or $\overline{WR}$ signal remains at "L". This extension function is valid only for writing to and reading from addresses 0000_{16} to 0007_{16} and 0840_{16} to $FFFF_{16}$, and only read and write cycles are extended.



* Period during which $\overline{ONW}$ input signal is received
During this period, the $\overline{ONW}$ signal must be fixed at either "H" or "L". At all times, the input level of the $\overline{ONW}$ signal has no affect on operations. The bus cycles is not extended for an address in the area 0008_{16} to $083F_{16}$, regardless of whether the $\overline{ONW}$ signal is received.

Fig. 61. $\overline{ONW}$ function timing

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1." After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. Only the ADC and SBC instructions yield proper decimal results. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the S_{RDY1} signal, set the transmit enable bit, the receive enable bit, and the S_{RDY1} output enable bit to "1."

Serial I/O1 continues to output the final bit from the T_XD pin after transmission is completed. S_{OUT2} pin for serial I/O2 goes to high impedance after transfer is completed.

When in serial I/O1 (clock-synchronous mode) or in serial I/O2 an external clock is used as synchronous clock, write transmission data to both the transmit buffer register and serial I/O2 register, during transfer clock is “H.”

A-D Converter

The comparator uses internal capacitors whose charge will be lost if the clock frequency is too low.

Therefore, make sure that $f(X_{IN})$ is at least on 500 kHz during an A-D conversion. (When the $\overline{ONW}$ pin has been set to "L", the A-D conversion will take twice as long to match the longer bus cycle, and so $f(X_{IN})$ must be at least 1 MHz.)

Do not execute the STP or WIT instruction during an A-D conversion.

D-A Converter

The accuracy of the D-A converter becomes rapidly poor under the V_{CC} = 4.0 V or less condition; a supply voltage of $V_{CC} \geq 4.0$ V is recommended. When a D-A converter is not used, set all values of D-Ai conversion registers (i=1 to 4) to "00_{16}."

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the X_{IN} frequency in high-speed mode.

When the $\overline{ONW}$ function is used in modes other than single-chip mode, the frequency of the internal clock ϕ may be one fourth of the X_{IN} frequency.

NOTES ON USAGE

Handling of Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (V_{CC} pin) and GND pin (Vss pin) and between power source pin (V_{CC} pin) and analog power source input pin (AV_{SS} pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μF—0.1 μF is recommended.

$P3_4$ clock output function

In the case of using an I/O port $P3_4$ as a clock output function, note the following : when an output clock frequency is changed during outputting a clock, the port may feed a noise having a shorter pulse width than the standard at the switch timing. Besides, it also may happen at the timing for switching the low-speed mode to the middle/high-speed mode.

Timer X and timer Y

In the pulse period measurement mode or the pulse width measurement mode for timers X and Y, set the "L" or "H" pulse width of input signal from $CNTR_0$/$CNTR_1$ pin to 2 cycles or more of a timer count source.

EPROM version/One Time PROM version

The CNV_{SS} pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (V_{PP} pin) as well.
To improve the noise reduction, connect a track between CNV_{SS} pin and V_{SS} pin or V_{CC} pin with 1 to 10 kΩ resistance.
The mask ROM version track of port CNV_{SS} has no operational interference even if it is connected via a resistor.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form (three identical copies)

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table. 8. Special programming adapter

Package	Name of Programming Adapter
80P6N-A	PCA4738F-80A
80D0	PCA4738L-80A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 64 is recommended to verify programming.

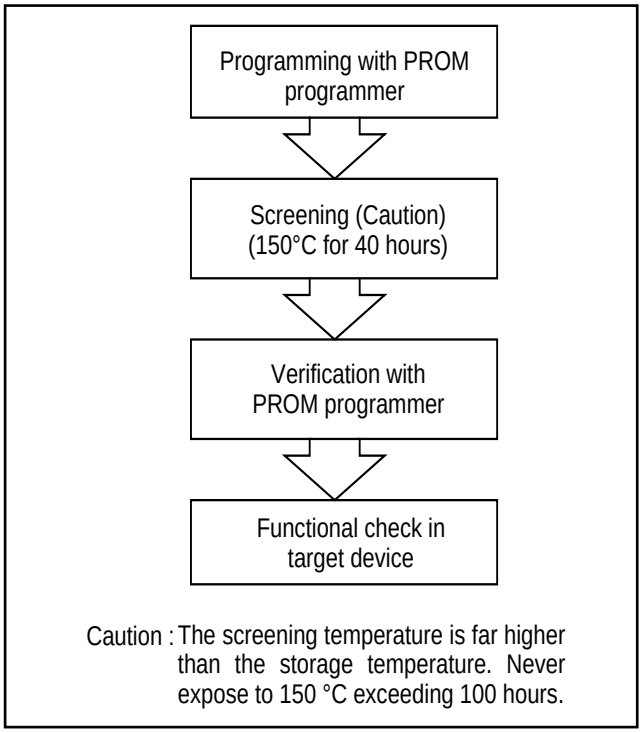


Fig. 62. Programming and testing of One Time PROM version

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Table 9 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 7.0	V
CMPV_{CC}	Analog comparator power source voltage		–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, ADV_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage CNV_{SS} (ROM version)		–0.3 to 7	V
V_I	Input voltage CNV_{SS} (PROM version)		–0.3 to 13	V
V_I	In-phase input voltage CMP_{IN}, CMP_{REF}		–0.3 to CMPV_{CC} +0.3	V
V_{ID}	Differential input voltage $\lvert CMP_{IN}–CMP_{REF}\rvert$		CMPV_{CC}	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage CMP_{OUT}		–0.3 to CMPV_{CC} +0.3	V
P_d	Power dissipation	Ta = 25°C	500	mW
T_{opr}	Operating temperature		–20 to 85	°C
T_{stg}	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

Table 10 Recommended operating conditions (1) (Vcc = 2.7 to 5.5 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
V_{CC}	Power source voltage	f(X_{IN}) ≦ 4.1MHz	2.7	5.0	5.5	V
		f(X_{IN}) = 8MHz	4.0	5.0	5.5	V
V_{SS}	Power source voltage			0		V
ADV_{REF}	A-D comparator reference voltage		2.0		V_{CC}	V
DAV_{REF}	D-A comparator reference voltage		2.7		V_{CC}	V
$CMPV_{CC}$	Analog comparator power source voltage			V_{CC}		V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	A-D comparator input voltage	AN_0—AN_{12}	AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	$P0_0$—$P0_7$, $P1_0$—$P1_7$, $P3_0$, $P3_1$, $P3_3$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_5$, $P7_0$—$P7_7$, $P8_0$—$P8_7$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (CMOS input level selected)	$P2_0$—$P2_7$, $P3_2$	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (TTL input level selected)	$P2_0$—$P2_7$, $P3_2$ (Note)	2.0		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	$P0_0$—$P0_7$, $P1_0$—$P1_7$, $P3_0$, $P3_1$, $P3_3$—$P3_7$, $P4_0$—$P4_7$, $P5_0$—$P5_7$, $P6_0$—$P6_5$, $P7_0$—$P7_7$, $P8_0$—$P8_7$	0		0.2V_{CC}	V
V_{IL}	“L” input voltage (CMOS input level selected)	$P2_0$—$P2_7$, $P3_2$	0		0.2V_{CC}	V
V_{IL}	“L” input voltage (TTL input level selected)	$P2_0$—$P2_7$, $P3_2$ (Note)	0		0.8	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V

Note: When Vcc is 4.0 to 5.5 V.

Table 11 Recommended operating conditions (2) (Vcc = 2.7 to 5.5 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$\Sigma I_{OH(peak)}$	“H” total peak output current (Note)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			–80	mA
$\Sigma I_{OH(peak)}$	“H” total peak output current (Note)	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$			–80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note) $P2_4$–$P2_7$	in single chip mode			80	mA
		in memory expansion mode and microprocessor mode			80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current (Note)	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$			80	mA
$\Sigma I_{OH(avg)}$	“H” total average output current (Note)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			–40	mA
$\Sigma I_{OH(avg)}$	“H” total average output current (Note)	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$			–40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P8_0$–$P8_7$			40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note) $P2_4$–$P2_7$	in single chip mode			40	mA
		in memory expansion mode and microprocessor mode			40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current (Note)	$P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$			40	mA

Note: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100ms. The total peak current is the peak value of all the currents.

Table 12 Recommended operating conditions (3) (Vcc = 2.7 to 5.5 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	"H" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$, $P8_0$–$P8_7$			10	mA
$I_{OL(peak)}$	"L" peak output current (Note 1) $P2_4$–$P2_7$	in single chip mode			20	mA
		in memory expansion mode and microprocessor mode			10	mA
$I_{OH(avg)}$	"H" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$, $P8_0$–$P8_7$			–5	mA
$I_{OL(avg)}$	"L" average output current (Note 2)	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_3$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, CMP_{OUT}, $P7_0$–$P7_7$, $P8_0$–$P8_7$			5	mA
$I_{OL(avg)}$	"L" average output current (Note 2) $P2_4$–$P2_7$	in single chip mode			15	mA
		in memory expansion mode and microprocessor mode			5	mA
$f(X_{IN})$	Main clock input oscillation frequency (Note 3)	High-speed mode $4.0V \leqq V_{CC} \leqq 5.5V$			8	MHz
		High-speed mode $2.7V \leqq V_{CC} \leqq 4.0V$			$3V_{CC}$–4	MHz
		Middle-speed mode $4.0V \leqq V_{CC} \leqq 5.5V$			8	MHz
		Middle-speed mode (Note 5) $2.7V \leqq V_{CC} \leqq 4.0V$			8	MHz
		Middle-speed mode (Note 5) $2.7V \leqq V_{CC} \leqq 4.0V$			$3V_{CC}$–4	MHz
$f(X_{CIN})$	Sub-clock input oscillation frequency (Note 3, 4)			32.768	50	kHz

Note 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL} (avg), I_{OH} (avg) in an average value measured over 100ms.
3: When the oscillation frequency has a duty cyde of 50%.
4: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that $f(X_{CIN}) < f(X_{IN})/3$.
5: When using the timer X/Y, timer A/B (real time output port), timer 1/2/3, serial I/O1, serial I/O2, and A-D converter, set the main clock input oscillation frequency to the max. 3 Vcc–4 (MHz).

ELECTRICAL CHARACTERISTICS

Table 13 Electrical characteristics (1) (V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
V_{OH}	"H" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, CMP_{OUT} (Note 1)	I_{OH} = –10mA V_{CC} = 4.0 to 5.5V	V_{CC}–2.0			V
			I_{OH} = –1.0mA V_{CC} = 2.7 to 5.5V	V_{CC}–1.0			V
V_{OL}	"L" output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_2$, $P6_5$, $P7_0$–$P7_7$, $P8_0$–$P8_7$, CMP_{OUT}	I_{OL} = 10mA V_{CC} = 4.0 to 5.5V			2.0	V
			I_{OL} = 1.6mA V_{CC} = 2.7 to 5.5V			0.4	V
V_{T+}–V_{T-}	Hysteresis	$P4_2$, $P4_3$, $P5_1$–$P5_5$, $P7_3$ (Note 2), $CNTR_0$, $CNTR_1$, INT_0–INT_4, ADT			0.4		V
V_{T+}–V_{T-}	Hysteresis	R_XD, S_{CLK1}, S_{IN2}, S_{CLK2}			0.5		V
V_{T+}–V_{T-}	Hysteresis	$\overline{RESET}$			0.5		V
I_{IH}	"H" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{CC} (Pin floating. Pull-up transistors "off")			5.0	µA
I_{IH}	"H" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current	X_{IN}	V_I = V_{CC}		4		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P3_0$–$P3_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_5$, $P7_0$–$P7_7$, $P8_0$–$P8_7$	V_I = V_{SS} (Pin floating. Pull-up transistors "off")			–5.0	µA
I_{IL}	"L" input current	$\overline{RESET}$, CNV_{SS}	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current	X_{IN}	V_I = V_{SS}		–4		µA
I_{IL}	"L" input current	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$	Pull-up transistors "on" V_I = V_{SS}		–0.2		mA
V_{RAM}	RAM hold voltage		When clock stopped	2.0		5.5	V

Note1: $P4_5$ is measured when the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
$P7_1$, and $P1_2$ are measured when the $P7_1/S_{OUT2}$ and $P7_2/S_{CLK2}$ P-channel output disable bit of the serial I/O2 control register 1 (bit 7 of address $001D_{16}$).

2: $P7_3$ is measured when the AD external trigger valid bit of the A–D control register (bit 6 of address 0034_{16}) is "1".

Table 14 Electrical characteristics (2) (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits			Unit
				Min.	Typ.	Max.	
I_{CC}	Power source current	High-speed mode $f(X_{IN})$ = 8MHz $f(X_{CIN})$ = 32.768kHz Output transistors “off”			6.8	13	mA
		High-speed mode $f(X_{IN})$ = 8MHz (in WIT state) $f(X_{CIN})$ = 32.768kHz Output transistors “off”			1.6		mA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768kHz Low-power dissipation mode (CM_3 = 0) Output transistors “off”			60	200	µA
		Low-speed mode $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768kHz (in WIT state) Low-power dissipation mode (CM_3 = 0) Output transistors “off”			20	40	µA
		Low-speed mode (V_{CC} = 3V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768kHz Low-power dissipation mode (CM_3 = 0) Output transistors “off”			20	55	µA
		Low-speed mode (V_{CC} = 3V) $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768kHz (in WIT state) Low-power dissipation mode (CM_3 = 0) Output transistors “off”			5.0	10.0	µA
		Middle-speed mode $f(X_{IN})$ = 8MHz $f(X_{CIN})$ = stopped Output transistors “off”			4.0	7.0	mA
		Middle-speed mode $f(X_{IN})$ = 8MHz (in WIT state) $f(X_{CIN})$ = stopped Output transistors “off”			1.5		mA
		Increment when A-D conversion is executed $f(X_{IN})$ = 8MHz			800		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25°C		0.1	1.0	µA
			Ta = 85°C			10	µA
$CMPI_{CC}$	Analog comparator Power source current				200	500	µA

A-D CONVERTER CHARACTERISTICS

Table 15 A-D converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = AVss = 0 V, ADV_{REF} = 2.0 V to Vcc, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy (excluding quantization error)		V_{CC} = ADV_{REF} = 5.0V			±2	LSB
t_{CONV}	Conversion time					50	tc(ϕ)
R_{LADDER}	Ladder resistor			12	35	100	kΩ
I_{ADVREF}	Reference power source input current	ADV_{REF} "on"	ADV_{REF} = 5.0V	50	150	200	µA
		ADV_{REF} "off"				5	µA
$I_{I(AD)}$	A-D port input current					5.0	µA

D-A CONVERTER CHARACTERISTICS

Table 16 D-A converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = AVss = 0 V, DAV_{REF} = 2.7 V to Vcc, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
—	Resolution					8	Bits
—	Absolute accuracy	V_{CC} = 4.0 to 5.5V				1.0	%
		V_{CC} = 2.7 to 4.0V				2.5	%
t_{su}	Setting time					3	µs
R_O	Output resistor			1	2.5	4	kΩ
I_{DAVREF}	Reference power source input current (Note)					3.2	mA

Note: Using one D-A converter, with the value in the D-A conversion register of the other D-A converter being "00_{16}".

ANALOG COMPARATOR CHARACTERISTICS

Table 17 Analog comparator characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = AVss = 0 V, CMPVcc = 2.7 V to Vcc, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{IO}	Input offset voltage	$CMPV_{CC}$ = 5.0V CMP_{REF} = 2.5V, Rs = 0Ω		3	50	mV
I_B	Input bias current				5	µA
I_{IO}	Input offset current				5	µA
V_{ICM}	In-phase input voltage range		1.2		$CMPV_{CC}$ –0.5	V
A_V	Voltage gain			∞		
t_{PD}	Response time	$CMPV_{CC}$ = 5.0V CMP_{REF} = 2.5V		60	2500	ns

TIMING REQUIREMENTS

Table 18 Timing requirements (1) (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	125			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	50			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	50			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{WH(INT)}$	INT_0 to INT_4 input “H” pulse width	80			ns
$t_{WL(INT)}$	INT_0 to INT_4 input “L” pulse width	80			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	800			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	370			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	370			ns
$t_{su(RXD–SCLK1)}$	Serial I/O1 clock input set up time	220			ns
$t_{h(SCLK1–RXD)}$	Serial I/O1 clock input hold time	100			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su(SIN2–SCLK2)}$	Serial I/O2 clock input set up time	200			ns
$t_{h(SCLK2–SIN2)}$	Serial I/O2 clock input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

Table 19 Timing requirements (2) (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{W(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{C(XIN)}$	External clock input cycle time	243			ns
$t_{WH(XIN)}$	External clock input “H” pulse width	100			ns
$t_{WL(XIN)}$	External clock input “L” pulse width	100			ns
$t_{C(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	230			ns
$t_{WL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	230			ns
$t_{WH(INT)}$	INT_0 to INT_4 input “H” pulse width	230			ns
$t_{WL(INT)}$	INT_0 to INT_4 input “L” pulse width	230			ns
$t_{C(SCLK1)}$	Serial I/O1 clock input cycle time (Note)	2000			ns
$t_{WH(SCLK1)}$	Serial I/O1 clock input “H” pulse width (Note)	950			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock input “L” pulse width (Note)	950			ns
$t_{su(RXD–SCLK1)}$	Serial I/O1 clock input set up time	400			ns
$t_{h(SCLK1–RXD)}$	Serial I/O1 clock input hold time	200			ns
$t_{C(SCLK2)}$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH(SCLK2)}$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su(SIN2–SCLK2)}$	Serial I/O2 clock input set up time	400			ns
$t_{h(SCLK2–SIN2)}$	Serial I/O2 clock input hold time	300			ns

Note: When bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when bit 6 of address $001A_{16}$ is “0” (UART).

SWITCHING CHARACTERISTICS

Table 20 Switching characteristics (1) (Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	Fig. 3.1.1	$t_{C(SCLK1)}$/2–30			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width		$t_{C(SCLK1)}$/2–30			ns
$t_{d(SCLK1–TXD)}$	Serial I/O1 output delay time (Note 1)				140	ns
$t_{v(SCLK1–TXD)}$	Serial I/O1 output valid time (Note 1)		–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time				30	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time				30	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	Fig. 3.1.1	$t_{C(SCLK2)}$/2–160			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–160			ns
$t_{d(SCLK2–SOUT2)}$	Serial I/O2 output delay time (Note 2)				200	ns
$t_{v(SCLK2–SOUT2)}$	Serial I/O2 output valid time (Note 2)		0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time				30	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 3)	Fig. 3.1.1		10	30	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 3)			10	30	ns

Note 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: When the $P7_1$/SOUT2, $P7_2$/SCLK2 P-channel output disable bit of the serial I/O2 control register1 (bit 7 of address $001D_{16}$) is “0”.
3: XOUT pin is excluded.

Table 21 Switching characteristics (2) (Vcc = 2.7 to 5.5 V, Vss = 0 V, Ta = – 20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{WH(SCLK1)}$	Serial I/O1 clock output “H” pulse width	Fig. 3.1.1	$t_{C(SCLK1)}$/2–50			ns
$t_{WL(SCLK1)}$	Serial I/O1 clock output “L” pulse width		$t_{C(SCLK1)}$/2–50			ns
$t_{d(SCLK1–TXD)}$	Serial I/O1 output delay time (Note 1)				350	ns
$t_{v(SCLK1–TXD)}$	Serial I/O1 output valid time (Note 1)		–30			ns
$t_{r(SCLK1)}$	Serial I/O1 clock output rising time				50	ns
$t_{f(SCLK1)}$	Serial I/O1 clock output falling time				50	ns
$t_{WH(SCLK2)}$	Serial I/O2 clock output “H” pulse width	Fig. 3.1.1	$t_{C(SCLK2)}$/2–240			ns
$t_{WL(SCLK2)}$	Serial I/O2 clock output “L” pulse width		$t_{C(SCLK2)}$/2–240			ns
$t_{d(SCLK2–SOUT2)}$	Serial I/O2 output delay time (Note 2)				400	ns
$t_{v(SCLK2–SOUT2)}$	Serial I/O2 output valid time (Note 2)		0			ns
$t_{f(SCLK2)}$	Serial I/O2 clock output falling time				50	ns
$t_{r(CMOS)}$	CMOS output rising time (Note 3)	Fig. 3.1.1		20	50	ns
$t_{f(CMOS)}$	CMOS output falling time (Note 3)			20	50	ns

Note 1: When the $P4_5$/TxD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: When the $P7_1$/SOUT2, $P7_2$/SCLK2 P-channel output disable bit of the serial I/O2 control register1 (bit 7 of address $001D_{16}$) is “0”.
3: XOUT pin is excluded.

TIMING REQUIREMENTS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

Table 22 Timing requirements in memory expansion and microprocessor mode(1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = – 20 to 85 °C, in high-speed mode, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{su(\overline{ONW}-\phi)}$	$\overline{ONW}$ input set up time	–20			ns
$t_{h(\phi-\overline{ONW})}$	$\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\phi)}$	Data bus set up time	50			ns
$t_{h(\phi-DB)}$	Data bus hold time	0			ns
$t_{su(\overline{ONW}-\overline{RD})}$, $t_{su(\overline{ONW}-\overline{WR})}$	$\overline{ONW}$ input set up time	–20			ns
$t_{h(\overline{RD}-\overline{ONW})}$, $t_{h(\overline{WR}-\overline{ONW})}$	$\overline{ONW}$ input hold time	–20			ns
$t_{su(DB-\overline{RD})}$	Data bus set up time	50			ns
$t_{h(\overline{RD}-DB)}$	Data bus hold time	0			ns

SWITCHING CHARACTERISTICS IN MEMORY EXPANSION MODE AND MICROPROCESSOR MODE

Table 23 Switching characteristics in memory expansion and microprocessor mode(1)

(Vcc = 4.0 to 5.5 V, Vss = 0 V, Ta = – 20 to 85 °C, in high-speed mode, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
$t_{C(\phi)}$	ϕ clock cycle time	Fig. 3.1.1		$2t_{C(X_{IN})}$		ns
$t_{WH(\phi)}$	ϕ clock “H” pulse width		$t_{C(X_{IN})}$–10			ns
$t_{WL(\phi)}$	ϕ clock “L” pulse width		$t_{C(X_{IN})}$–10			ns
$t_{d(\phi-AH)}$	AD_{15}–AD_8 delay time			16	35	ns
$t_{d(\phi-AL)}$	AD_7–AD_0 delay time			20	40	ns
$t_{v(\phi-AH)}$	AD_{15}–AD_8 valid time		2	5		ns
$t_{v(\phi-AL)}$	AD_7–AD_0 valid time		2	5		ns
$t_{d(\phi-SYNC)}$	SYNC delay time			16		ns
$t_{v(\phi-SYNC)}$	SYNC valid time			5		ns
$t_{d(\phi-DB)}$	Data bus delay time			15	30	ns
$t_{v(\phi-DB)}$	Data bus valid time		10			ns
$t_{WL(\overline{RD})}$, $t_{WL(\overline{WR})}$	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width		$t_{C(X_{IN})}$–10			ns
	$\overline{RD}$ pulse width, $\overline{WR}$ pulse width (When one-wait is valid)		$3t_{C(X_{IN})}$–10			ns
$t_{d(AH-\overline{RD})}$, $t_{d(AH-\overline{WR})}$	AD_{15}–AD_8 delay time		$t_{C(X_{IN})}$–35	$t_{C(X_{IN})}$–16		ns
$t_{d(AL-\overline{RD})}$, $t_{d(AL-\overline{WR})}$	AD_7–AD_0 delay time		$t_{C(X_{IN})}$–40	$t_{C(X_{IN})}$–20		ns
$t_{v(\overline{RD}-AH)}$, $t_{v(\overline{WR}-AH)}$	AD_{15}–AD_8 valid time		2	5		ns
$t_{v(\overline{RD}-AL)}$, $t_{v(\overline{WR}-AL)}$	AD_7–AD_0 valid time		2	5		ns
$t_{d(\overline{WR}-DB)}$	Data bus delay time			15	30	ns
$t_{v(\overline{WR}-DB)}$	Data bus valid time		10			ns
$t_{d(\overline{RESET}-\overline{RESET_{OUT}})}$	$\overline{RESET_{OUT}}$ output delay time				200	ns
$t_{v(\phi-\overline{RESET_{OUT}})}$	$\overline{RESET_{OUT}}$ output valid time (Note)		0		100	ns

Note: The $RESET_{OUT}$ output goes “H” in sync with the fall of the ϕ clock that is anywhere between about 8 cycle and 13 cycles after the $\overline{RESET}$ input goes “H”.

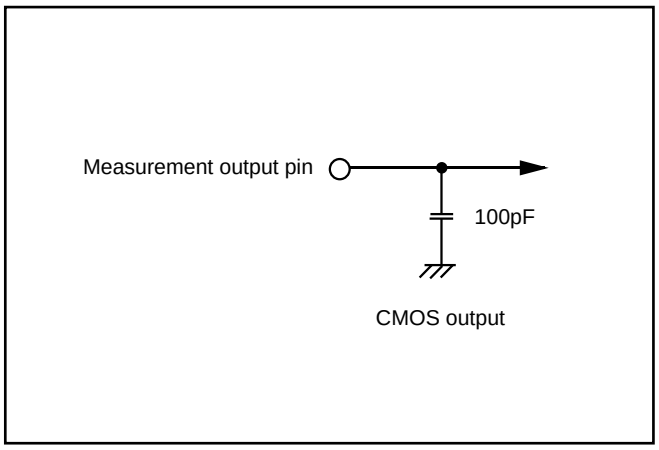


Fig. 63 Circuit for measuring output switching characteristics(1)

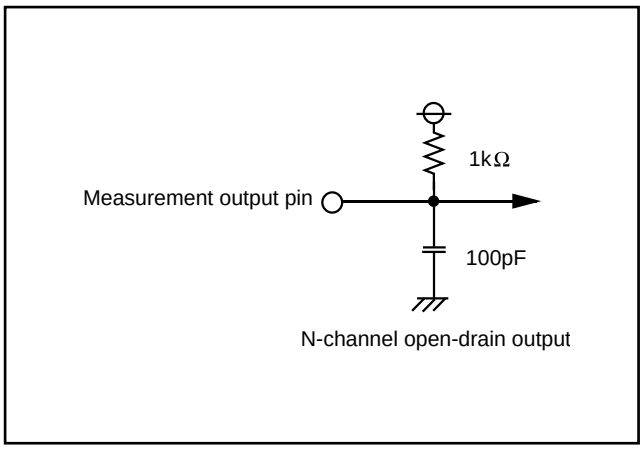


Fig. 64 Circuit for measuring output switching characteristics (2)

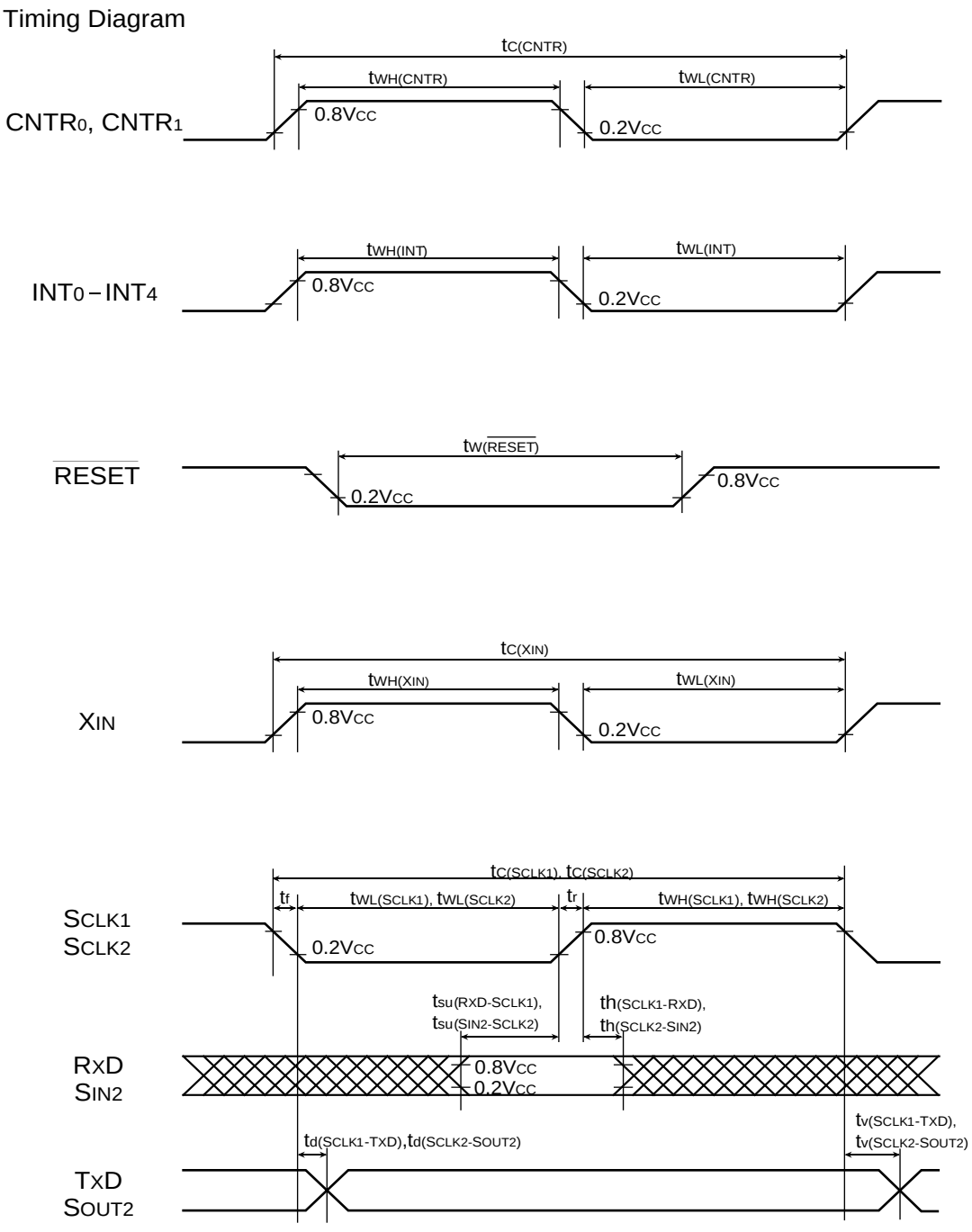
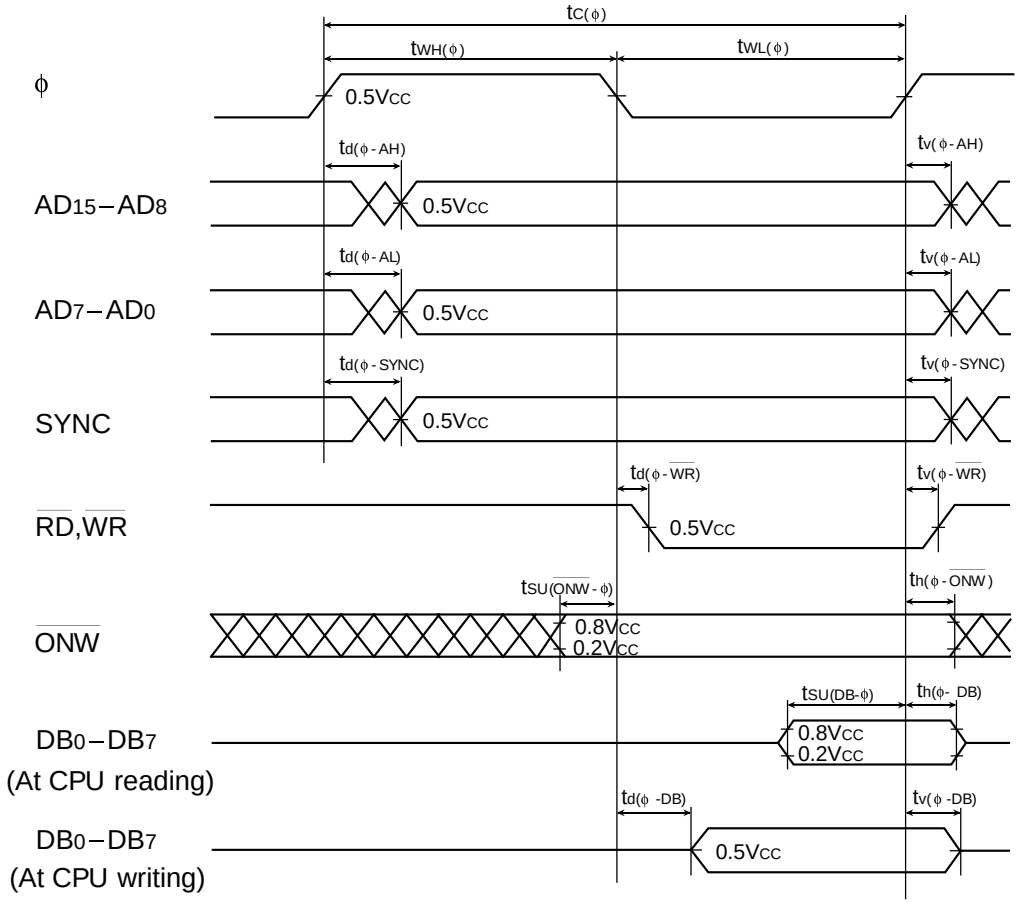


Fig. 65 Timing diagram (1) (in single-chip mode)

Timing Diagram in Memory Expansion Mode and Microprocessor Mode (CMOS level input)



Timing Diagram in Microprocessor Mode

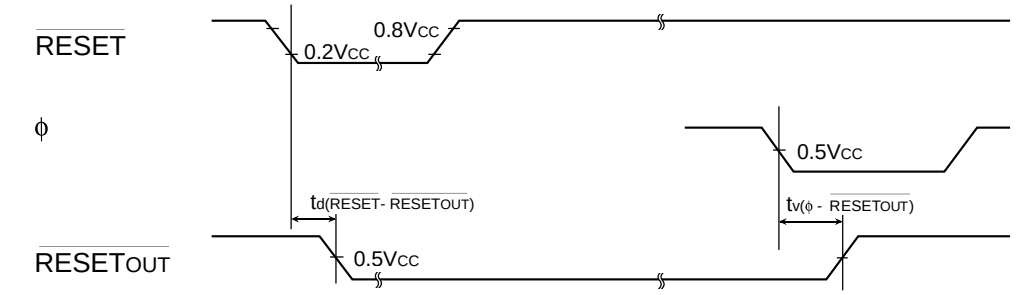


Fig. 66 Timing diagram (2) (in memory expansion mode and microprocessor mode)

Timing Diagram in Memory Expansion Mode and Microprocessor Mode (CMOS level input)

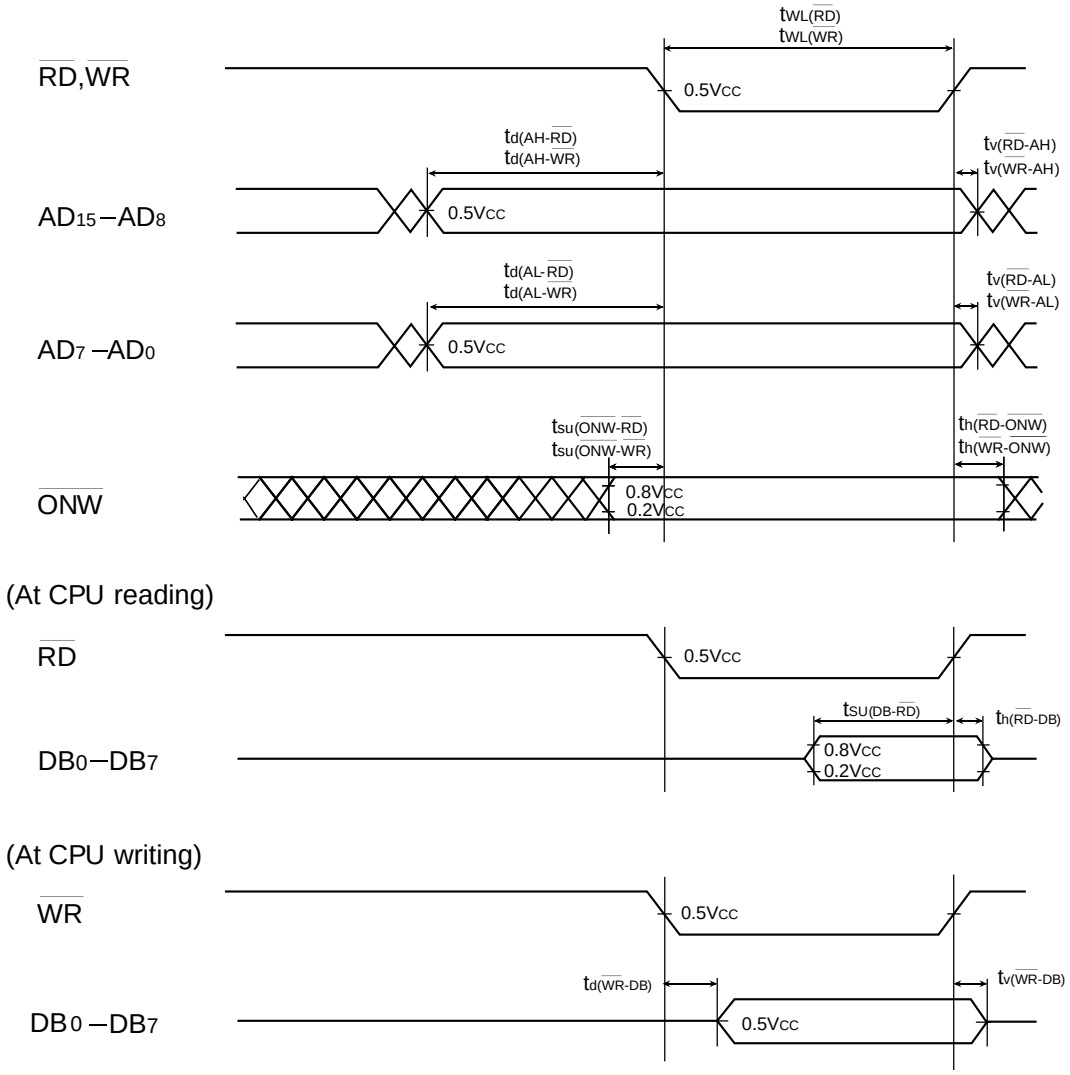
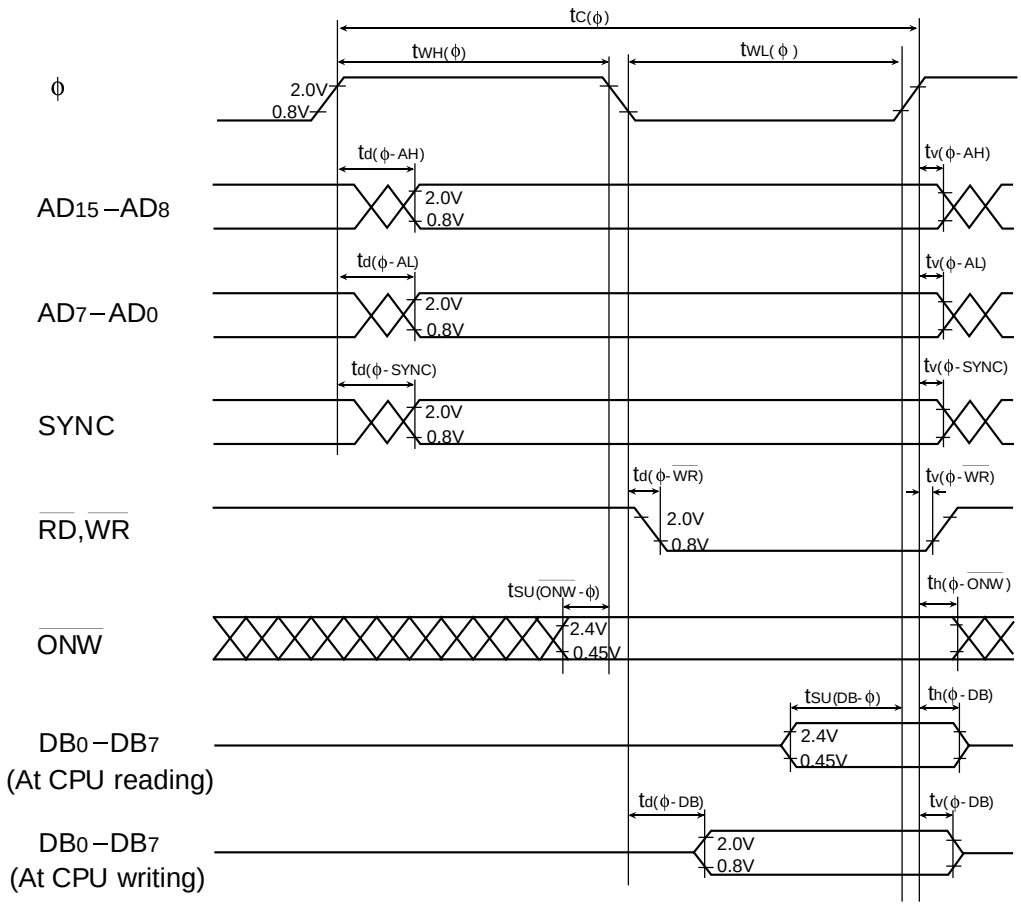


Fig. 67 Timing diagram (3) (in memory expansion mode and microprocessor mode)

Timing Diagram in Memory Expansion Mode and Microprocessor Mode (TTL level input)



Timing Diagram in Microprocessor Mode

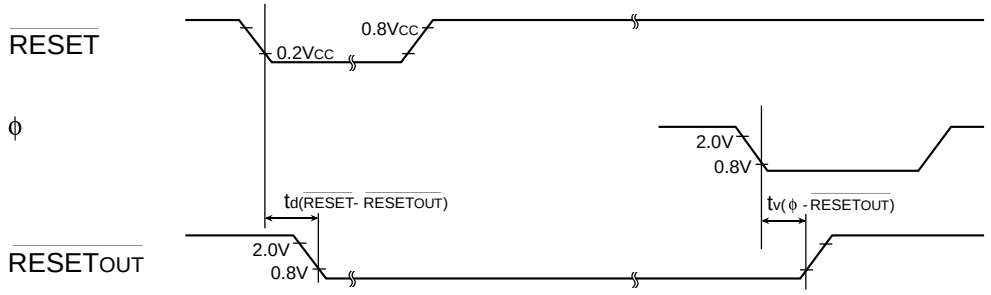


Fig. 68 Timing diagram (4) (in memory expansion mode and microprocessor mode)

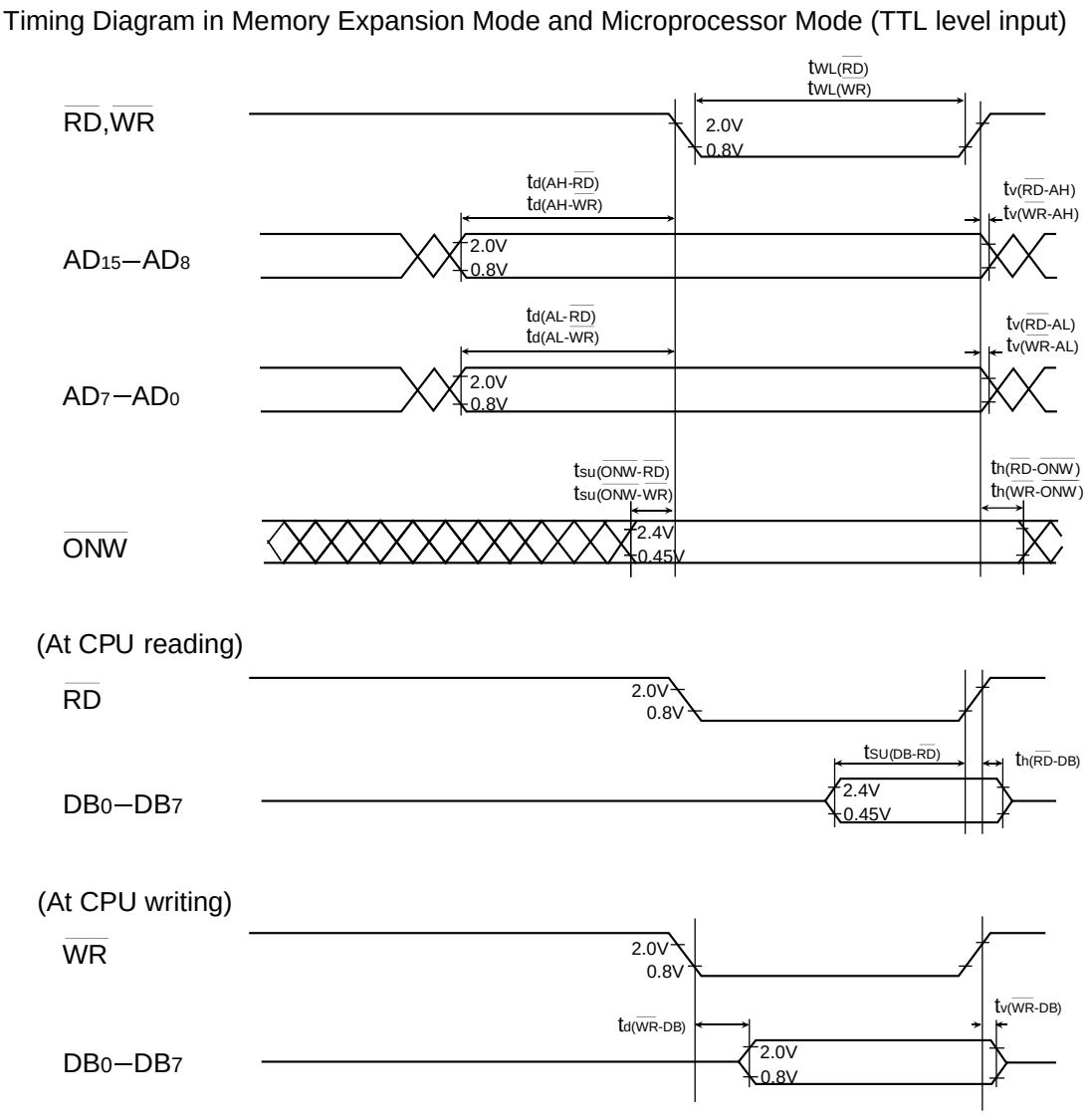


Fig. 69 Timing diagram (5) (in memory expansion mode and microprocessor mode)

3807 Group

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

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