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April 1st, 2010
Renesas Electronics Corporation

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DESCRIPTION

The 3804 group (Spec. H) is the 8-bit microcomputer based on the 740 family core technology.

The 3804 group (Spec. H) is designed for household products, office automation equipment, and controlling systems that require analog signal processing, including the A/D converter and D/A converters.

FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time 0.24 μ s
(at 16.8 MHz oscillation frequency)
- Memory size
 - Flash memory 60 K bytes
 - RAM 2048 bytes
- Programmable input/output ports 56
- Software pull-up resistors Built-in
- Interrupts
 - 21 sources, 16 vectors
(external 8, internal 12, software 1)
- Timers 16-bit X 1
8-bit X 4
(with 8-bit prescaler)
- Watchdog timer 16-bit X 1
- Serial interface
 - Serial I/O1, 3 8-bit X 2 (UART or Clock-synchronized)
 - Serial I/O2 8-bit X 1 (Clock-synchronized)
- PWM 8-bit X 1 (with 8-bit prescaler)
- Multi-master I²C-BUS interface 1 channel
- A/D converter 10-bit X 16 channels
(8-bit reading enabled)
- D/A converter 8-bit X 2 channels
- LED direct drive port 8
- Clock generating circuit Built-in 2 circuits
(connect to external ceramic resonator or quartz-crystal oscillator)

- Power source voltage
 - In high-speed mode
 - At 16.8 MHz oscillation frequency 4.5 to 5.5 V
 - At 12.5 MHz oscillation frequency 4.0 to 5.5 V
 - At 8.4 MHz oscillation frequency) 2.7 to 5.5 V
 - In middle-speed mode
 - At 16.8 MHz oscillation frequency 4.5 to 5.5 V
 - At 12.5 MHz oscillation frequency 2.7 to 5.5 V
 - In low-speed mode
 - At 32 kHz oscillation frequency 2.7 to 5.5 V
- Power dissipation
 - In high-speed mode 27.5 mW (typ.)
(at 16.8 MHz oscillation frequency, at 5 V power source voltage)
 - In low-speed mode 1200 μ W (typ.)
(at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range -20 to 85°C
- Packages
 - SP 64P4B (64-pin 750 mil SDIP)
 - FP 64P6N-A (64-pin 14 X 14 mm QFP)
 - HP 64P6Q-A (64-pin 10 X 10 mm LQFP)
 - KP 64P6U-A (64-pin 14 X 14 mm LQFP)

<Flash memory mode>

- Power source voltage Vcc = 2.7 to 5.5 V
- Program/Erase voltage Vcc = 2.7 to 5.5 V
- Programming method Programming in unit of byte
- Erasing method Block erasing
- Program/Erase control by software command
- Number of times for programming/erasing 100

■ Notes

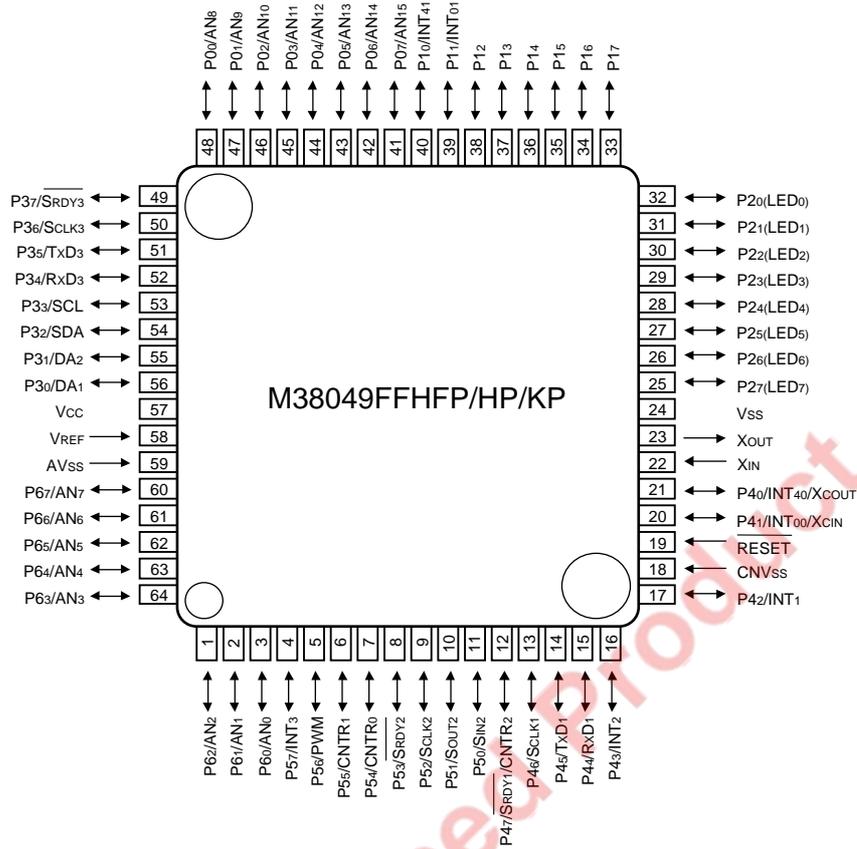
Cannot be used for application embedded in the MCU card.

Currently support products are listed below.

Table 1 Support products

| Product name | Flash memory size (bytes) | RAM size (bytes) | Package | Remarks |
|--------------|---------------------------|------------------|---------|--------------------|
| M38049FFHSP | 61440 | 2048 | 64P4B | Vcc = 2.7 to 5.5 V |
| M38049FFHFP | | | 64P6N-A | |
| M38049FFHHP | | | 64P6Q-A | |
| M38049FFHKP | | | 64P6U-A | |

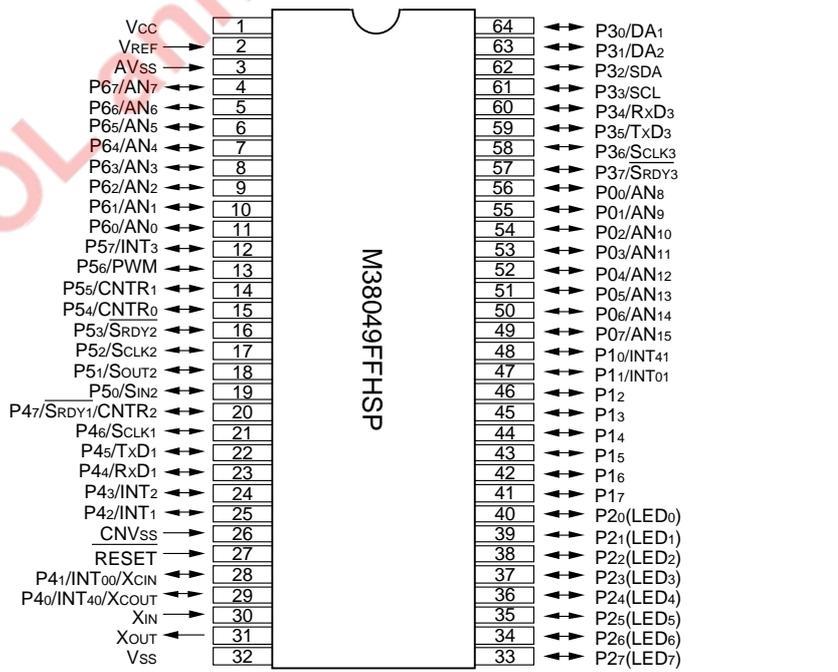
PIN CONFIGURATION (TOP VIEW)



Package type : 64P6N-A/64P6Q-A/64P6U-A

Fig. 1 3804 group (Spec. H) pin configuration

PIN CONFIGURATION (TOP VIEW)



Package type : 64P4B

Fig. 2 3804 group (Spec. H) pin configuration

FUNCTIONAL BLOCK

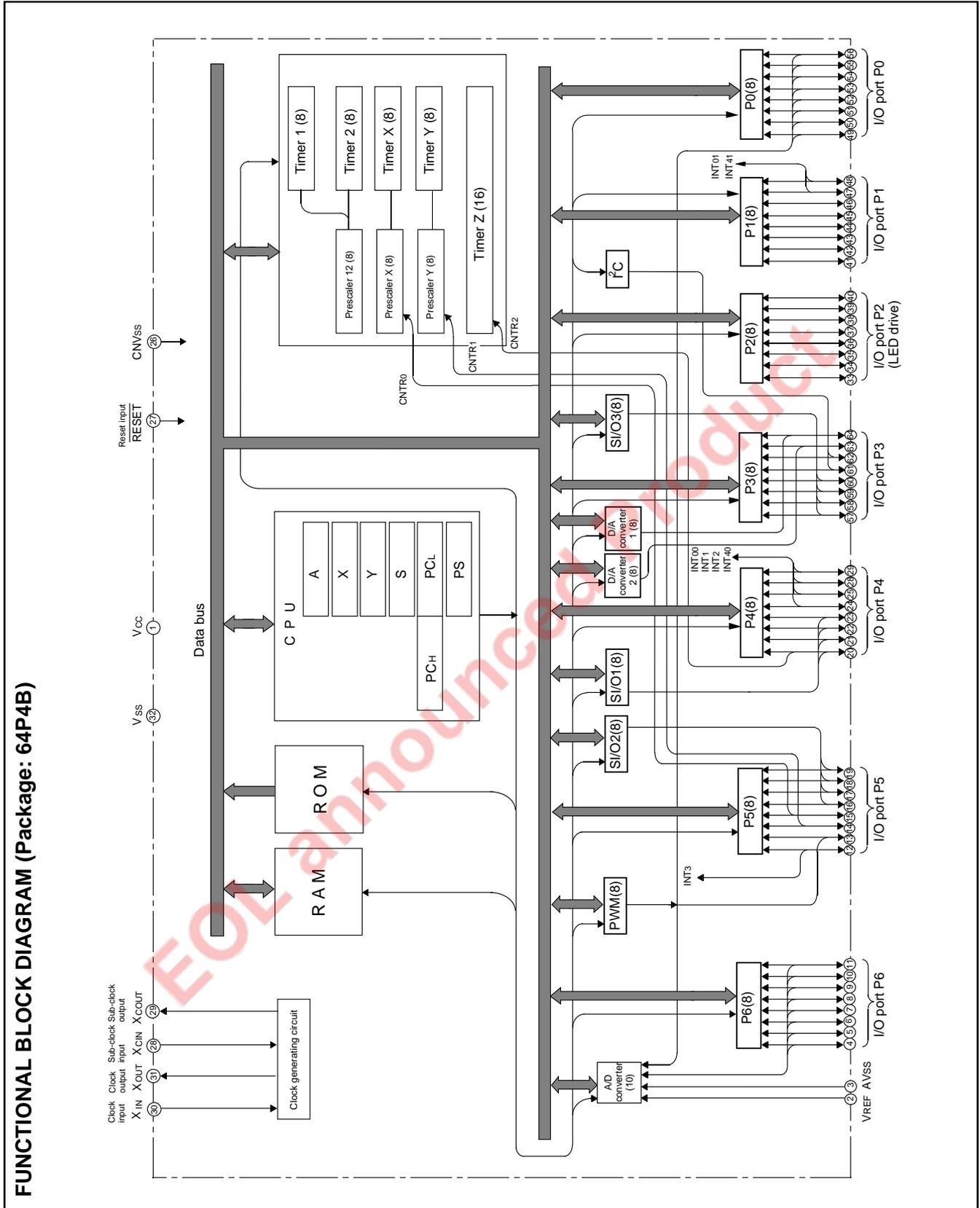


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 2 Pin description

| Pin | Name | Functions | Function except a port function |
|---|---------------------|---|---|
| | | | |
| VCC, VSS | Power source | •Apply voltage of 2.7 V–5.5 V to Vcc, and 0 V to Vss. | |
| CNVSS | CNVSS input | •This pin controls the operation mode of the chip. •Normally connected to Vss. | |
| VREF | Reference voltage | •Reference voltage input pin for A/D and D/A converters. | |
| AVSS | Analog power source | •Analog power source input pin for A/D and D/A converters. •Connect to Vss. | |
| RESET | Reset input | •Reset input pin for active L". | " |
| XIN | Clock input | •Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. | |
| XOUT | Clock output | •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open. | |
| P00/AN8– P07/AN15 | I/O port P0 | •8-bit CMOS I/O port. | •A/D converter input pin |
| P10/INT41 P11/INT01 | I/O port P1 | •I/O direction register allows each pin to be individually programmed as either input or output. | •Interrupt input pin |
| P12–P17 | | •CMOS compatible input level. | |
| P20–P27 | | •CMOS 3-state output structure. | |
| P20–P27 | I/O port P2 | •Pull-up control is enabled in a bit unit. •P20–P27 are enabled to output large current for LED drive. | |
| P30/DA1 P31/DA2 | I/O port P3 | •8-bit CMOS I/O port. | •D/A converter input pin |
| P32/SDA P33/SCL | | •I/O direction register allows each pin to be individually programmed as either input or output. | •I ² C-BUS interface function pins |
| P34/RxD3 P35/TxD3 P36/SCLK3 P37/SRDY3 | | •CMOS compatible input level. •P32 to P33 can be switched between CMOS compatible input level or SMBUS input level in the I ² C-BUS interface function. •P30, P31, P34–P37 are CMOS 3-state output structure. •P32, P33 are N-channel open-drain output structure. •Pull-up control of P30, P31, P34–P37 is enabled in a bit unit. | •Serial I/O3 function pin |
| | | | |
| P40/INT40/ XCOUT P41/INT00/ XCIN | I/O port P4 | •8-bit CMOS I/O port. | •Interrupt input pin |
| P42/INT1 P43/INT2 | | •I/O direction register allows each pin to be individually programmed as either input or output. | •Sub-clock generating I/O pin (resonator connected) |
| P44/RxD1 P45/TxD1 P46/SCLK1 | | •CMOS compatible input level. •CMOS 3-state output structure. | •Interrupt input pin |
| P47/SRDY1 /CNTR2 | | •Pull-up control is enabled in a bit unit. | •Serial I/O1 function pin |
| P50/SIN2 P51/SOUT2 P52/SCLK2 P53/SRDY2 | I/O port P5 | •8-bit CMOS I/O port. | •Serial I/O2 function pin |
| P54/CNTR0 | | •I/O direction register allows each pin to be individually programmed as either input or output. | |
| P55/CNTR1 | | •CMOS compatible input level. | •Timer X function pin |
| P56/PWM | | •CMOS 3-state output structure. | •Timer Y function pin |
| P57/INT3 | | •Pull-up control is enabled in a bit unit. | •PWM output pin |
| P60/AN0– P67/AN7 | I/O port P6 | | •Interrupt input pin •A/D converter input pin |

PART NUMBERING

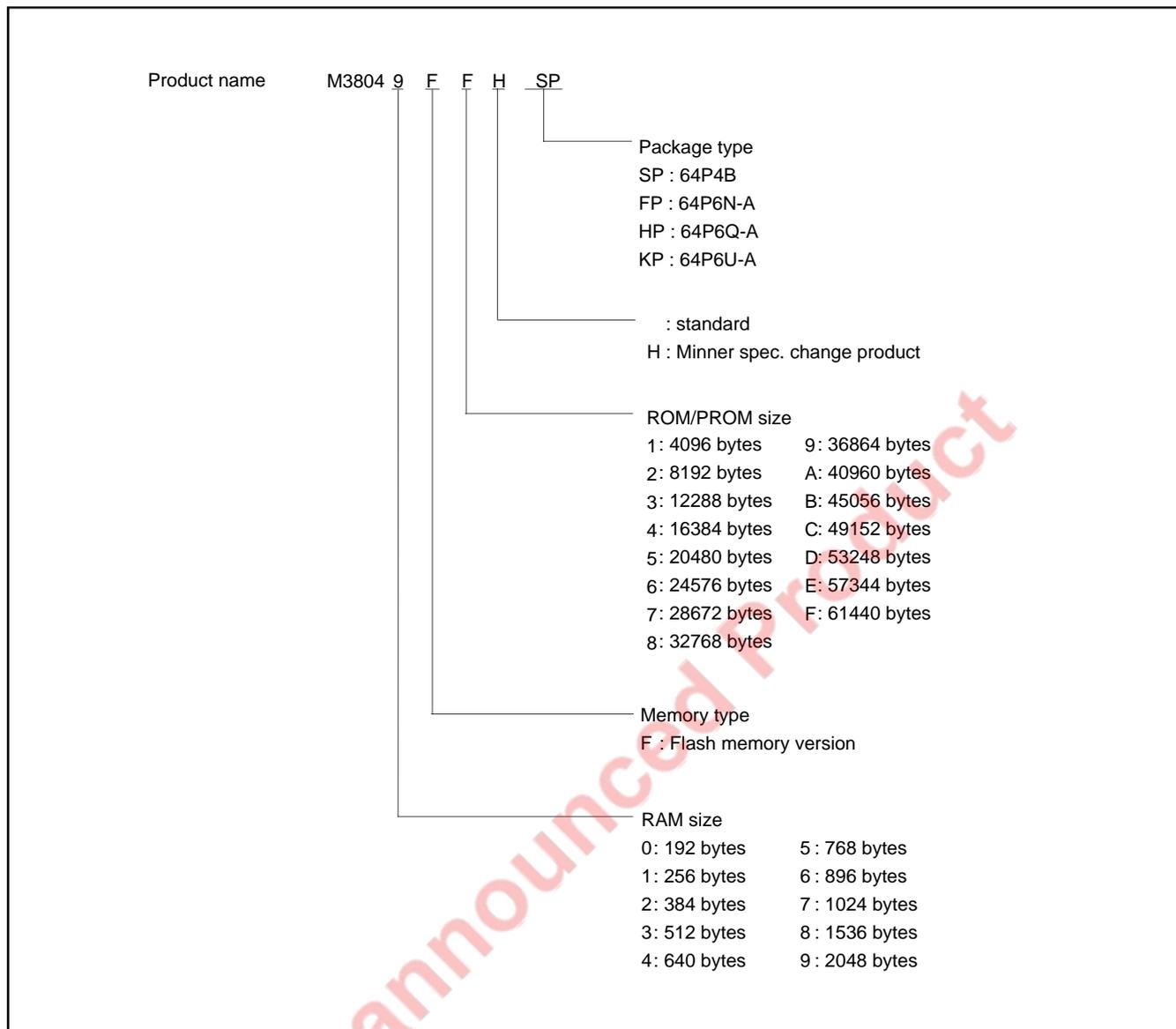


Fig. 4 Part numbering

GROUP EXPANSION

Renesas plans to expand the 3804 group (Spec. H) as follows.

Memory Size

Flash memory size 60 K bytes
 RAM size 2048 bytes

Packages

64P4B 64-pin shrink plastic-molded DIP
 64P6N-A 0.8 mm-pitch plastic molded QFP
 64P6Q-A 0.5 mm-pitch plastic molded LQFP
 64P6U-A 0.8 mm-pitch plastic molded LQFP

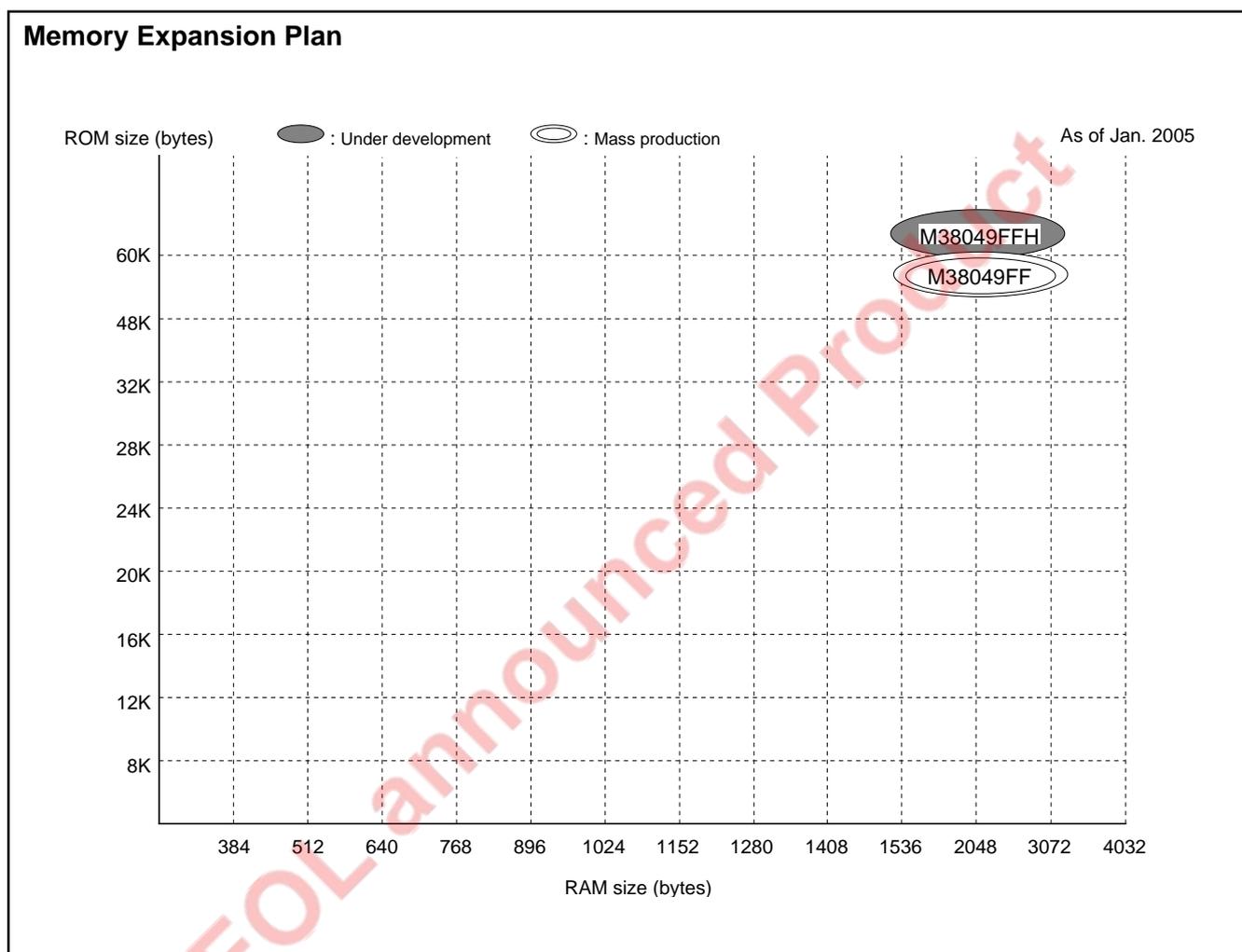


Fig. 5 Memory expansion plan

**FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)**

The 3804 group (Spec. H) uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

- The FST and SLW instructions cannot be used.
- The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc. are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is "0", the high-order 8 bits becomes "0016". If the stack page selection bit is "1", the high-order 8 bits becomes "06".

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 7.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls (see Table 3).

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PCH and PCL. It is used to indicate the address of the next instruction to be executed.

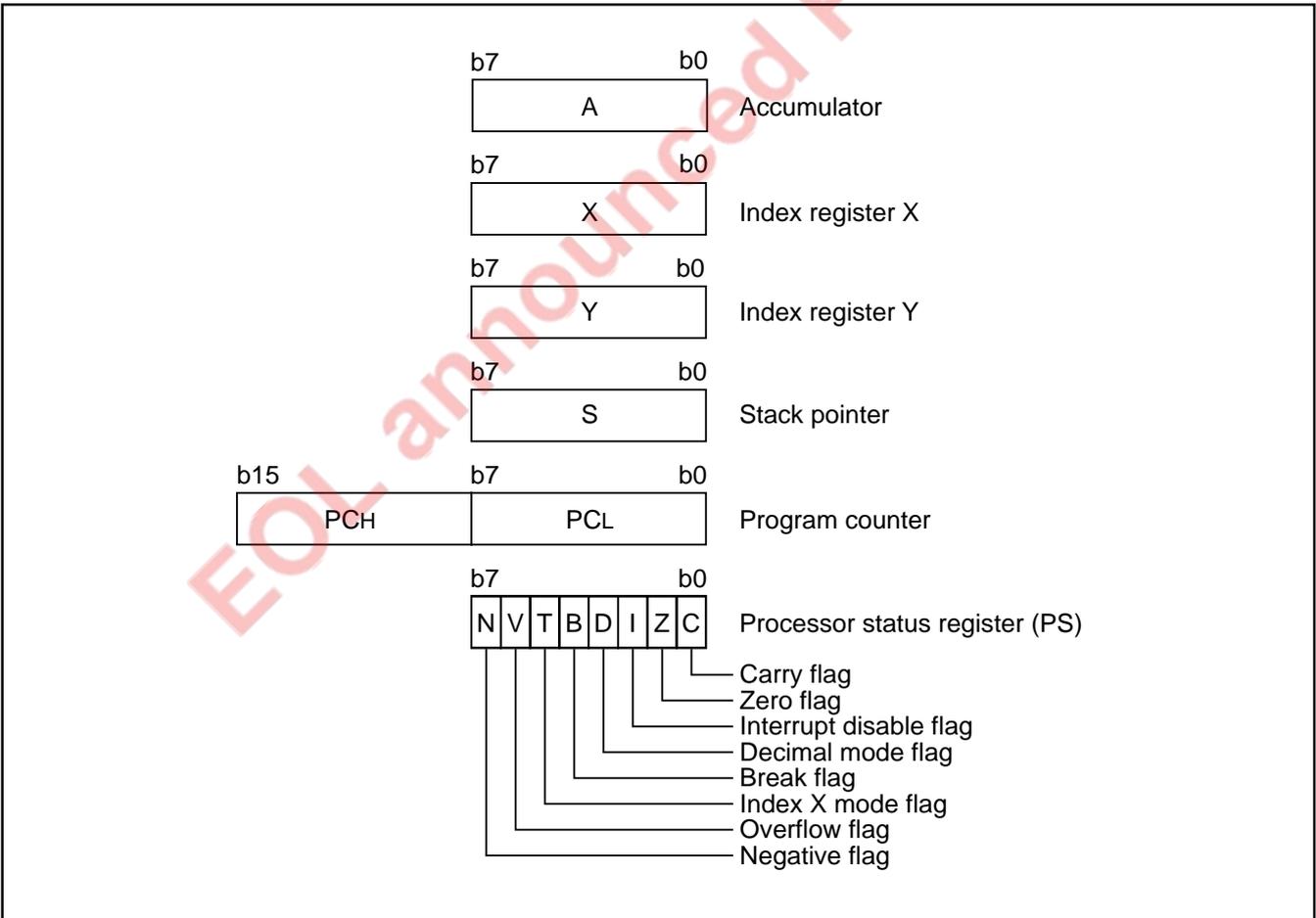


Fig. 6 740 Family CPU register structure

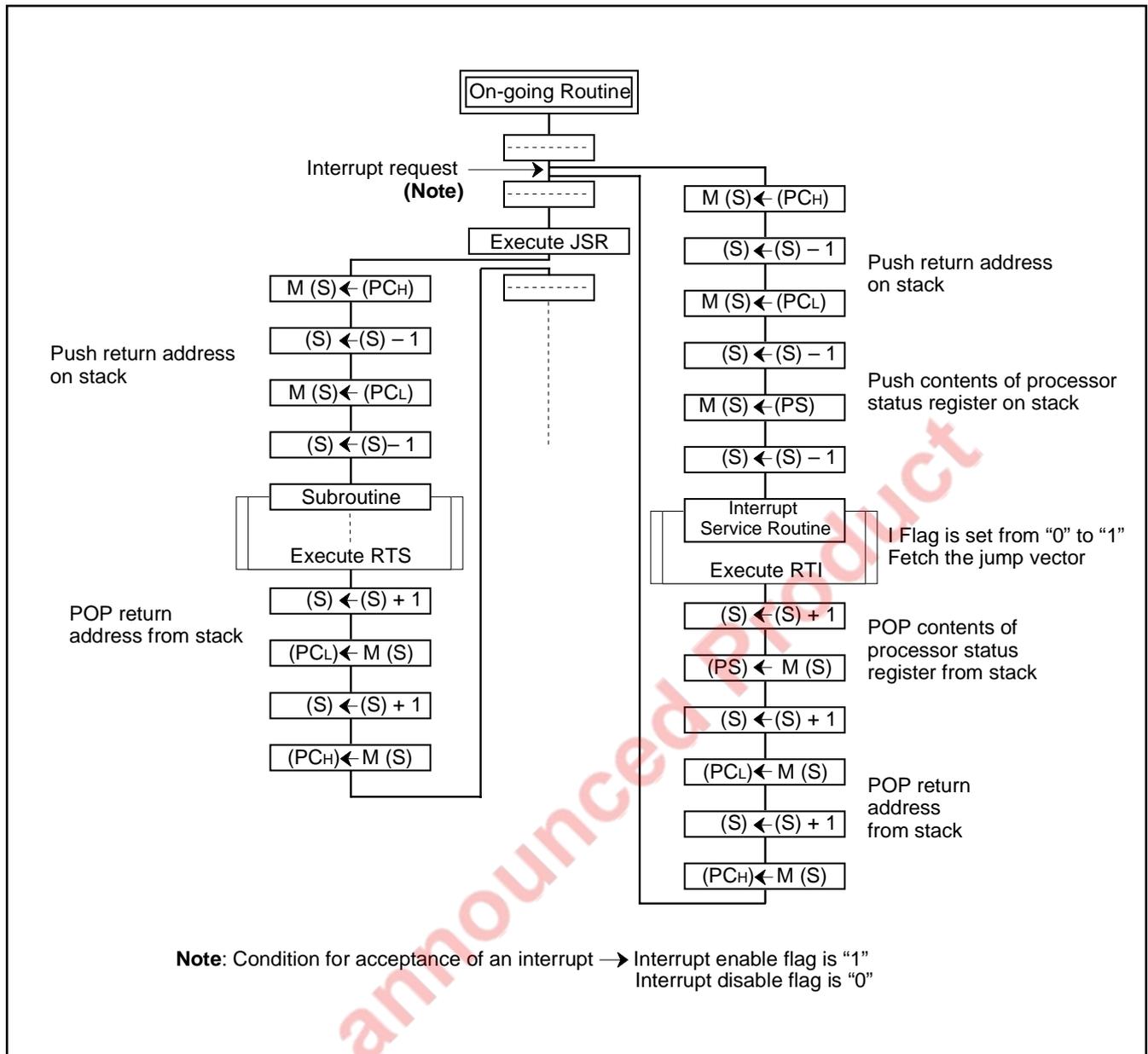


Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 3 Push and pop instructions of accumulator or processor status register

| | Push instruction to stack | Pop instruction from stack |
|---------------------------|---------------------------|----------------------------|
| Accumulator | PHA | PLA |
| Processor status register | PHP | PLP |

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag, Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

- Bit 0: Carry flag (C)

The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

- Bit 1: Zero flag (Z)

The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

- Bit 2: Interrupt disable flag (I)

The I flag disables all interrupts except for the interrupt generated by the BRK instruction.

Interrupts are disabled when the I flag is "1".

- Bit 3: Decimal mode flag (D)

The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1".

Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can execute decimal arithmetic.

- Bit 4: Break flag (B)

The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

- Bit 5: Index X mode flag (T)

When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

- Bit 6: Overflow flag (V)

The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

- Bit 7: Negative flag (N)

The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 4 Set and clear instructions of each bit of processor status register

| | C flag | Z flag | I flag | D flag | B flag | T flag | V flag | N flag |
|-------------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Set instruction | SEC | – | SEI | SED | – | SET | – | – |
| Clear instruction | CLC | – | CLI | CLD | – | CLT | CLV | – |

[CPU Mode Register (CPUM)] 003B16

The CPU mode register contains the stack page selection bit, etc.

The CPU mode register is allocated at address 003B16.

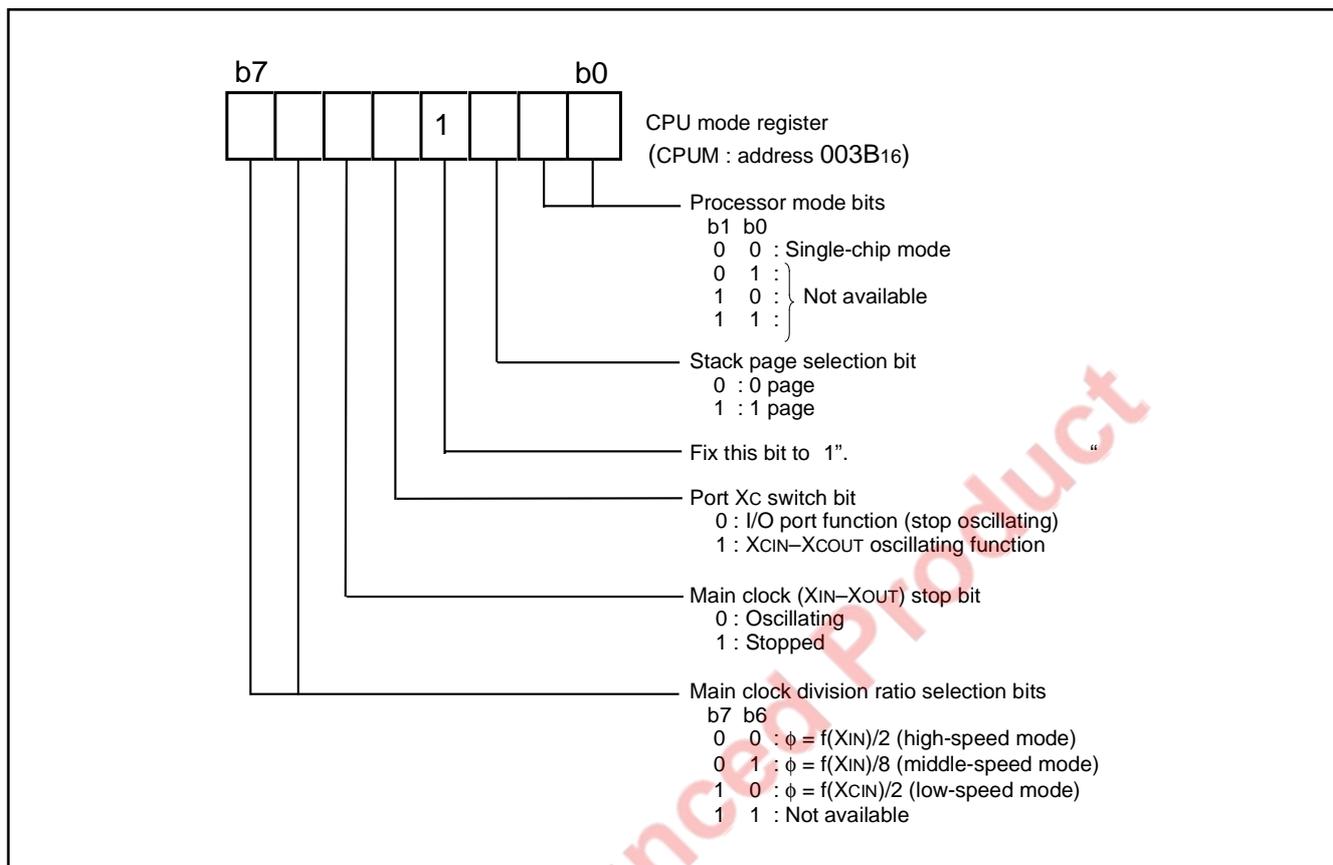


Fig. 8 Structure of CPU mode register

MISRG

(1) Bit 0 of address 0010₁₆: Oscillation stabilizing time set after STP instruction released bit

When the MCU stops the clock oscillation by the STP instruction and the STP instruction has been released by an external interrupt source, usually, the fixed values of Timer 1 and Prescaler 12 (Timer 1 = 01₁₆, Prescaler 12 = FF₁₆) are automatically reloaded in order for the oscillation to stabilize. The user can inhibit the automatic setting by setting "1" to bit 0 of MISRG (address 0010₁₆). However, by setting this bit to "1", the previous values, set just before the STP instruction was executed, will remain in Timer 1 and Prescaler 12. Therefore, you will need to set an appropriate value to each register, in accordance with the oscillation stabilizing time, before executing the STP instruction.

Figure 9 shows the structure of MISRG.

(2) Bits 1, 2, 3 of address 0010₁₆: Middle-speed Mode Automatic Switch Function

In order to switch the clock mode of an MCU which has a sub-clock, the following procedure is necessary:

set CPU mode register (003B₁₆) --> start main clock oscillation --> wait for oscillation stabilization --> switch to middle-speed mode (or high-speed mode).

However, the 3804 group (Spec. H) has the built-in function which automatically switches from low to middle-speed mode either by the SCL/SDA interrupt or by program.

●Middle-speed mode automatic switch by SCL/SDA Interrupt

The SCL/SDA interrupt source enables an automatic switch when the middle-speed mode automatic switch set bit (bit 1) of MISRG (address 0010₁₆) is set to "1". The conditions for an automatic switch execution depend on the settings of bits 5 and 6 of the I²C START/STOP condition control register (address 0016₁₆). Bit 5 is the SCL/SDA interrupt pin polarity selection bit and bit 6 is the SCL/SDA interrupt pin selection bit. The main clock oscillation stabilizing time can also be selected by middle-speed mode automatic switch wait time set bit (bit 2) of the MISRG.

●Middle-speed mode automatic switch by program

The middle-speed mode can also be automatically switched by program while operating in low-speed mode. By setting the middle-speed automatic switch start bit (bit 3) of MISRG (address 0010₁₆) to "1" in the condition that the middle-speed mode automatic switch set bit is "1" while operating in low-speed mode, the MCU will automatically switch to middle-speed mode. In this case, the oscillation stabilizing time of the main clock can be selected by the middle-speed automatic switch wait time set bit (bit 2) of MISRG (address 0010₁₆).

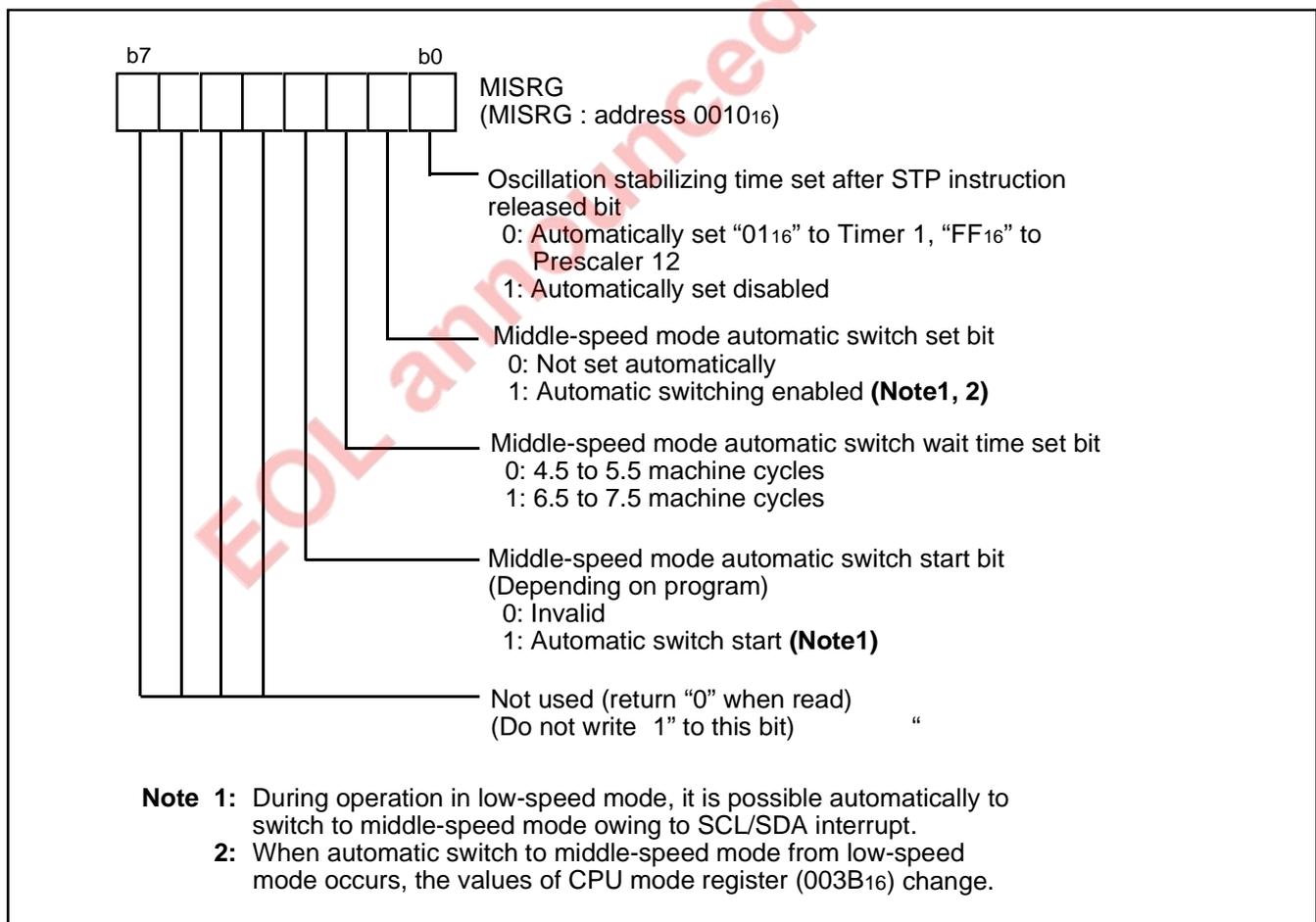


Fig. 9 Structure of MISRG

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

The RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The ROM area can program/erase.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

Access to this area with only 2 bytes is possible in the special page addressing mode.

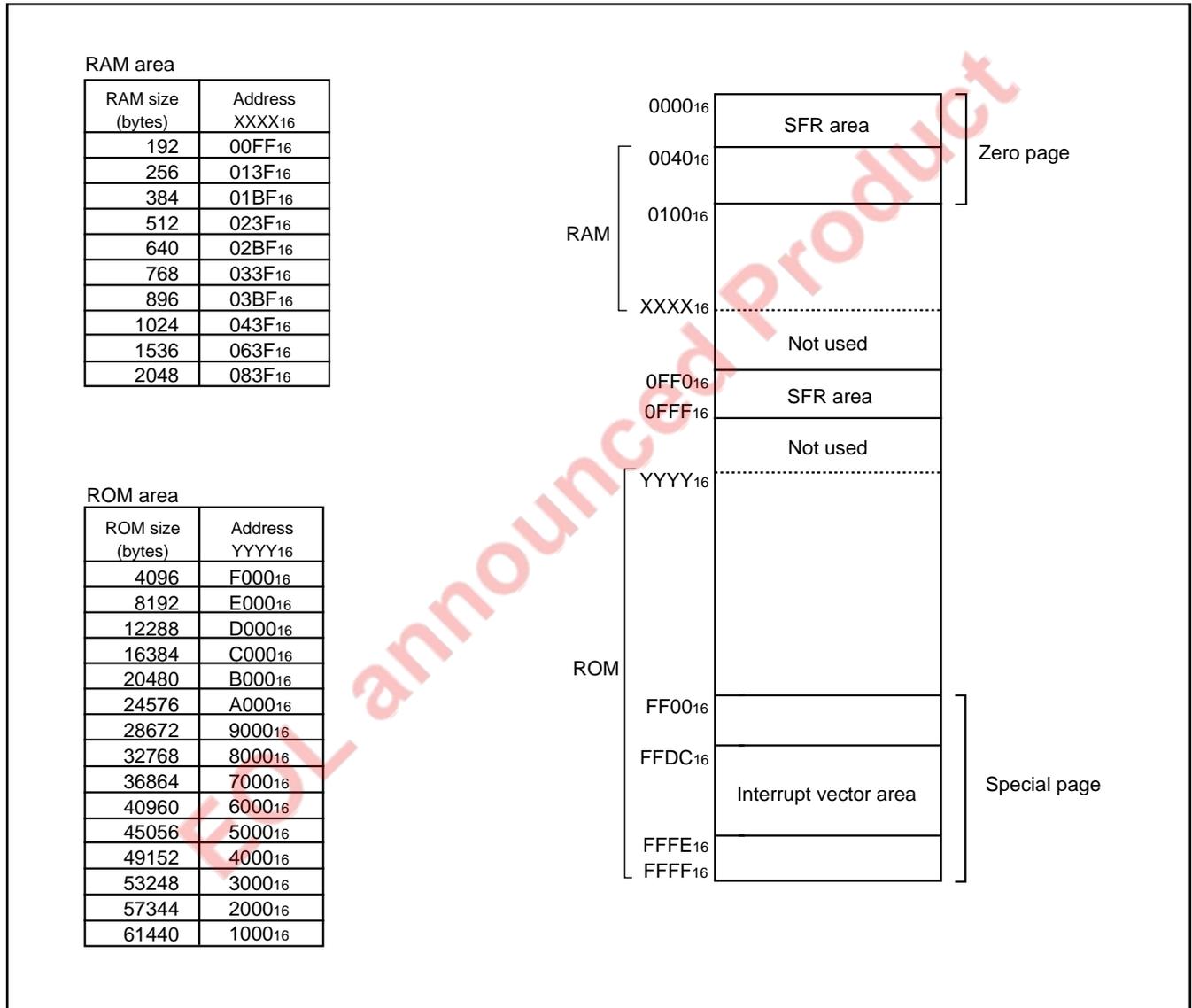


Fig. 10 Memory map diagram

| | | | |
|--------------------|--|--------------------|--|
| 0000 ₁₆ | Port P0 (P0) | 0020 ₁₆ | Prescaler 12 (PRE12) |
| 0001 ₁₆ | Port P0 direction register (P0D) | 0021 ₁₆ | Timer 1 (T1) |
| 0002 ₁₆ | Port P1 (P1) | 0022 ₁₆ | Timer 2 (T2) |
| 0003 ₁₆ | Port P1 direction register (P1D) | 0023 ₁₆ | Timer XY mode register (TM) |
| 0004 ₁₆ | Port P2 (P2) | 0024 ₁₆ | Prescaler X (PREX) |
| 0005 ₁₆ | Port P2 direction register (P2D) | 0025 ₁₆ | Timer X (TX) |
| 0006 ₁₆ | Port P3 (P3) | 0026 ₁₆ | Prescaler Y (PREY) |
| 0007 ₁₆ | Port P3 direction register (P3D) | 0027 ₁₆ | Timer Y (TY) |
| 0008 ₁₆ | Port P4 (P4) | 0028 ₁₆ | Timer Z low-order (TZL) |
| 0009 ₁₆ | Port P4 direction register (P4D) | 0029 ₁₆ | Timer Z high-order (TZH) |
| 000A ₁₆ | Port P5 (P5) | 002A ₁₆ | Timer Z mode register (TzM) |
| 000B ₁₆ | Port P5 direction register (P5D) | 002B ₁₆ | PWM control register (PWMCON) |
| 000C ₁₆ | Port P6 (P6) | 002C ₁₆ | PWM prescaler (PREPWM) |
| 000D ₁₆ | Port P6 direction register (P6D) | 002D ₁₆ | PWM register (PWM) |
| 000E ₁₆ | Timer 12, X count source selection register (T12XCSS) | 002E ₁₆ | |
| 000F ₁₆ | Timer Y, Z count source selection register (TYZCSS) | 002F ₁₆ | Baud rate generator 3 (BRG3) |
| 0010 ₁₆ | MISRG | 0030 ₁₆ | Transmit/Receive buffer register 3 (TB3/RB3) |
| 0011 ₁₆ | I ² C data shift register (S0) | 0031 ₁₆ | Serial I/O3 status register (SIO3STS) |
| 0012 ₁₆ | I ² C special mode status register (S3) | 0032 ₁₆ | Serial I/O3 control register (SIO3CON) |
| 0013 ₁₆ | I ² C status register (S1) | 0033 ₁₆ | UART3 control register (UART3CON) |
| 0014 ₁₆ | I ² C control register (S1D) | 0034 ₁₆ | AD/DA control register (ADCON) |
| 0015 ₁₆ | I ² C clock control register (S2) | 0035 ₁₆ | AD conversion register 1 (AD1) |
| 0016 ₁₆ | I ² C START/STOP condition control register (S2D) | 0036 ₁₆ | DA1 conversion register (DA1) |
| 0017 ₁₆ | I ² C special mode control register (S3D) | 0037 ₁₆ | DA2 conversion register (DA2) |
| 0018 ₁₆ | Transmit/Receive buffer register 1 (TB1/RB1) | 0038 ₁₆ | AD conversion register 2 (AD2) |
| 0019 ₁₆ | Serial I/O1 status register (SIO1STS) | 0039 ₁₆ | Interrupt source selection register (INTSEL) |
| 001A ₁₆ | Serial I/O1 control register (SIO1CON) | 003A ₁₆ | Interrupt edge selection register (INTEDGE) |
| 001B ₁₆ | UART1 control register (UART1CON) | 003B ₁₆ | CPU mode register (CPUM) |
| 001C ₁₆ | Baud rate generator 1 (BRG1) | 003C ₁₆ | Interrupt request register 1 (IREQ1) |
| 001D ₁₆ | Serial I/O2 control register (SIO2CON) | 003D ₁₆ | Interrupt request register 2 (IREQ2) |
| 001E ₁₆ | Watchdog timer control register (WDTCON) | 003E ₁₆ | Interrupt control register 1 (ICON1) |
| 001F ₁₆ | Serial I/O2 register (SIO2) | 003F ₁₆ | Interrupt control register 2 (ICON2) |
| 0FE0 ₁₆ | Flash memory control register 0 (FMCR0) | 0FF0 ₁₆ | Port P0 pull-up control register (PULL0) |
| 0FE1 ₁₆ | Flash memory control register 1 (FMCR1) | 0FF1 ₁₆ | Port P1 pull-up control register (PULL1) |
| 0FE2 ₁₆ | Flash memory control register 2 (FMCR2) | 0FF2 ₁₆ | Port P2 pull-up control register (PULL2) |
| 0FE3 ₁₆ | Reserved * | 0FF3 ₁₆ | Port P3 pull-up control register (PULL3) |
| 0FE4 ₁₆ | Reserved * | 0FF4 ₁₆ | Port P4 pull-up control register (PULL4) |
| 0FE5 ₁₆ | Reserved * | 0FF5 ₁₆ | Port P5 pull-up control register (PULL5) |
| 0FE6 ₁₆ | Reserved * | 0FF6 ₁₆ | Port P6 pull-up control register (PULL6) |
| 0FE7 ₁₆ | Reserved * | 0FF7 ₁₆ | I ² C slave address register 0 (S0D0) |
| 0FE8 ₁₆ | Reserved * | 0FF8 ₁₆ | I ² C slave address register 1 (S0D1) |
| 0FE9 ₁₆ | Reserved * | 0FF9 ₁₆ | I ² C slave address register 2 (S0D2) |
| 0FEA ₁₆ | Reserved * | | |
| 0FEB ₁₆ | Reserved * | | |
| 0FEC ₁₆ | Reserved * | | |
| 0FED ₁₆ | Reserved * | | |
| 0FEE ₁₆ | Reserved * | | |
| 0FEF ₁₆ | Reserved * | | |

* Reserved area: Do not write any data to these addresses, because these areas are reserved.

Fig. 11 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When "0" is written to the bit corresponding to a pin, that pin be-

comes an input pin. When "1" is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 5 I/O port function

| Pin | Name | I/O Structure | Non-Port Function | Related SFRs | Ref.No. |
|---|---------|---|--|--|------------------------------|
| P00/AN8–P07/AN15 | Port P0 | CMOS compatible input level | A/D converter input | AD/DA control register | (1) |
| P10/INT41 P11/INT01 | Port P1 | CMOS 3-state output | External interrupt input | Interrupt edge selection register | (2) |
| P12–P17 | | | | | (3) |
| P20/LED0– P27/LED7 | Port P2 | | | | |
| P30/DA1 P31/DA2 | Port P3 | CMOS compatible input level | D/A converter output | AD/DA control register | (4) |
| P32/SDA P33/SCL | | CMOS 3-state output | | | |
| | | CMOS compatible input level N-channel open-drain output CMOS/SMBUS input level (when selecting I ² C-BUS interface function) | I ² C-BUS interface function I/O | I ² C control register | (5) |
| P34/RxD3 P35/TxD3 P36/SCLK3 P37/SRDY3 | | CMOS compatible input level CMOS 3-state output | Serial I/O3 function I/O | Serial I/O3 control register UART3 control register | (6) (7) (8) (9) |
| P40/INT40/XCIN P41/INT00/XCOUT | Port P4 | CMOS compatible input level CMOS 3-state output | External interrupt input | Interrupt edge selection register | (10) |
| P42/INT1 P43/INT2 | | | Sub-clock generating circuit | Interrupt edge selection register CPU mode register | (11) |
| P44/RxD1 P45/TxD1 P46/SCLK1 | | | External interrupt input | Interrupt edge selection register | (2) |
| P47/SRDY1/CNTR2 | | | Serial I/O1 function I/O | Serial I/O1 control register UART1 control register | (6) (7) (8) |
| P50/SIN2 P51/SOUT2 P52/SCLK2 P53/SRDY2 | Port P5 | CMOS compatible input level CMOS 3-state output | Serial I/O1 function I/O Timer Z function I/O | Serial I/O1 control register Timer Z mode register | (12) |
| P54/CNTR0 P55/CNTR1 | | | Serial I/O2 function I/O | Serial I/O2 control register | (13) (14) (15) (16) |
| P56/PWM | | | Timer X, Y function I/O | Timer XY mode register | (17) |
| P57/INT3 | | | PWM output | PWM control register | (18) |
| | | | External interrupt input | Interrupt edge selection register | (2) |
| P60/AN0–P67/AN7 | Port P6 | CMOS compatible input level CMOS 3-state output | A/D converter input | AD/DA control register | (1) |

Notes 1: Refer to the applicable sections how to use double-function ports as function I/O ports.

2: Make sure that the input level at each pin is either 0 V or V_{CC} during execution of the STP instruction.

When an input level is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate.

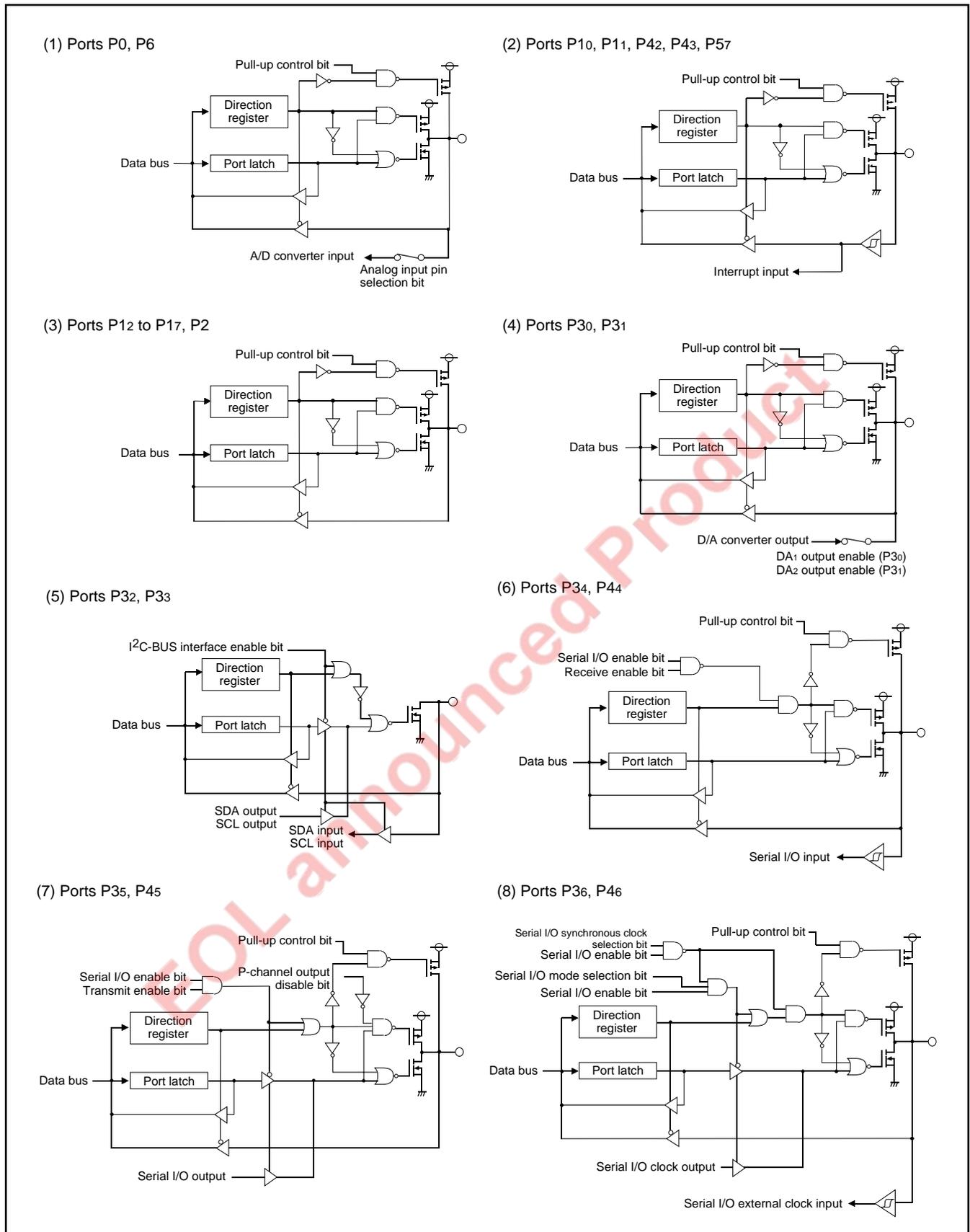


Fig. 12 Port block diagram (1)

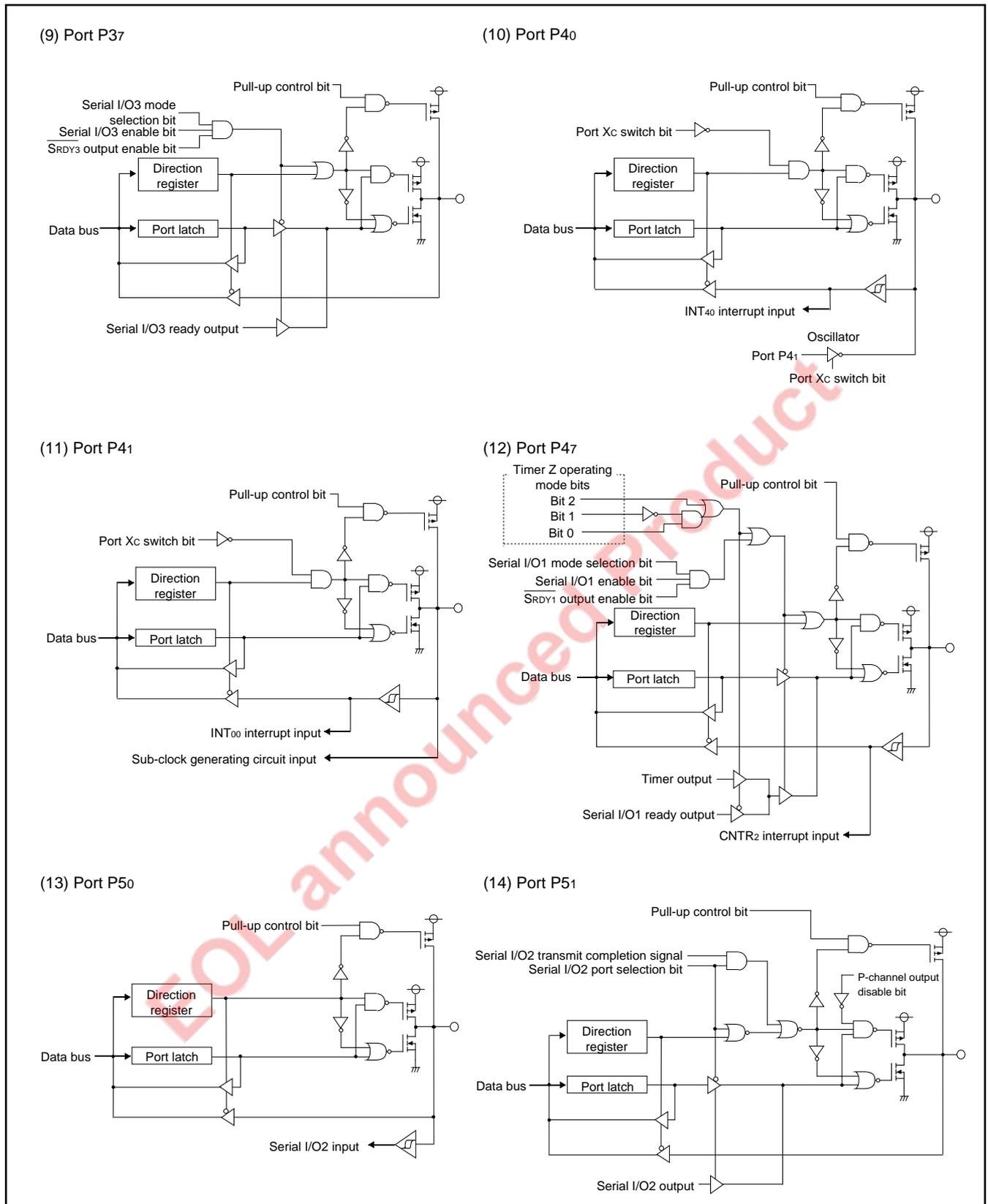


Fig. 13 Port block diagram (2)

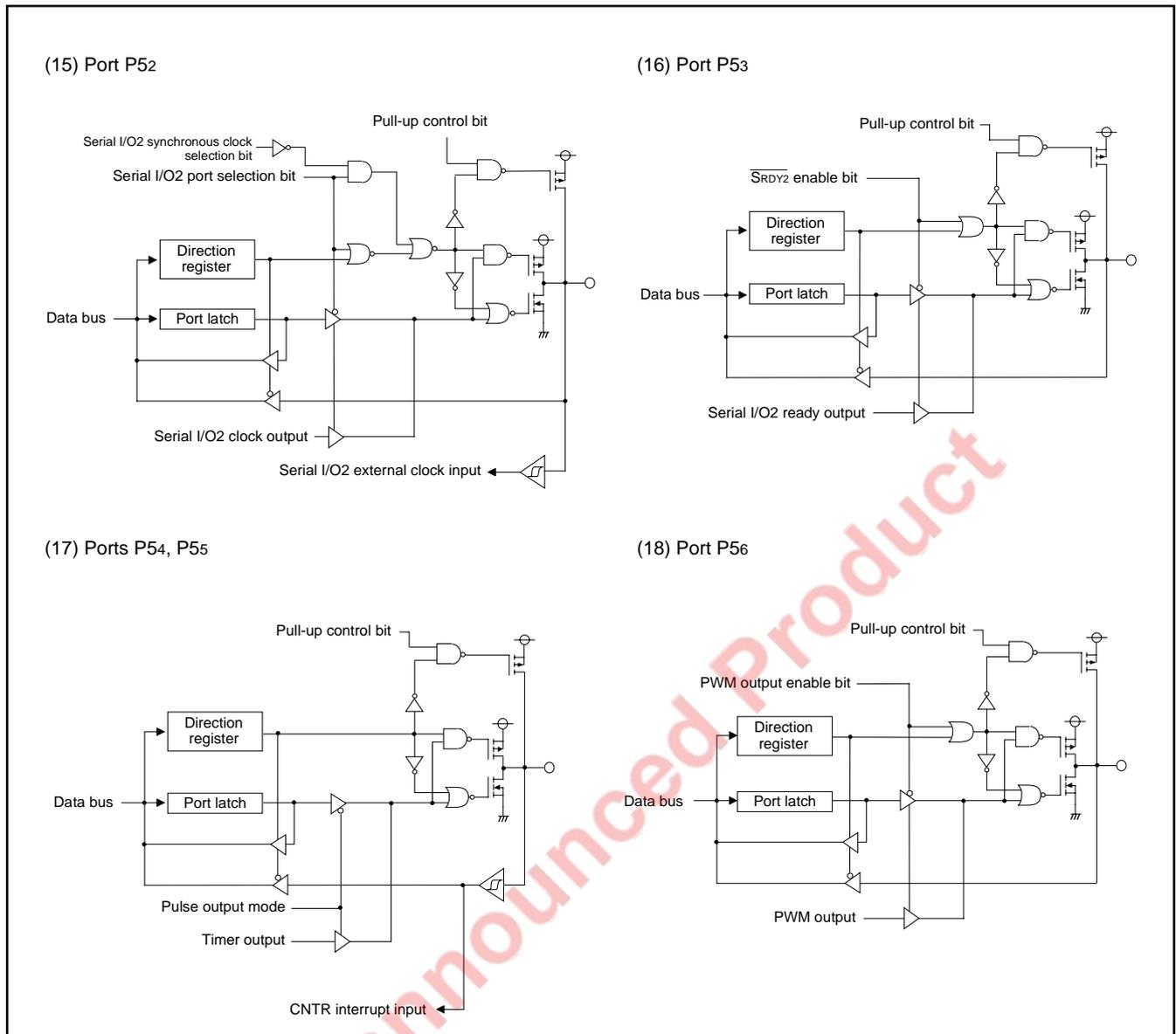


Fig. 14 Port block diagram (3)

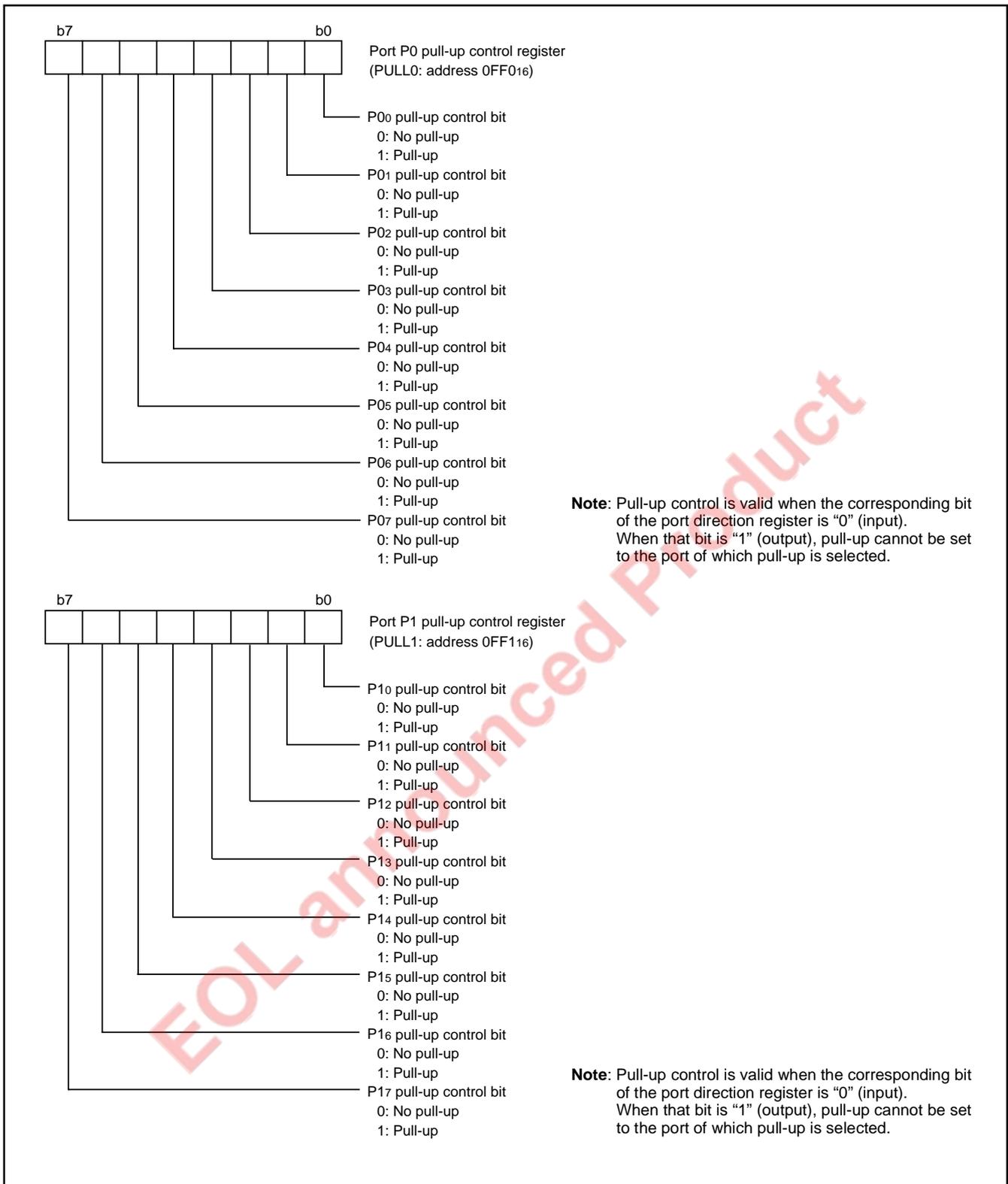


Fig. 15 Structure of port pull-up control register (1)

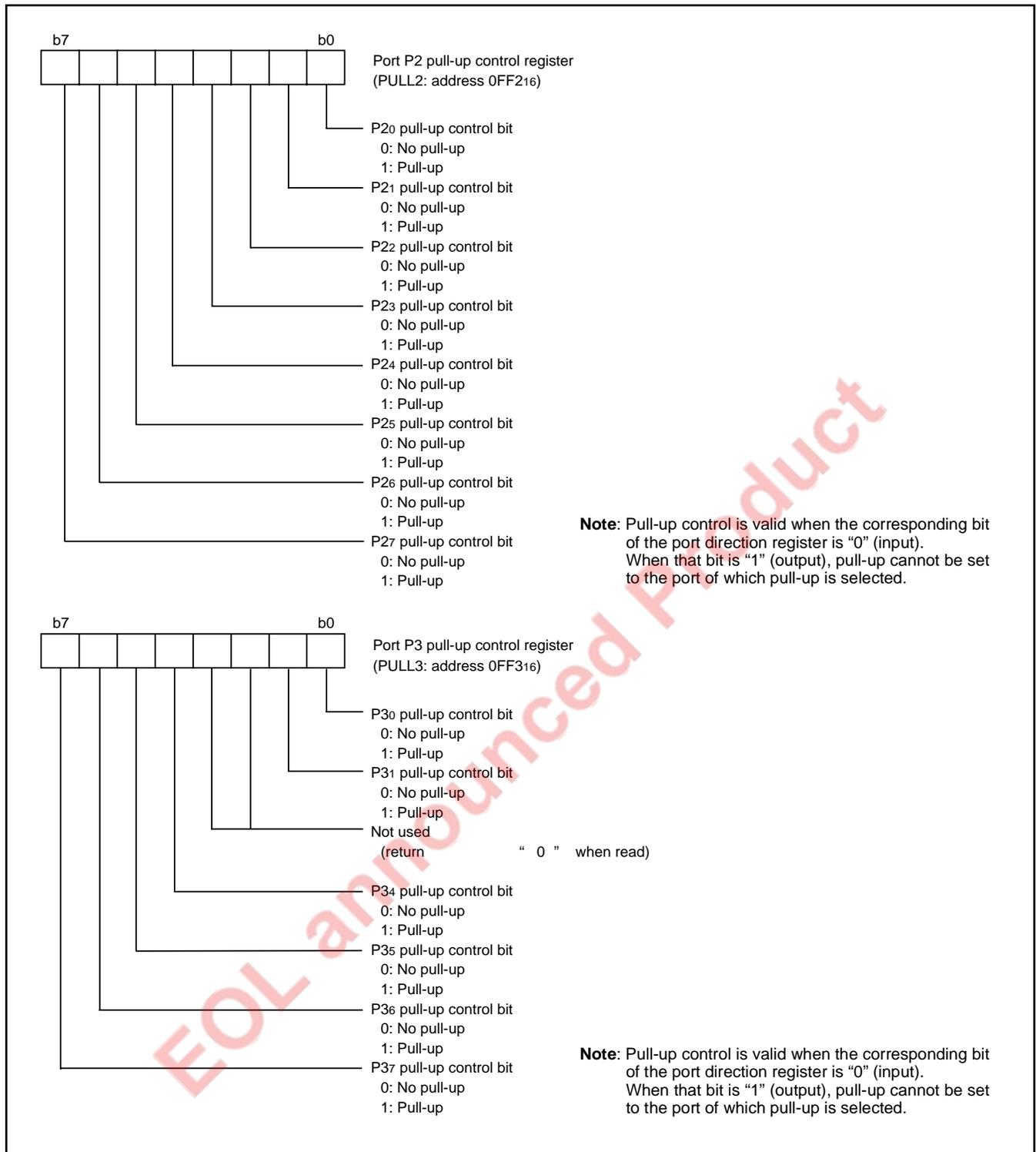


Fig. 16 Structure of port pull-up control register (2)

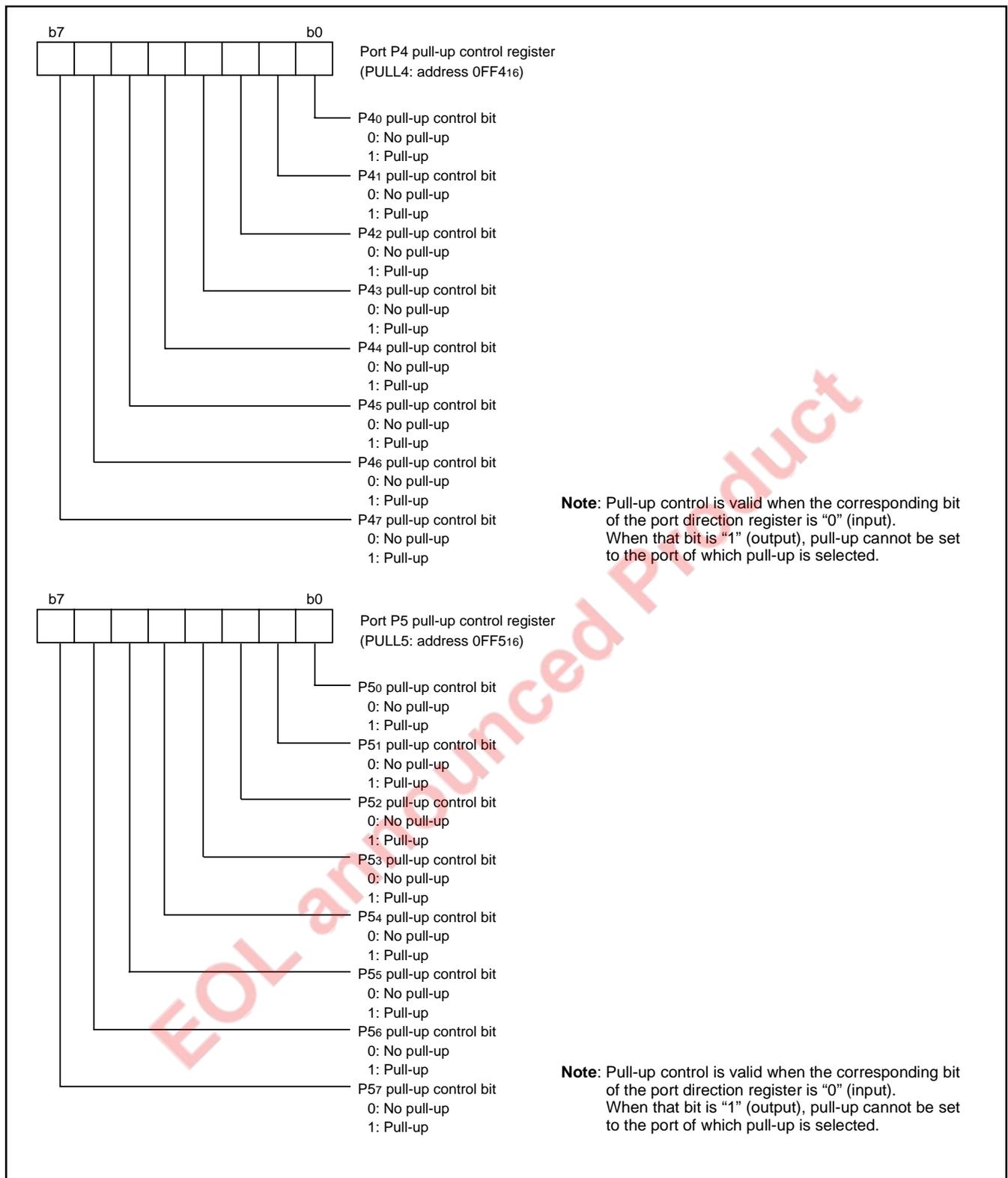


Fig. 17 Structure of port pull-up control register (3)

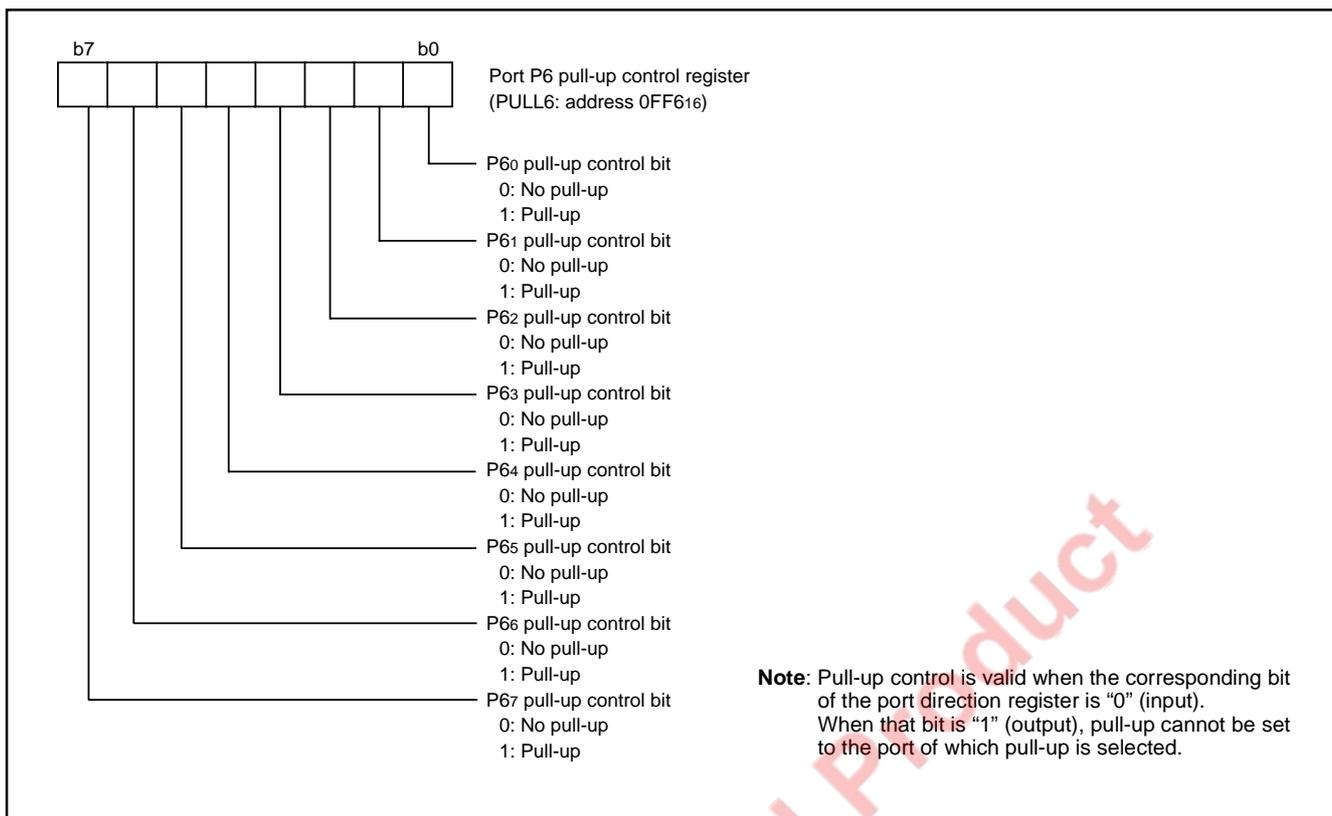


Fig. 18 Structure of port pull-up control register (4)

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INTERRUPTS

The 3804 group (Spec. H)'s interrupts are a type of vector and occur by 16 sources among 23 sources: nine external, thirteen internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are "1" and the interrupt disable flag is "0".

Interrupt enable bits can be set or cleared by software.

Interrupt request bits can be cleared by software, but cannot be set by software.

The reset and the BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the reset and the BRK instruction interrupt.

When several interrupt requests occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

Interrupt Source Selection

Which of each combination of the following interrupt sources can be selected by the interrupt source selection register (address 003916).

1. INT₀ or Timer Z
2. Serial I/O1 transmission or SCL, SDA
3. CNTR₀ or SCL, SDA
4. CNTR₁ or Serial I/O3 reception
5. Serial I/O2 or Timer Z
6. INT₂ or I²C
7. INT₄ or CNTR₂
8. A/D converter or serial I/O3 transmission

External Interrupt Pin Selection

The occurrence sources of the external interrupt INT₀ and INT₄ can be selected from either input from INT₀₀ and INT₄₀ pin, or input from INT₀₁ and INT₄₁ pin by the INT₀, INT₄ interrupt switch bit of interrupt edge selection register (bit 6 of address 003A16).

■ Notes

When setting the followings, the interrupt request bit may be set to "1".

- When setting external interrupt active edge

Related register: Interrupt edge selection register (address 003A16)
 Timer XY mode register (address 002316)
 Timer Z mode register (address 002A16)
 I²C START/STOP condition control register
 (address 001616)

- When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Related register: Interrupt source selection register
 (address 003916)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

- ① Set the corresponding interrupt enable bit to "0" (disabled).
- ② Set the interrupt edge select bit or the interrupt source select bit to "1".
- ③ Set the corresponding interrupt request bit to "0" after 1 or more instructions have been executed.
- ④ Set the corresponding interrupt enable bit to "1" (enabled).

Table 6 Interrupt vector addresses and priority

| Interrupt Source | Priority | Vector Addresses (Note 1) | | Interrupt Request Generating Conditions | Remarks |
|--------------------------|----------|---------------------------|--------------------|--|---|
| | | High | Low | | |
| Reset (Note 2) | 1 | FFFD ₁₆ | FFFC ₁₆ | At reset | Non-maskable |
| INT ₀ | 2 | FFFB ₁₆ | FFFA ₁₆ | At detection of either rising or falling edge of INT ₀ input | External interrupt (active edge selectable) |
| Timer Z | | | | At timer Z underflow | |
| INT ₁ | 3 | FFF9 ₁₆ | FFF8 ₁₆ | At detection of either rising or falling edge of INT ₁ input | External interrupt (active edge selectable) |
| Serial I/O1 reception | 4 | FFF7 ₁₆ | FFF6 ₁₆ | At completion of serial I/O1 data reception | Valid when serial I/O1 is selected |
| Serial I/O1 transmission | 5 | FFF5 ₁₆ | FFF4 ₁₆ | At completion of serial I/O1 transmission shift or when transmission buffer is empty | Valid when serial I/O1 is selected |
| SCL, SDA | | | | At detection of either rising or falling edge of SCL or SDA | |
| Timer X | 6 | FFF3 ₁₆ | FFF2 ₁₆ | At timer X underflow | |
| Timer Y | 7 | FFF1 ₁₆ | FFF0 ₁₆ | At timer Y underflow | |
| Timer 1 | 8 | FFEF ₁₆ | FFEE ₁₆ | At timer 1 underflow | STP release timer underflow |
| Timer 2 | 9 | FFED ₁₆ | FFEC ₁₆ | At timer 2 underflow | |
| CNTR ₀ | 10 | FFEB ₁₆ | FFEA ₁₆ | At detection of either rising or falling edge of CNTR ₀ input | External interrupt (active edge selectable) |
| SCL, SDA | | | | At detection of either rising or falling edge of SCL or SDA | |
| CNTR ₁ | 11 | FFE9 ₁₆ | FFE8 ₁₆ | At detection of either rising or falling edge of CNTR ₁ input | External interrupt (active edge selectable) |
| Serial I/O3 reception | | | | At completion of serial I/O3 data reception | |
| Serial I/O2 | 12 | FFE7 ₁₆ | FFE6 ₁₆ | At completion of serial I/O2 data transmission or reception | Valid when serial I/O2 is selected |
| Timer Z | | | | At timer Z underflow | |
| INT ₂ | 13 | FFE5 ₁₆ | FFE4 ₁₆ | At detection of either rising or falling edge of INT ₂ input | External interrupt (active edge selectable) |
| I ² C | | | | At completion of data transfer | |
| INT ₃ | 14 | FFE3 ₁₆ | FFE2 ₁₆ | At detection of either rising or falling edge of INT ₃ input | External interrupt (active edge selectable) |
| INT ₄ | 15 | FFE1 ₁₆ | FFE0 ₁₆ | At detection of either rising or falling edge of INT ₄ input | External interrupt (active edge selectable) |
| CNTR ₂ | | | | At detection of either rising or falling edge of CNTR ₂ input | |
| A/D converter | 16 | FFDF ₁₆ | FFDE ₁₆ | At completion of A/D conversion | Valid when serial I/O3 is selected |
| Serial I/O3 transmission | | | | At completion of serial I/O3 transmission shift or when transmission buffer is empty | |
| BRK instruction | 17 | FFDD ₁₆ | FFDC ₁₆ | At BRK instruction execution | Non-maskable software interrupt |

Notes 1: Vector addresses contain interrupt jump destination addresses.

2: Reset function in the same way as an interrupt with the highest priority.

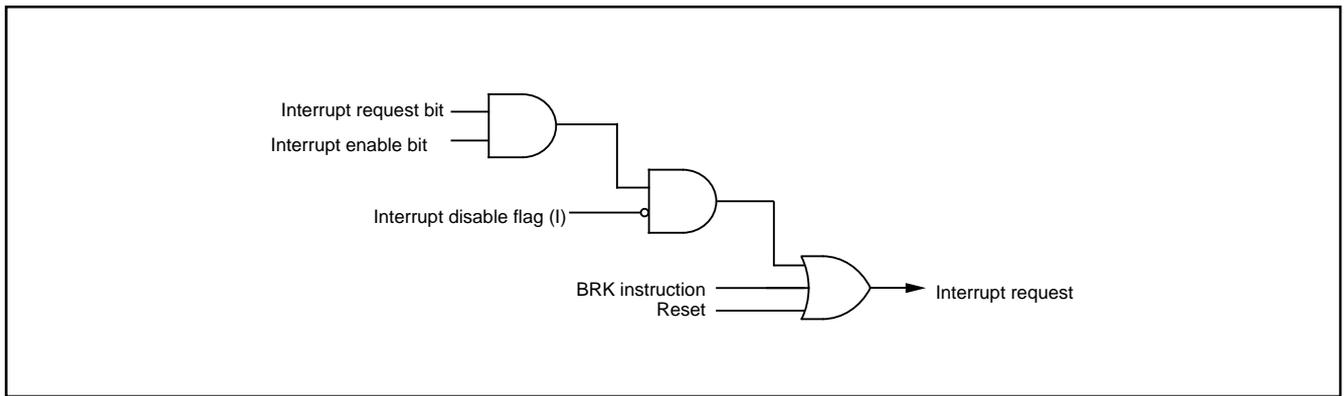


Fig. 19 Interrupt control

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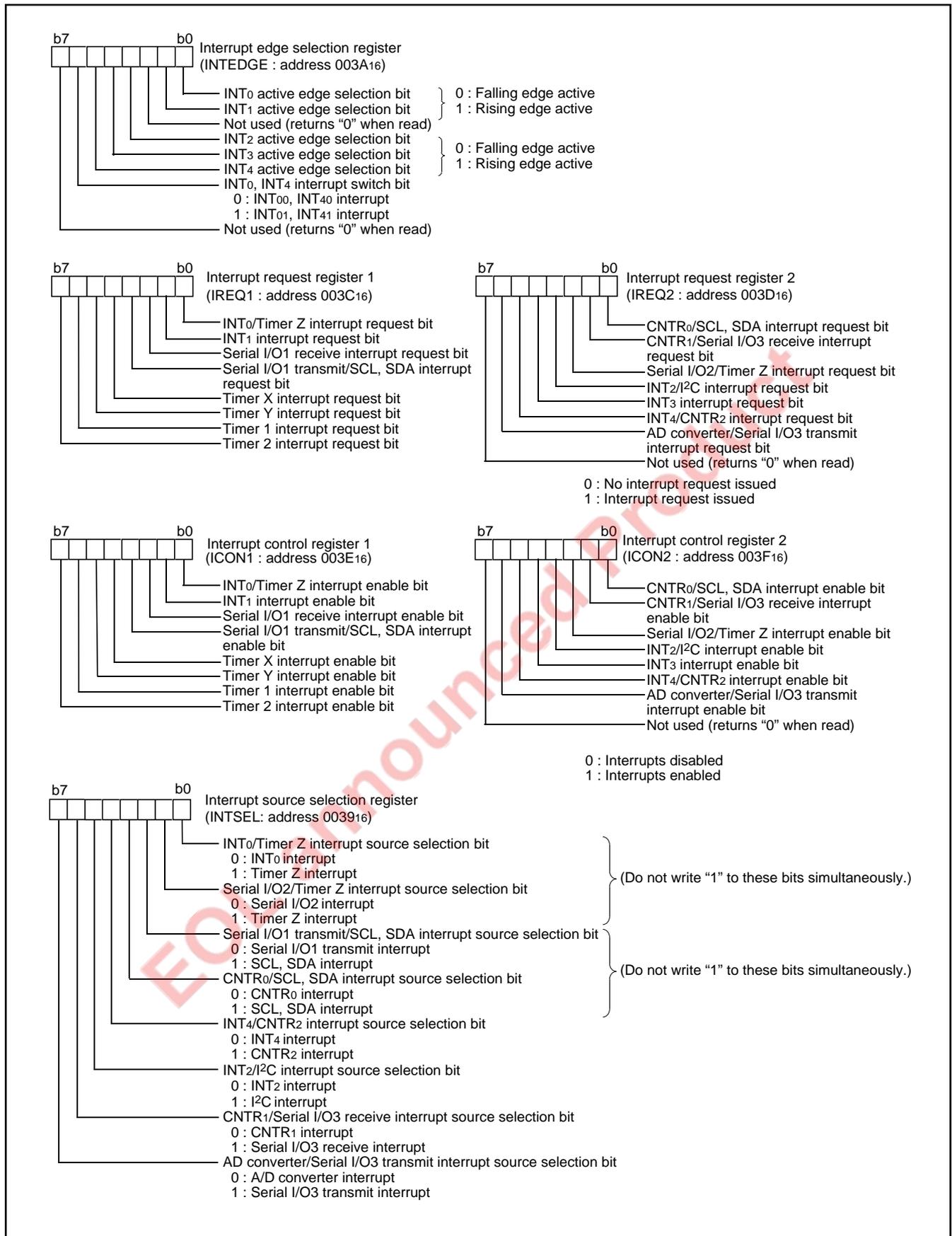


Fig. 20 Structure of interrupt-related registers

TIMERS

●8-bit Timers

The 3804 group (Spec. H) has four 8-bit timers: timer 1, timer 2, timer X, and timer Y.

The timer 1 and timer 2 use one prescaler in common, and the timer X and timer Y use each prescaler. Those are 8-bit prescalers. Each of the timers and prescalers has a timer latch or a prescaler latch.

The division ratio of each timer or prescaler is given by $1/(n + 1)$, where n is the value in the corresponding timer or prescaler latch. All timers are down-counters. When the timer reaches "00₁₆", an underflow occurs at the next count pulse and the contents of the corresponding timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

●Timer divider

The divider count source is switched by the main clock division ratio selection bits of CPU mode register (bits 7 and 6 at address 003B₁₆). When these bits are "00" (high-speed mode) or "01" (middle-speed mode), X_{IN} is selected. When these bits are "10" (low-speed mode), X_{CIN} is selected.

●Prescaler 12

The prescaler 12 counts the output of the timer divider. The count source is selected by the timer 12, X count source selection register among $1/2$, $1/4$, $1/8$, $1/16$, $1/32$, $1/64$, $1/128$, $1/256$, $1/512$, $1/1024$ of $f(X_{IN})$ or $f(X_{CIN})$.

Timer 1 and Timer 2

The timer 1 and timer 2 counts the output of prescaler 12 and periodically set the interrupt request bit.

●Prescaler X and prescaler Y

The prescaler X and prescaler Y count the output of the timer divider or $f(X_{CIN})$. The count source is selected by the timer 12, X count source selection register (address 000E₁₆) and the timer Y, Z count source selection register (address 000F₁₆) among $1/2$, $1/4$, $1/8$, $1/16$, $1/32$, $1/64$, $1/128$, $1/256$, $1/512$, and $1/1024$ of $f(X_{IN})$ or $f(X_{CIN})$; and $f(X_{CIN})$.

Timer X and Timer Y

The timer X and timer Y can each select one of four operating modes by setting the timer XY mode register (address 0023₁₆).

(1) Timer mode

●Mode selection

This mode can be selected by setting "00" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023₁₆).

●Explanation of operation

The timer count operation is started by setting "0" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 0023₁₆).

When the timer reaches "00₁₆", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

(2) Pulse output mode

●Mode selection

This mode can be selected by setting "01" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 0023₁₆).

●Explanation of operation

The operation is the same as the timer mode s. Moreover the pulse which is inverted each time the timer underflows is output from CNTR₀/CNTR₁ pin. Regardless of the timer counting or not the output of CNTR₀/CNTR₁ pin is initialized to the level of specified by their active edge switch bits when writing to the timer. When the CNTR₀ active edge switch bit (bit 2) and the CNTR₁ active edge switch bit (bit 6) of the timer XY mode register (address 0023₁₆) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

Switching the CNTR₀ or CNTR₁ active edge switch bit will reverse the output level of the corresponding CNTR₀ or CNTR₁ pin.

■Precautions

Set the double-function port of CNTR₀/CNTR₁ pin and port P54/P55 to output in this mode.

(3) Event counter mode

●Mode selection

This mode can be selected by setting "10" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 002316).

●Explanation of operation

The operation is the same as the timer mode's except that the timer counts signals input from the CNTR0 or CNTR1 pin. The valid edge for the count operation depends on the CNTR0 active edge switch bit (bit 2) or the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 002316). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

■Precautions

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in this mode.

(4) Pulse width measurement mode

●Mode selection

This mode can be selected by setting "11" to the timer X operating mode bits (bits 1 and 0) and the timer Y operating mode bits (bits 5 and 4) of the timer XY mode register (address 002316).

●Explanation of operation

When the CNTR0 active edge switch bit (bit 2) or the CNTR1 active edge switch bit (bit 6) of the timer XY mode register (address 002316) is "1", the timer counts during the term of one falling edge of CNTR0/CNTR1 pin input until the next rising edge of input ("L" term). When it is "0", the timer counts during the term of one rising edge input until the next falling edge input ("H" term).

■Precautions

Set the double-function port of CNTR0/CNTR1 pin and port P54/P55 to input in this mode.

The count operation can be stopped by setting "1" to the timer X count stop bit (bit 3) and the timer Y count stop bit (bit 7) of the timer XY mode register (address 002316). The interrupt request bit is set to "1" each time the timer underflows.

●Precautions when switching count source

When switching the count source by the timer 12, X and Y count source selection bits, the value of timer count is altered in considerable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

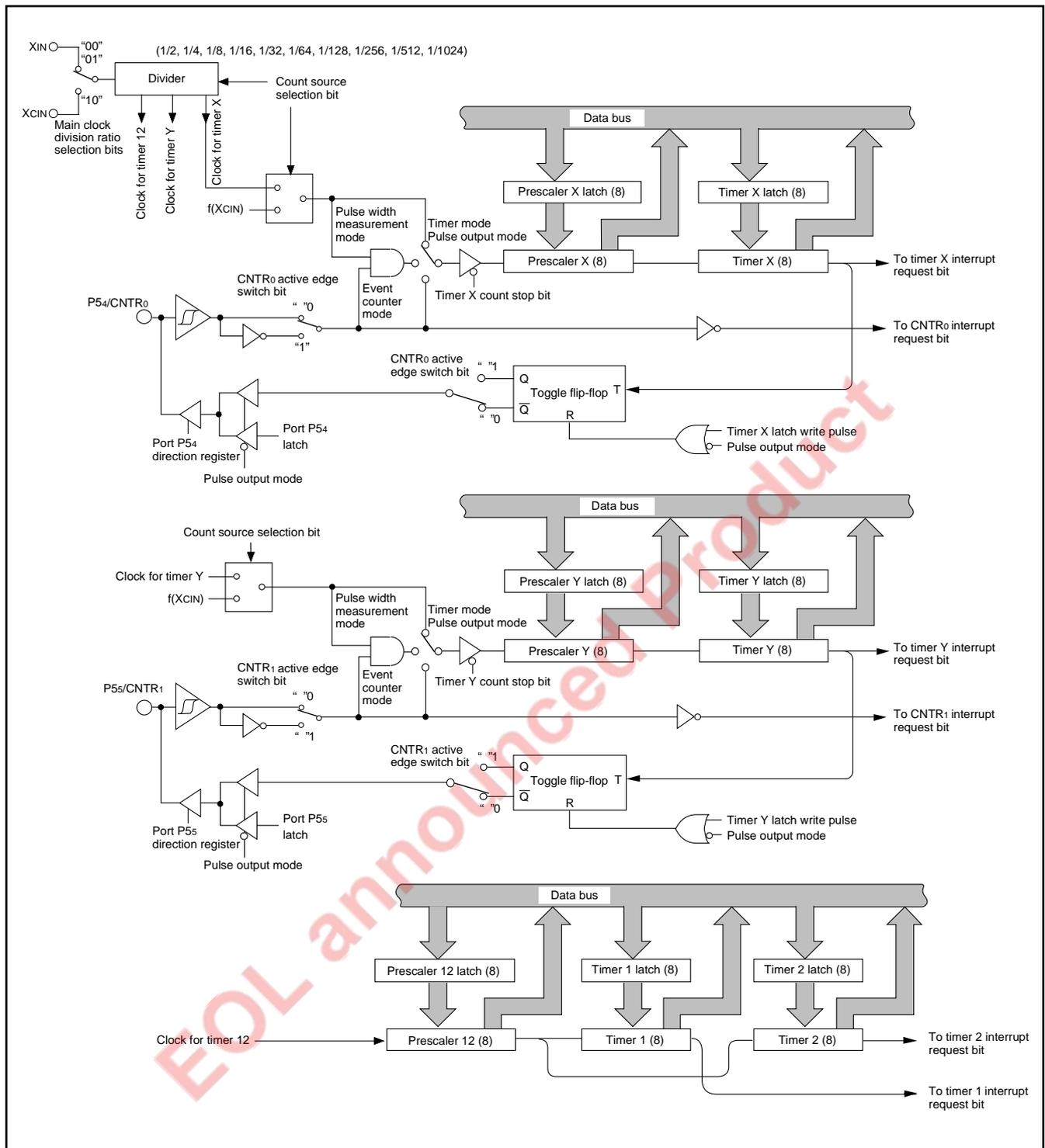


Fig. 21 Block diagram of timer X, timer Y, timer 1, and timer 2

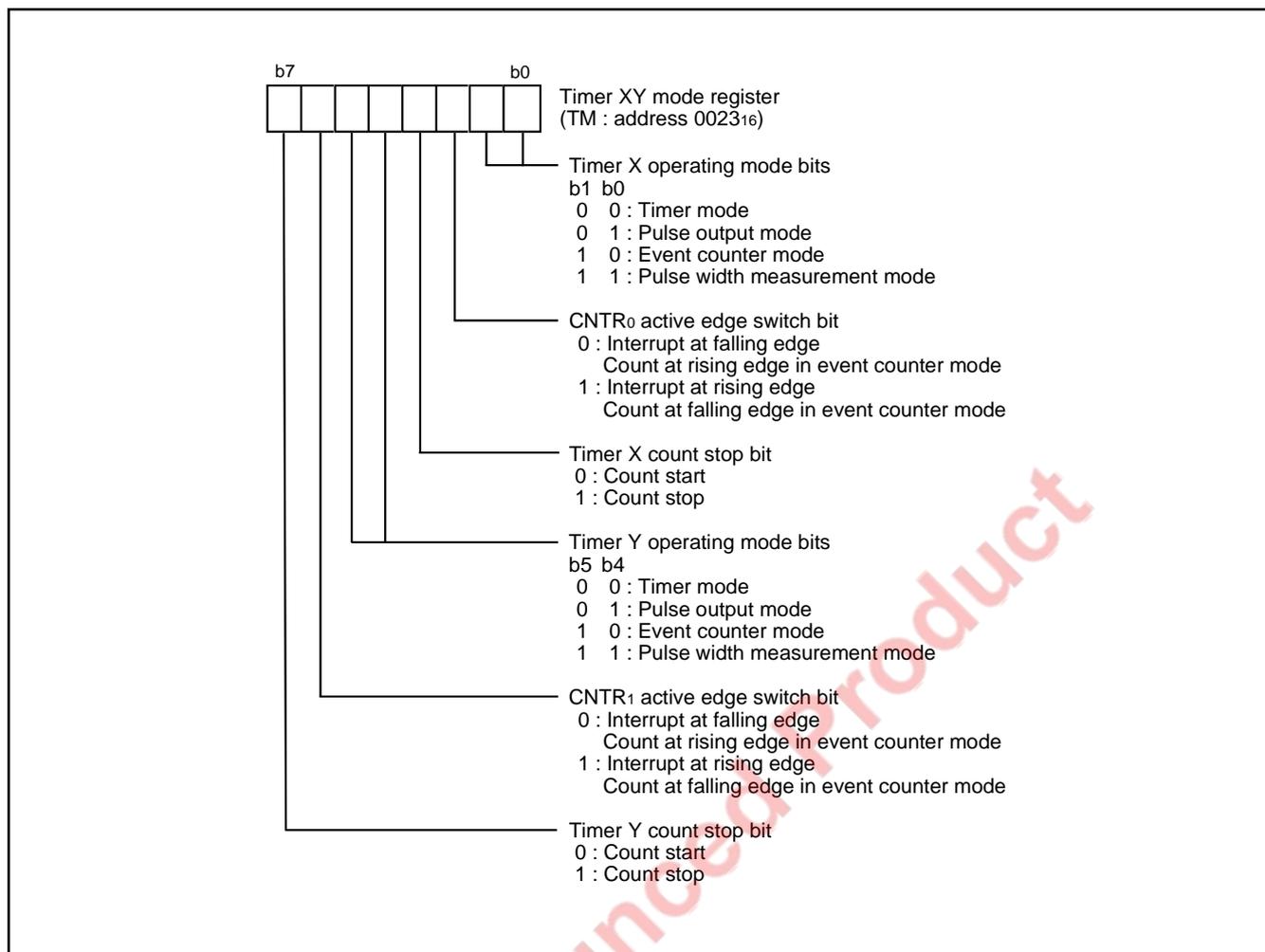


Fig. 22 Structure of timer XY mode register

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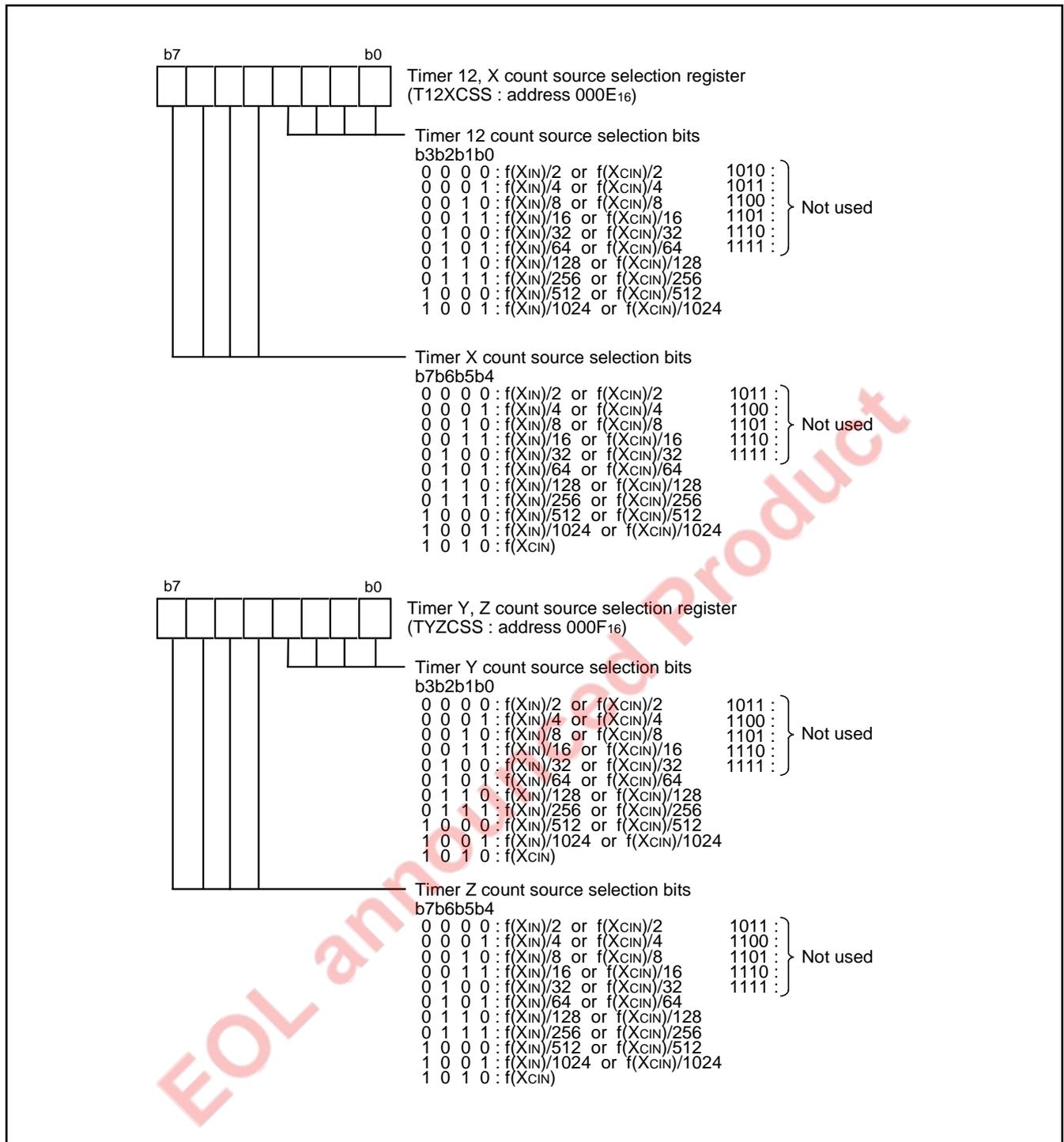


Fig. 23 Structure of timer 12, X and timer Y, Z count source selection registers

●16-bit Timer

The timer Z is a 16-bit timer. When the timer reaches "0000₁₆", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to the timer Z is set to "1".

When reading/writing to the timer Z, perform reading/writing to both the high-order byte and the low-order byte. When reading the timer Z, read from the high-order byte first, followed by the low-order byte. Do not perform the writing to the timer Z between read operation of the high-order byte and read operation of the low-order byte. When writing to the timer Z, write to the low-order byte first, followed by the high-order byte. Do not perform the reading to the timer Z between write operation of the low-order byte and write operation of the high-order byte.

The timer Z can select the count source by the timer Z count source selection bits of timer Y, Z count source selection register (bits 7 to 4 at address 000F₁₆).

Timer Z can select one of seven operating modes by setting the timer Z mode register (address 002A₁₆).

(1) Timer mode

●Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A₁₆).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(X_{IN})$; or $f(X_{CIN})$ can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(X_{CIN})$; or $f(X_{CIN})$ can be selected as the count source.

●Interrupt

When an underflow occurs, the INT0/timer Z interrupt request bit (bit 0) of the interrupt request register 1 (address 003C₁₆) is set to "1".

●Explanation of operation

During timer stop, usually write data to a latch and a timer at the same time to set the timer value.

The timer count operation is started by setting "0" to the timer Z count stop bit (bit 6) of the timer Z mode register (address 002A₁₆).

When the timer reaches "0000₁₆", an underflow occurs at the next count pulse and the contents of timer latch are reloaded into the timer and the count is continued.

When writing data to the timer during operation, the data is written only into the latch. Then the new latch value is reloaded into the timer at the next underflow.

(2) Event counter mode

●Mode selection

This mode can be selected by setting "000" to the timer Z operating mode bits (bits 2 to 0) and setting "1" to the timer/event counter mode switch bit (bit 7) of the timer Z mode register (address 002A₁₆).

The valid edge for the count operation depends on the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A₁₆). When it is "0", the rising edge is valid. When it is "1", the falling edge is valid.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

●Explanation of operation

The operation is the same as the timer mode's.

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

Figure 26 shows the timing chart of the timer/event counter mode.

(3) Pulse output mode

●Mode selection

This mode can be selected by setting "001" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A₁₆).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(X_{IN})$; or $f(X_{CIN})$ can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(X_{CIN})$; or $f(X_{CIN})$ can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

●Explanation of operation

The operation is the same as the timer mode's. Moreover the pulse which is inverted each time the timer underflows is output from CNTR2 pin. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A₁₆) is "0", the output starts with "H" level. When it is "1", the output starts with "L" level.

■Precautions

The double-function port of CNTR2 pin and port P47 is automatically set to the timer pulse output port in this mode.

The output from CNTR2 pin is initialized to the level depending on CNTR2 active edge switch bit by writing to the timer.

When the value of the CNTR2 active edge switch bit is changed, the output level of CNTR2 pin is inverted.

Figure 27 shows the timing chart of the pulse output mode.

(4) Pulse period measurement mode

●Mode selection

This mode can be selected by setting "010" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(XIN)$; or $f(XCIN)$ can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(XCIN)$; or $f(XCIN)$ can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse period measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to "1".

●Explanation of operation

The cycle of the pulse which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is "0", the timer counts during the term from one falling edge of CNTR2 pin input to the next falling edge. When it is "1", the timer counts during the term from one rising edge input to the next rising edge input.

When the valid edge of measurement completion/start is detected, the 1's complement of the timer value is written to the timer latch and "FFFF16" is set to the timer.

Furthermore when the timer underflows, the timer Z interrupt request occurs and "FFFF16" is set to the timer. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

■Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse period).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

"FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse period measurement depends on the timer value just before measurement start.

Figure 28 shows the timing chart of the pulse period measurement mode.

(5) Pulse width measurement mode

●Mode selection

This mode can be selected by setting "011" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(XIN)$; or $f(XCIN)$ can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(XCIN)$; or $f(XCIN)$ can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's. When the pulse widths measurement is completed, the INT4/CNTR2 interrupt request bit (bit 5) of the interrupt request register 2 (address 003D16) is set to "1".

●Explanation of operation

The pulse width which is input from the CNTR2 pin is measured. When the CNTR2 active edge switch bit (bit 5) of the timer Z mode register (address 002A16) is "0", the timer counts during the term from one rising edge input to the next falling edge input ("H" term). When it is "1", the timer counts during the term from one falling edge of CNTR2 pin input to the next rising edge of input ("L" term). When the valid edge of measurement completion is detected, the 1's complement of the timer value is written to the timer latch.

When the valid edge of measurement completion/start is detected, "FFFF16" is set to the timer.

When the timer Z underflows, the timer Z interrupt occurs and "FFFF16" is set to the timer Z. When reading the timer Z, the value of the timer latch (measured value) is read. The measured value is retained until the next measurement completion.

■Precautions

Set the double-function port of CNTR2 pin and port P47 to input in this mode.

A read-out of timer value is impossible in this mode. The timer can be written to only during timer stop (no measurement of pulse widths).

Since the timer latch in this mode is specialized for the read-out of measured values, do not perform any write operation during measurement.

"FFFF16" is set to the timer when the timer underflows or when the valid edge of measurement start/completion is detected. Consequently, the timer value at start of pulse width measurement depends on the timer value just before measurement start.

Figure 29 shows the timing chart of the pulse width measurement mode.

(6) Programmable waveform generating mode

●Mode selection

This mode can be selected by setting "100" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(XIN)$; or $f(XCIN)$ can be selected as the count source.

In low-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(XCIN)$; or $f(XCIN)$ can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

●Explanation of operation

The operation is the same as the timer mode's. Moreover the timer outputs the data set in the output level latch (bit 4) of the timer Z mode register (address 002A16) from the CNTR2 pin each time the timer underflows.

Changing the value of the output level latch and the timer latch after an underflow makes it possible to output an optional waveform from the CNTR2 pin.

■Precautions

The double-function port of CNTR2 pin and port P47 is automatically set to the programmable waveform generating port in this mode.

Figure 30 shows the timing chart of the programmable waveform generating mode.

(7) Programmable one-shot generating mode

●Mode selection

This mode can be selected by setting "101" to the timer Z operating mode bits (bits 2 to 0) and setting "0" to the timer/event counter mode switch bit (b7) of the timer Z mode register (address 002A16).

●Count source selection

In high- or middle-speed mode, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256, 1/512 or 1/1024 of $f(XIN)$; or $f(XCIN)$ can be selected as the count source.

●Interrupt

The interrupt at an underflow is the same as the timer mode's.

The trigger to generate one-shot pulse can be selected by the INT1 active edge selection bit (bit 1) of the interrupt edge selection register (address 003A16). When it is "0", the falling edge active is selected; when it is "1", the rising edge active is selected.

When the valid edge of the INT1 pin is detected, the INT1 interrupt request bit (bit 1) of the interrupt request register 1 (address 003C16) is set to "1".

●Explanation of operation

•"H" one-shot pulse; Bit 5 of timer Z mode register = "0"

The output level of the CNTR2 pin is initialized to "L" at mode selection. When trigger generation (input signal to INT1 pin) is detected, "H" is output from the CNTR2 pin. When an underflow occurs, "L" is output. The "H" one-shot pulse width is set by the setting value to the timer Z register low-order and high-order. When trigger generating is detected during timer count stop, although "H" is output from the CNTR2 pin, "H" output state continues because an underflow does not occur.

•"L" one-shot pulse; Bit 5 of timer Z mode register = "1"

The output level of the CNTR2 pin is initialized to "H" at mode selection. When trigger generation (input signal to INT1 pin) is detected, "L" is output from the CNTR2 pin. When an underflow occurs, "H" is output. The "L" one-shot pulse width is set by the setting value to the timer Z low-order and high-order. When trigger generating is detected during timer count stop, although "L" is output from the CNTR2 pin, "L" output state continues because an underflow does not occur.

■Precautions

Set the double-function port of INT1 pin and port P42 to input in this mode.

Set the double-function port of CNTR2 pin and port P22 is automatically set to the programmable one-shot generating port in this mode.

This mode cannot be used in low-speed mode.

If the value of the CNTR2 active edge switch bit is changed during one-shot generating enabled or generating one-shot pulse, then the output level from CNTR2 pin changes.

Figure 31 shows the timing chart of the programmable one-shot generating mode.

■Notes regarding all modes

●Timer Z write control

Which write control can be selected by the timer Z write control bit (bit 3) of the timer Z mode register (address 002A16), writing data to both the latch and the timer at the same time or writing data only to the latch.

When the operation "writing data only to the latch" is selected, the value is set to the timer latch by writing data to the address of timer Z and the timer is updated at next underflow. After reset release, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the latch and the timer at the same time by writing data to the address of timer Z.

In the case of writing data only to the latch, if writing data to the latch and an underflow are performed almost at the same time, the timer value may become undefined.

●Timer Z read control

A read-out of timer value is impossible in pulse period measurement mode and pulse width measurement mode. In the other modes, a read-out of timer value is possible regardless of count operating or stopped.

However, a read-out of timer latch value is impossible.

●Switch of interrupt active edge of CNTR2 and INT1

Each interrupt active edge depends on setting of the CNTR2 active edge switch bit and the INT1 active edge selection bit.

●Switch of count source

When switching the count source by the timer Z count source selection bits, the value of timer count is altered in inconsiderable amount owing to generating of thin pulses on the count input signals.

Therefore, select the timer count source before setting the value to the prescaler and the timer.

●Usage of CNTR2 pin as normal I/O port

To use the CNTR2 pin as normal I/O port P47, set timer Z operating mode bits (b2, b1, b0) of timer Z mode register (address 002A16) to "000".

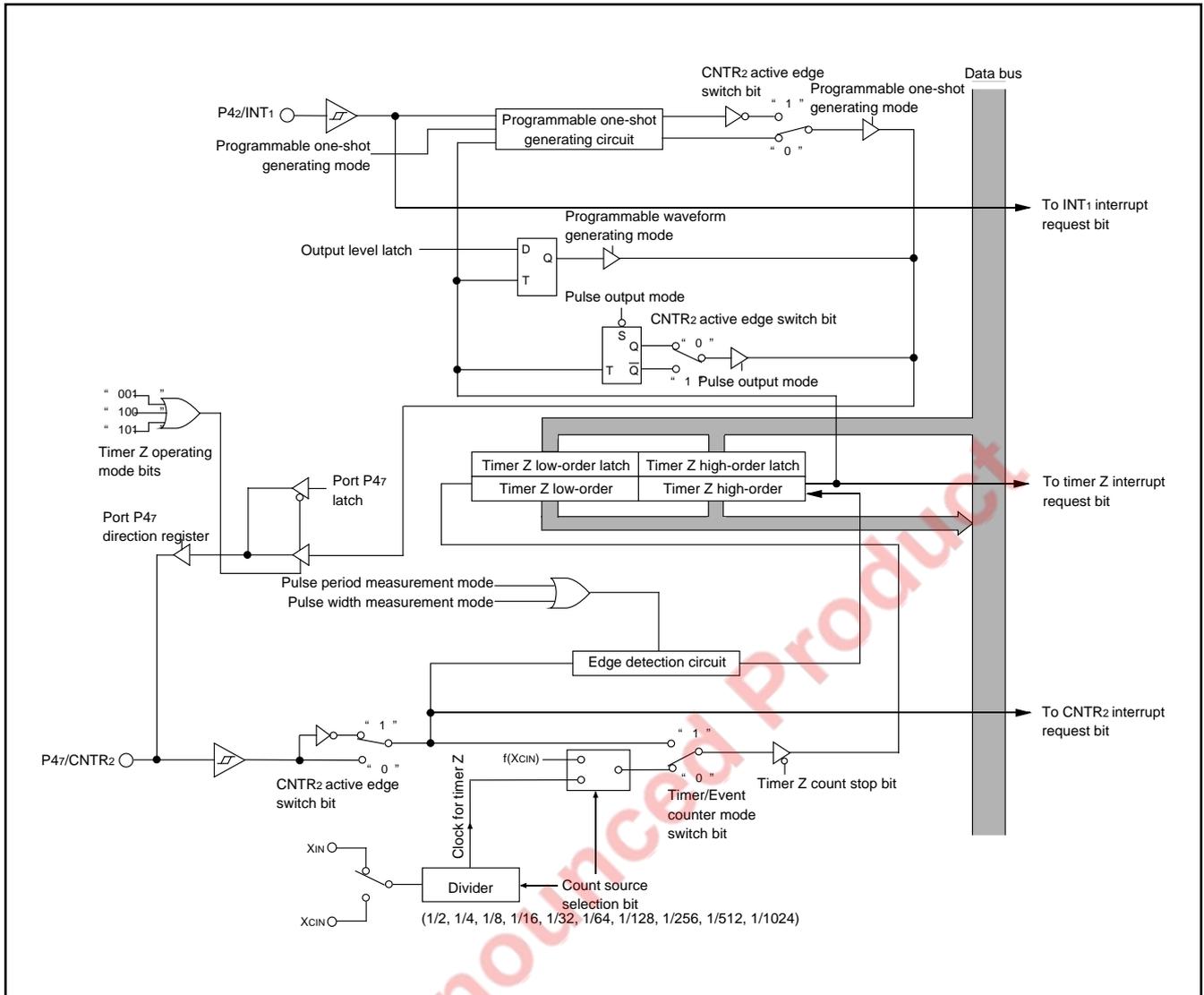


Fig. 24 Block diagram of timer Z

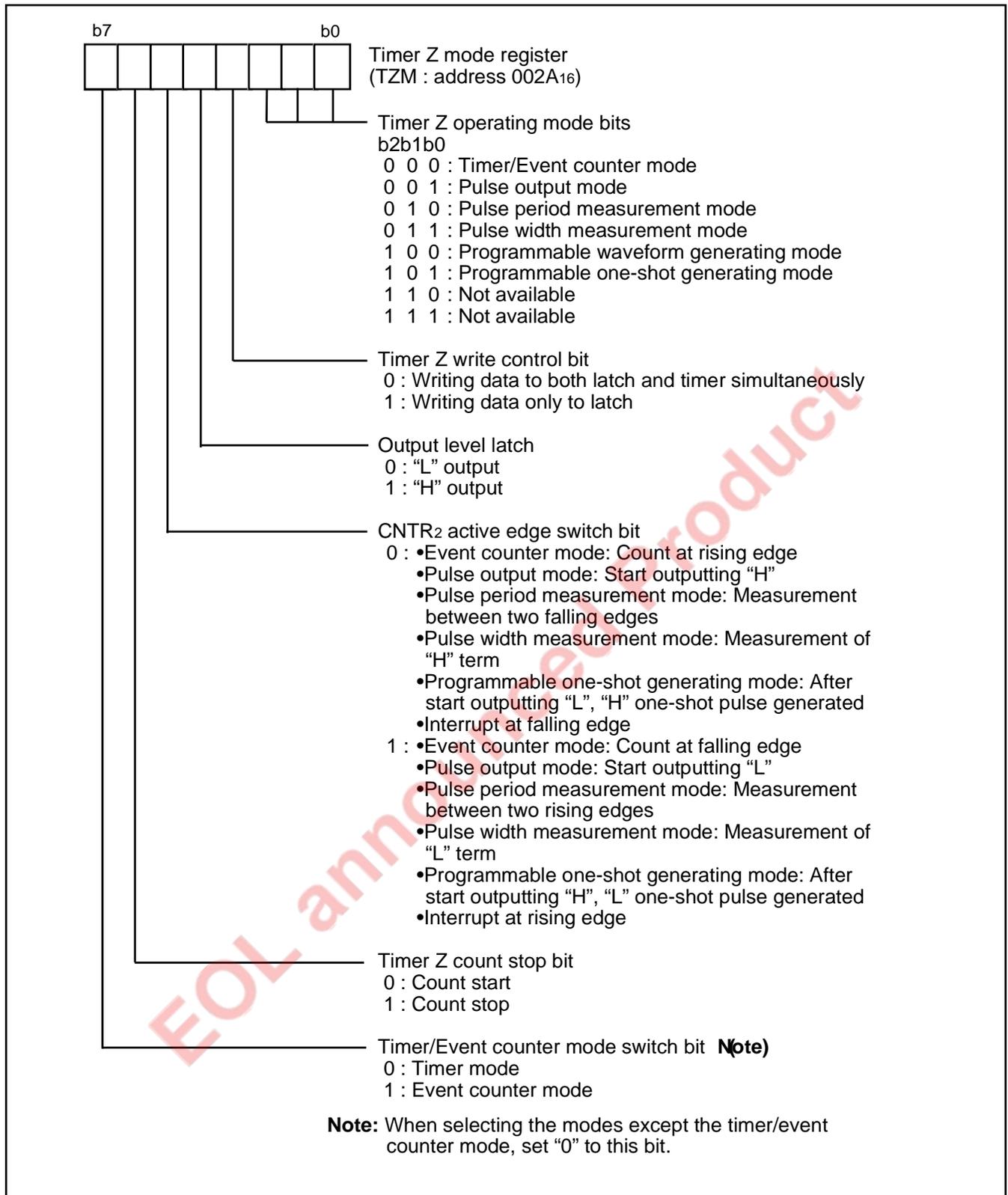


Fig. 25 Structure of timer Z mode register

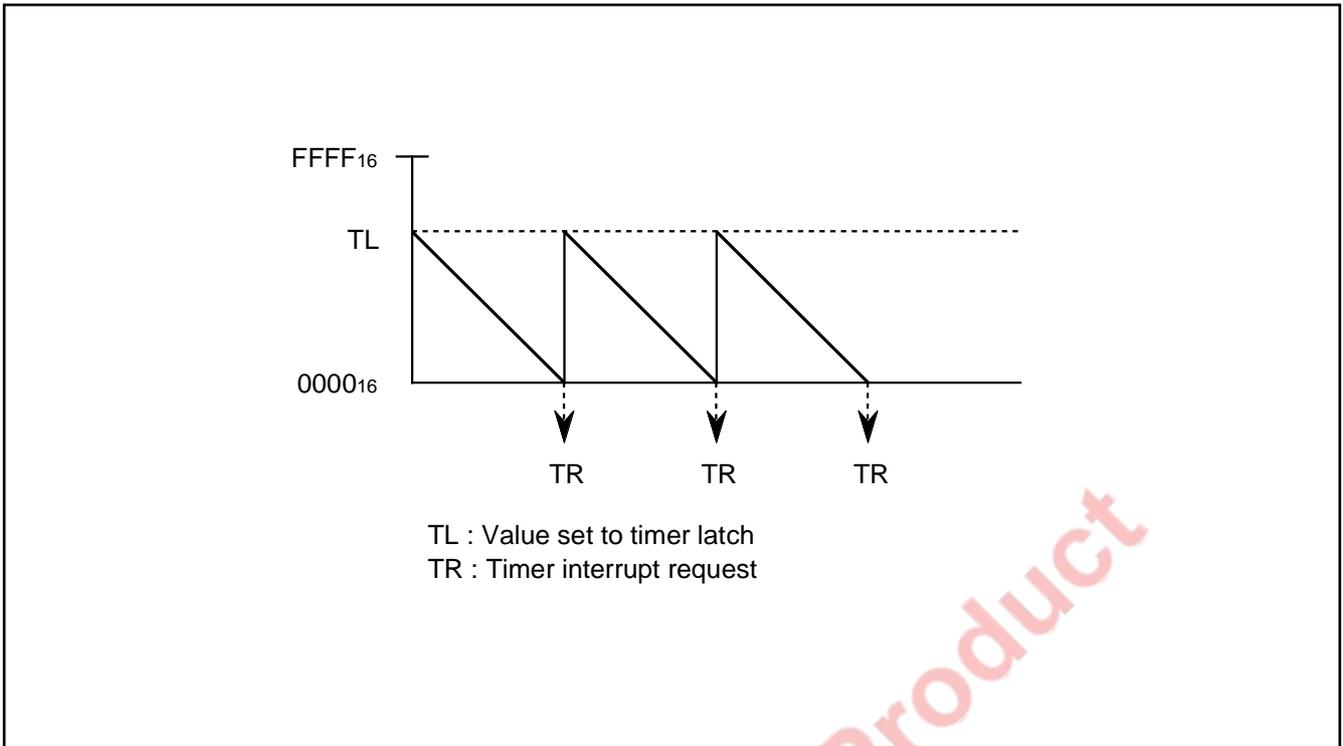


Fig. 26 Timing chart of timer/event counter mode

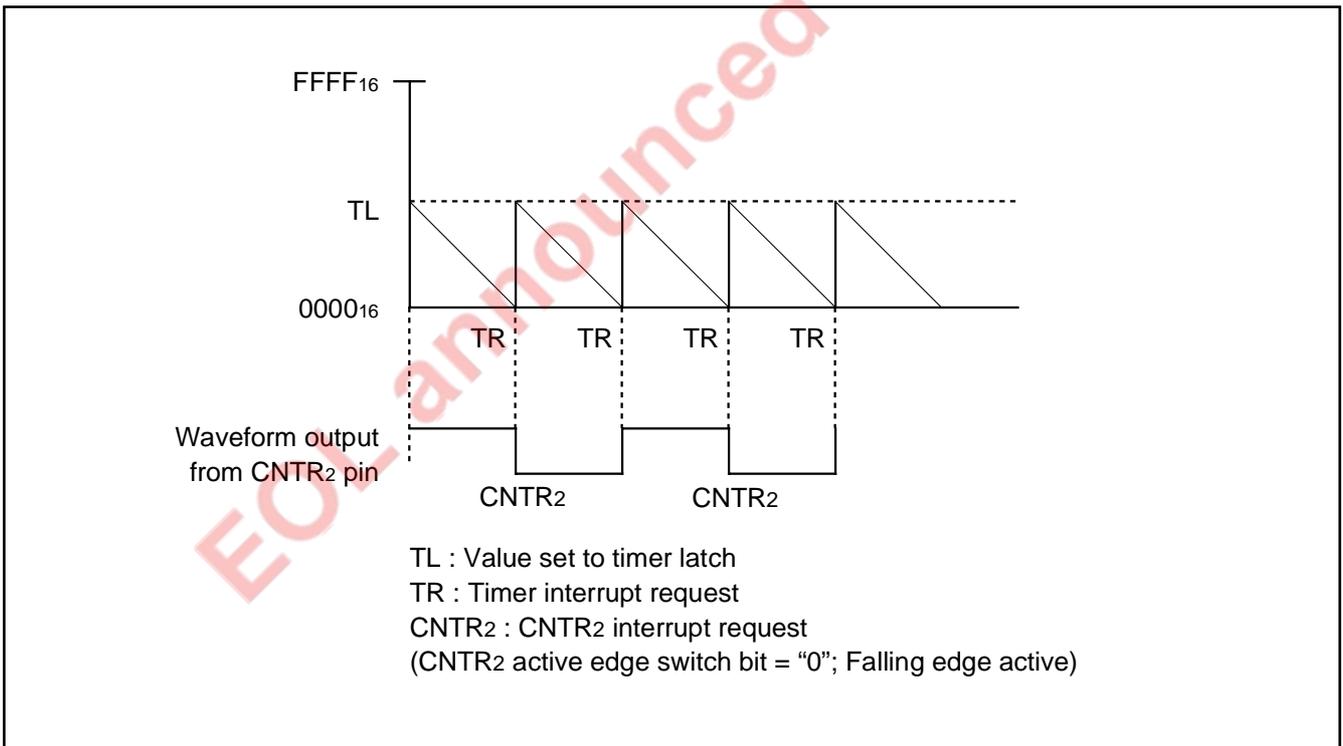


Fig. 27 Timing chart of pulse output mode

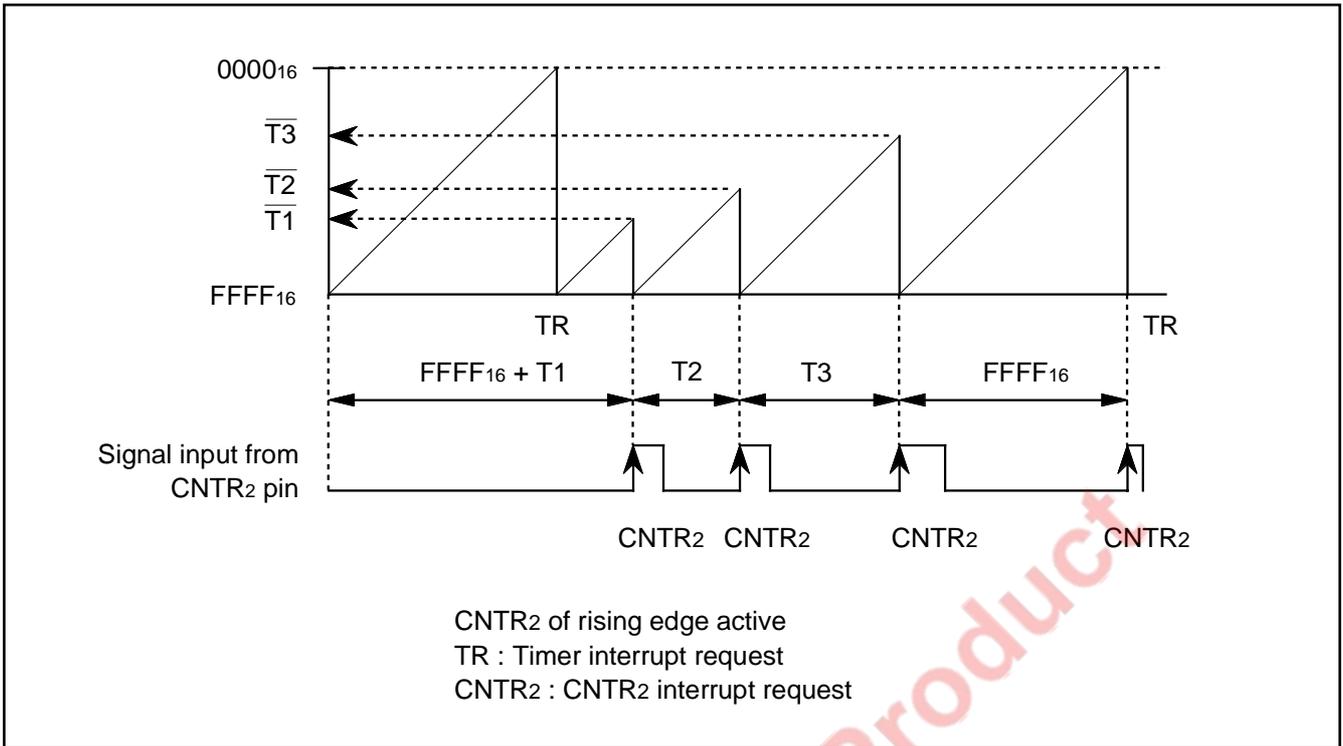


Fig. 28 Timing chart of pulse period measurement mode (Measuring term between two rising edges)

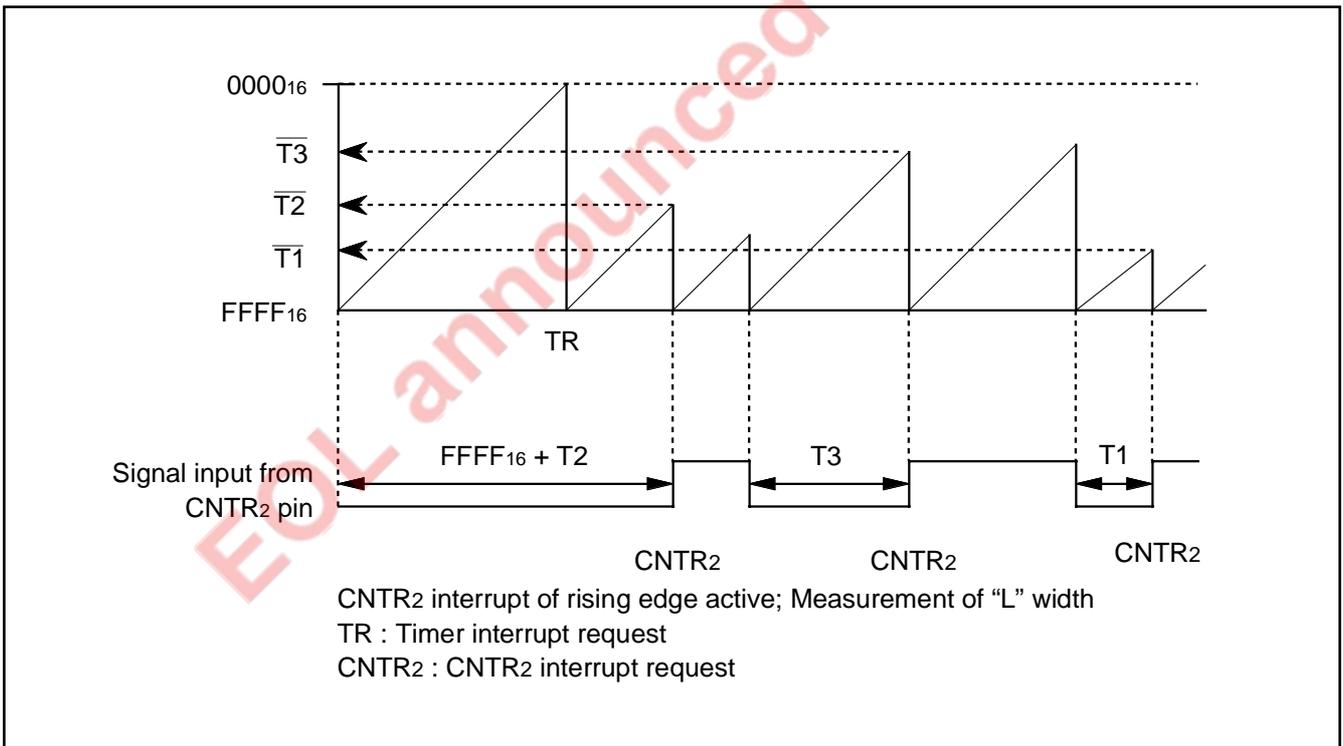


Fig. 29 Timing chart of pulse width measurement mode (Measuring "L" term)

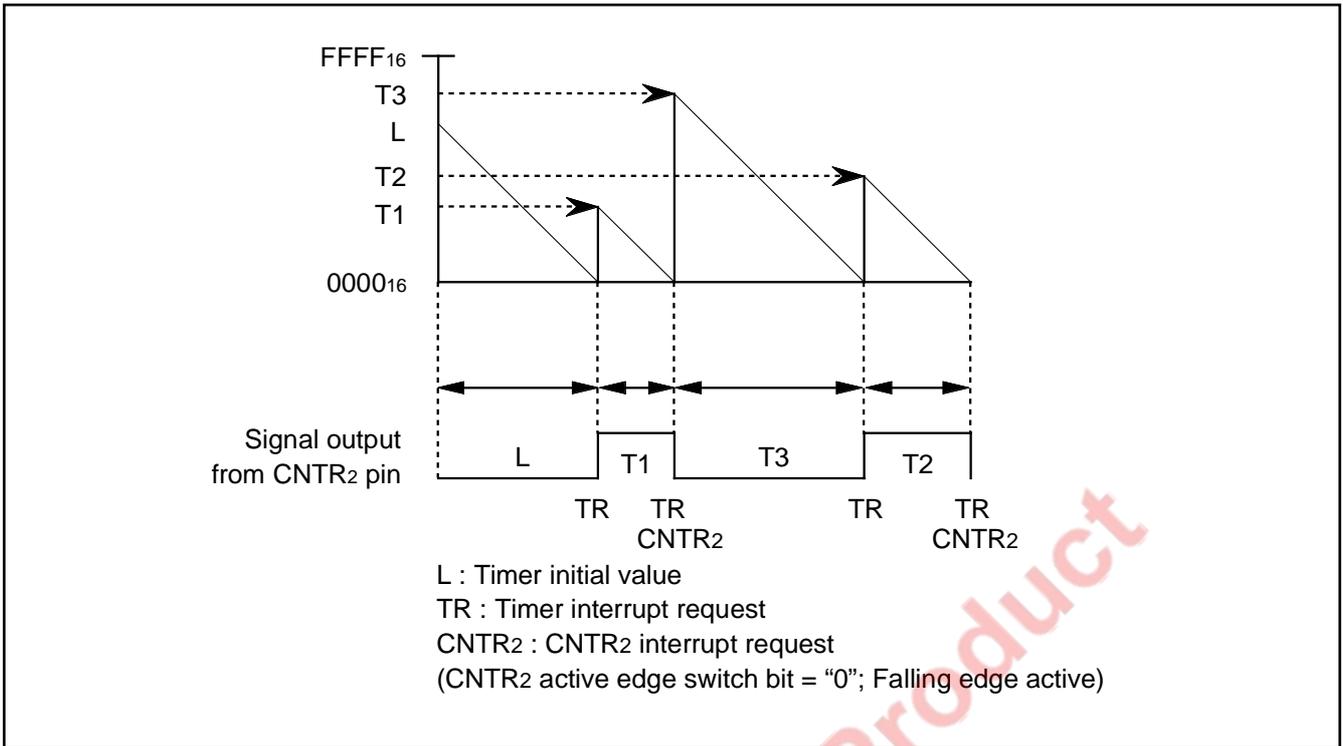


Fig. 30 Timing chart of programmable waveform generating mode

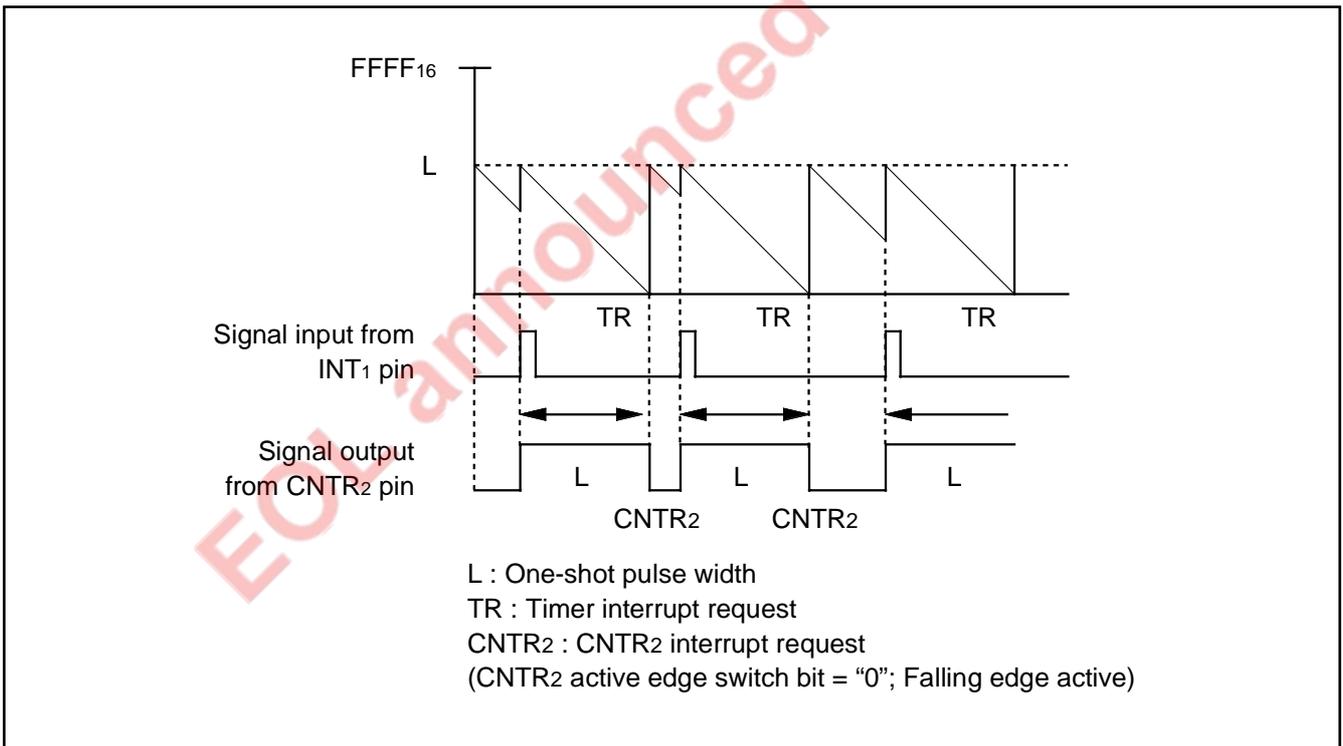


Fig. 31 Timing chart of programmable one-shot generating mode (H" one-shot pulse generating)

SERIAL INTERFACE
Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O1. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O1 mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address 001A16) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

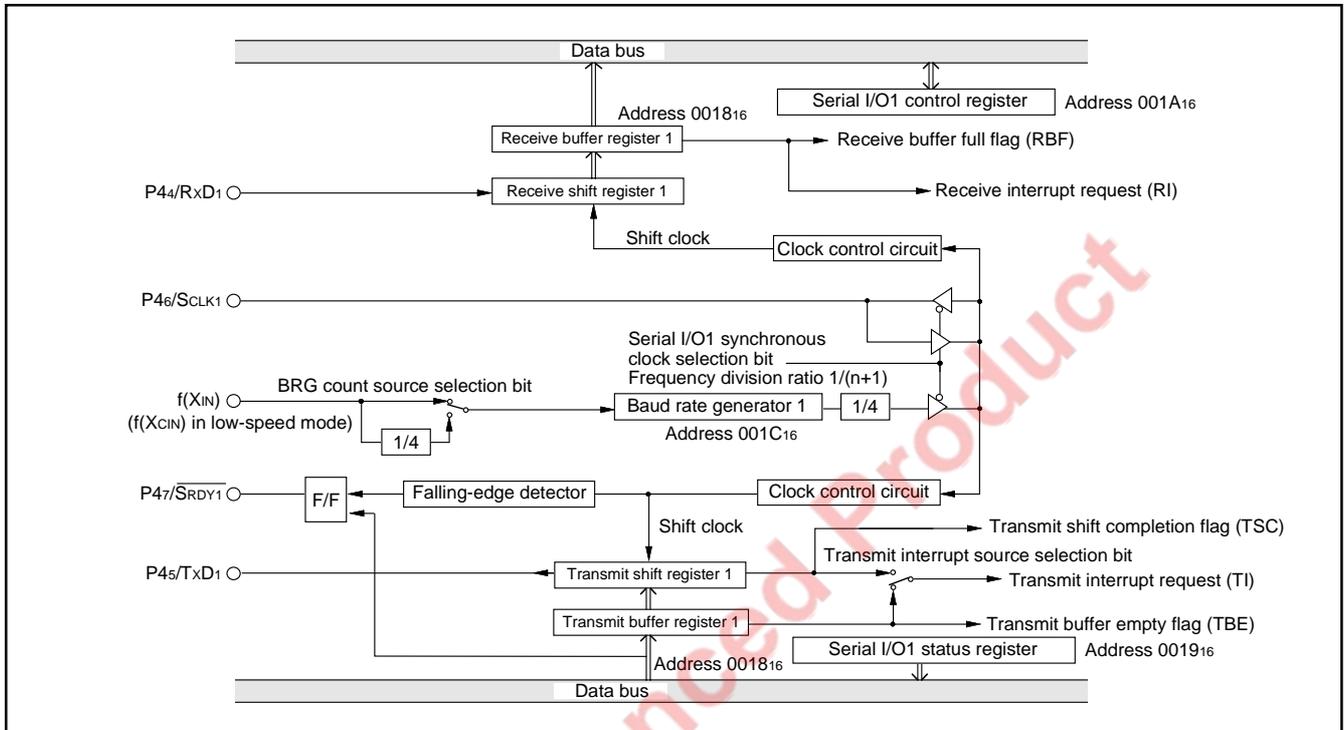


Fig. 32 Block diagram of clock synchronous serial I/O1

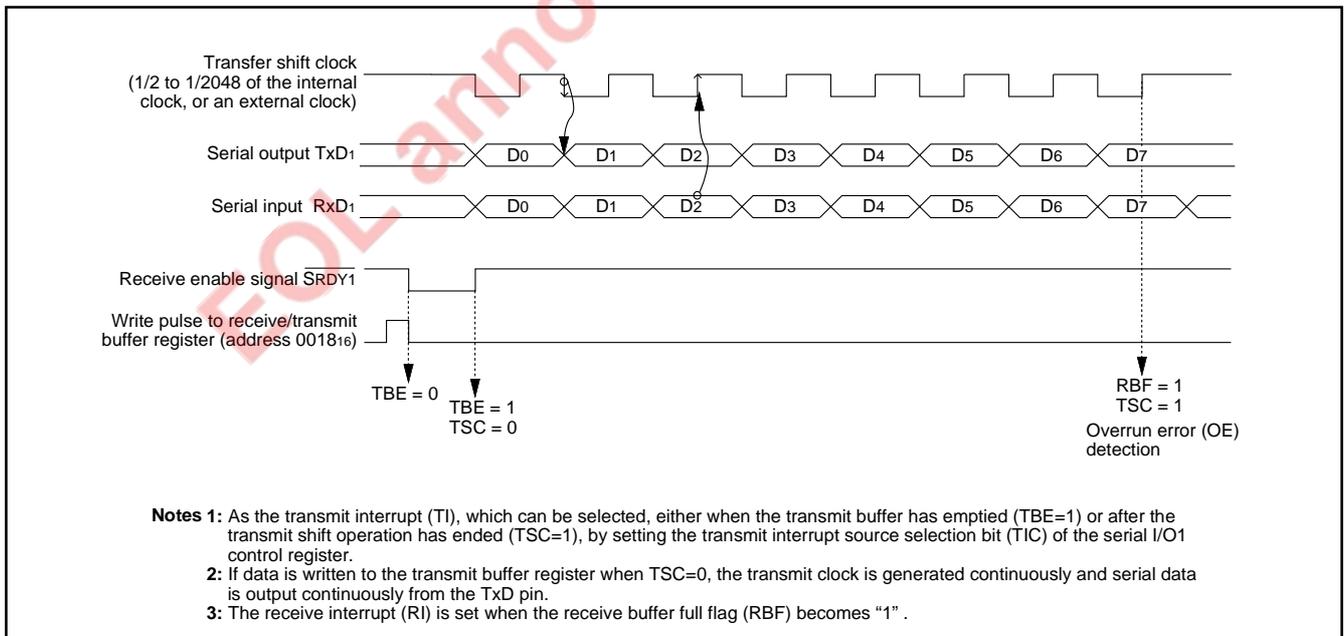


Fig. 33 Operation of clock synchronous serial I/O1

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit of the serial I/O1 control register to 0.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

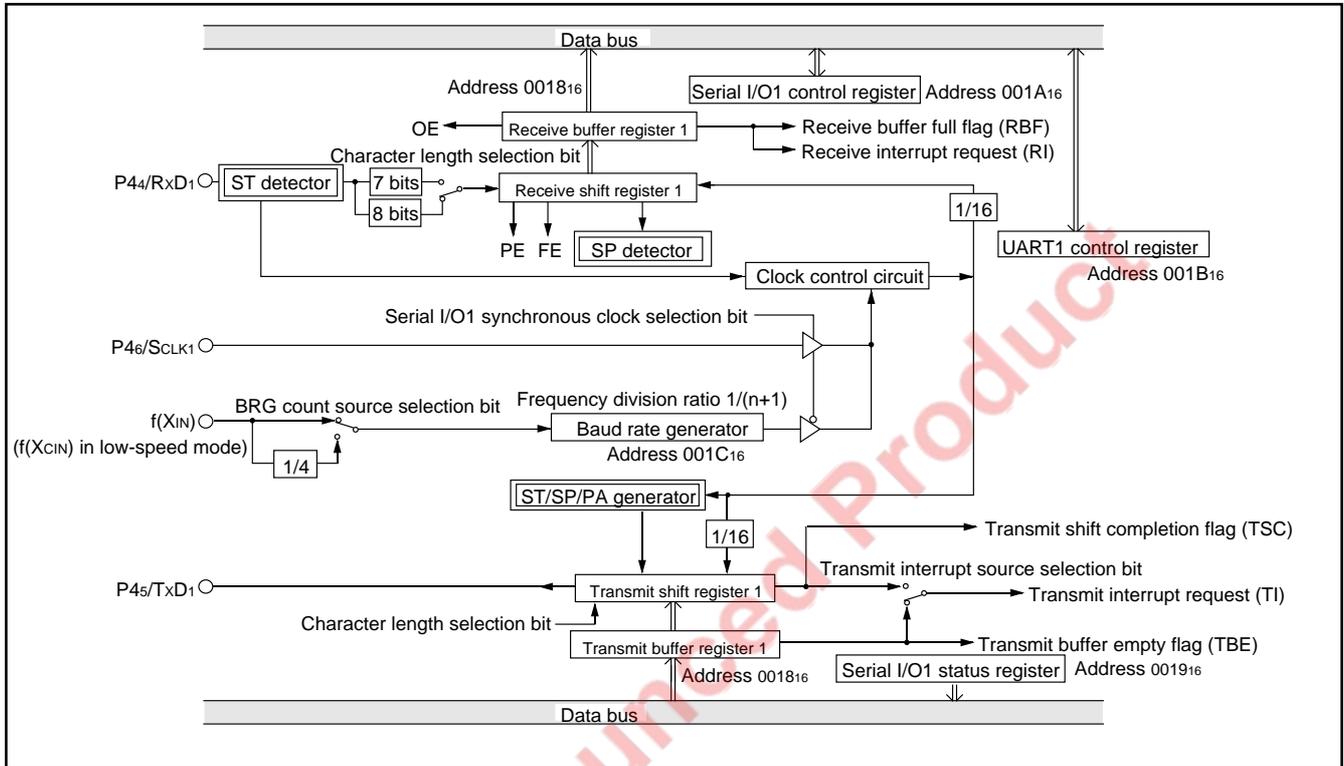


Fig. 34 Block diagram of UART serial I/O1

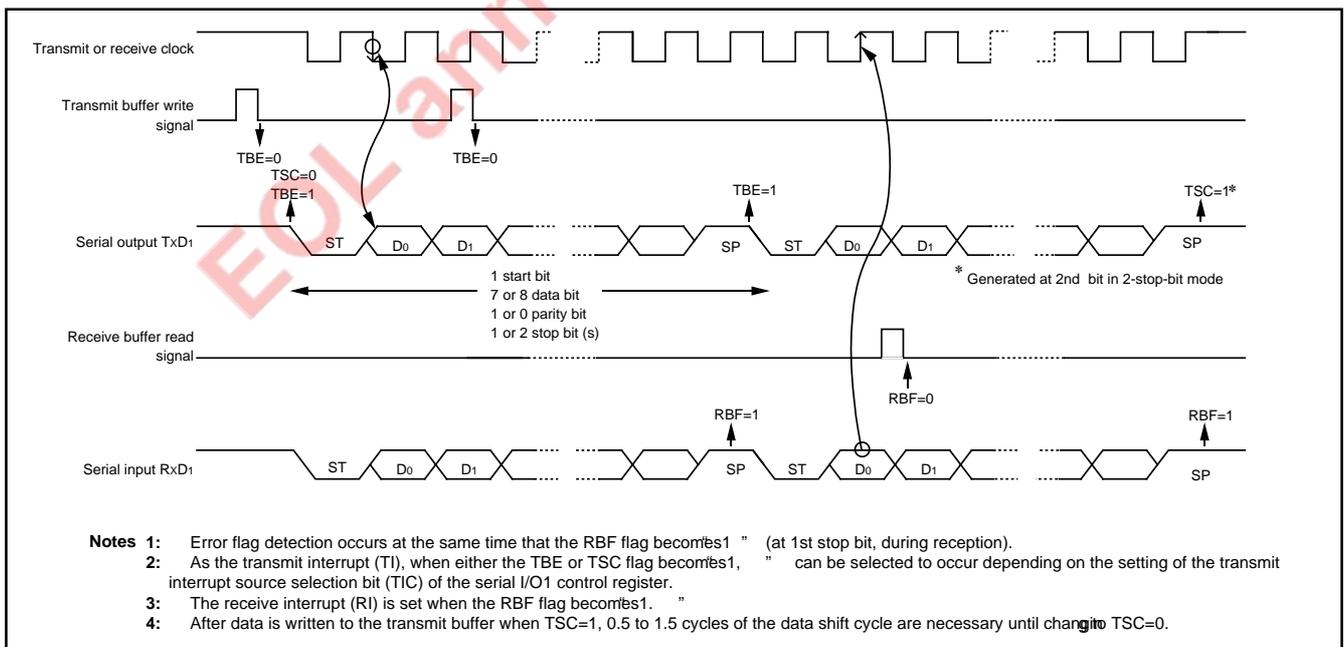


Fig. 35 Operation of UART serial I/O1

[Serial I/O1 Control Register (SIO1CON)] **001A16**

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART1 Control Register (UART1CON)] **001B16**

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P45/TxD1 pin.

[Serial I/O1 Status Register (SIO1STS)] **001916**

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O1 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Transmit Buffer Register 1/Receive Buffer Register 1 (TB1/RB1)] 001816

The transmit buffer register 1 and the receive buffer register 1 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator 1 (BRG1)] 001C16

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

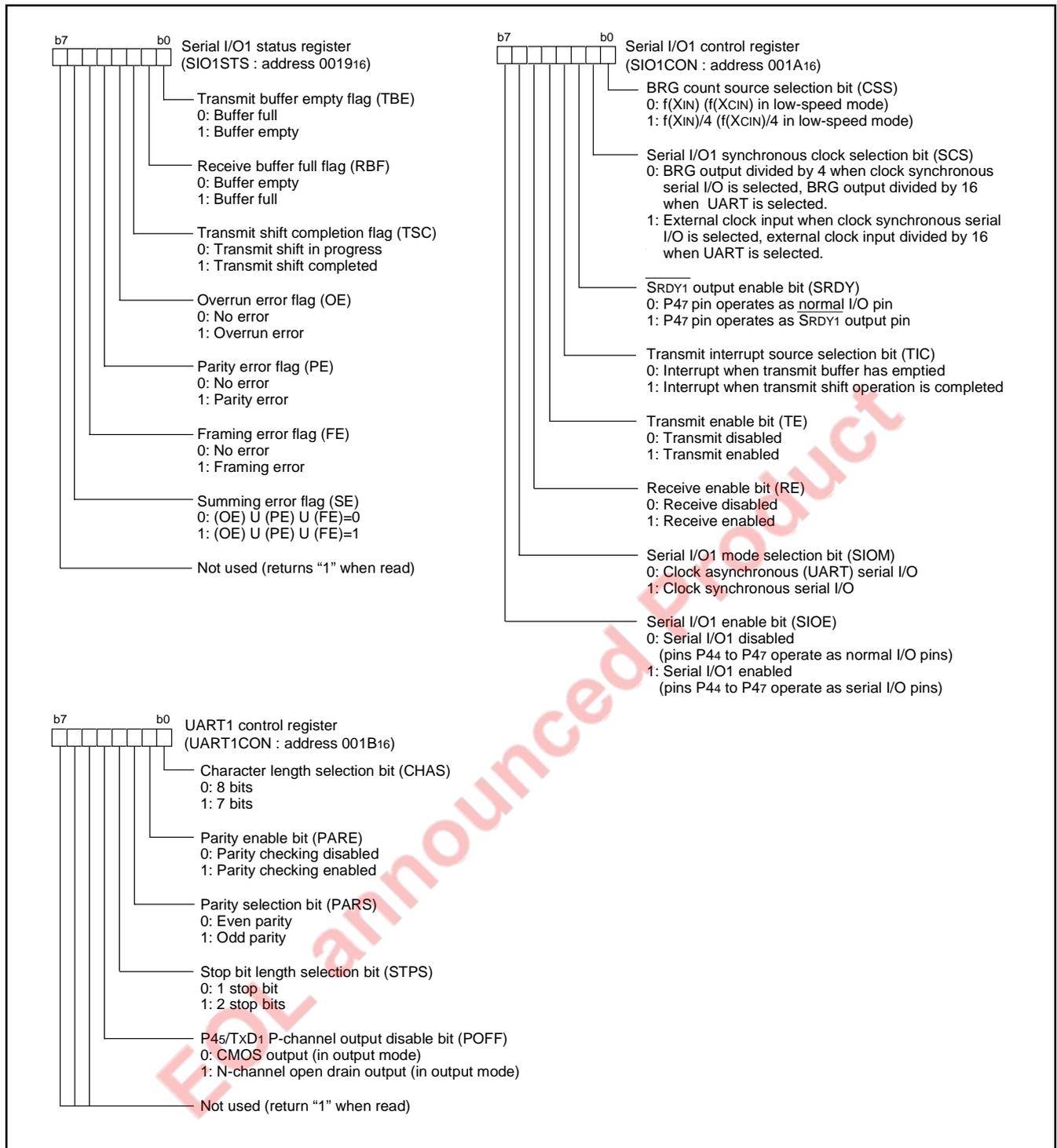


Fig. 36 Structure of serial I/O1 control registers

■ Notes concerning serial I/O1

1. Notes when selecting clock synchronous serial I/O

1.1 Stop of transmission operation

● Note

Clear the serial I/O1 enable bit and the transmit enable bit to "0" (serial I/O and transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

1.2 Stop of receive operation

● Note

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O1 enable bit to "0" (serial I/O disabled).

1.3 Stop of transmit/receive operation

● Note

Clear both the transmit enable bit and receive enable bit to "0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O1 enable bit to "0" (serial I/O disabled) (refer to 1.1).

2. Notes when selecting clock asynchronous serial I/O

2.1 Stop of transmission operation

● Note

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to "0".

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

2.2 Stop of receive operation

● Note

Clear the receive enable bit to "0" (receive disabled).

2.3 Stop of transmit/receive operation

● Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O1 enable bit to "0".

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O1 enable bit is cleared to "0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD1, RxD1, SCLK1, and $\overline{\text{SRDY1}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O1 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD1 pin and an operation failure occurs.

● Note 2 (only receive operation is stopped)

Clear the receive enable bit to "0" (receive disabled).

3. $\overline{\text{SRDY1}}$ output of reception side

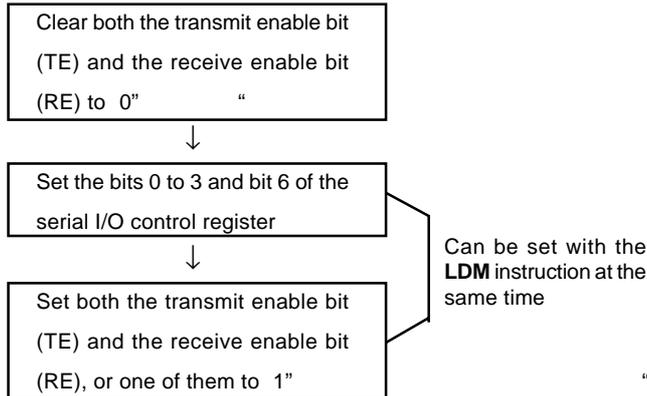
● Note

When signals are output from the $\overline{\text{SRDY1}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY1}}$ output enable bit, and the transmit enable bit to "1" (transmit enabled).

4. Setting serial I/O1 control register again

● Note

Set the serial I/O1 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0".



5. Data transmission control with referring to transmit shift register completion flag

● Note

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected

● Note

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK1 input level. Also, write data to the transmit buffer register at "H" of the SCLK1 input level.

7. Transmit interrupt request when transmit enable bit is set

● Note

When using the transmit interrupt, take the following sequence.

- ① Set the serial I/O1 transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O1 transmit interrupt request bit to "0" after 1 or more instruction has executed.
- ④ Set the serial I/O1 transmit interrupt enable bit to "1" (enabled).

● Reason

When the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

Serial I/O2

The serial I/O2 function can be used only for clock synchronous serial I/O2.

For clock synchronous serial I/O2, the transmitter and the receiver must use the same clock. If the internal clock is used, transfer is started by a write signal to the serial I/O2 register.

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains eight bits which control various serial I/O2 functions.

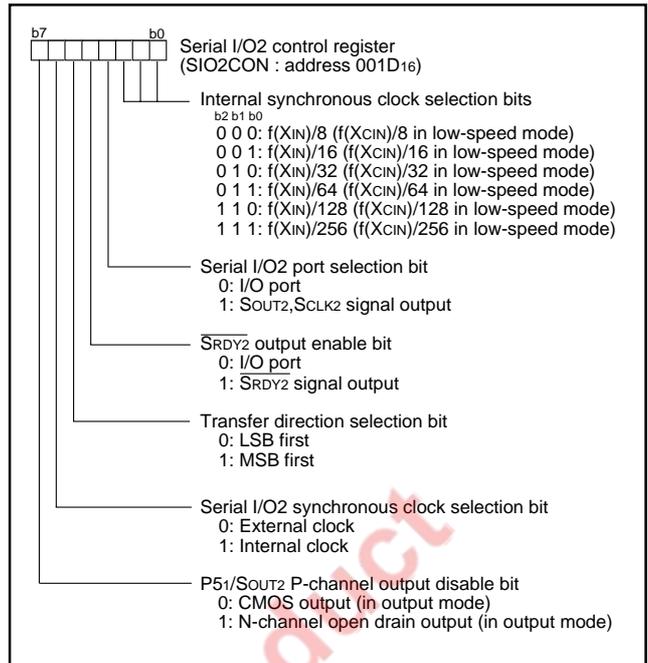


Fig. 37 Structure of serial I/O2 control register

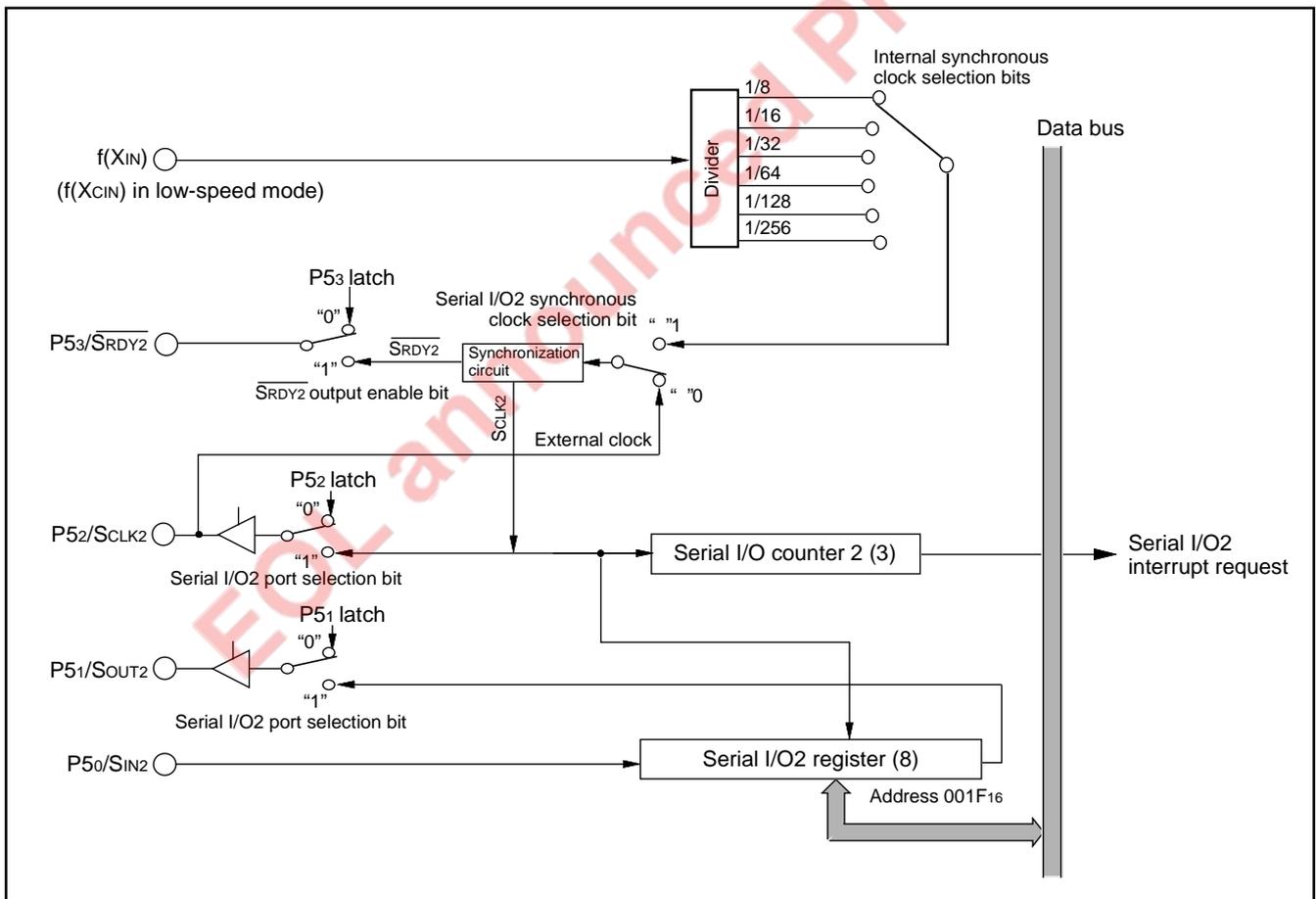


Fig. 38 Block diagram of serial I/O2

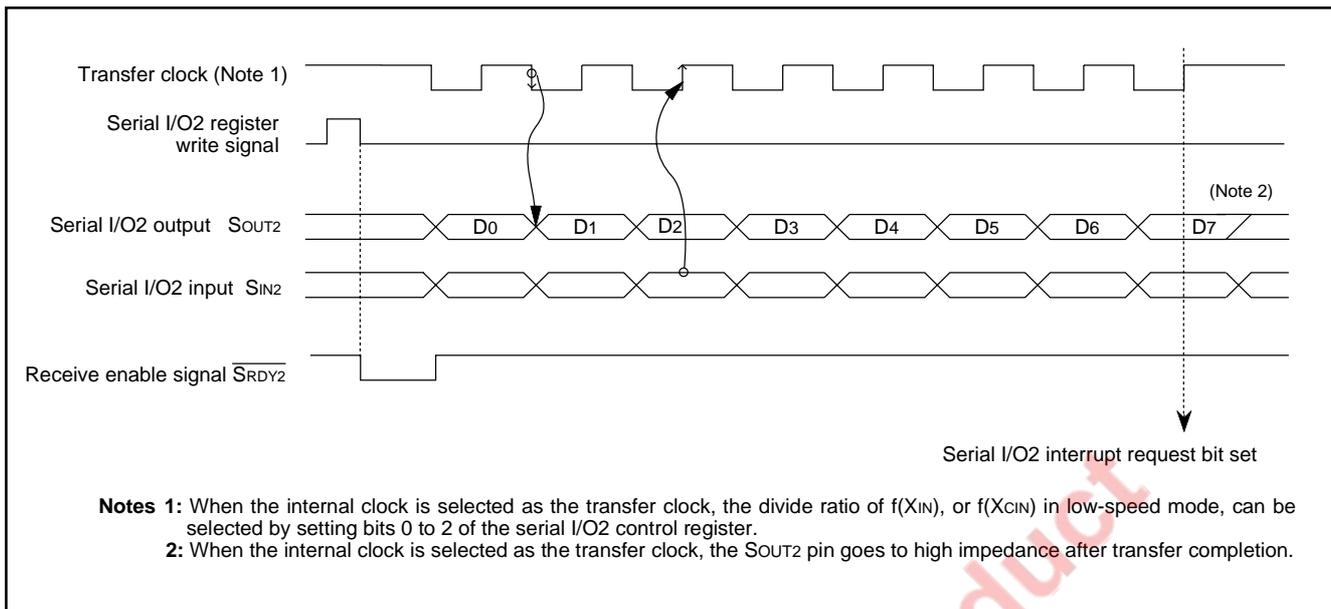


Fig. 39 Timing of serial I/O2

EOL announced Product

Serial I/O3

Serial I/O3 can be used as either clock synchronous or asynchronous (UART) serial I/O3. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O3 mode can be selected by setting the serial I/O3 mode selection bit of the serial I/O3 control register (bit 6 of address 003216) to "1".

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the transmit/receive buffer register.

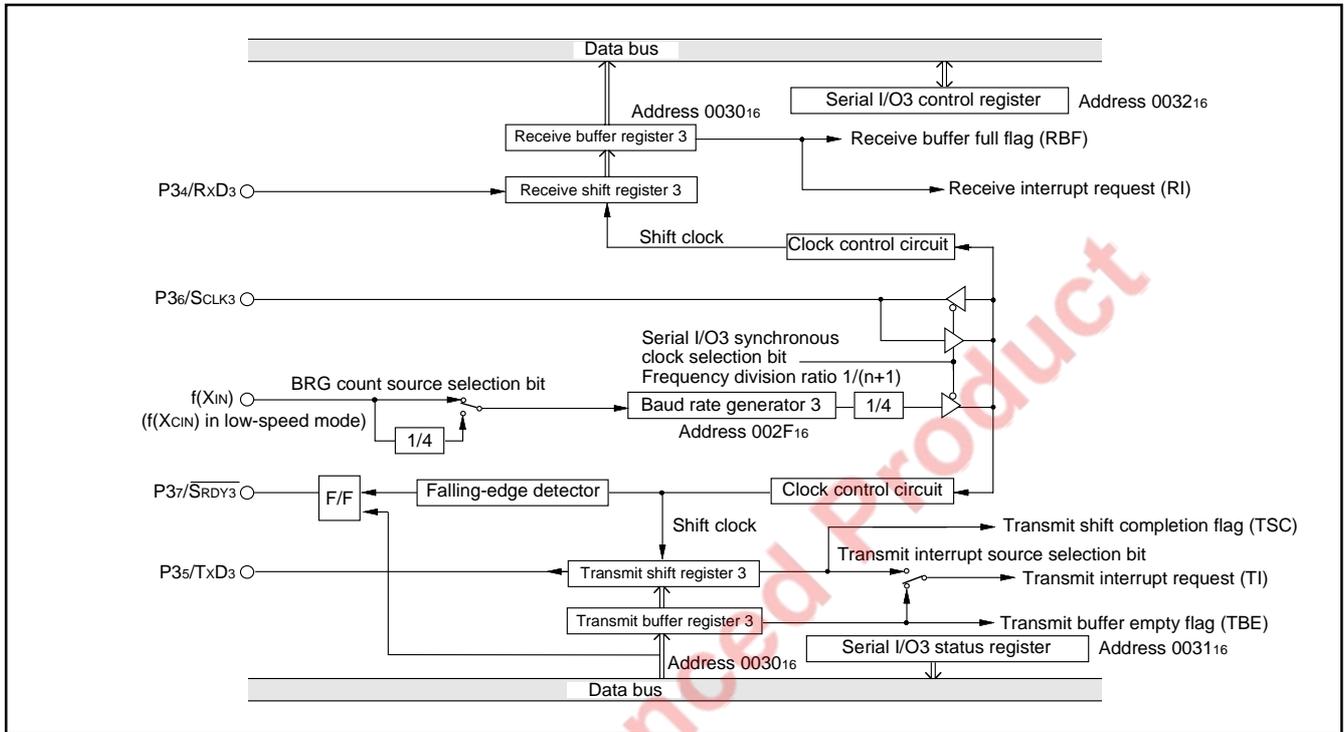


Fig. 40 Block diagram of clock synchronous serial I/O3

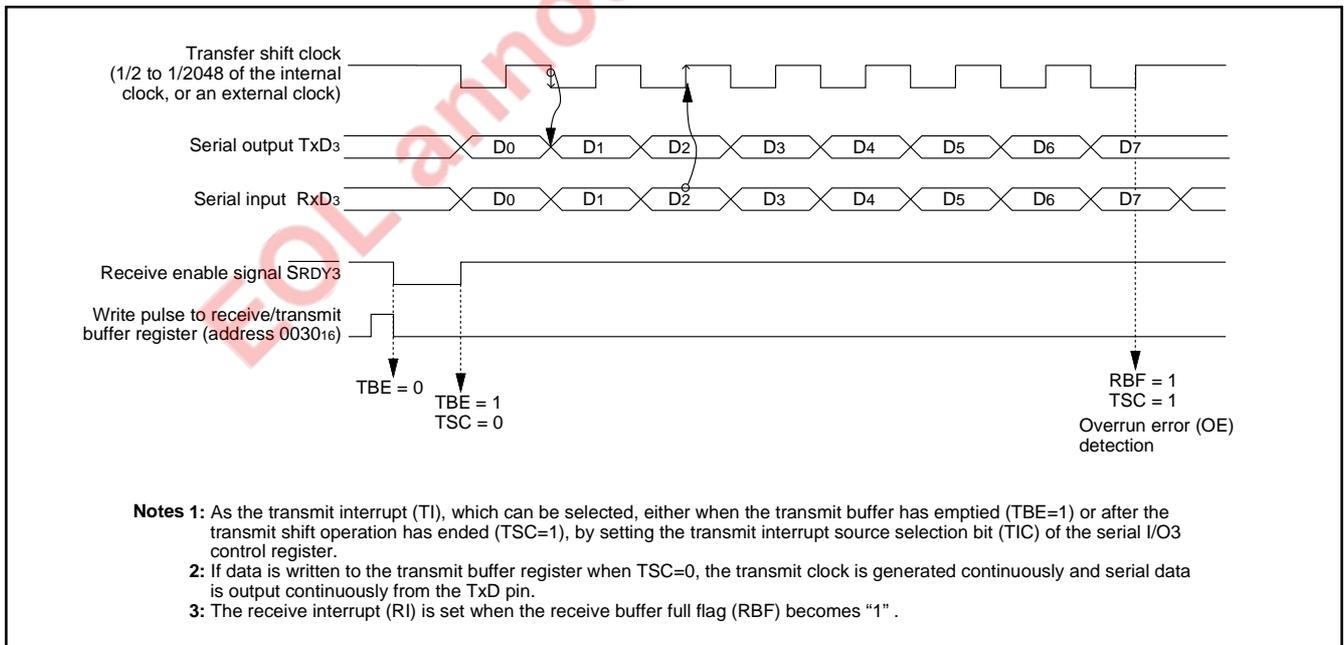


Fig. 41 Operation of clock synchronous serial I/O3

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O3 mode selection bit of the serial I/O3 control register to 0.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the

two buffers have the same address in a memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

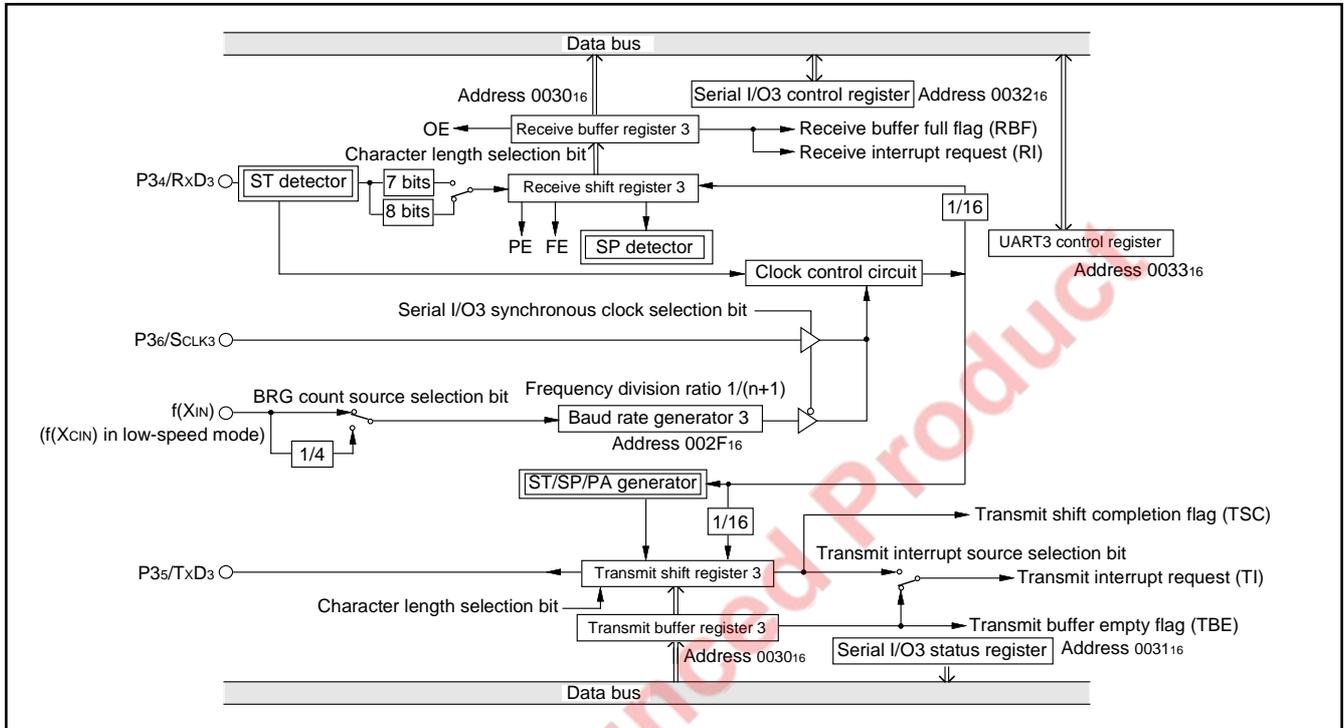


Fig. 42 Block diagram of UART serial I/O3

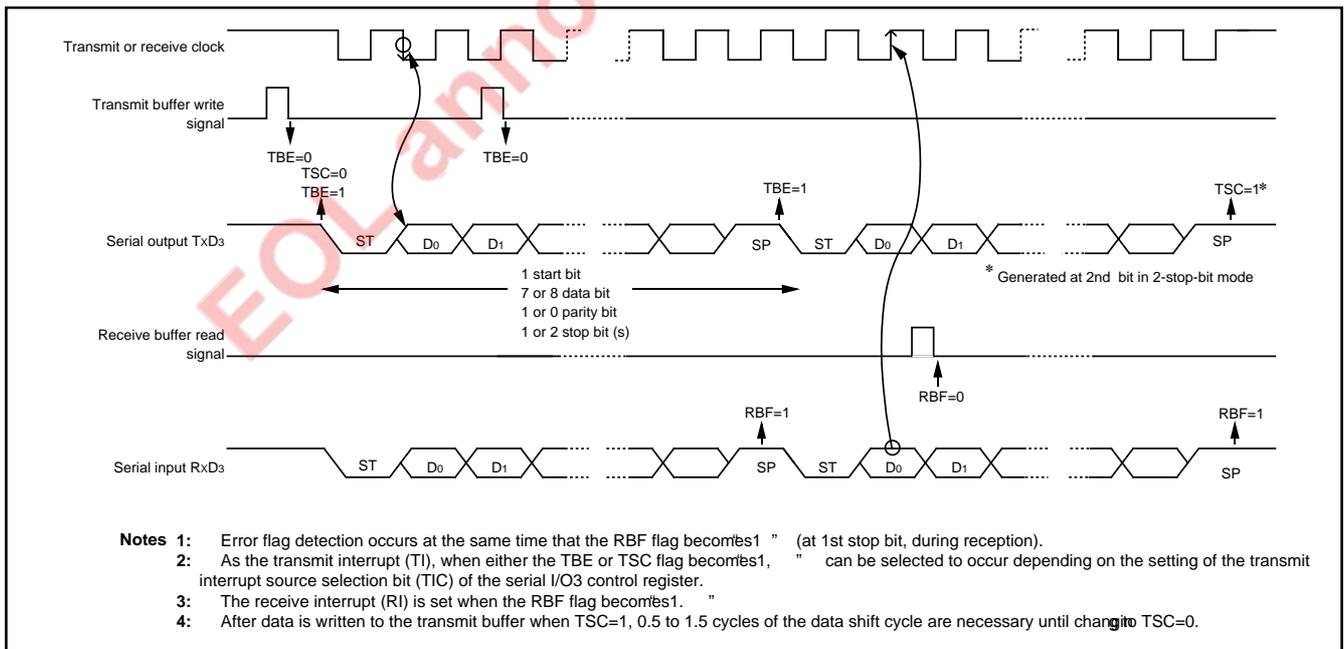


Fig. 43 Operation of UART serial I/O3

[Serial I/O3 Control Register (SIO3CON)]
003216

The serial I/O3 control register consists of eight control bits for the serial I/O3 function.

[UART3 Control Register (UART3CON)]
003316

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer, and one bit (bit 4) which is always valid and sets the output structure of the P35/TxD3 pin.

[Serial I/O3 Status Register (SIO3STS)] 003116

The read-only serial I/O3 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O3 function and various errors.

Three of the flags (bits 4 to 6) are valid only in UART mode.

The receive buffer full flag (bit 1) is cleared to "0" when the receive buffer register is read.

If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O3 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing "0" to the serial I/O3 enable bit SIOE (bit 7 of the serial I/O3 control register) also clears all the status flags, including the error flags.

Bits 0 to 6 of the serial I/O3 status register are initialized to "0" at reset, but if the transmit enable bit (bit 4) of the serial I/O3 control register has been set to "1", the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become "1".

[Transmit Buffer Register 3/Receive Buffer Register 3 (TB3/RB3)] 003016

The transmit buffer register 3 and the receive buffer register 3 are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is "0".

[Baud Rate Generator 3 (BRG3)] 002F16

The baud rate generator determines the baud rate for serial transfer.

The baud rate generator divides the frequency of the count source by $1/(n + 1)$, where n is the value written to the baud rate generator.

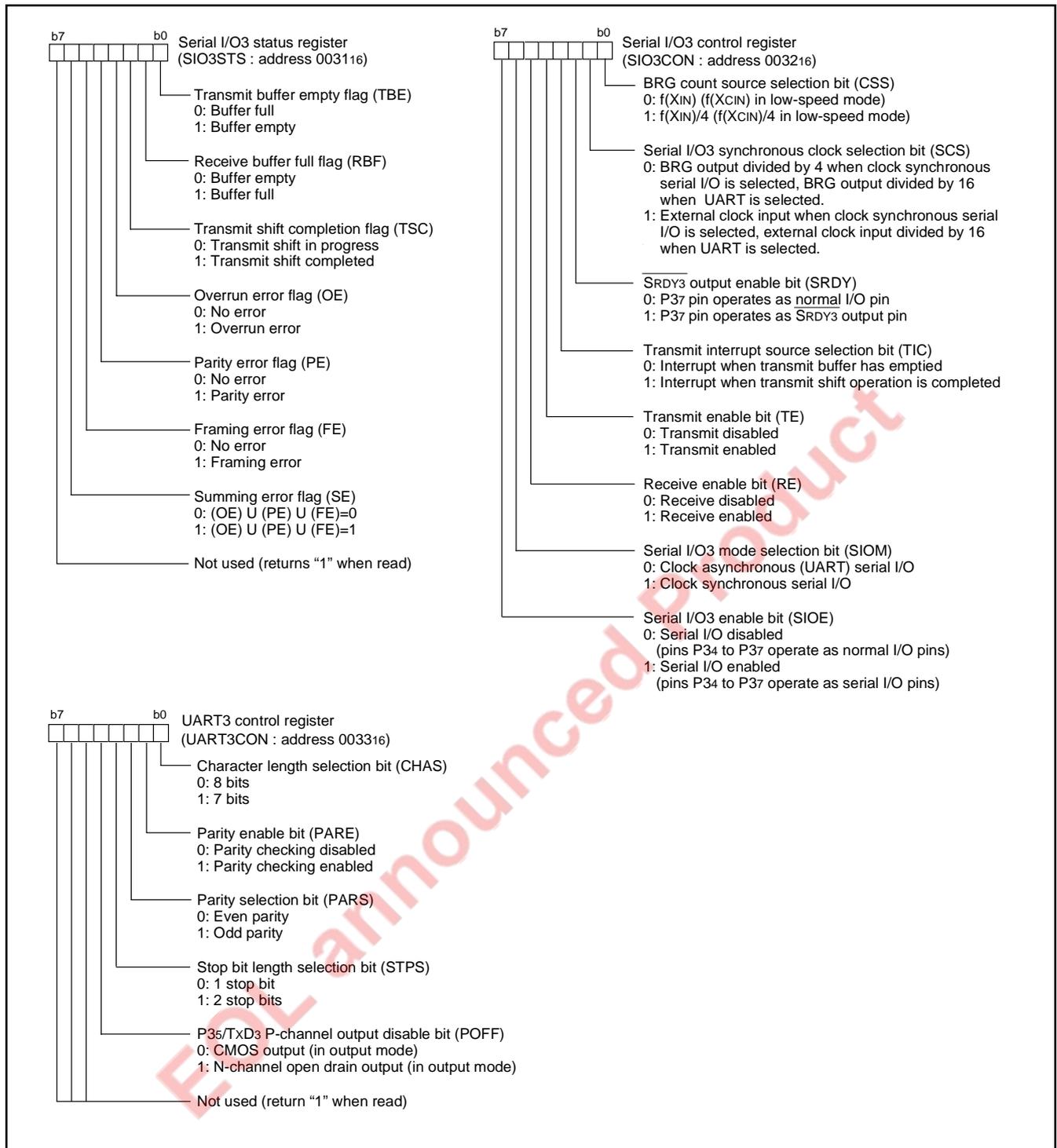


Fig. 44 Structure of serial I/O3 control registers

■ Notes concerning serial I/O3

1. Notes when selecting clock synchronous serial I/O

1.1 Stop of transmission operation

● Note

Clear the serial I/O3 enable bit and the transmit enable bit to "0" (serial I/O and transmit disabled).

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to 0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and $\overline{\text{SRDY3}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O enable bit is set to "1" at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

1.2 Stop of receive operation

● Note

Clear the receive enable bit to "0" (receive disabled), or clear the serial I/O3 enable bit to 0" (serial I/O disabled).

1.3 Stop of transmit/receive operation

● Note

Clear both the transmit enable bit and receive enable bit to 0" (transmit and receive disabled).

(when data is transmitted and received in the clock synchronous serial I/O mode, any one of data transmission and reception cannot be stopped.)

● Reason

In the clock synchronous serial I/O mode, the same clock is used for transmission and reception. If any one of transmission and reception is disabled, a bit error occurs because transmission and reception cannot be synchronized.

In this mode, the clock circuit of the transmission circuit also operates for data reception. Accordingly, the transmission circuit does not stop by clearing only the transmit enable bit to "0" (transmit disabled). Also, the transmission circuit is not initialized by clearing the serial I/O3 enable bit to 0" (serial I/O disabled) (refer to 1.1).

2. Notes when selecting clock asynchronous serial I/O

2.1 Stop of transmission operation

● Note

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to 0".

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to 0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and $\overline{\text{SRDY3}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

2.2 Stop of receive operation

● Note

Clear the receive enable bit to 0" (receive disabled).

2.3 Stop of transmit/receive operation

● Note 1 (only transmission operation is stopped)

Clear the transmit enable bit to "0" (transmit disabled). The transmission operation does not stop by clearing the serial I/O3 enable bit to 0".

● Reason

Since transmission is not stopped and the transmission circuit is not initialized even if only the serial I/O3 enable bit is cleared to 0" (serial I/O disabled), the internal transmission is running (in this case, since pins TxD3, RxD3, SCLK3, and $\overline{\text{SRDY3}}$ function as I/O ports, the transmission data is not output). When data is written to the transmit buffer register in this state, data starts to be shifted to the transmit shift register. When the serial I/O3 enable bit is set to "1" at this time, the data during internally shifting is output to the TxD3 pin and an operation failure occurs.

● Note 2 (only receive operation is stopped)

Clear the receive enable bit to 0" (receive disabled).

3. $\overline{\text{SRDY3}}$ output of reception side

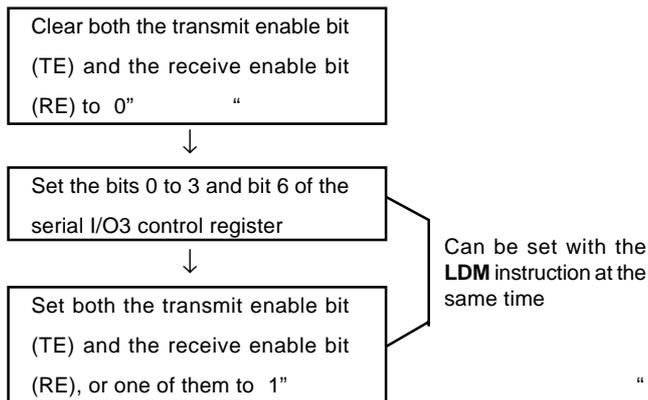
● Note

When signals are output from the $\overline{\text{SRDY3}}$ pin on the reception side by using an external clock in the clock synchronous serial I/O mode, set all of the receive enable bit, the $\overline{\text{SRDY3}}$ output enable bit, and the transmit enable bit to "1" (transmit enabled).

4. Setting serial I/O3 control register again

● Note

Set the serial I/O3 control register again after the transmission and the reception circuits are reset by clearing both the transmit enable bit and the receive enable bit to "0".



5. Data transmission control with referring to transmit shift register completion flag

● Note

After the transmit data is written to the transmit buffer register, the transmit shift register completion flag changes from "1" to "0" with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

6. Transmission control when external clock is selected

● Note

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to "1" at "H" of the SCLK3 input level. Also, write data to the transmit buffer register at "H" of the SCLK input level.

7. Transmit interrupt request when transmit enable bit is set

● Note

When using the transmit interrupt, take the following sequence.

- ① Set the serial I/O3 transmit interrupt enable bit to "0" (disabled).
- ② Set the transmit enable bit to "1".
- ③ Set the serial I/O3 transmit interrupt request bit to "0" after 1 or more instruction has executed.
- ④ Set the serial I/O3 transmit interrupt enable bit to "1" (enabled).

● Reason

When the transmit enable bit is set to "1", the transmit buffer empty flag and the transmit shift register shift completion flag are also set to "1". Therefore, regardless of selecting which timing for the generating of transmit interrupts, the interrupt request is generated and the transmit interrupt request bit is set at this point.

PULSE WIDTH MODULATION (PWM)

The 3804 group (Spec. H) has PWM functions with an 8-bit resolution, based on a signal that is the clock input X_{IN} or that clock input divided by 2 or the clock input X_{CIN} or that clock input divided by 2 in low-speed mode.

Data Setting

The PWM output pin also functions as port P5₆. Set the PWM period by the PWM prescaler, and set the "H" term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

$$\begin{aligned} \text{PWM period} &= 255 \times (n+1) / f(X_{IN}) \\ &= 31.875 \times (n+1) \mu\text{s} \quad (\text{when } f(X_{IN}) = 8 \text{ MHz}) \end{aligned}$$

$$\begin{aligned} \text{Output pulse "H" term} &= \text{PWM period} \times m / 255 \\ &= 0.125 \times (n+1) \times m \mu\text{s} \\ &\quad (\text{when } f(X_{IN}) = 8 \text{ MHz}) \end{aligned}$$

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to "1", operation starts by initializing the PWM output circuit, and pulses are output starting at an "H".

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

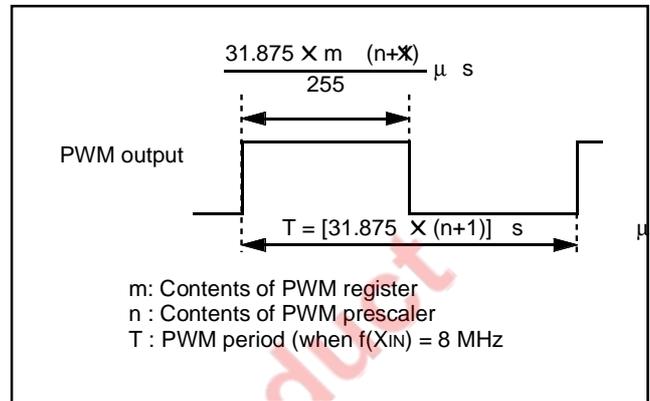


Fig. 45 Timing of PWM period

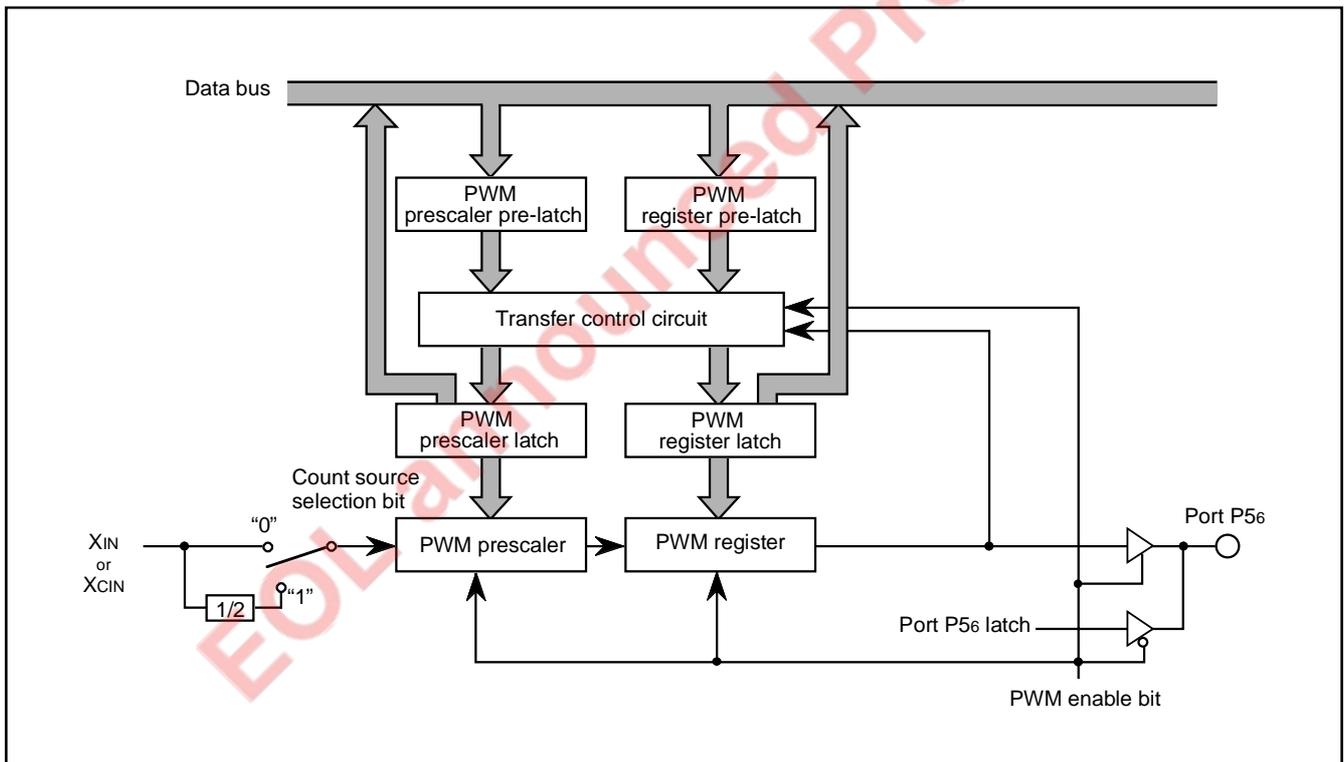


Fig. 46 Block diagram of PWM function

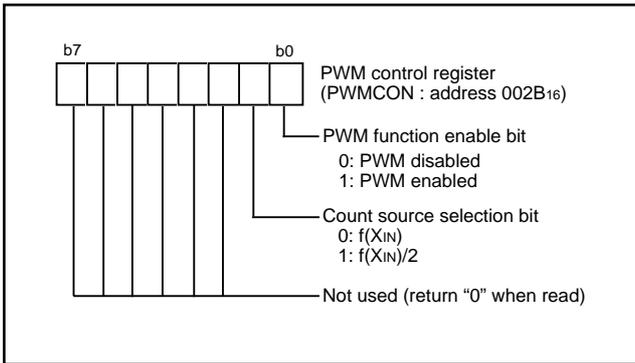


Fig. 47 Structure of PWM control register

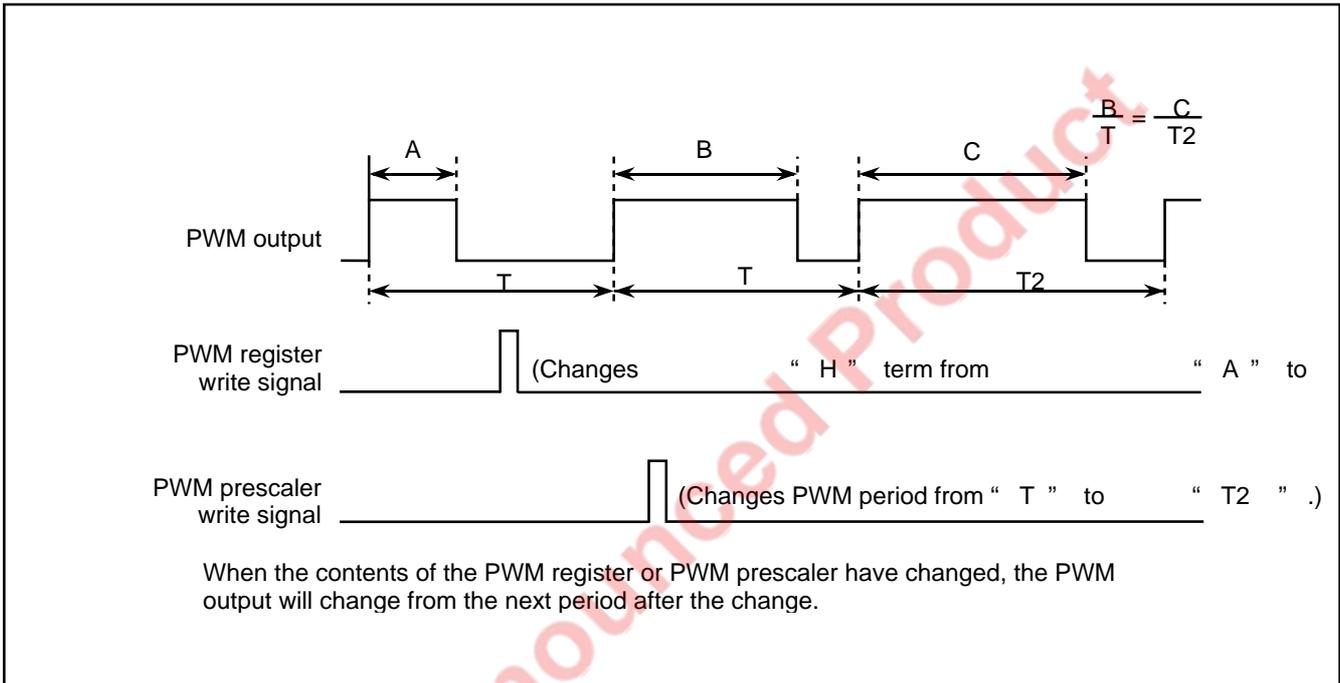


Fig. 48 PWM output timing when PWM register or PWM prescaler is changed

A/D CONVERTER

**[AD Conversion Register 1, 2 (AD1, AD2)]
003516, 003816**

The AD conversion register is a read-only register that stores the result of an A/D conversion. When reading this register during an A/D conversion, the previous conversion result is read.

Bit 7 of the AD conversion register 2 is the conversion mode selection bit. When this bit is set to "0", the A/D converter becomes the 10-bit A/D mode. When this bit is set to 1, that becomes the 8-bit A/D mode. The conversion result of the 8-bit A/D mode is stored in the AD conversion register 1. As for 10-bit A/D mode, not only 10-bit reading but also only high-order 8-bit reading of conversion result can be performed by selecting the reading procedure of the AD conversion registers 1, 2 after A/D conversion is completed (in Figure 50).

As for 10-bit A/D mode, the 8-bit reading inclined to MSB is performed when reading the AD converter register 1 after A/D conversion is started; and when the AD converter register 1 is read after reading the AD converter register 2, the 8-bit reading inclined to LSB is performed.

[AD/DA Control Register (ADCON)] 003416

The AD/DA control register controls the A/D conversion process. Bits 0 to 2 and bit 4 select a specific analog input pin. Bit 3 signals the completion of an A/D conversion. The value of this bit remains at "0" during an A/D conversion, and changes to "1" when an A/D conversion ends. Writing "0" to this bit starts the A/D conversion. "

Comparison Voltage Generator

The comparison voltage generator divides the voltage between VREF and AVSS into 1024, and that outputs the comparison voltage in the 10-bit A/D mode (256 division in 8-bit A/D mode).

The A/D converter successively compares the comparison voltage Vref in each mode, dividing the VREF voltage (see below), with the input voltage.

- 10-bit A/D mode (10-bit reading)

$$V_{ref} = \frac{V_{REF}}{1024} \times n \quad (n = 0 \sim 1023) \quad -$$

- 10-bit A/D mode (8-bit reading)

$$V_{ref} = \frac{V_{REF}}{256} \times n \quad (n = 0 \sim 255) \quad -$$

- 8-bit A/D mode

$$V_{ref} = \frac{V_{REF}}{256} \times (n \cdot 0.5) \quad (n = 1 \sim 255) \quad -$$

$$= 0 \quad (n = 0)$$

Channel Selector

The channel selector selects one of ports P67/AN7 to P60/AN0 or P07/AN15 to P00/AN8, and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compares an analog input voltage with the comparison voltage, and then stores the result in the AD conversion registers 1, 2. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the AD interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A/D conversion.

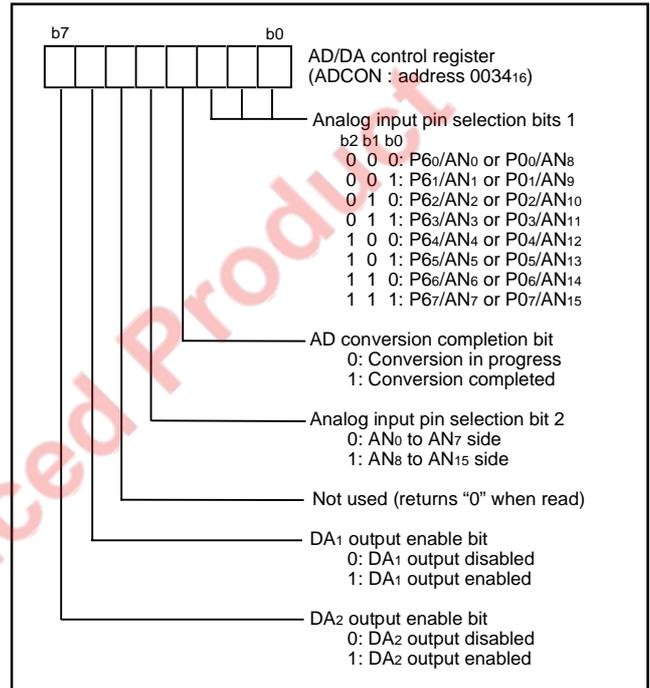


Fig. 49 Structure of AD/DA control register

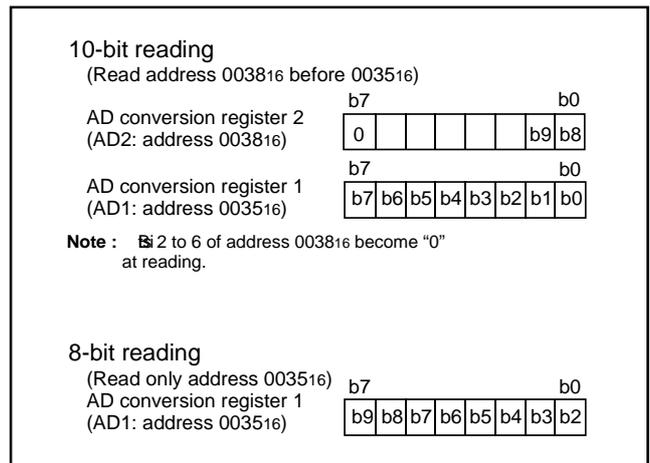


Fig. 50 Structure of 10-bit A/D mode reading

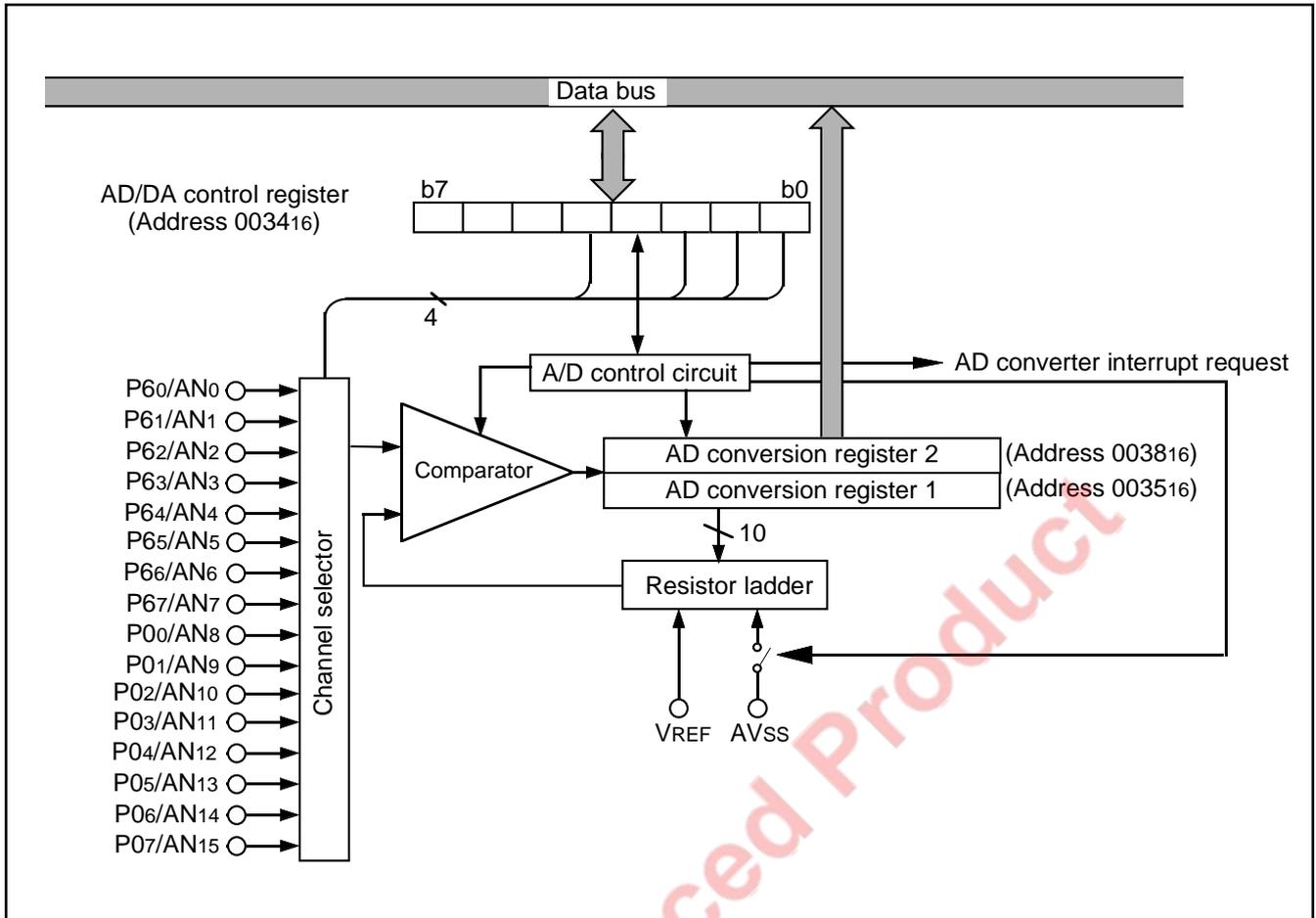


Fig. 51 Block diagram of A/D converter

EOL announced Product

D/A CONVERTER

The 3804 group (Spec. H) has two internal D/A converters (DA1 and DA2) with 8-bit resolution.

The D/A conversion is performed by setting the value in each DA conversion register. The result of D/A conversion is output from the DA1 or DA2 pin by setting the DA output enable bit to "1".

When using the D/A converter, the corresponding port direction register bit (P30/DA1 or P31/DA2) must be set to "0" (input status). The output analog voltage V is determined by the value n (decimal notation) in the DA conversion register as follows:

$$V = V_{REF} \times n / 256 \quad (n = 0 \text{ to } 255)$$

Where VREF is the reference voltage.

At reset, the DA conversion registers are cleared to "0016", and the DA output enable bits are cleared to "0", and the P30/DA1 and P31/DA2 pins become high impedance.

The DA output does not have buffers. Accordingly, connect an external buffer when driving a low-impedance load.

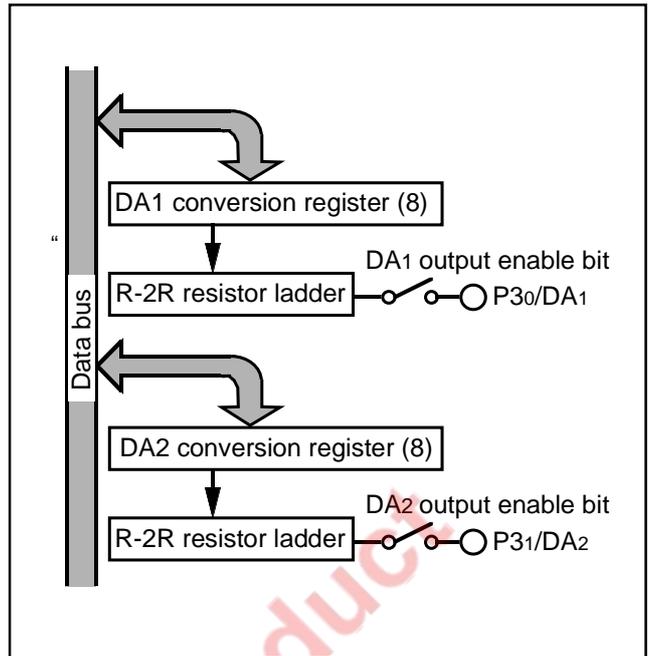


Fig. 52 Block diagram of D/A converter

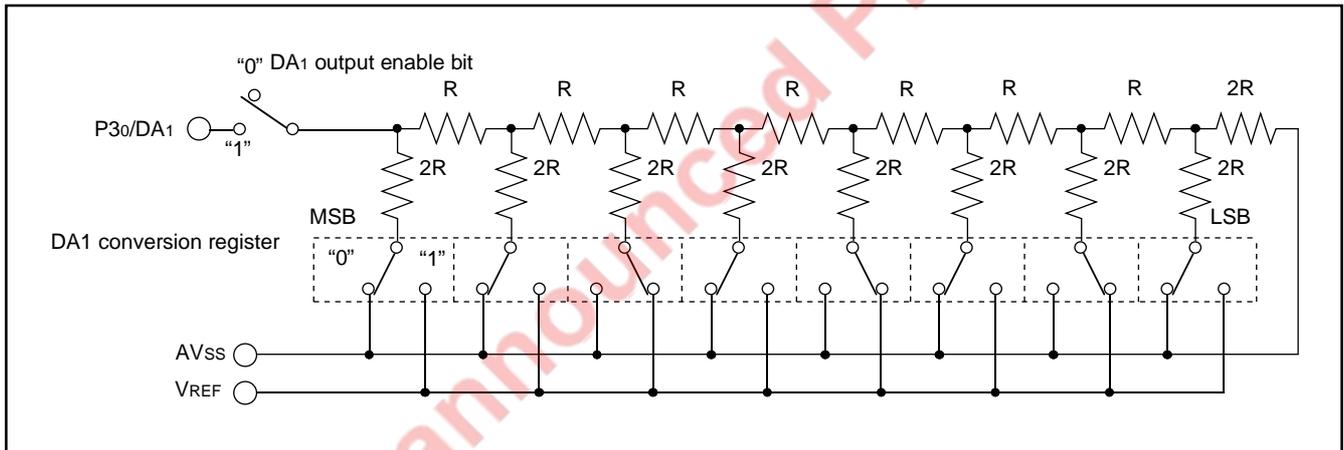


Fig. 53 Equivalent connection circuit of D/A converter (DA1)

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Watchdog Timer Initial Value

Watchdog timer L is set to "FF16" and watchdog timer H is set to "FF16" by writing to the watchdog timer control register (address 001E16) or at a reset. Any write instruction that causes a write signal can be used, such as the STA, LDM, CLB, etc. Data can only be written to bits 6 and 7 of the watchdog timer control register. Regardless of the value written to bits 0 to 5, the above-mentioned value will be set to each timer.

Watchdog Timer Operations

The watchdog timer stops at reset and a countdown is started by the writing to the watchdog timer control register. An internal reset occurs when watchdog timer H underflows. The reset is released after its release time. After the release, the program is restarted from the reset vector address. Usually, write to the watchdog timer control register by software before an underflow of the watchdog timer H. The watchdog timer does not function if the watchdog timer control register is not written to at least once.

When bit 6 of the watchdog timer control register is kept at "0", the STP instruction is enabled. When that is executed, both the clock and the watchdog timer stop. Count re-starts at the same time as the release of stop mode (**Note**). The watchdog timer does not stop while a WIT instruction is executed. In addition, the STP instruction is disabled by writing "1" to this bit again. When the STP instruction is executed at this time, it is processed as an undefined instruction, and an internal reset occurs. Once a "1" is written to this bit, it cannot be programmed to "0" again.

The following shows the period between the write execution to the watchdog timer control register and the underflow of watchdog timer H.

Bit 7 of the watchdog timer control register is "0":

when XCIN = 32.768 kHz; 32 s

when XIN = 16 MHz; 65.536 ms

Bit 7 of the watchdog timer control register is "1":

when XCIN = 32.768 kHz; 125 ms

when XIN = 16 MHz; 256 μs

Note: The watchdog timer continues to count even while waiting for a stop release. Therefore, make sure that watchdog timer H does not underflow during this period.

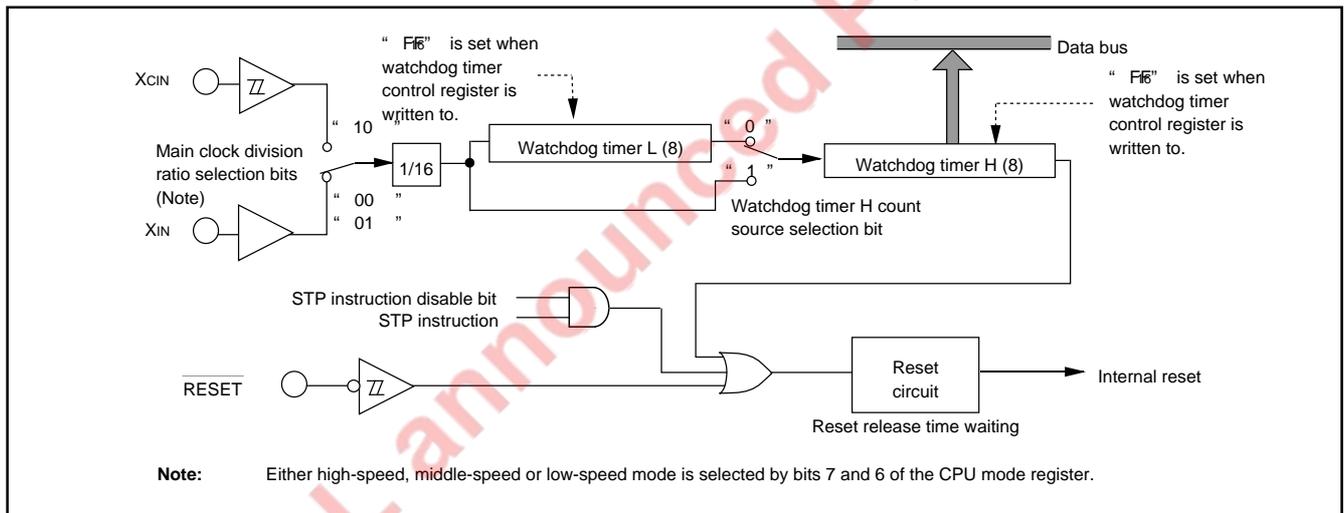


Fig. 54 Block diagram of Watchdog timer

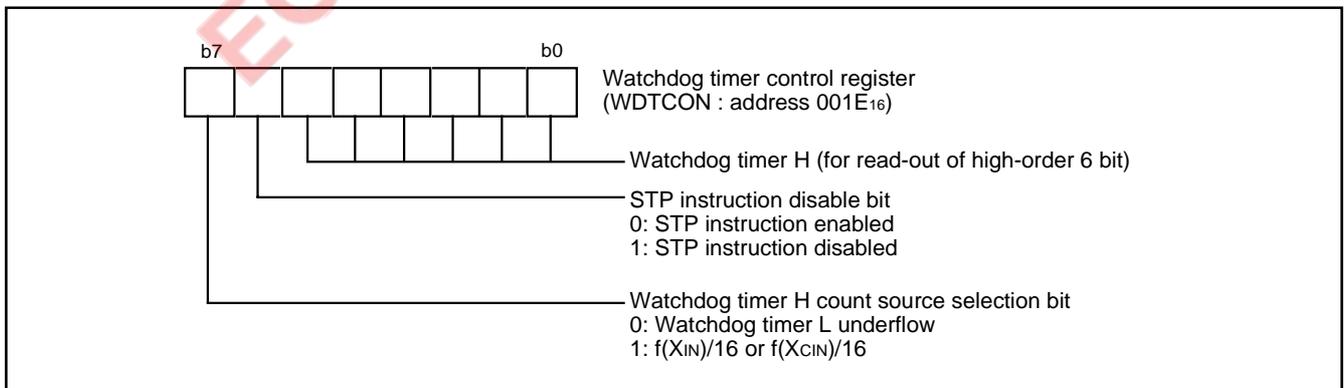


Fig. 55 Structure of Watchdog timer control register

MULTI-MASTER I²C-BUS INTERFACE

The 3804 group (Spec. H) has the multi-master I²C-BUS interface. The multi-master I²C-BUS interface is a serial communications circuit, conforming to the Philips I²C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.

Figure 56 shows a block diagram of the multi-master I²C-BUS interface and Table 7 lists the multi-master I²C-BUS interface functions.

This multi-master I²C-BUS interface consists of the I²C slave address registers 0 to 2, the I²C data shift register, the I²C clock control register, the I²C control register, the I²C status register, the I²C START/STOP condition control register, the I²C special mode control register, the I²C special mode status register, and other control circuits.

When using the multi-master I²C-BUS interface, set 1 MHz or more to the internal clock .

Table 7 Multi-master I²C-BUS interface functions

| Item | Function |
|---------------------|--|
| Format | In conformity with Philips I ² C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode |
| Communication mode | In conformity with Philips I ² C-BUS standard: Master transmission Master reception Slave transmission Slave reception |
| SCL clock frequency | 16.1 kHz to 400 kHz (at $\phi = 4$ MHz) |

System clock $\phi = f(X_{IN})/2$ (high-speed mode)
 $\phi = f(X_{IN})/8$ (middle-speed mode)

ϕ

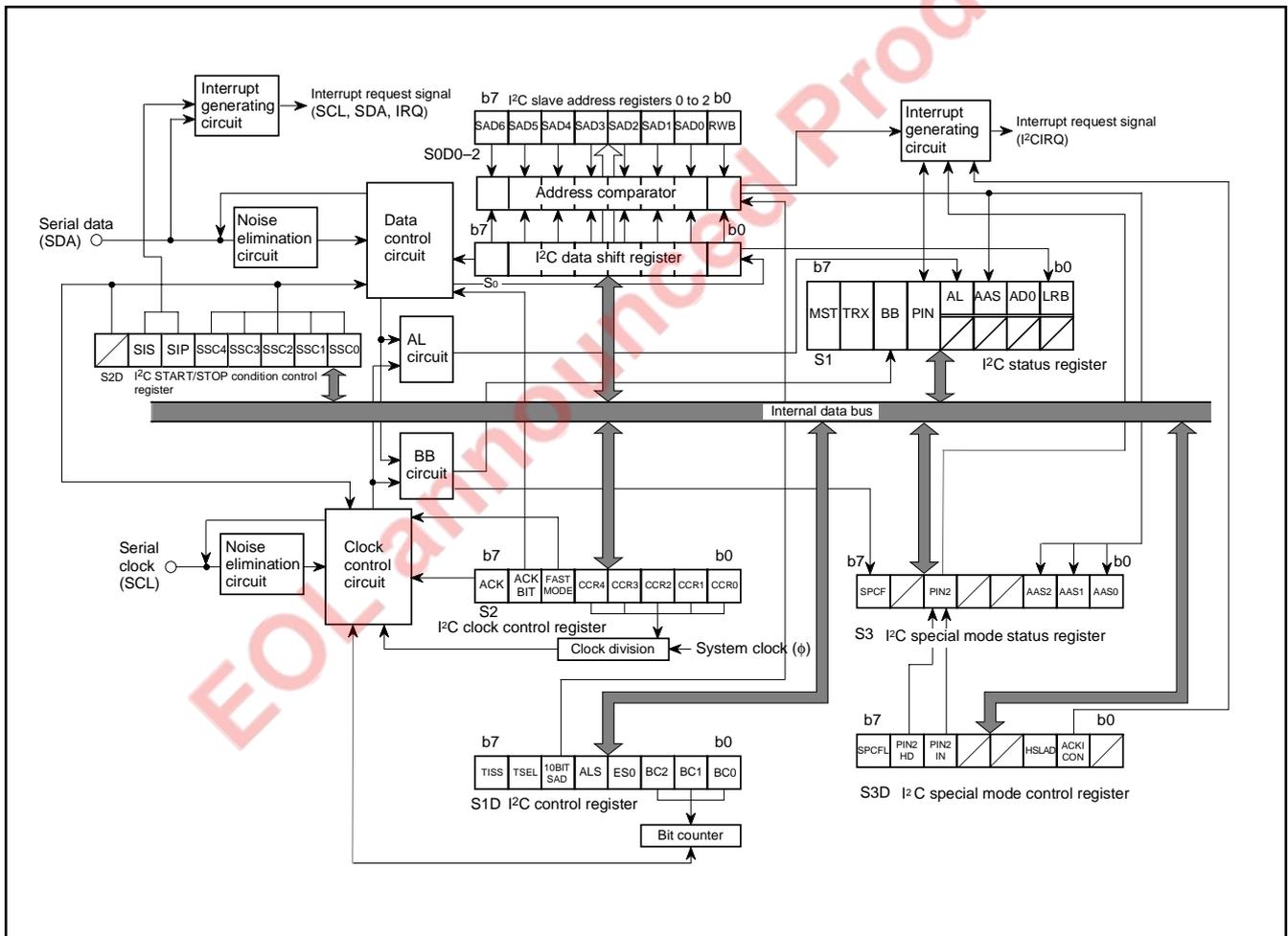


Fig. 56 Block diagram of multi-master I²C-BUS interface

* : Purchase of MITSUBISHI ELECTRIC CORPORATIONS I²C components conveys a license under the Philips I²C Patent Rights to use these components an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

[I²C Data Shift Register (S0)] 001116

The I²C data shift register (S0: address 001116) is an 8-bit shift register to store receive data and write transmit data.

When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL, and each time one-bit data is output, the data of this register are shifted by one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL, and each time one-bit data is input, the data of this register are shifted by one bit to the left. The minimum 2 cycles of the internal clock ϕ are required from the rising of the SCL until input to this register.

The I²C data shift register is in a write enable status only when the I²C-BUS interface enable bit (ES0 bit) of the I²C control register (S1D: address 001416) is "1". The bit counter is reset by a write instruction to the I²C data shift register. When both the ES0 bit and the MST bit of the I²C status register (S1: address 001316) are "1", the SCL is output by a write instruction to the I²C data shift register. Reading data from the I²C data shift register is always enabled regardless of the ES0 bit value.

[I²C Slave Address Registers 0 to 2 (S0D0 to S0D2)] 0FF716 to 0FF916

The I²C slave address registers 0 to 2 (S0D0 to S0D2: addresses 0FF716 to 0FF916) consists of a 7-bit slave address and a read/write bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition is detected.

•Bit 0: Read/write bit (RWB)

This is not used in the 7-bit addressing mode. In the 10-bit addressing mode, set RWB to "0" because the first address data to be received is compared with the contents (SAD6 to SAD0 + RWB) of the I²C slave address registers 0 to 2.

When 2-byte address data match slave address, a 7-bit slave address which is received after restart condition has detected and R/W data can be matched by setting "1" to RWB with software. The RWB is cleared to "0" automatically when the stop condition is detected.

•Bits 1 to 7: Slave address (SAD0 SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode or the 10-bit addressing mode, the address data transmitted from the master is compared with these bits' contents.

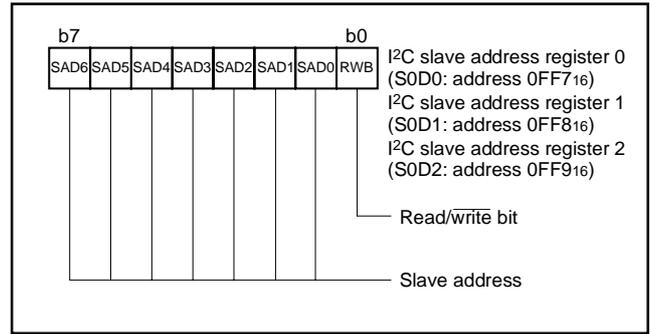


Fig. 57 Structure of I²C slave address registers 0 to 2

[I²C Clock Control Register (S2)] 001516

The I²C clock control register (S2: address 001516) is used to set ACK control, SCL mode and SCL frequency.

•Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 8.

•Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to “0”, the standard clock mode is selected. When the bit is set to “1”, the high-speed clock mode is selected.

When connecting the bus of the high-speed mode I²C bus standard (maximum 400 kbits/s), use 8 MHz or more oscillation frequency f(XIN) in the high-speed mode (2 division clock).

•Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to 0, the ACK return mode is selected and SDA goes to “L” at the occurrence of an ACK clock. When the bit is set to 1, the ACK non-return mode is selected. The SDA is held in the “H” status at the occurrence of an ACK clock.

However, when the slave address agree with the address data in the reception of address data at ACK BIT = “0”, the SDA is automatically made “L” (ACK is returned). If there is a disagreement between the slave address and the address data, the SDA is automatically made “H” (ACK is not returned).

*ACK clock: Clock for acknowledgment

•Bit 7: ACK clock bit (ACK)

This bit specifies the mode of acknowledgment which is an acknowledgment response of data transfer. When this bit is set to “0”, the no ACK clock mode is selected. In this case, no ACK clock occurs after data transmission. When the bit is set to “1”, the ACK clock mode is selected and the master generates an ACK clock each completion of each 1-byte data transfer. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (makes SDA “H”) and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transfer. If data is written during transfer, the I²C clock generator is reset, so that data cannot be transferred normally.

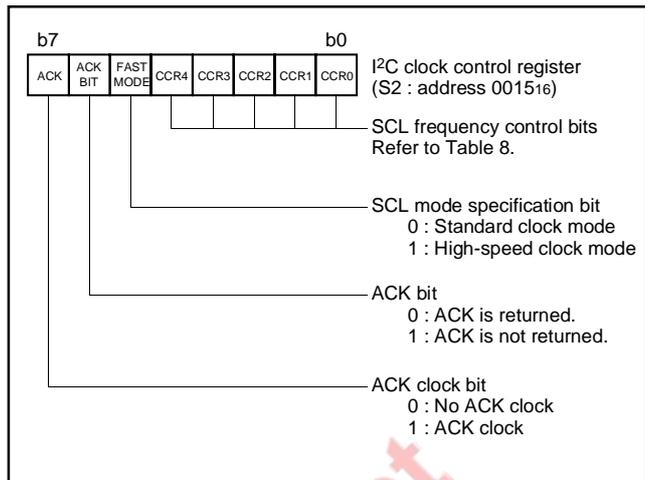


Fig. 58 Structure of I²C clock control register

Table 8 Set values of I²C clock control register and SCL frequency

| Setting value of CCR4 CCR0 | | | | | SCL frequency (at $\phi = 4$ MHz, unit : kHz) (Note 1) | |
|----------------------------|------|------|------|------|--|-------------------------|
| CCR4 | CCR3 | CCR2 | CCR1 | CCR0 | Standard clock mode | High-speed clock mode |
| 0 | 0 | 0 | 0 | 0 | Setting disabled | Setting disabled |
| 0 | 0 | 0 | 0 | 1 | Setting disabled | Setting disabled |
| 0 | 0 | 0 | 1 | 0 | Setting disabled | Setting disabled |
| 0 | 0 | 0 | 1 | 1 | – (Note 2) | 333 |
| 0 | 0 | 1 | 0 | 0 | – (Note 2) | 250 |
| 0 | 0 | 1 | 0 | 1 | 100 | 400 (Note 3) |
| 0 | 0 | 1 | 1 | 0 | 83.3 | 166 |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | 500/CCR value (Note 3) | 1000/CCR value (Note 3) |
| 1 | 1 | 1 | 0 | 1 | 17.2 | 34.5 |
| 1 | 1 | 1 | 1 | 0 | 16.6 | 33.3 |
| 1 | 1 | 1 | 1 | 1 | 16.1 | 32.3 |

Notes 1: Duty of SCL output is 50 %. The duty becomes 35 to 45 % only when the high-speed clock mode is selected and CCR value = 5 (400 kHz, at $\phi = 4$ MHz). “H” duration of the clock fluctuates from –4 to +2 machine cycles in the standard clock mode, and fluctuates from –2 to +2 machine cycles in the high-speed clock mode. In the case of negative fluctuation, the frequency does not increase because “L” duration is extended instead of “H” duration reduction.

These are values when SCL synchronization by the synchronous function is not performed. CCR value is the decimal notation value of the SCL frequency control bits CCR4 to CCR0.

2: Each value of SCL frequency exceeds the limit at $\phi = 4$ MHz or more. When using these setting value, use ϕ of 4 MHz or less.

3: The data formula of SCL frequency is described below:

$\phi / (8 \times \text{CCR value})$ Standard clock mode

$\phi / (4 \times \text{CCR value})$ High-speed clock mode (CCR value $\neq 5$)

$\phi / (2 \times \text{CCR value})$ High-speed clock mode (CCR value = 5)

Do not set 0 to 2 as CCR value regardless of ϕ frequency.

Set 100 kHz (max.) in the standard clock mode and 400 kHz (max.) in the high-speed clock mode to the SCL frequency by setting the SCL frequency control bits CCR4 to CCR0.

[I²C Control Register (S1D)] 001416

The I²C control register (S1D: address 001416) controls data communication format.

•Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. The I²C interrupt request signal occurs immediately after the number of count specified with these bits (ACK clock is added to the number of count when ACK clock is selected by ACK clock bit (bit 7 of S2, address 001516) have been transferred, and BC0 to BC2 are returned to “0002”.

Also when a START condition is received, these bits become “0002” and the address data is always transmitted and received in 8 bits.

•Bit 3: I²C interface enable bit (ES0)

This bit enables to use the multi-master I²C-BUS interface. When this bit is set to 0, the use disable status is provided, so that the SDA and the SCL become high-impedance. When the bit is set to “1”, use of the interface is enabled.

When ES0 = “0”, the following is performed.

- PIN = 1, BB = “0” and AL = 0” are set (which are bits of the I²C status register, S1, at address 001316).
- Writing data to the I²C data shift register (S0: address 001116) is disabled.

•Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to 0, the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to I²C Status Register, bit 1) is received, transfer processing can be performed. When this bit is set to “1”, the free data format is selected, so that slave addresses are not recognized.

•Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to 0, the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I²C slave address registers 0 to 2 are compared with address data. When this bit is set to 1, the 10-bit addressing format is selected, and all the bits of the I²C slave address registers 0 to 2 are compared with address data.

•Bit 7: I²C-BUS interface pin input level selection bit (TISS)

This bit selects the input level of the SCL and SDA pins of the multi-master I²C-BUS interface.

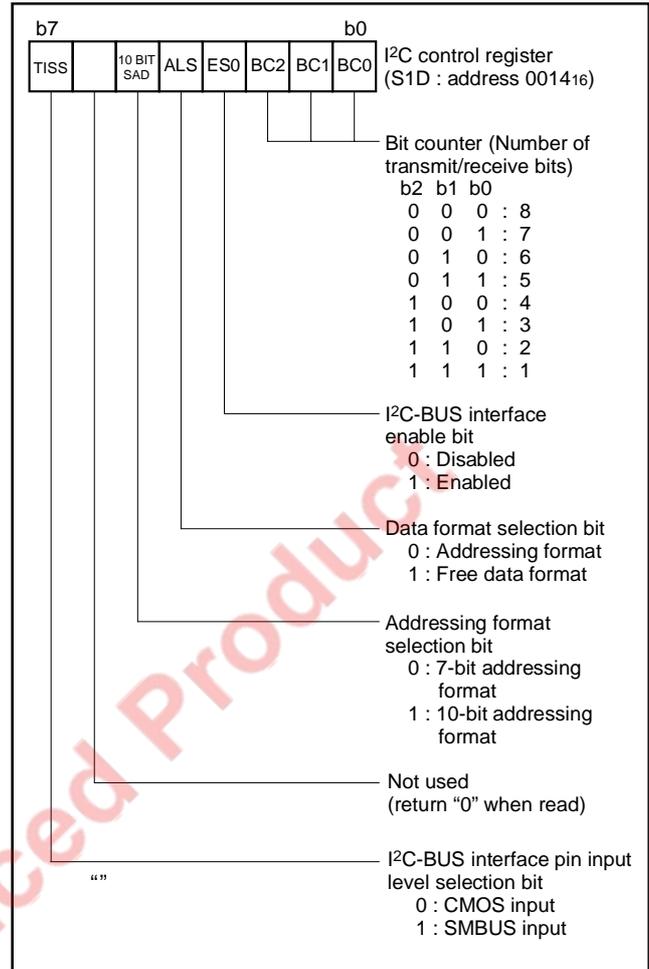


Fig. 59 Structure of I²C control register

[I²C Status Register (S1)] 001316

The I²C status register (S1: address 001316) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

Set "00002" to the low-order 4 bits, because these bits become the reserved bits at writing.

•Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to 0. If ACK is not returned, this bit is set to "1". Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (S0: address 001116).

•Bit 1: General call detecting flag (AD0)

When the ALS bit is "0", this bit is set to "1" when a general call* whose address data is all 0 is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition, or reset.

*General call: The master transmits the general call address "0016" to all slaves.

•Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data when the ALS bit is 0.

- ① In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions:
 - The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C slave address register.
 - A general call is received.
- ② In the slave receive mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition:
 - When the address data is compared with the I²C slave address register (8 bits consisting of slave address and RWB bit), the first bytes agree.
- ③ This bit is set to 0 by executing a write instruction to the I²C data shift register (S0: address 001116) when ES0 is set to 1 or reset.

•Bit 3: Arbitration lost* detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to 1. At the same time, the TRX bit is set to 0, so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0". The arbitration lost can be detected only in the master transmission mode. When arbitration is lost during slave address transmission, the TRX bit is set to 0 and the reception mode is set. Consequently, it becomes possible to detect the agreement of its own slave address and address data transmitted by another master device.

The AL bit is set to "0" in one of the following conditions:

- Executing a write instruction to the I²C data shift register (S0: address 001116)
- When the ES0 bit is 0
- At reset

*Arbitration lost: The status in which communication as a master is disabled.

•Bit 4: SCL pin low hold bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the PIN bit changes from "1" to 0. At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to 0 in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is 0, the SCL is kept in the 0 state and clock generation is disabled. Figure 61 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions:

- Executing a write instruction to the I²C data shift register (S0: address 001116). (This is the only condition which the prohibition of the internal clock is released and data can be communicated except for the start condition detection.)

- When the ES0 bit is 0

- At reset

- When writing 1 to the PIN bit by Software

The PIN bit is set to 0 in one of the following conditions:

- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = 0 and immediately after completion of slave address agreement or general call address reception
- In the slave reception mode, with ALS = 1 and immediately after completion of address data reception

•Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to 0, this bus system is not busy and a START condition can be generated. The BB flag is set/reset by the SCL, SDA pins input signal regardless of master/slave. This flag is set to 1 by detecting the START condition, and is set to 0 by detecting the STOP condition. The condition of these detecting is set by the START/STOP condition setting bits (SSC4–SSC0) of the I²C START/STOP condition control register (S2D: address 001616). When the ES0 bit of the I²C control register (bit 3 of S1D, address 001416) is 0 or reset, the BB flag is set to 0.

For the writing function to the BB flag, refer to the sections "START Condition Generating Method" and "STOP Condition Generating Method" described later.

•**Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)**

This bit decides a direction of transfer for data communication. When this bit is 0, the reception mode is selected and the data of a transmitting device is received. When the bit is 1, the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

This bit is set/reset by software and hardware. About set/reset by hardware is described below. This bit is set to "1" by hardware when all the following conditions are satisfied:

- When ALS is 0
- In the slave reception mode or the slave transmission mode
- When the R/W bit reception is "1"

This bit is set to 0 in one of the following conditions:

- When arbitration lost is detected.
- When a STOP condition is detected.
- When writing "1" to this bit by software is invalid by the START condition duplication preventing function (**Note**).
- With MST = 0 and when a START condition is detected.
- With MST = 0 and when ACK non-return is detected.
- At reset

•**Bit 7: Communication mode specification bit (master/slave specification bit: MST)**

This bit is used for master/slave specification for data communication. When this bit is 0, the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is "1", the master is specified and a START condition and a STOP condition are generated. Additionally, the clocks required for data communication are generated on the SCL.

This bit is set to 0 in one of the following conditions.

- Immediately after completion of the byte which has lost arbitration when arbitration lost is detected
- When a STOP condition is detected.
- Writing "1" to this bit by software is invalid by the START condition duplication preventing function (**Note**).
- At reset

Note: START condition duplication preventing function

The MST, TRX, and BB bits is set to 1 at the same time after confirming that the BB flag is 0 in the procedure of a START condition occurrence. However, when a START condition by another master device occurs and the BB flag is set to "1" immediately after the contents of the BB flag is confirmed, the START condition duplication preventing function makes the writing to the MST and TRX bits invalid. The duplication preventing function becomes valid from the rising of the BB flag to reception completion of slave address.

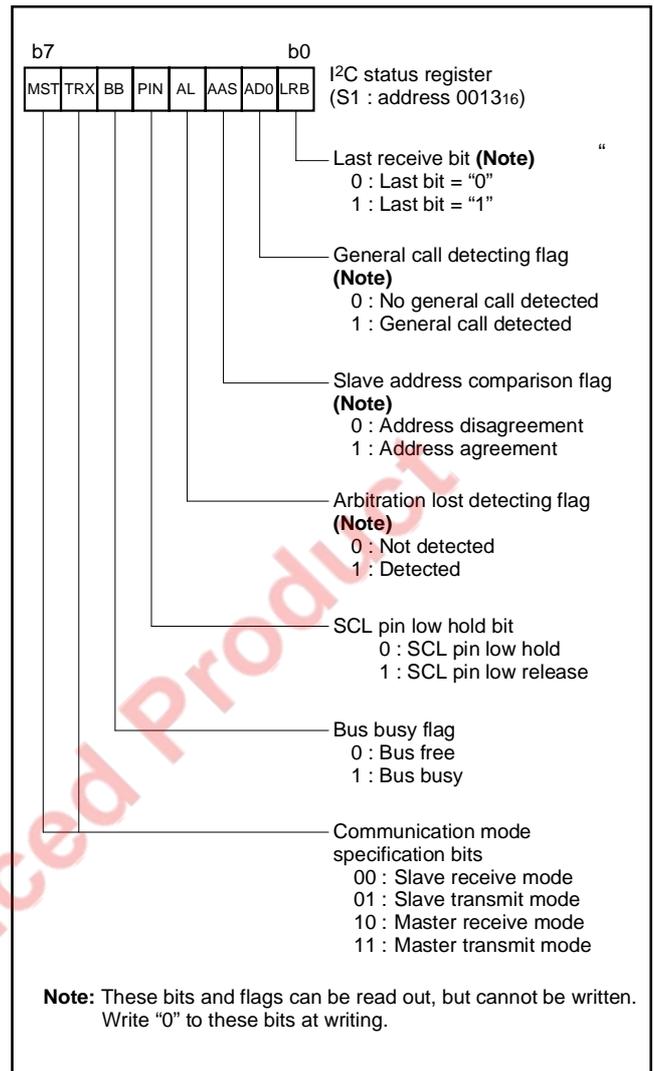


Fig. 60 Structure of I²C status register

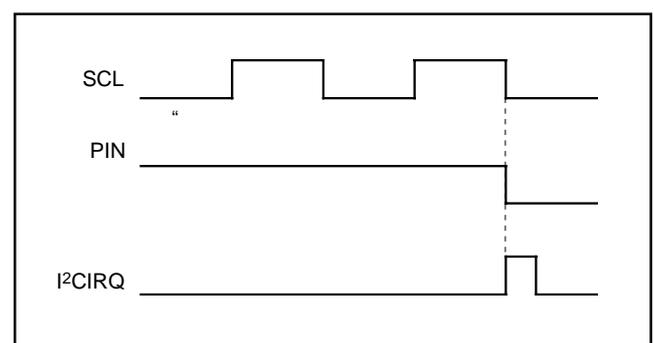


Fig. 61 Interrupt request signal generating timing

START Condition Generating Method

When writing "1" to the MST, TRX, and BB bits of the I²C status register (S1: address 0013₁₆) at the same time after writing the slave address to the I²C data shift register (S0: address 0011₁₆) with the condition in which the ES0 bit of the I²C control register (S1D: address 0014₁₆) is "1" and the BB flag is "0", a START condition occurs. After that, the bit counter becomes "0002" and an SCL for 1 byte is output. The START condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 62, the START condition generating timing diagram, and Table 9, the START condition generating timing table.

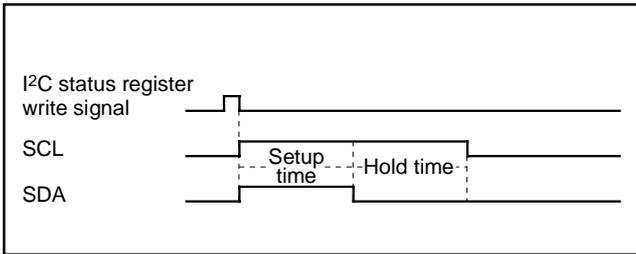


Fig. 62 START condition generating timing diagram

Table 9 START condition generating timing table

| Item | Standard clock mode | High-speed clock mode |
|------------|---------------------|-----------------------|
| Setup time | 5.0 μs (20 cycles) | 2.5 μs (10 cycles) |
| Hold time | 5.0 μs (20 cycles) | 2.5 μs (10 cycles) |

Note: Absolute time at φ = 4 MHz. The value in parentheses denotes the number of φ cycles.

STOP Condition Generating Method

When the ES0 bit of the I²C control register (S1D: address 0014₁₆) is "1", write "1" to the MST and TRX bits, and write "0" to the BB bit of the I²C status register (S1: address 0013₁₆) simultaneously. Then a STOP condition occurs. The STOP condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 63, the STOP condition generating timing diagram, and Table 10, the STOP condition generating timing table.

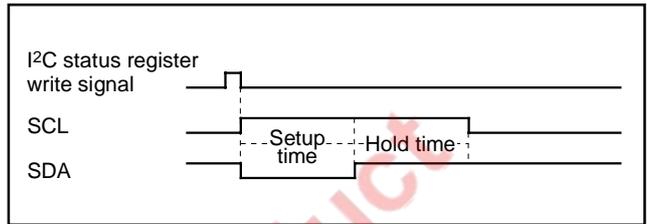


Fig. 63 STOP condition generating timing diagram

Table 10 STOP condition generating timing table

| Item | Standard clock mode | High-speed clock mode |
|------------|---------------------|-----------------------|
| Setup time | 5.0 μs (20 cycles) | 3.0 μs (12 cycles) |
| Hold time | 4.5 μs (18 cycles) | 2.5 μs (10 cycles) |

Note: Absolute time at φ = 4 MHz. The value in parentheses denotes the number of φ cycles.

START/STOP Condition Detecting Operation

The START/STOP condition detection operations are shown in Figures 64, 65, and Table 11. The START/STOP condition is set by the START/STOP condition set bit.

The START/STOP condition can be detected only when the input signal of the SCL and SDA pins satisfy three conditions: SCL release time, setup time, and hold time (see Table 11).

The BB flag is set to "1" by detecting the START condition and is reset to "0" by detecting the STOP condition.

The BB flag set/reset timing is different in the standard clock mode and the high-speed clock mode. Refer to Table 11, the BB flag set/reset time.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal "I²CIRQ" occurs to the CPU.

Table 11 START condition/STOP condition detecting conditions

| | Standard clock mode | High-speed clock mode |
|------------------------|---|-----------------------|
| SCL release time | SSC value + 1 cycle (6.25 μs) | 4 cycles (1.0 μs) |
| Setup time | $\frac{SSC \text{ value} + 1}{2}$ cycle < 4.0 μs (3.125 μs) | 2 cycles (0.5 μs) |
| Hold time | $\frac{SSC \text{ value} + 1}{2}$ cycle < 4.0 μs (3.125 μs) | 2 cycles (0.5 μs) |
| BB flag set/reset time | $\frac{SSC \text{ value} + 1}{2} + 2$ cycles (3.375 μs) | 3.5 cycles (0.875 μs) |

Note: Unit : Cycle number of internal clock φ

SSC value is the decimal notation value of the START/STOP condition set bits SSC4 to SSC0. Do not set "0" or an odd number to SSC value. The value in parentheses is an example when the I²C START/STOP condition control register is set to "1816" at φ = 4 MHz.

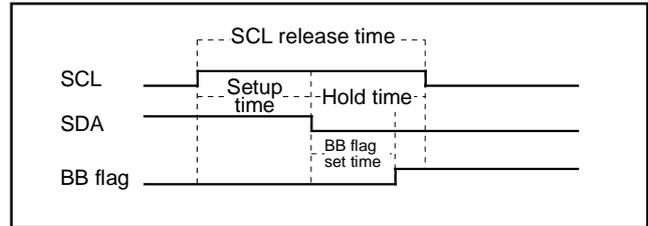


Fig. 64 START/STOP condition detecting timing diagram

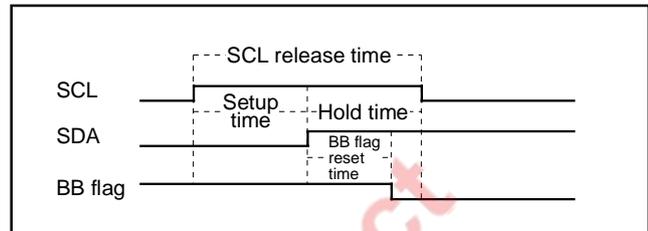


Fig. 65 STOP condition detecting timing diagram

[[I²C START/STOP Condition Control Register (S2D)] 001616

The I²C START/STOP condition control register (S2D: address 001616) controls START/STOP condition detection.

•Bits 0 to 4: START/STOP condition set bits (SSC4–SSC0)

SCL release time, setup time, and hold time change the detection condition by value of the main clock divide ratio selection bit and the oscillation frequency $f(X_{IN})$ because these time are measured by the internal system clock. Accordingly, set the proper value to the START/STOP condition set bits (SSC4 to SSC0) in considered of the system clock frequency. Refer to Table 11.

Do not set "000002" or an odd number to the START/STOP condition set bits (SSC4 to SSC0).

Refer to Table 12, the recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency.–

•Bit 5: SCL/SDA interrupt pin polarity selection bit (SIP)

An interrupt can occur when detecting the falling or rising edge of the SCL or SDA pin. This bit selects the polarity of the SCL or SDA pin interrupt pin.

•Bit 6: SCL/SDA interrupt pin selection bit (SIS)

This bit selects the pin of which interrupt becomes valid between the SCL pin and the SDA pin.

Note: When changing the setting of the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0, the SCL/SDA interrupt request bit may be set. When selecting the SCL/SDA interrupt source, disable the interrupt before the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I²C-BUS interface enable bit ES0 is set. Reset the request bit to "0" after setting these bits, and enable the interrupt.

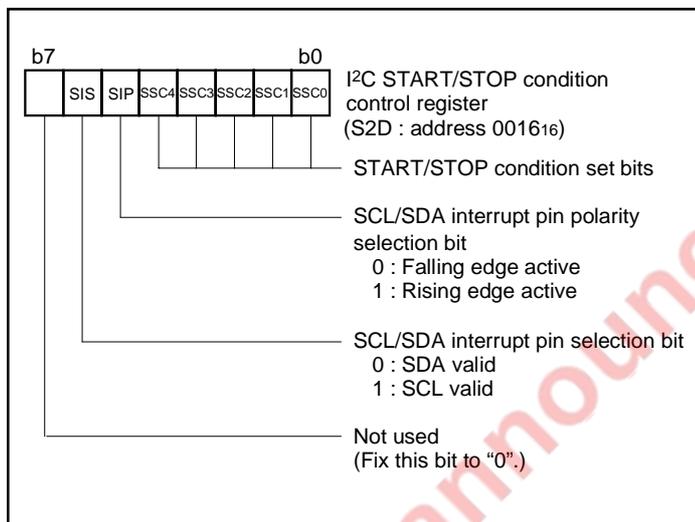


Fig. 66 Structure of I²C START/STOP condition control register

Table 12 Recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency

| Oscillation frequency $f(X_{IN})$ (MHz) | Main clock divide ratio | Internal clock ϕ (MHz) | START/STOP condition control register | SCL release time (μ s) | Setup time (μ s) | Hold time (μ s) |
|---|-------------------------|-----------------------------|---------------------------------------|-----------------------------|--------------------------|--------------------------|
| 8 | 2 | 4 | XXX11010 | 6.75 μ s (27 cycles) | 3.5 μ s (14 cycles) | 3.25 μ s (13 cycles) |
| | | | XXX11000 | 6.25 μ s (25 cycles) | 3.25 μ s (13 cycles) | 3.0 μ s (12 cycles) |
| 8 | 8 | 1 | XXX00100 | 5.0 μ s (5 cycles) | 3.0 μ s (3 cycles) | 2.0 μ s (2 cycles) |
| 4 | 2 | 2 | XXX01100 | 6.5 μ s (13 cycles) | 3.5 μ s (7 cycles) | 3.0 μ s (6 cycles) |
| | | | XXX01010 | 5.5 μ s (11 cycles) | 3.0 μ s (6 cycles) | 2.5 μ s (5 cycles) |
| 2 | 2 | 1 | XXX00100 | 5.0 μ s (5 cycles) | 3.0 μ s (3 cycles) | 2.0 μ s (2 cycles) |

Note: Do not set an odd number to the START/STOP condition set bits (SSC4 to SSC0) and "000002".

[I²C Special Mode Status Register (S3)] 001216

The I²C special mode status register (S3: address 001216) consists of the flags indicating I²C operating state in the I²C special mode, which is set by the I²C special mode control register (S3D: address 001716).

The stop condition flag is valid in all operating modes.

•**Bit 0: Slave address 0 comparison flag (AAS0)**

Bit 1: Slave address 1 comparison flag (AAS1)

Bit 2: Slave address 2 comparison flag (AAS2)

These flags indicate a comparison result of address data. These flags are valid only when the slave address control bit (MSLAD) is "1".

In the 7-bit addressing format of the slave reception mode, the respective slave address *i* (*i* = 0, 1, 2) comparison flags corresponding to the I²C slave address registers 0 to 2 are set to "1" when an address data immediately after an occurrence of a START condition agrees with the high-order 7-bit slave address stored in the I²C slave address registers 0 to 2 (addresses 0FF716 to 0FF916).

In the 10-bit addressing format of the slave mode, the respective slave address *i* (*i* = 0, 1, 2) comparison flags corresponding to the I²C slave address registers are set to "1" when an address data is compared with the 8 bits consisting of the slave address stored in the I²C slave address registers 0 to 2 and the RWB bit, and the first byte agrees.

These flags are initialized to "0" at reset, when the slave address control bit (MSLAD) is "0", or when writing data to the I²C data shift register (S0: address 001116).

•**Bit 5: SCL pin low hold 2 flag (PIN2)**

When the ACK interrupt control bit (ACKICON) and the ACK clock bit (ACK) are "1", this flag is set to "0" in synchronization with the falling of the data's last SCL clock, just before the ACK clock. The SCL pin is simultaneously held low, and the I²C interrupt request occurs.

This flag is initialized to "1" at reset, when the ACK interrupt control bit (ACKICON) is "0", or when writing "1" to the SCL pin low hold 2 flag set bit (PIN2IN).

The SCL pin is held low when either the SCL pin low hold bit (PIN) or the SCL pin low hold 2 flag (PIN2) becomes "0". The low hold state of the SCL pin is released when both the SCL pin low hold bit (PIN) and the SCL pin low hold 2 flag (PIN2) are "1".

•**Bit 7: Stop condition flag (SPCF)**

This flag is set to "1" when a STOP condition occurs.

This flag is initialized to "0" at reset, when the I²C-BUS interface enable bit (ES0) is "0", or when writing "1" to the STOP condition flag clear bit (SPFCL).

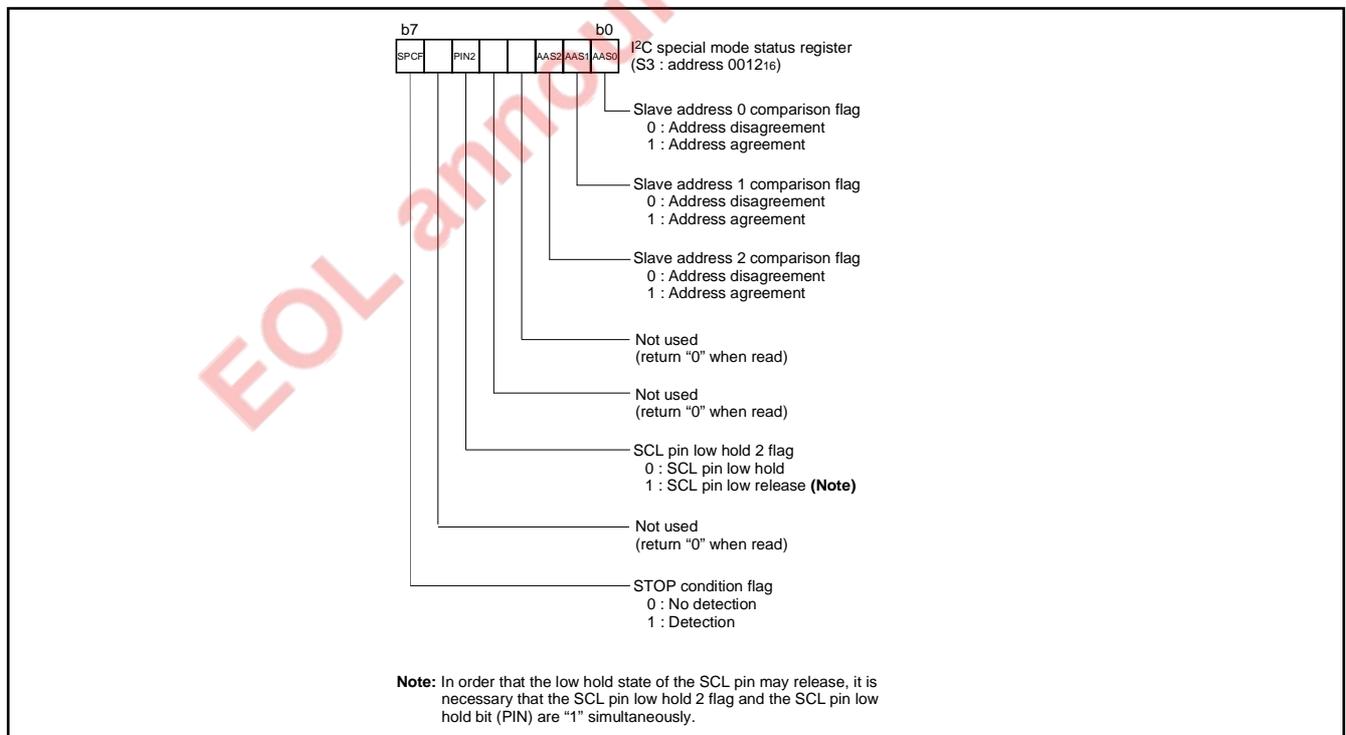


Fig. 67 Structure of I²C special mode status register

[I²C Special Mode Control Register (S3D)] 001716

The I²C special mode control register (S3D: address 001716) controls special functions such as occurrence timing of reception interrupt request and extending slave address comparison to 3 bytes.

•Bit 1: ACK interrupt control bit (ACKICON)

This bit controls the timing of I²C interrupt request occurrence at completion of data receiving due to master reception or slave reception.

When this bit is "0", the SCL pin low hold bit (PIN) is set to "0" in synchronization with the falling of the last SCL clock, including the ACK clock. The SCL pin is simultaneously held low, and the I²C interrupt request occurs.

When this bit is "1" and the ACK clock bit (ACK) is "1", the SCL pin low hold 2 flag (PIN2) is set to "0" in synchronization with the falling of the data's last SCL clock, just before the ACK clock. The SCL pin is simultaneously held low, and the I²C interrupt request occurs again. The ACK bit can be changed after the contents of data are confirmed by using this function.

•Bit 2: I²C slave address control bit (MSLAD)

This bit controls a slave address. When this bit is "0", only the I²C slave address register 0 (address 0FF716) becomes valid as a slave address and a read/write bit.

When this bit is "1", all of the I²C slave address registers 0 to 2 (addresses 0FF716 to 0FF916) become valid as a slave address and a read/write bit. In this case, when an address data agrees with any one of the I²C slave address registers 0 to 2, the slave address comparison flag (AAS) is set to "1" and the I²C slave address comparison flag corresponding to the agreed I²C slave address registers 0 to 2 is also set to "1".

•Bit 5: SCL pin low hold 2 flag set bit (PIN2IN)

Writing "1" to this bit initializes the SCL pin low hold 2 flag (PIN2) to "1".

When writing "0", nothing is generated.

•Bit 6: SCL pin low hold set bit (PIN2HD)

When the SCL pin low hold bit (PIN) becomes "0", the SCL pin is held low. However, the SCL pin low hold bit (PIN) cannot be set to "0" by software. The SCL pin low hold set bit (PIN2HD) is used to hold the SCL pin in the low state by software. When writing "1" to this bit, the SCL pin low hold 2 flag (PIN2) becomes "0", and the SCL pin is held low. When writing "0", nothing occurs.

•Bit 7: STOP condition flag clear bit (SPFCL)

Writing "1" to this bit initializes the STOP condition flag (SPCF) to "0".

When writing "0", nothing is generated.

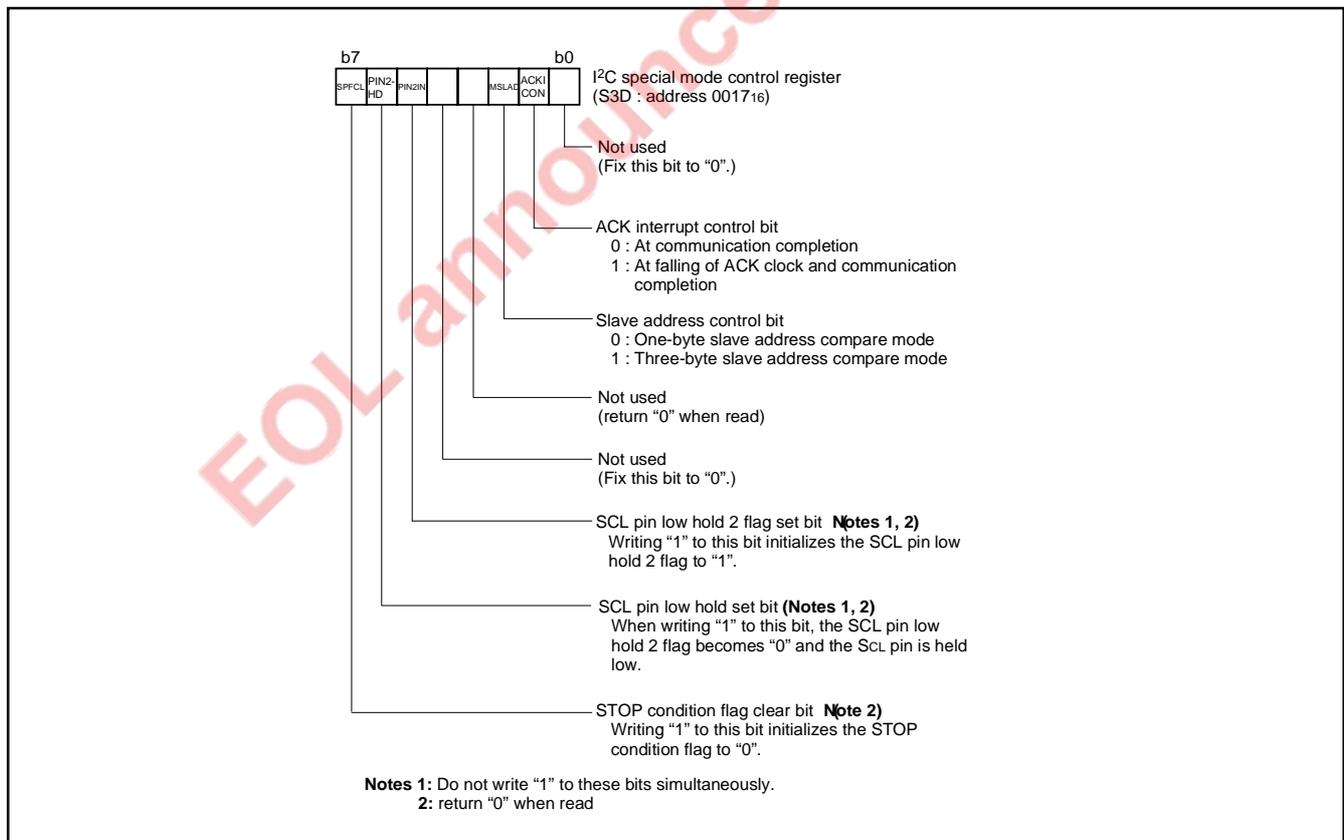


Fig. 68 Structure of I²C special mode control register

Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

① 7-bit addressing format

To adapt the 7-bit addressing format, set the 10BIT SAD bit of the I²C control register (S1D: address 0014₁₆) to 0". The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I²C slave address register. At the time of this comparison, address comparison of the RWB bit of the I²C slave address register is not performed. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 69, (1) and (2).

② 10-bit addressing format

To adapt the 10-bit addressing format, set the 10BIT SAD bit of the I²C control register (S1D: address 0014₁₆) to 1. An address comparison is performed between the first-byte address data transmitted from the master and the 8-bit slave address stored in the I²C slave address register. At the time of this comparison, an address comparison between the RWB bit of the I²C slave address register and the R \bar{W} bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the RWB bit which is the last bit of the address data not only specifies the direction of communication for control data, but also is processed as an address data bit. When the first-byte address data agree with the slave address, the AAS bit of the I²C status register (S1: address 0013₁₆) is set to 1. After the second-byte address data is stored into the I²C data shift register (S0: address 0011₁₆), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes agree with the slave address, set the RWB bit of the I²C slave address register to 1" by software. This processing can make the 7-bit slave address and R \bar{W} data agree, which are received after a RESTART condition is detected, with the value of the I²C slave address register. For the data transmission format when the 10-bit addressing format is selected, refer to Figure 69, (3) and (4).

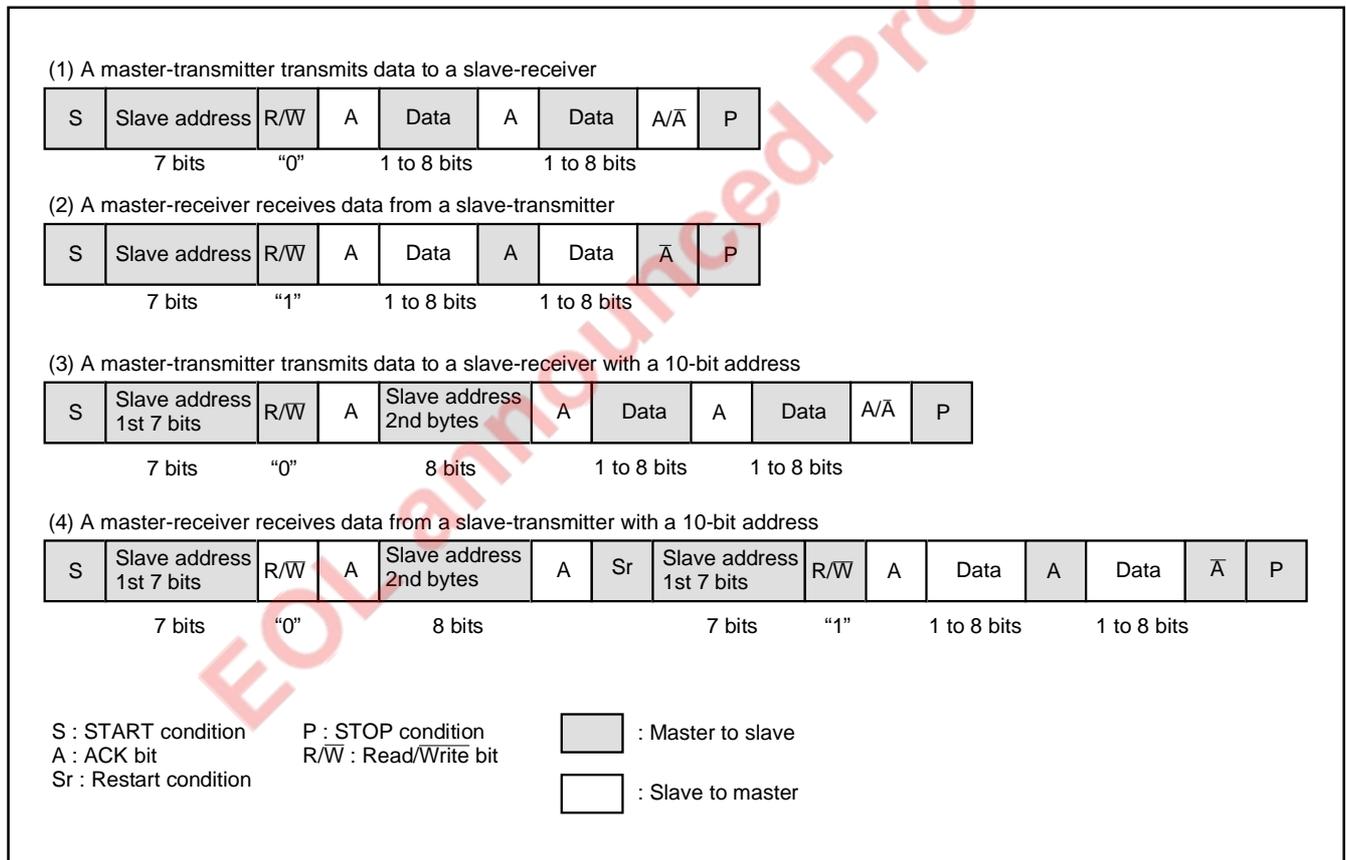


Fig. 69 Address data communication format

Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C slave address register and "0" into the RWB bit.
- ② Set the ACK return mode and SCL = 100 kHz by setting "85₁₆" in the I²C clock control register (S2: address 0015₁₆).
- ③ Set "00₁₆" in the I²C status register (S1: address 0013₁₆) so that transmission/reception mode can become initializing condition.
- ④ Set a communication enable status by setting "08₁₆" in the I²C control register (S1D: address 0014₁₆).
- ⑤ Confirm the bus free condition by the BB flag of the I²C status register (S1: address 0013₁₆).
- ⑥ Set the address data of the destination of transmission in the high-order 7 bits of the I²C data shift register (S0: address 0011₁₆) and set "0" in the least significant bit.
- ⑦ Set "F0₁₆" in the I²C status register (S1: address 0013₁₆) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occur.
- ⑧ Set transmit data in the I²C data shift register (S0: address 0011₁₆). At this time, an SCL and an ACK clock automatically occur.
- ⑨ When transmitting control data of more than 1 byte, repeat step ⑧.
- ⑩ Set "D0₁₆" in the I²C status register (S1: address 0013₁₆) to generate a STOP condition if ACK is not returned from slave reception side or transmission ends.

Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

- ① Set a slave address in the high-order 7 bits of the I²C slave address register and "0" in the RWB bit.
- ② Set the no ACK clock mode and SCL = 400 kHz by setting "25₁₆" in the I²C clock control register (S2: address 0015₁₆).
- ③ Set "00₁₆" in the I²C status register (S1: address 0013₁₆) so that transmission/reception mode can become initializing condition.
- ④ Set a communication enable status by setting "08₁₆" in the I²C control register (S1D: address 0014₁₆).
- ⑤ When a START condition is received, an address comparison is performed.
- ⑥ •When all transmitted addresses are "0" (general call):
 ADO of the I²C status register (S1: address 0013₁₆) is set to "1" and an interrupt request signal occurs.
 • When the transmitted addresses agree with the address set in ①:
 AAS of the I²C status register (S1: address 0013₁₆) is set to "1" and an interrupt request signal occurs.
 • In the cases other than the above ADO and AAS of the I²C status register (S1: address 0013₁₆) are set to "0" and no interrupt request signal occurs.
- ⑦ Set dummy data in the I²C data shift register (S0: address 0011₁₆).
- ⑧ When receiving control data of more than 1 byte, repeat step ⑦.
- ⑨ When a STOP condition is detected, the communication ends.

■Precautions when using multi-master I²C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I²C-BUS interface are described below.

- I²C data shift register (S0: address 0011₁₆)
When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I²C slave address registers 0 to 2 (S0D0 to S0D2: addresses 0FF7₁₆ to 0FF9₁₆)
When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because H/W changes the read/write bit (RWB) at the above timing.
- I²C status register (S1: address 0013₁₆)
Do not execute the read-modify-write instruction for this register because all bits of this register are changed by H/W.
- I²C control register (S1D: address 0014₁₆)
When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because H/W changes the bit counter (BC0-BC2) at the above timing.
- I²C clock control register (S2: address 0015₁₆)
The read-modify-write instruction can be executed for this register.
- I²C START/STOP condition control register (S2D: address 0016₁₆)
The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 5.)

```

∴
LDA — (Taking out of slave address value)
SEI (Interrupt disabled)
BBS 5, S1, BUSBUSY (BB flag confirming and branch process)
BUSFREE:
STA S0 (Writing of slave address value)
LDM #F0, S1 (Trigger of START condition generating)
CLI (Interrupt enabled)
∴
BUSBUSY:
CLI (Interrupt enabled)
∴

```

2. Use Branch on "Bit Set of BBS 5", S1, " —" for the BB flag confirming and branch process.
3. Use STA \$12, STX \$12 or STY \$12 of the zero page addressing instruction for writing the slave address value to the I²C data shift register.
4. Execute the branch instruction of above 2 and the store instruction of above 3 continuously shown the above procedure example.

5. Disable interrupts during the following three process steps:

- BB flag confirming
- Writing of slave address value
- Trigger of START condition generating

When the condition of the BB flag is bus busy, enable interrupts immediately.

- (3) RESTART condition generating procedure

1. Procedure example (The necessary conditions of the generating procedure are described as the following 2 to 4.)

Execute the following procedure when the PIN bit is "0. "

```

∴
LDM #S00, S1 (Select slave receive mode)
LDA — (Taking out of slave address value)
SEI (Interrupt disabled)
STA S0 (Writing of slave address value)
LDM #F0, S1 (Trigger of RESTART condition generating)
CLI (Interrupt enabled)
∴

```

2. Select the slave receive mode when the PIN bit is "0. Do not write "1" to the PIN bit. Neither "0" nor "1" is specified for the writing to the BB bit.

The TRX bit becomes "0" and the SDA pin is released.

3. The SCL pin is released by writing the slave address value to the I²C data shift register.

4. Disable interrupts during the following two process steps:

- Writing of slave address value
- Trigger of RESTART condition generating

- (4) Writing to I²C status register

Do not execute an instruction to set the PIN bit to "1" from "0" and an instruction to set the MST and TRX bits to "0" from "1" simultaneously. It is because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to "0" from "1" simultaneously when the PIN bit is "1. It is because it may become the same as above.

- (5) Process of after STOP condition generating

Do not write data in the I²C data shift register S0 and the I²C status register S1 until the bus busy flag BB becomes "0" after generating the STOP condition in the master mode. It is because the STOP condition waveform might not be normally generated. Reading to the above registers does not have the problem.

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin should be held at an "L" level for 16 cycles or more of X_{IN} . Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage should be between 2.7 V to 5.5 V, and the oscillation should be stable), reset is released. After the reset is completed, the program starts from the address FFFD_{16} (high-order byte) and address FFFC_{16} (low-order byte).

Input to the $\overline{\text{RESET}}$ pin in the following procedure.

- When power source is stabilized
 - (1) Input "L" level to $\overline{\text{RESET}}$ pin.
 - (2) Input "L" level for 16 cycles or more to X_{IN} pin.
 - (3) Input "H" level to $\overline{\text{RESET}}$ pin.
- At power-on
 - (1) Input "L" level to $\overline{\text{RESET}}$ pin.
 - (2) Increase the power source voltage to 2.7 V.
 - (3) Wait for $t_d(P-R)$ until internal power source has stabilized.
 - (4) Input "L" level for 16 cycles or more to X_{IN} pin.
 - (5) Input "H" level to $\overline{\text{RESET}}$ pin.

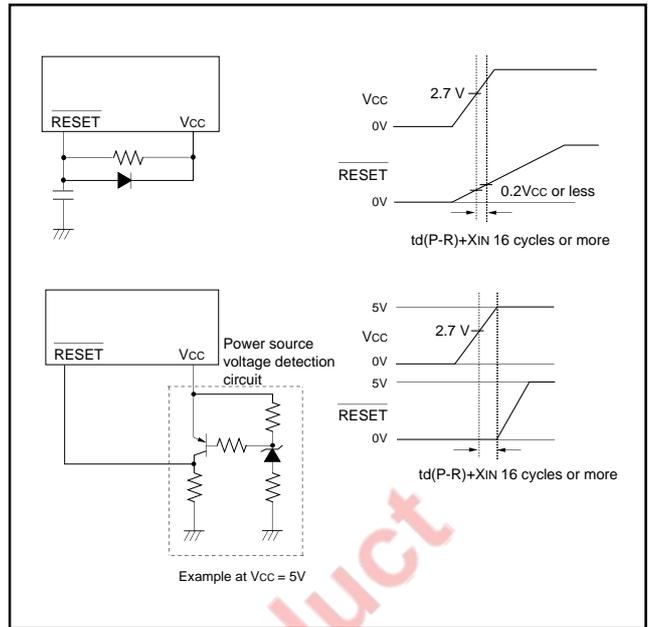


Fig. 70 Reset circuit example

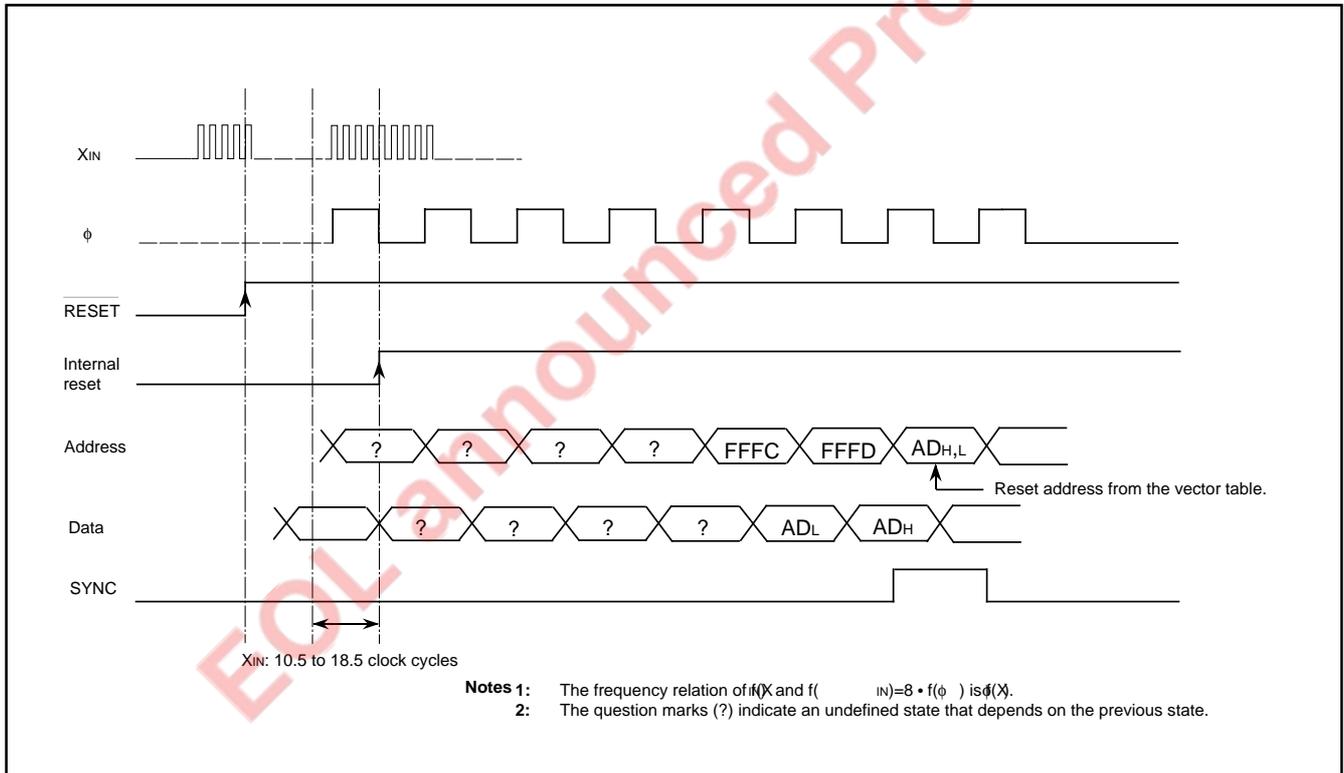


Fig. 71 Reset sequence

| | Address | Register contents | | Address | Register contents |
|---|--------------------|-------------------|---|-----------------------------|-------------------|
| (1) Port P0 (P0) | 0000 ₁₆ | 00 ₁₆ | (41) Timer Z (low-order) (TZL) | 0028 ₁₆ | FF ₁₆ |
| (2) Port P0 direction register (P0D) | 0001 ₁₆ | 00 ₁₆ | (42) Timer Z (high-order) (TZH) | 0029 ₁₆ | FF ₁₆ |
| (3) Port P1 (P1) | 0002 ₁₆ | 00 ₁₆ | (43) Timer Z mode register (TZM) | 002A ₁₆ | 00 ₁₆ |
| (4) Port P1 direction register (P1D) | 0003 ₁₆ | 00 ₁₆ | (44) PWM control register (PWMCON) | 002B ₁₆ | 00 ₁₆ |
| (5) Port P2 (P2) | 0004 ₁₆ | 00 ₁₆ | (45) PWM prescaler (PREPWM) | 002C ₁₆ | X X X X X X X X |
| (6) Port P2 direction register (P2D) | 0005 ₁₆ | 00 ₁₆ | (46) PWM register (PWM) | 002D ₁₆ | X X X X X X X X |
| (7) Port P3 (P3) | 0006 ₁₆ | 00 ₁₆ | (47) Baud rate generator 3 (BRG3) | 002F ₁₆ | X X X X X X X X |
| (8) Port P3 direction register (P3D) | 0007 ₁₆ | 00 ₁₆ | (48) Transmit/Receive buffer register 3 (TB3/RB3) | 0030 ₁₆ | X X X X X X X X |
| (9) Port P4 (P4) | 0008 ₁₆ | 00 ₁₆ | (49) Serial I/O3 status register (SIO3STS) | 0031 ₁₆ | 1 0 0 0 0 0 0 0 |
| (10) Port P4 direction register (P4D) | 0009 ₁₆ | 00 ₁₆ | (50) Serial I/O3 control register (SIO3CON) | 0032 ₁₆ | 00 ₁₆ |
| (11) Port P5 (P5) | 000A ₁₆ | 00 ₁₆ | (51) UART3 control register (UART3CON) | 0033 ₁₆ | 1 1 1 0 0 0 0 0 |
| (12) Port P5 direction register (P5D) | 000B ₁₆ | 00 ₁₆ | (52) AD/DA control register (ADCON) | 0034 ₁₆ | 0 0 0 0 1 0 0 0 |
| (13) Port P6 (P6) | 000C ₁₆ | 00 ₁₆ | (53) AD conversion register 1 (AD1) | 0035 ₁₆ | X X X X X X X X |
| (14) Port P6 direction register (P6D) | 000D ₁₆ | 00 ₁₆ | (54) DA1 conversion register (DA1) | 0036 ₁₆ | 00 ₁₆ |
| (15) Timer 12, X count source selection register (T12XCSS) | 000E ₁₆ | 0 0 1 1 0 0 1 1 | (55) DA2 conversion register (DA2) | 0037 ₁₆ | 00 ₁₆ |
| (16) Timer Y, Z count source selection register (TYZCSS) | 000F ₁₆ | 0 0 1 1 0 0 1 1 | (56) AD conversion register 2 (AD2) | 0038 ₁₆ | 0 0 0 0 0 0 X X |
| (17) MISRG | 0010 ₁₆ | 00 ₁₆ | (57) Interrupt source selection register (INTSEL) | 0039 ₁₆ | 00 ₁₆ |
| (18) I ² C data shift register (S0) | 0011 ₁₆ | X X X X X X X X | (58) Interrupt edge selection register (INTEGE) | 003A ₁₆ | 00 ₁₆ |
| (19) I ² C special mode status register (S3) | 0012 ₁₆ | 0 0 1 0 0 0 0 0 | (59) CPU mode register (CPUM) | 003B ₁₆ | 0 1 0 0 1 0 0 0 |
| (20) I ² C status register (S1) | 0013 ₁₆ | 0 0 0 1 0 0 0 X | (60) Interrupt request register 1 (IREQ1) | 003C ₁₆ | 00 ₁₆ |
| (21) I ² C control register (S1D) | 0014 ₁₆ | 00 ₁₆ | (61) Interrupt request register 2 (IREQ2) | 003D ₁₆ | 00 ₁₆ |
| (22) I ² C clock control register (S2) | 0015 ₁₆ | 00 ₁₆ | (62) Interrupt control register 1 (ICON1) | 003E ₁₆ | 00 ₁₆ |
| (23) I ² C START/STOP condition control register (S2D) | 0016 ₁₆ | 0 0 0 1 1 0 1 0 | (63) Interrupt control register 2 (ICON2) | 003F ₁₆ | 00 ₁₆ |
| (24) I ² C special mode control register (S3D) | 0017 ₁₆ | 00 ₁₆ | (64) Flash memory control register 0 (FMCR0) | 0FE0 ₁₆ | 01 ₁₆ |
| (25) Transmit/Receive buffer register 1 (TB1/RB1) | 0018 ₁₆ | X X X X X X X X | (65) Flash memory control register 1 (FMCR1) | 0FE1 ₁₆ | 40 ₁₆ |
| (26) Serial I/O1 status register (SIO1STS) | 0019 ₁₆ | 1 0 0 0 0 0 0 0 | (66) Flash memory control register 2 (FMCR2) | 0FE2 ₁₆ | 45 ₁₆ |
| (27) Serial I/O1 control register (SIO1CON) | 001A ₁₆ | 00 ₁₆ | (67) Port P0 pull-up control register (PULL0) | 0FF0 ₁₆ | 00 ₁₆ |
| (28) UART1 control register (UART1CON) | 001B ₁₆ | 1 1 1 0 0 0 0 0 | (68) Port P1 pull-up control register (PULL1) | 0FF1 ₁₆ | 00 ₁₆ |
| (29) Baud rate generator 1 (BRG1) | 001C ₁₆ | X X X X X X X X | (69) Port P2 pull-up control register (PULL2) | 0FF2 ₁₆ | 00 ₁₆ |
| (30) Serial I/O2 control register (SIO2CON) | 001D ₁₆ | 00 ₁₆ | (70) Port P3 pull-up control register (PULL3) | 0FF3 ₁₆ | 00 ₁₆ |
| (31) Watchdog timer control register (WDTCON) | 001E ₁₆ | 0 0 1 1 1 1 1 1 | (71) Port P4 pull-up control register (PULL4) | 0FF4 ₁₆ | 00 ₁₆ |
| (32) Serial I/O2 register (SIO2) | 001F ₁₆ | X X X X X X X X | (72) Port P5 pull-up control register (PULL5) | 0FF5 ₁₆ | 00 ₁₆ |
| (33) Prescaler 12 (PRE12) | 0020 ₁₆ | FF ₁₆ | (73) Port P6 pull-up control register (PULL6) | 0FF6 ₁₆ | 00 ₁₆ |
| (34) Timer 1 (T1) | 0021 ₁₆ | 01 ₁₆ | (74) I ² C slave address register 0 (S0D0) | 0FF7 ₁₆ | 00 ₁₆ |
| (35) Timer 2 (T2) | 0022 ₁₆ | FF ₁₆ | (75) I ² C slave address register 1 (S0D1) | 0FF8 ₁₆ | 00 ₁₆ |
| (36) Timer XY mode register (TM) | 0023 ₁₆ | 00 ₁₆ | (76) I ² C slave address register 2 (S0D3) | 0FF9 ₁₆ | 00 ₁₆ |
| (37) Prescaler X (PREX) | 0024 ₁₆ | FF ₁₆ | (77) Processor status register (PS) | X X X X X 1 X X | |
| (38) Timer X (TX) | 0025 ₁₆ | FF ₁₆ | Program counter (PC _H) | FFFF ₁₆ contents | |
| (39) Prescaler Y (PREY) | 0026 ₁₆ | FF ₁₆ | (PC _L) | FFFC ₁₆ contents | |
| (40) Timer Y (TY) | 0027 ₁₆ | FF ₁₆ | | | |

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 72 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3804 group (Spec. H) has two built-in oscillation circuits: main clock X_{IN}-X_{OUT} oscillation circuit and sub clock X_{CIN}-X_{COU}T oscillation circuit. An oscillation circuit can be formed by connecting a resonator between X_{IN} and X_{OUT} (X_{CIN} and X_{COU}T). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between X_{IN} and X_{OUT} since a feed-back resistor exists on-chip. (An external feed-back resistor may be needed depending on conditions.) However, an external feed-back resistor is needed between X_{CIN} and X_{COU}T.

Immediately after power on, only the X_{IN} oscillation circuit starts oscillating, and X_{CIN} and X_{COU}T pins function as I/O ports.

Frequency Control

(1) Middle-speed mode

The internal clock ϕ is the frequency of X_{IN} divided by 8. After reset is released, this mode is selected.

(2) High-speed mode

The internal clock ϕ is half the frequency of X_{IN}.

(3) Low-speed mode

The internal clock ϕ is half the frequency of X_{CIN}.

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock X_{IN} in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock X_{IN} is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the internal clock ϕ stops at an "H" level, and X_{IN} and X_{CIN} oscillators stop. When the oscillation stabilizing time set after STP instruction released bit is "0", the prescaler 12 is set to FF₁₆" and timer 1 is set to 01₁₆." When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.

After STP instruction is released, the input of the prescaler 12 is connected to count source which had set at executing the STP instruction, and the output of the prescaler 12 is connected to timer 1. Set the timer 1 interrupt enable bit to disabled ("0") before executing the STP instruction. Oscillator restarts when an external interrupt is received, but the internal clock ϕ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock ϕ is supplied for the first time, when timer 1 underflows. Therefore make sure not to set the timer 1 interrupt request bit to "1" before the STP instruction stops the oscillator. When the oscillator is restarted by reset, apply "L" level to the RESET pin until the oscillation is stable since a wait time will not be generated.

The internal power supply circuit is changed to low power consumption mode for consumption current reduction at the time of STP instruction execution.

Although an internal power supply circuit is usually changed to the normal operation mode at the time of the return from an STP instruction, since a certain time is required to start the power supply to the flash memory and operation of flash memory to be enabled, set wait time 100 μ s or more by the oscillation stabilization time set function after release of the STP instruction which used the timer 1.

(2) Wait mode

If the WIT instruction is executed, the internal clock ϕ stops at an "H" level, but the oscillator does not stop. The internal clock ϕ restarts when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.

■Note

- If you switch the mode between middle/high-speed and low-speed, stabilize both X_{IN} and X_{CIN} oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after power on and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that $f(X_{IN}) > 3f(X_{CIN})$.
- When using the quartz-crystal oscillator of high frequency, such as 16 MHz etc., it may be necessary to select a specific oscillator with the specification demanded.

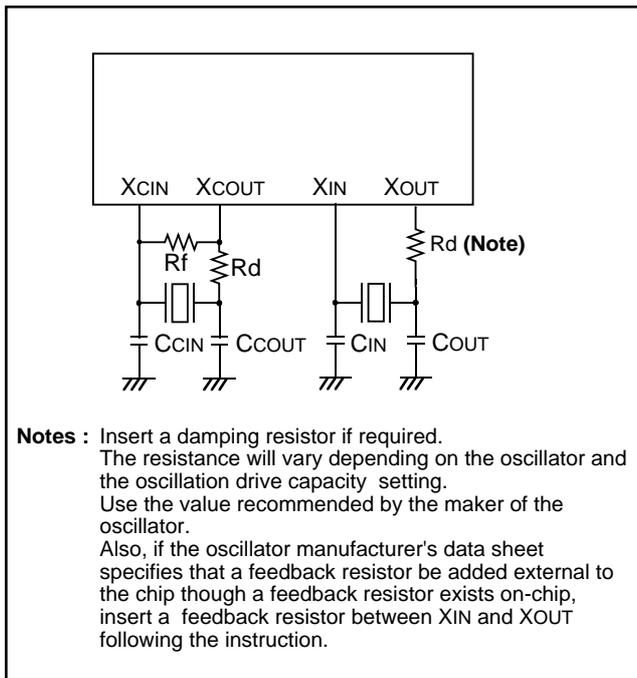


Fig. 73 Ceramic resonator circuit

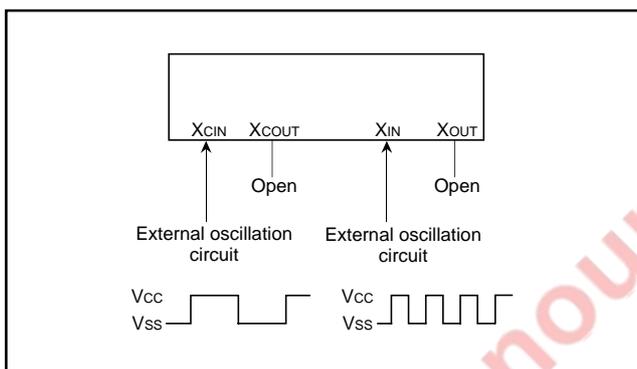


Fig. 74 External clock input circuit

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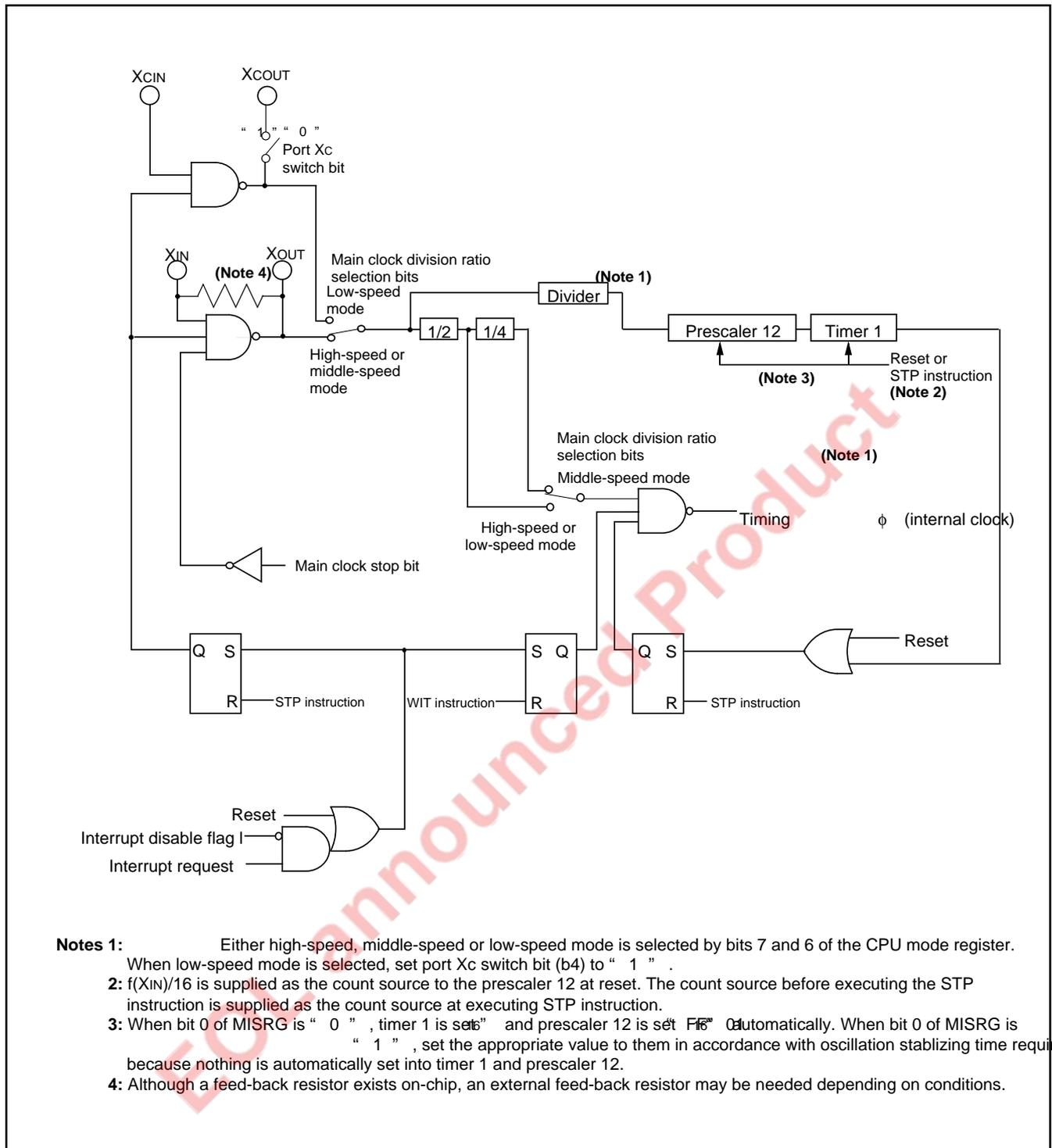


Fig. 75 System clock generating circuit block diagram

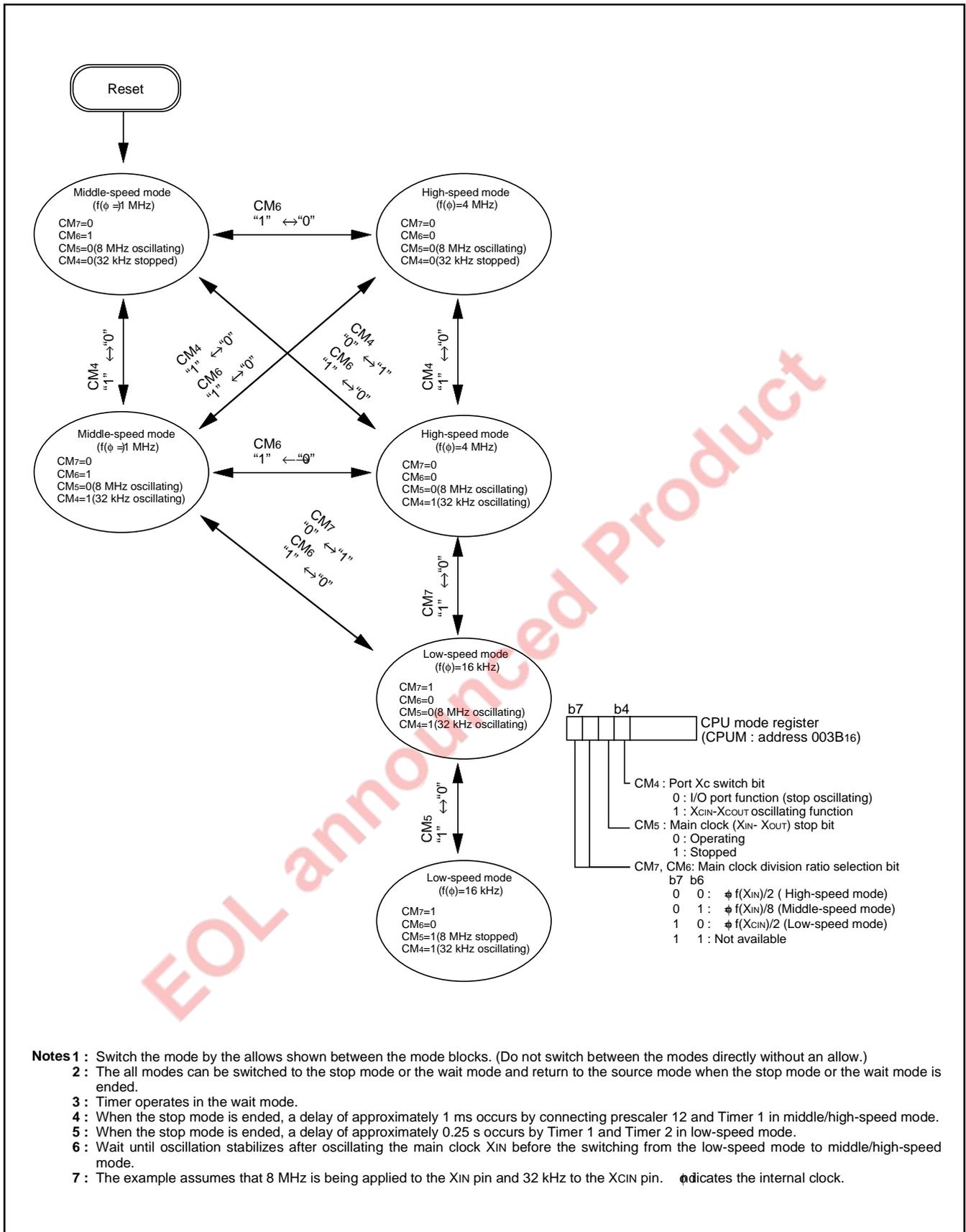


Fig. 76 State transitions of system clock

- Notes 1 :** Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)
2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.
3 : Timer operates in the wait mode.
4 : When the stop mode is ended, a delay of approximately 1 ms occurs by connecting prescaler 12 and Timer 1 in middle/high-speed mode.
5 : When the stop mode is ended, a delay of approximately 0.25 s occurs by Timer 1 and Timer 2 in low-speed mode.
6 : Wait until oscillation stabilizes after oscillating the main clock XIN before the switching from the low-speed mode to middle/high-speed mode.
7 : The example assumes that 8 MHz is being applied to the XIN pin and 32 kHz to the XCIN pin. φ indicates the internal clock.

FLASH MEMORY MODE

The 3804 group (spec. H) has the flash memory that can be re-written with a single power source.

For this flash memory, three flash memory modes are available in which to read, program, and erase: the parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU).

This flash memory has some blocks on it as shown in Figure 77 and each block can be erased.

In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

● Summary

Table 13 lists the summary of the 3804 Group (spec. H).

Table 13 Summary of 3804 group (spec. H)

| Item | | Specifications |
|---------------------------------|-----------------------------|--|
| Power source voltage (Vcc) | | VCC = 2.7 to 5.5 V |
| Program/Erase VPP voltage (VPP) | | VCC = 2.7 to 5.5 V |
| Flash memory mode | | 3 modes; Parallel I/O mode, Standard serial I/O mode, CPU rewrite mode |
| Erase block division | User ROM area/Data ROM area | Refer to Fig. 77. |
| | Boot ROM area (Note) | Not divided (4K bytes) |
| Program method | | In units of bytes |
| Erase method | | Block erase |
| Program/Erase control method | | Program/Erase control by software command |
| Number of commands | | 5 commands |
| Number of program/Erase times | | 100 |
| ROM code protection | | Available in parallel I/O mode and standard serial I/O mode |

Note: The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. This Boot ROM area can be erased and written in only parallel I/O mode.

● **Boot Mode**

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)

See Figure 77 for details about the Boot ROM area.

Normal microcomputer mode is entered when the microcomputer is reset with pulling CNVss pin low. In this case, the CPU starts operating using the control program in the User ROM area.

When the microcomputer is reset and the CNVss pin high after pulling the P45/TxD1 pin and CNVss pin high, the CPU starts operating (start address of program is stored into addresses FFFC16 and FFFD16) using the control program in the Boot ROM area. This mode is called the "Boot mode". Also, User ROM area can be rewritten using the control program in the Boot ROM area.

● **CPU Rewrite Mode**

In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).

In CPU rewrite mode, only the User ROM area shown in Figure 77 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.

The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area before it can be executed.

● **Block Address**

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command.

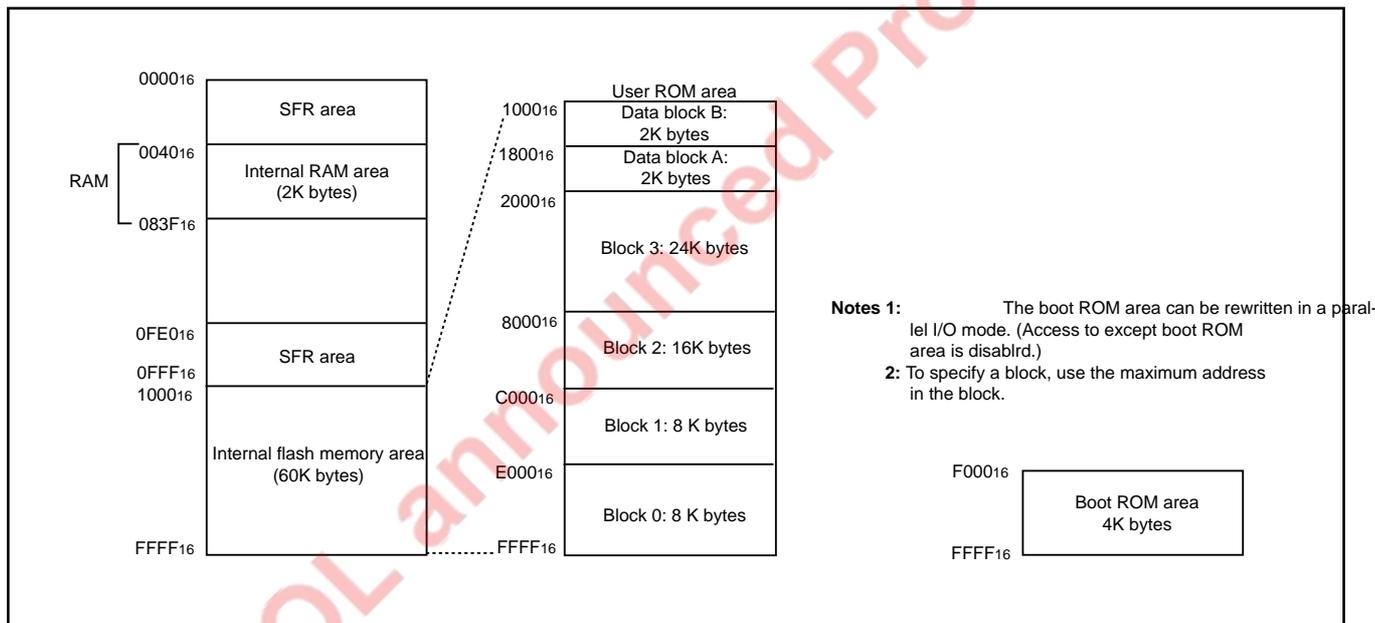


Fig. 77 Block diagram of built-in flash memory

●Outline Performance

CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten.

In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory as instructed by software commands. This rewrite control program must be transferred to internal RAM area before it can be executed.

The MCU enters CPU rewrite mode by setting "1" to the CPU rewrite mode select bit (bit 1 of address 0FE016). Then, software commands can be accepted.

Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 78 shows the flash memory control register 0.

Bit 0 of the flash memory control register 0 is the RY/BY status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is "0" (busy). Otherwise, it is "1" (ready).

Bit 1 of the flash memory control register 0 is the CPU rewrite mode select bit. When this bit is set to "1", the MCU enters CPU rewrite mode. And then, software commands can be accepted. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the internal RAM for write to bit 1. To set this bit 1 to "1", it is necessary to write "0" and then write "1" in succession to bit 1. The bit can be set to "0" by only writing "0".

Bit 2 of the flash memory control register 0 is the 8 KB user block E/W enable bit. By setting combination of bit 4 of the flash memory control register 2 and this bit as shown in Table 14, E/W is disabled to user block in the CPU rewriting mode.

Bit 3 of the flash memory control register 0 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when flash memory access has failed. When the CPU rewrite mode select bit is "1", setting "1" for this bit resets the control circuit. To release the reset, it is necessary to set this bit to "0".

Bit 5 of the flash memory control register 0 is the User ROM area select bit and is valid only in the boot mode. Setting this bit to "1" in the boot mode switches an accessible area from the boot ROM area to the user ROM area. To use the CPU rewrite mode in the boot mode, set this bit to "1". To rewrite bit 5, execute the user-original reprogramming control software transferred to the internal RAM in advance.

Bit 6 of the flash memory control register 0 is the program status flag. This bit is set to "1" when writing to flash memory is failed. When program error occurs, the block cannot be used.

Bit 7 of the flash memory control register 0 is the erase status flag. This bit is set to "1" when erasing flash memory is failed. When erase error occurs, the block cannot be used.

Figure 79 shows the flash memory control register 1.

Bit 0 of the flash memory control register 1 is the Erase suspend enable bit. By setting this bit to "1", the erase suspend mode to suspend erase processing temporarily when block erase command is executed can be used. In order to set this bit to "1", writing "0" and "1" in succession to bit 0. In order to set this bit to "0", write "0" only to bit 0.

Bit 1 of the flash memory control register 1 is the erase suspend request bit. By setting this bit to "1" when erase suspend enable bit is "1", the erase processing is suspended.

Bit 6 of the flash memory control register 1 is the erase suspend flag. This bit is cleared to "0" at the flash erasing.

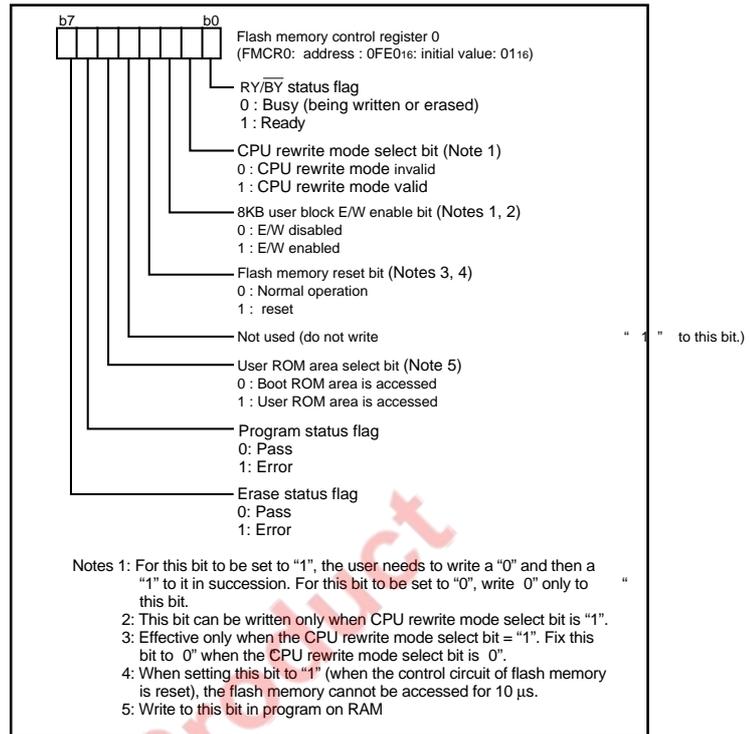


Fig. 78 Structure of flash memory control register 0

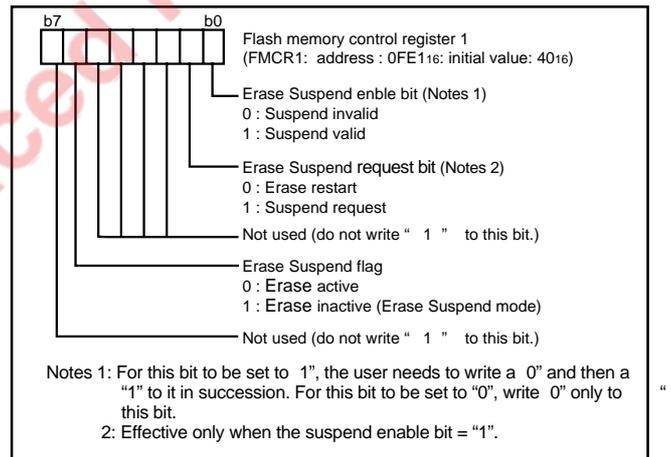
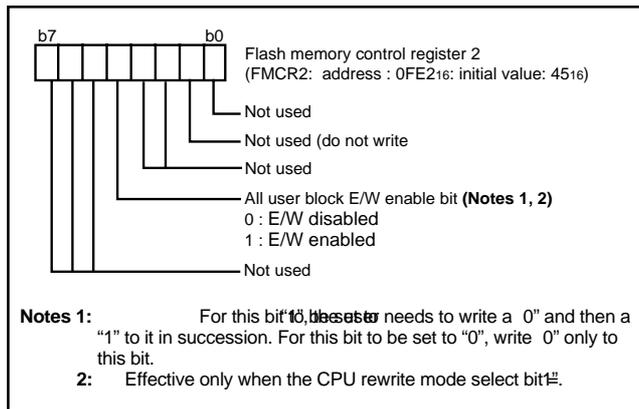


Fig. 79 Structure of flash memory control register 1



" 1 " to this bit.)

Fig. 80 Structure of flash memory control register 2

Table 14 State of E/W inhibition function

| All user block E/W enable bit | 8 KB user block E/W enable bit | 8 KB X 2 block Addresses C000 ₁₆ to FFFF ₁₆ | 16 KB + 24 KB block Addresses 2000 ₁₆ to BFFF ₁₆ | Data block Addresses 1000 ₁₆ to 1FFF ₁₆ |
|-------------------------------|--------------------------------|--|---|--|
| 0 | 0 | E/W disabled | E/W disabled | E/W enabled |
| 0 | 1 | E/W disabled | E/W disabled | E/W enabled |
| 1 | 0 | E/W disabled | E/W enabled | E/W enabled |
| 1 | 1 | E/W enabled | E/W enabled | E/W enabled |

Figure 81 shows a flowchart for setting/releasing CPU rewrite mode.

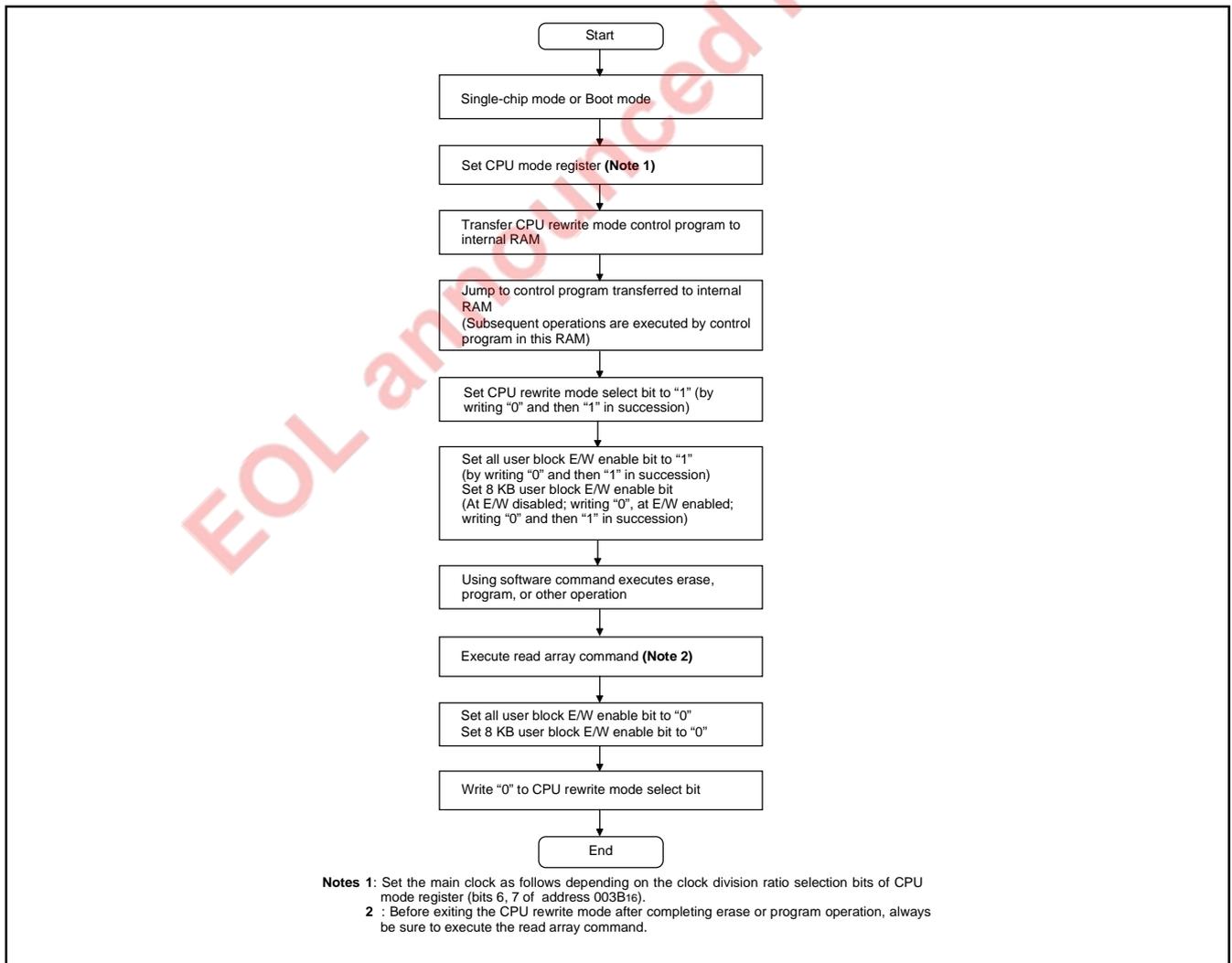


Fig. 81 CPU rewrite mode set/release flowchart

■ Notes on CPU Rewrite Mode

Take the notes described below when rewriting the flash memory in CPU rewrite mode.

● Operation speed

During CPU rewrite mode, set the system clock ϕ to 4.0 MHz or less using the clock division ratio selection bits (bits 6 and 7 of address 003B₁₆).

● Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode.

● Interrupts

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

● Watchdog timer

If the watchdog timer has been already activated, internal reset due to an underflow will not occur because the watchdog timer is surely cleared during program or erase.

● Reset

Reset is always valid. The MCU is activated using the boot mode at release of reset in the condition of CNV_{ss} = "H", so that the program will begin at the address which is stored in addresses FFFC₁₆ and FFFD₁₆ of the boot ROM area.

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● **Software Commands**

Table 15 lists the software commands.

After setting the CPU rewrite mode select bit to 1, execute a software command to specify an erase or program operation. Each software command is explained below.

• **Read Array Command (FF16)**

The read array mode is entered by writing the command code "FF16" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D0 to D7).

The read array mode is retained until another command is written.

• **Read Status Register Command (7016)**

When the command code 7016" is written in the first bus cycle, the contents of the status register are read out at the data bus (D0 to D7) by a read in the second bus cycle.

The status register is explained in the next section.

• **Clear Status Register Command (5016)**

This command is used to clear the bits SR4 and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code 5016" in the first bus cycle.

• **Program Command (4016)**

Program operation starts when the command code "4016" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.

Whether the write operation is completed can be confirmed by read status register or the RY/BY status flag. When the program starts, the read status register mode is entered automatically and the contents of the status register is read at the data bus (D0 to D7). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the read array command (FF16) is written.

The RY/BY status flag of the flash memory control register is "0" during write operation and 1" when the write operation is completed as is the status register bit 7.

At program end, program results can be checked by reading the status register.

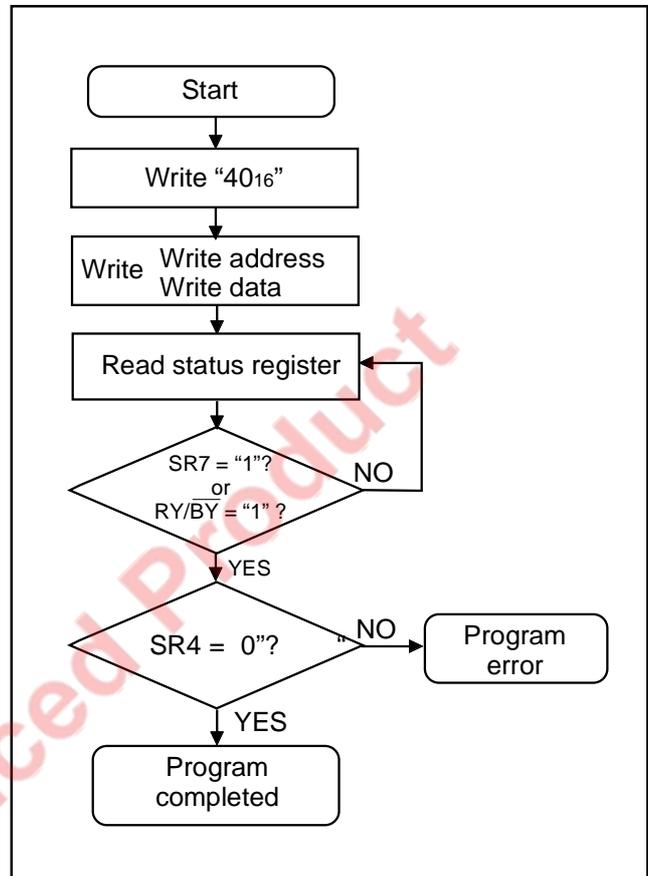


Fig. 82 Program flowchart

Table 15 List of software commands (CPU rewrite mode)

| Command | Cycle number | First bus cycle | | | Second bus cycle | | |
|-----------------------|--------------|-----------------|------------|-----------------|------------------|-------------|-----------------|
| | | Mode | Address | Data (D0 to D7) | Mode | Address | Data (D0 to D7) |
| Read array | 1 | Write | X (Note 4) | FF16 | | | |
| Read status register | 2 | Write | X | 7016 | Read | X | SRD (Note 1) |
| Clear status register | 1 | Write | X | 5016 | | | |
| Program | 2 | Write | X | 4016 | Write | WA (Note 2) | WD (Note 2) |
| Block erase | 2 | Write | X | 2016 | Write | BA (Note 3) | D016 |

Notes 1: SRD = Status Register Data

2: WA = Write Address, WD = Write Data

3: BA = Block Address to be erased (Input the maximum address of each block.)

4: X denotes a given address in the User ROM area.

• Block Erase Command (20₁₆/D0₁₆)

By writing the command code "20₁₆" in the first bus cycle and the confirmation command code "D0₁₆" and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.

Whether the block erase operation is completed can be confirmed by read status register or the RY/B \bar{Y} status flag of flash memory control register. At the same time the block erase operation starts, the read status register mode is automatically entered, so that the contents of the status register can be read out. The status register bit 7 (SR7) is set to "0" at the same time the block erase operation starts and is returned to "1" upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF₁₆) is written.

The RY/B \bar{Y} status flag is 0 during block erase operation and 1 when the block erase operation is completed as is the status register bit 7.

After the block erase ends, erase results can be checked by reading the status register. For details, refer to the section where the status register is detailed.

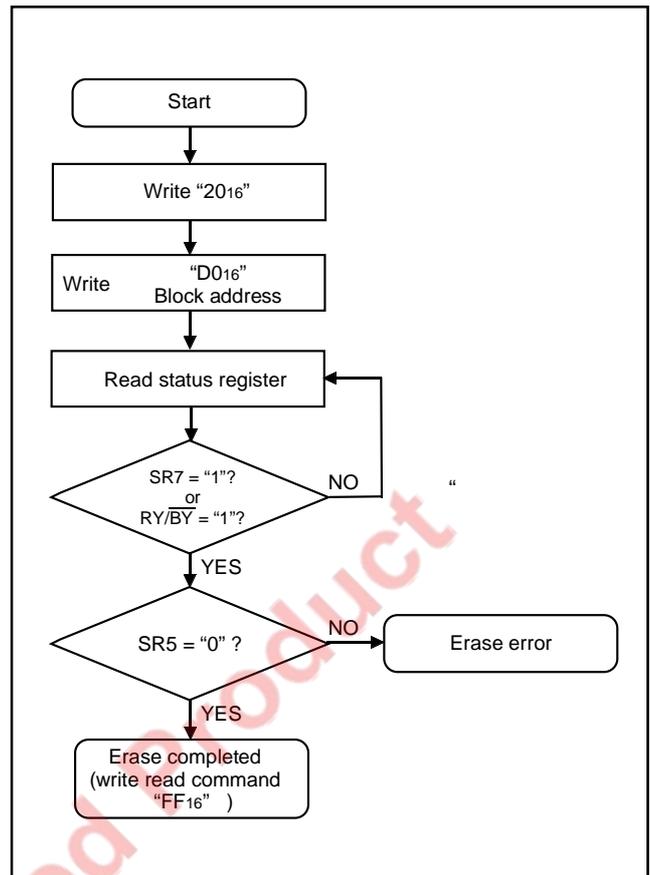


Fig. 83 Erase flowchart

● Status Register

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways:

- (1) By reading an arbitrary address from the User ROM area after writing the read status register command (70₁₆)
- (2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF₁₆) is input.

Also, the status register can be cleared by writing the clear status register command (50₁₆).

After reset, the status register is set to "80₁₆".

Table 16 shows the status register. Each bit in this register is explained below.

•Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. This bit is set to "0" (busy) during write or erase operation and is set to "1" when these operations ends.

After power-on, the sequencer status is set to "1" (ready).

•Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is reset to "0".

•Program status (SR4)

The program status indicates the operating status of write operation. When a write error occurs, it is set to "1".

The program status is reset to "0" when it is cleared.

If "1" is written for any of the SR5 and SR4 bits, the read array, program, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50₁₆) and clear the status register.

Also, if any commands are not correct, both SR5 and SR4 are set to "1".

Table 16 Definition of each bit in status register

| Each bit of SRD bits | Status name | Definition | |
|----------------------|------------------|---------------------|---------------------|
| | | "1" | "0" |
| SR7 (bit7) | Sequencer status | Ready | Busy |
| SR6 (bit6) | Reserved | - | - |
| SR5 (bit5) | Erase status | Terminated in error | Terminated normally |
| SR4 (bit4) | Program status | Terminated in error | Terminated normally |
| SR3 (bit3) | Reserved | - | - |
| SR2 (bit2) | Reserved | - | - |
| SR1 (bit1) | Reserved | - | - |
| SR0 (bit0) | Reserved | - | - |

● Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 84 shows a full status check flowchart and the action to be taken when each error occurs.

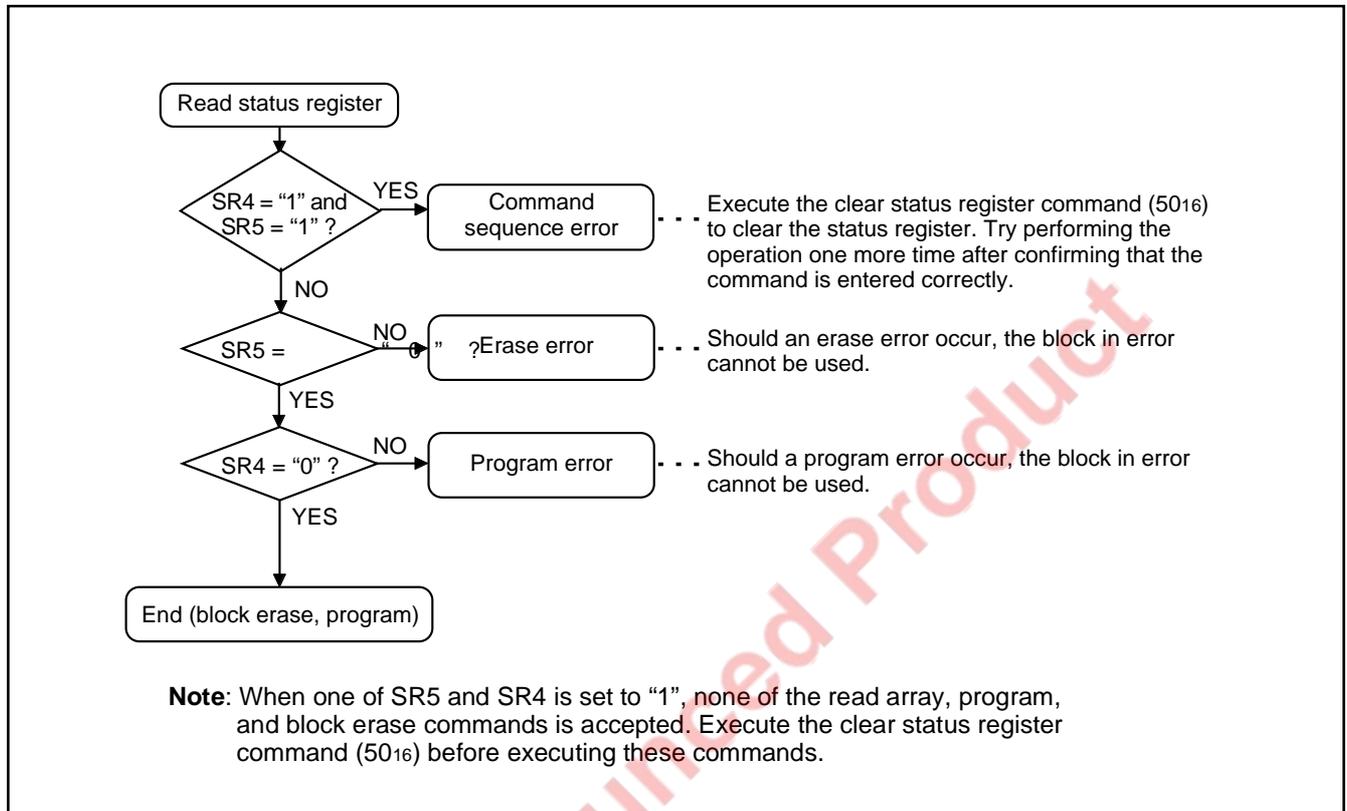


Fig. 84 Full status check flowchart and remedial procedure for errors

● Functions To Inhibit Rewriting Flash Memory Version

To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

(1) ROM Code Protect Function

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control address (address FFDB₁₆) in parallel I/O mode. Figure 85 shows the ROM code protect control address (address FFDB₁₆). (This address exists in the User ROM area.)

If one or both of the pair of ROM code protect bits is set to 0, the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM code protect reset bits are set to 00, the ROM code protect is turned off, so that the contents of internal flash memory can be readout or modified. Once the ROM code protect is turned on, the contents of the ROM code protect reset bits cannot be modified in parallel I/O mode. Use the serial I/O or CPU rewrite mode to rewrite the contents of the ROM code protect reset bits.

Rewriting of only the ROM code protect control address (address FFDB₁₆) cannot be performed. When rewriting the ROM code protect reset bit, rewrite the whole user ROM area (block 0) containing the ROM code protect control address.

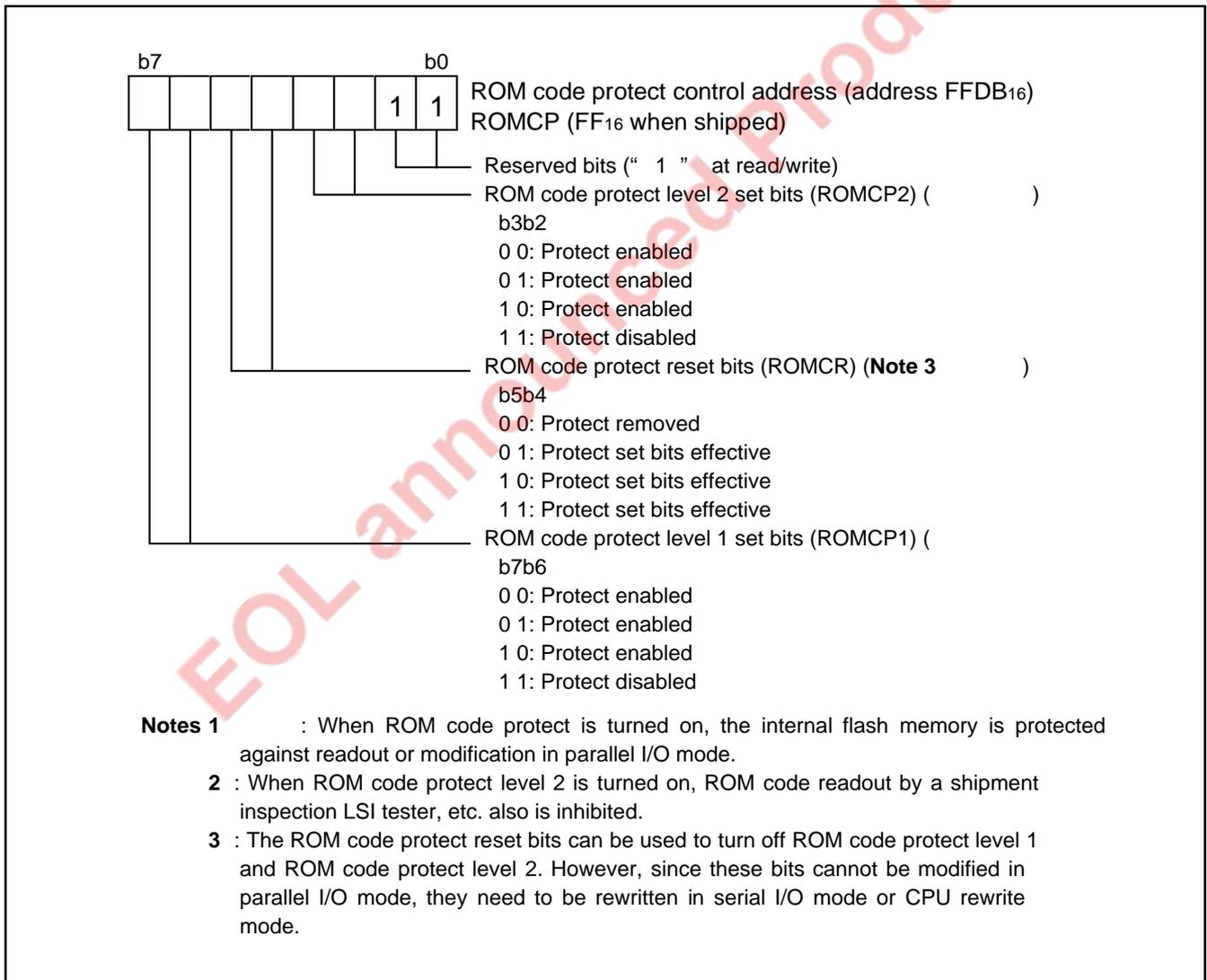


Fig. 85 Structure of ROM code protect control address

(2) ID Code Check Function

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are FFD4₁₆ to FFDA₁₆. Write a program which has had the ID code preset at these addresses to the flash memory.

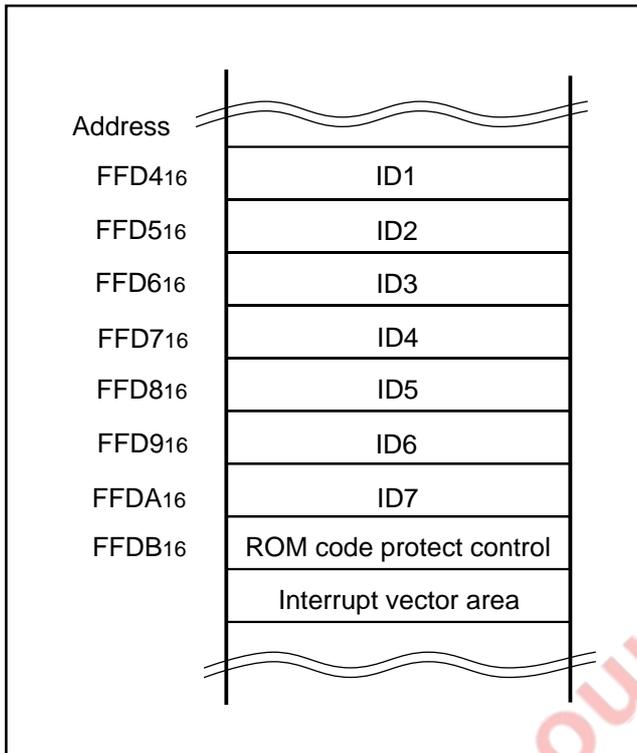


Fig. 86 ID code store addresses

● Parallel I/O Mode

The parallel I/O mode is used to input/output software commands, address and data in parallel for operation (read, program and erase) to internal flash memory.

Use the external device (writer) only for 3804 Group (spec. H). For details, refer to the user's manual of each writer manufacturer.

• User ROM and Boot ROM Areas

In parallel I/O mode, the User ROM and Boot ROM areas shown in Figure 77 can be rewritten. Both areas of flash memory can be operated on in the same way.

The Boot ROM area is 4 Kbytes in size and located at addresses F000₁₆ through FFFF₁₆. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)

In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. Therefore, using the MCU in standard serial I/O mode, do not rewrite to the Boot ROM area.

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● Standard serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires a purpose-specific peripheral unit.

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started by connecting "H" to the CNVss pin and "H" to the P45 (BOOTENT) pin, and releasing the reset operation. (In the ordinary microcomputer mode, set CNVss pin to "L" level.) This control program is written in the Boot ROM area when the product is shipped from Renesas. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. The standard serial I/O mode has standard serial I/O mode 1 of the clock synchronous serial and standard serial I/O mode 2 of the clock asynchronous serial. Tables 17 and 18 show description of pin function (standard serial I/O mode). Figures 87 to 90 show the pin connections for the standard serial I/O mode.

In standard serial I/O mode, only the User ROM area shown in Figure 77 can be rewritten. The Boot ROM area cannot be written. In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, this function determines whether the ID code sent from the peripheral unit (programmer) and those written in the flash memory match. The commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

EOL announced Product

Table 17 Description of pin function (Flash Memory Serial I/O Mode 1)

| Pin name | Signal name | I/O | Function |
|---|---------------------------|-----|---|
| Vcc,Vss | Power supply | I | Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the Vss pin. |
| CNVss | CNVss | I | After input of port is set, input "H" level. |
| RESET | Reset input | I | Reset input pin. To reset the microcomputer, RESET pin should be held at an "L" level for 16 cycles or more of XIN. |
| XIN | Clock input | I | Connect an oscillation circuit between the XIN and XOUT pins. |
| XOUT | Clock output | O | As for the connection method, refer to the "clock generating circuit . |
| AVss | Analog power supply input | | Connect AVss to Vss. |
| VREF | Reference voltage input | I | Apply reference voltage of A/D to this pin. |
| P00–P07,P10–P17, P20–P27,P30–P37, P40–P43,P50–P57, P60–P67 | I/O port | I/O | Input "L" or "H" level, or keep open. |
| P44 | RxD input | I | Serial data input pin. |
| P45 | TxD output | O | Serial data output pin. |
| P46 | SCLK input | I | Serial clock input pin. |
| P47 | BUSY output | O | BUSY signal output pin. |

Table 18 Description of pin function (Flash Memory Serial I/O Mode 2)

| Pin name | Signal name | I/O | Function |
|---|---------------------------|-----|---|
| Vcc,Vss | Power supply | I | Apply 2.7 to 5.5 V to the Vcc pin and 0 V to the Vss pin. |
| CNVss | CNVss | I | After input of port is set, input "H" level. |
| RESET | Reset input | I | Reset input pin. To reset the microcomputer, RESET pin should be held at an "L" level for 16 cycles or more of XIN. |
| XIN | Clock input | I | Connect an oscillation circuit between the XIN and XOUT pins. |
| XOUT | Clock output | O | As for the connection method, refer to the "clock generating circuit . |
| AVss | Analog power supply input | | Connect AVss to Vss. |
| VREF | Reference voltage input | I | Apply reference voltage of A/D to this pin. |
| P00–P07,P10–P17, P20–P27,P30–P37, P40–P43,P50–P57, P60–P67 | I/O port | I/O | Input "L" or "H" level, or keep open. |
| P44 | RxD input | I | Serial data input pin. |
| P45 | TxD output | O | Serial data output pin. |
| P46 | SCLK input | I | Input "L" level. " |
| P47 | BUSY output | O | BUSY signal output pin. |

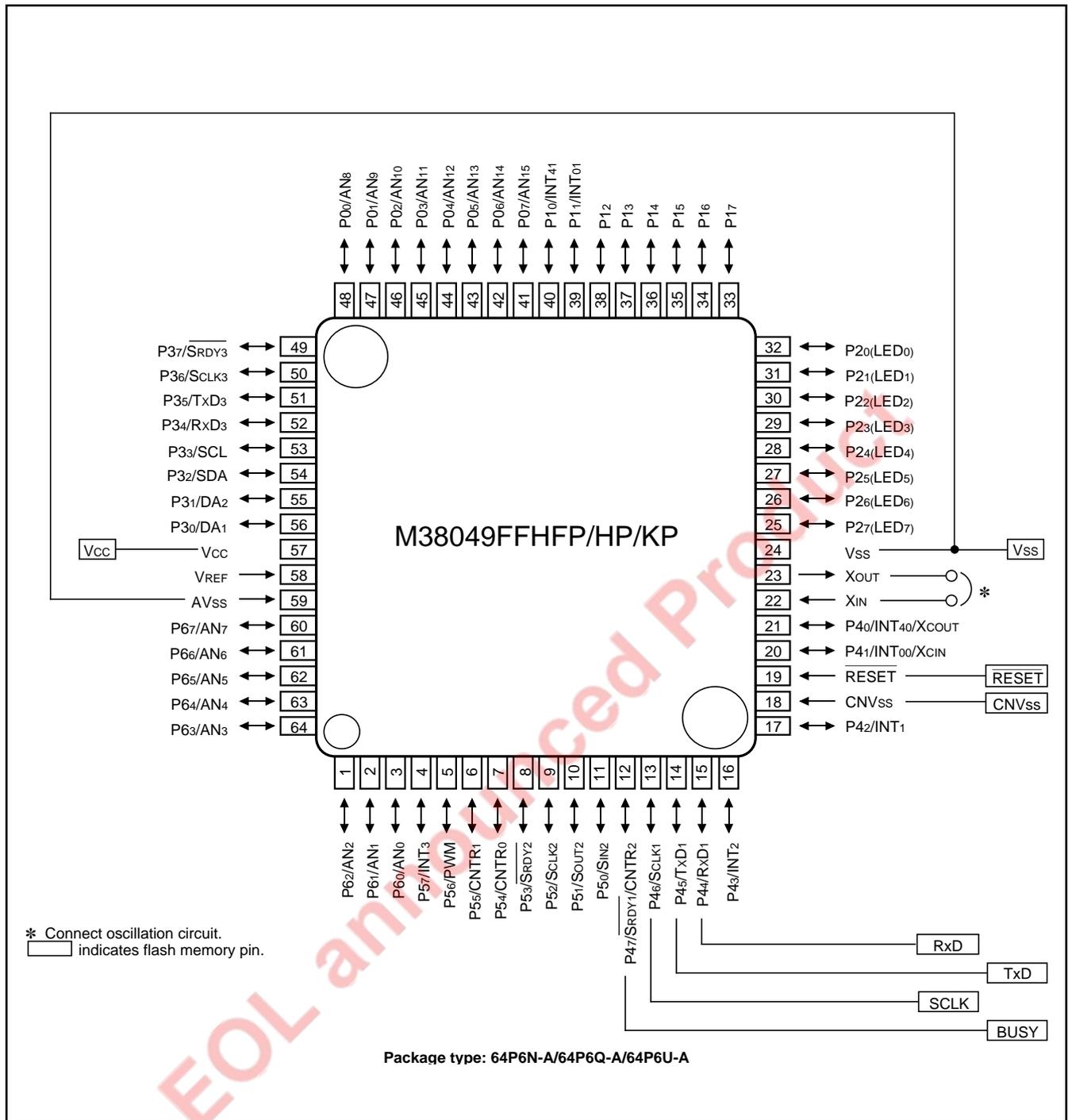


Fig. 87 Connection for standard serial I/O mode 1 (M38049FFHFP/HP/KP)

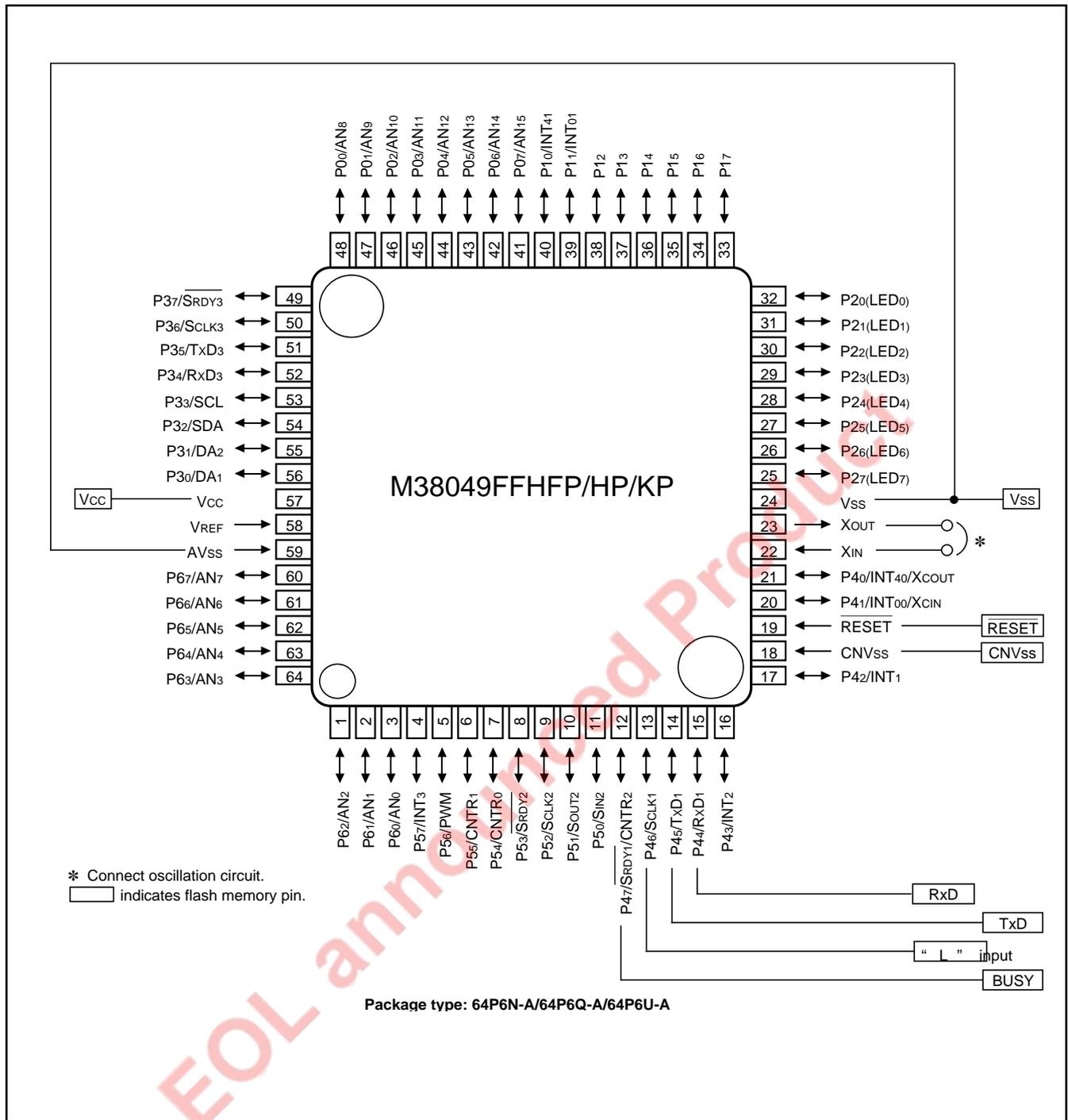


Fig. 88 Connection for standard serial I/O mode 2 (M38049FFHFP/HP/KP)

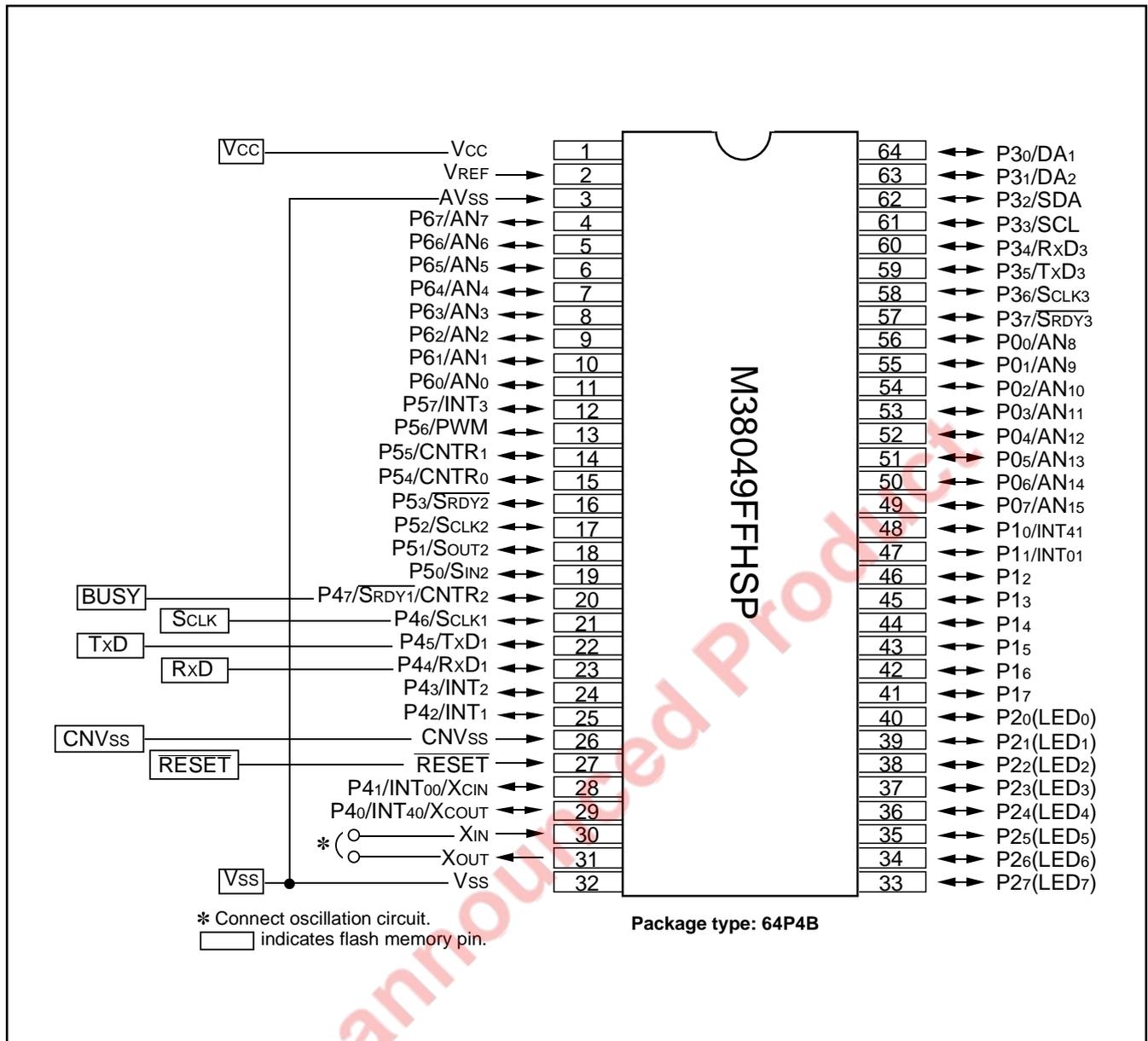


Fig. 89 Connection for standard serial I/O mode 1 (M38049FFHSP)

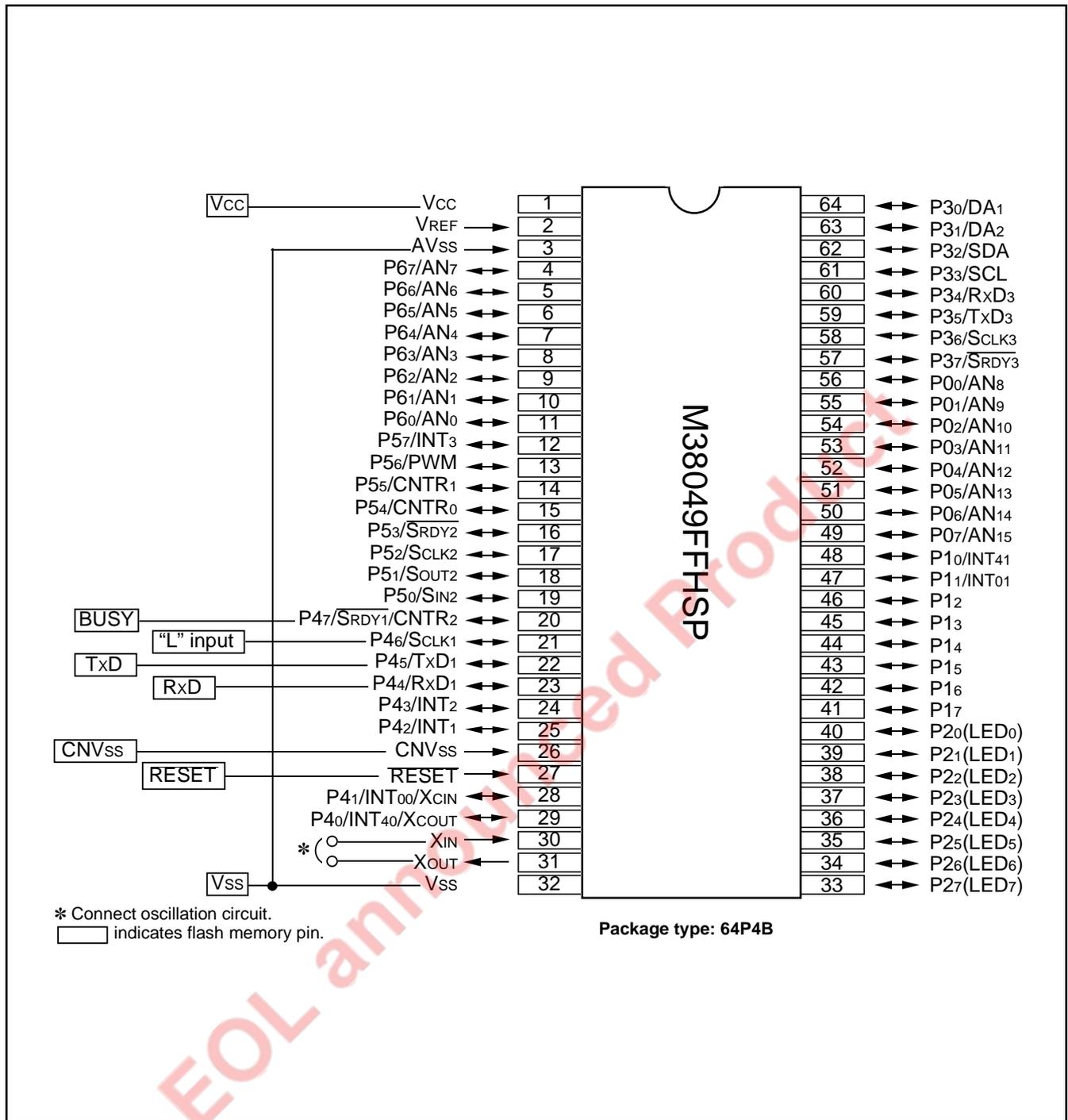


Fig. 90 Connection for standard serial I/O mode 2 (M38049FFHSP)

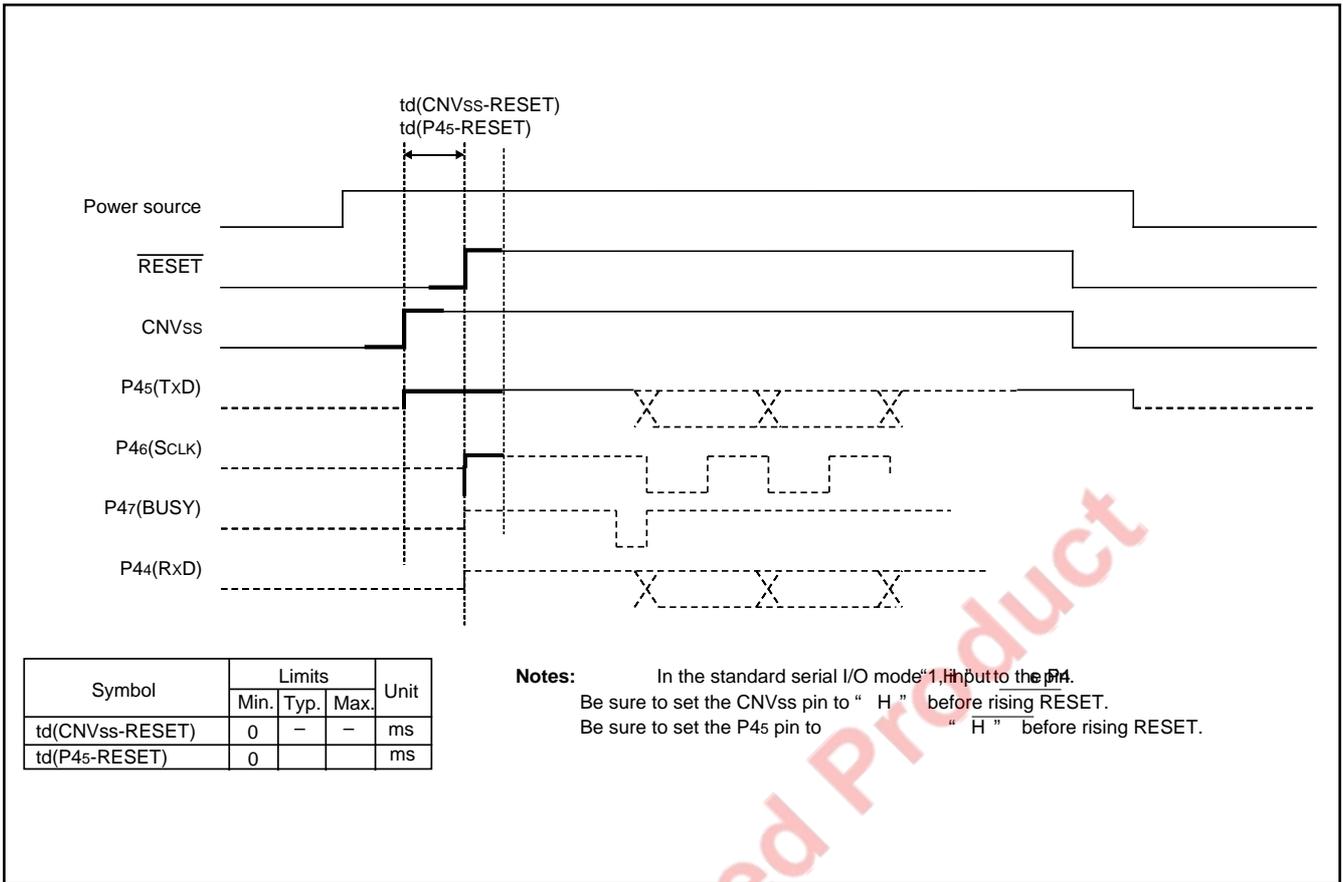


Fig. 91 Operating waveform for standard serial I/O mode 1

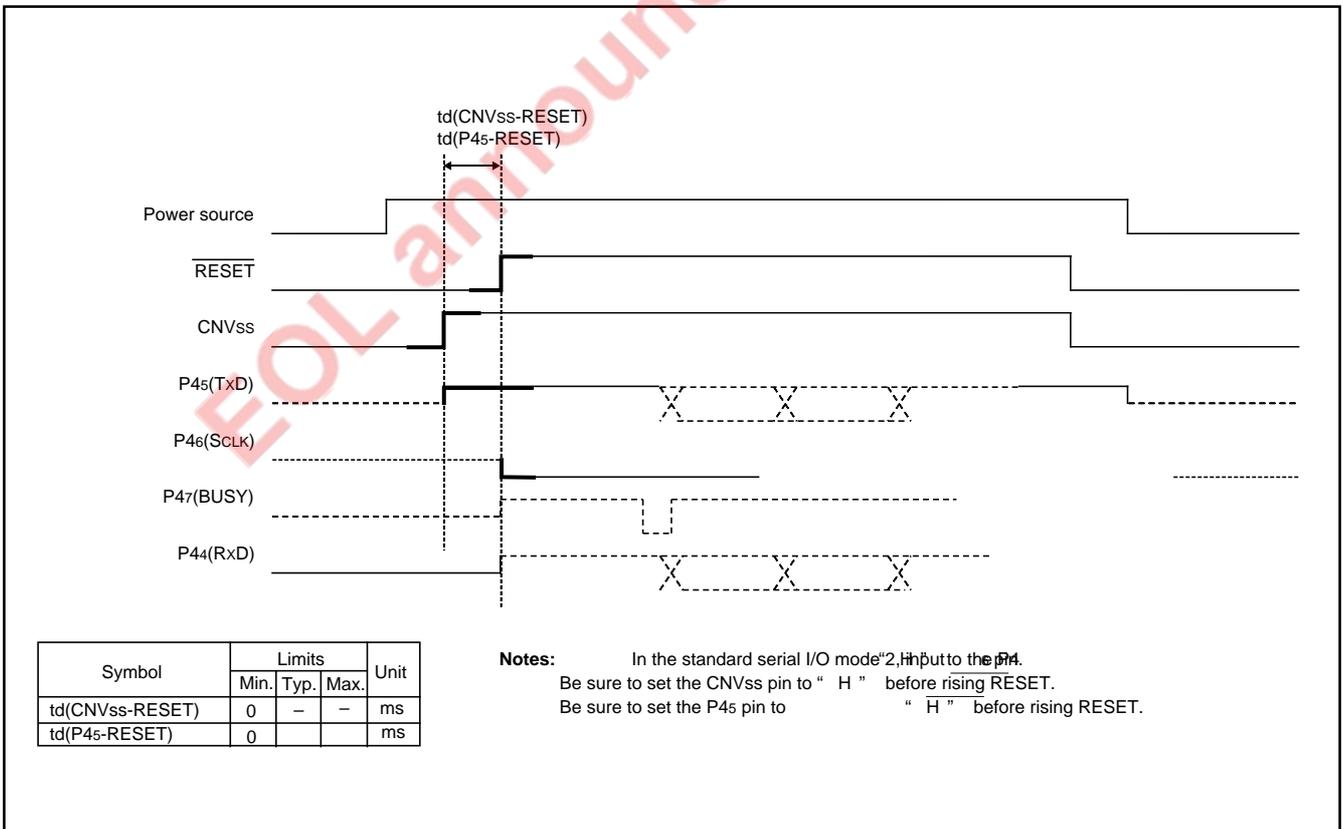


Fig. 92 Operating waveform for standard serial I/O mode 2

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is "1". After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to "1", then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is $1/(n+1)$.

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is "1"
- The instruction with the addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial Interface

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to "1".

Serial I/O continues to output the final bit from the TxD pin after transmission is completed. SOUT2 pin for serial I/O2 goes to high impedance after transfer is completed.

When in serial I/Os 1 and 3 (clock-synchronous mode) or in serial I/O2, an external clock is used as synchronous clock, write transmission data to the transmit buffer register or serial I/O2 register, during transfer clock is H.

A/D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that $f(\text{XIN})$ is at least on 500 kHz during an A/D conversion.

Do not execute the STP instruction during an A/D conversion.

D/A Converter

The accuracy of the D/A converter becomes rapidly poor under the $V_{CC} = 4.0$ V or less condition; a supply voltage of $V_{CC} \geq 4.0$ V is recommended. When a D/A converter is not used, set all values of D/A i conversion registers ($i=1, 2$) to "0016."

Instruction Execution Time

The instruction execution time is obtained by multiplying the period of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The period of the internal clock ϕ is double of the XIN period in high-speed mode.

NOTES ON USAGE

Handling of Power Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin), and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 μ F–0.1 μ F is recommended.

Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

Flash Memory Version

The CNVss pin determines the flash memory mode. To improve the noise reduction, connect a track between CNVss pin and Vss pin or Vcc pin with 1 to 10 k Ω resistance. The mask ROM version track of CNVss pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

Electric Characteristic Differences Between Mask ROM and Flash Memory Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation between Mask ROM and Flash Memory version MCUs due to the difference in the manufacturing processes, built-in ROM, and layout pattern etc. When manufacturing an application system with the Flash Memory version and then switching to use of the Mask ROM version, please conduct evaluations equivalent to the system evaluations conducted for the flash memory version.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

- 1.Mask ROM Confirmation Form *
- 2.Mark Specification Form *
- 3.Data to be written to ROM, in EPROM form (three identical copies)

* For the mask ROM confirmation and the mark specifications, refer to the Renesas Technology Corp.* Homepage (<http://www.renesas.com/en/rom>).

ELECTRICAL CHARACTERISTICS

Absolute maximum ratings

Table 19 Absolute maximum ratings

| Symbol | Parameter | Conditions | Ratings | Unit |
|------------------|--|--|------------------------------|-------------|
| V _{CC} | Power source voltages | All voltages are based on V _{SS} . Output transistors are cut off. | -0.3 to 6.5 | V |
| V _I | Input voltage P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67, V _{REF} | | -0.3 to V _{CC} +0.3 | V |
| V _I | Input voltage P32, P33 | | -0.3 to 5.8 | V |
| V _I | Input voltage RESET, X _{IN} | | -0.3 to V _{CC} +0.3 | V |
| V _I | Input voltage CNV _{SS} | | -0.3 to V _{CC} +0.3 | V |
| V _O | Output voltage P00-P07, P10-P17, P20-P27, P30, P31, P34-P37, P40-P47, P50-P57, P60-P67, X _{OUT} | | -0.3 to V _{CC} +0.3 | V |
| V _O | Output voltage P32, P33 | | -0.3 to 5.8 | V |
| P _d | Power dissipation | | T _a = 25 C ° | 1000 (Note) |
| T _{opr} | Operating temperature | | -20 to 85 | °C |
| T _{stg} | Storage temperature | | -65 to 125 | °C |

Note: This value is 300 mW except SP package.

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Recommended operating conditions

Table 20 Recommended operating conditions (1)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit | |
|---------------------------|--|--|---------------------------|------|---------------------|------|---|
| | | | Min. | Typ. | Max. | | |
| V _{CC} | Power source voltage (Note 1) | When start oscillating (Note 2) | 2.7 | 5.0 | 5.5 | V | |
| | | High-speed mode $f(\phi) = f(X_{IN})/2$ | $f(X_{IN}) \leq 8.4$ MHz | 2.7 | 5.0 | 5.5 | V |
| | | | $f(X_{IN}) \leq 12.5$ MHz | 4.0 | 5.0 | 5.5 | V |
| | | | $f(X_{IN}) \leq 16.8$ MHz | 4.5 | 5.0 | 5.5 | V |
| | | Middle-speed mode $f(\phi) = f(X_{IN})/8$ | $f(X_{IN}) \leq 12.5$ MHz | 2.7 | 5.0 | 5.5 | V |
| $f(X_{IN}) \leq 16.8$ MHz | 4.5 | | 5.0 | 5.5 | V | | |
| V _{SS} | Power source voltage | | 0 | | | V | |
| V _{IH} | "H" input voltage P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 | | 0.8V _{CC} | | V _{CC} | V | |
| V _{IH} | "H" input voltage P32, P33 | | 0.8V _{CC} | | 5.5 | V | |
| V _{IH} | "H" input voltage (when I ² C-BUS input level is selected) SDA, SCL | | 0.7V _{CC} | | 5.5 | V | |
| V _{IH} | "H" input voltage (when SMBUS input level is selected) SDA, SCL | | 1.4 | | 5.5 | V | |
| V _{IH} | "H" input voltage RESET, X _{IN} , CNV _{SS} | | 0.8V _{CC} | | V _{CC} | V | |
| V _{IH} | "H" input voltage XCIN | | 2 | | V _{CC} | V | |
| V _{IL} | "L" input voltage P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P67 | | 0 | | 0.2V _{CC} | V | |
| V _{IL} | "L" input voltage (when I ² C-BUS input level is selected) SDA, SCL | | 0 | | 0.3V _{CC} | V | |
| V _{IL} | "L" input voltage (when SMBUS input level is selected) SDA, SCL | | 0 | | 0.6 | V | |
| V _{IL} | "L" input voltage RESET, CNV _{SS} | | 0 | | 0.2V _{CC} | V | |
| V _{IL} | "L" input voltage X _{IN} | | | | 0.16V _{CC} | V | |
| V _{IL} | "L" input voltage XCIN | | | | 0.4 | V | |

Notes 1: When using A/D converter, see A/D converter recommended operating conditions.

2: The start voltage and the start time for oscillation depend on the using oscillator, oscillation circuit constant value and operating temperature range, etc.. Particularly a high-frequency oscillator might require some notes in the low voltage operation.

Table 21 Recommended operating conditions (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|----------------------|---|---|-------------------------------|--------|---|------|
| | | | Min. | Typ. | Max. | |
| f(X _{IN}) | Main clock input oscillation frequency (Note 1) | High-speed mode f(φ) = f(X _{IN})/2 | 2.7 ≤ V _{CC} < 4.0 V | | $\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$ | MHz |
| | | | 4.0 ≤ V _{CC} < 4.5 V | | $\frac{(24 \times V_{CC} - 60) \times 1.05}{3}$ | MHz |
| | | | 4.5 ≤ V _{CC} ≤ 5.5 V | | 16.8 | MHz |
| | | Middle-speed mode f(φ) = f(X _{IN})/8 | 2.7 ≤ V _{CC} < 4.5 V | | $\frac{(15 \times V_{CC} + 39)}{7} \times 1.1$ | MHz |
| | | | 4.5 ≤ V _{CC} ≤ 5.5 V | | 16.8 | MHz |
| f(X _{CIN}) | Sub-clock input oscillation frequency (Notes 1, 2) | | | 32.768 | 50 | kHz |

Notes 1: When the oscillation frequency has a duty cycle of 50%.

2: When using the microcomputer in low-speed mode, set the sub-clock input oscillation frequency on condition that f(X_{CIN}) < f(X_{IN})/3.

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Table 22 Recommended operating conditions (3)(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|------------|---|--------|------|------|------|
| | | Min. | Typ. | Max. | |
| ΣIOH(peak) | "H" total peak output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37 (Note 1) | | | –80 | mA |
| ΣIOH(peak) | "H" total peak output current P40–P47, P50–P57, P60–P67 (Note 1) | | | –80 | mA |
| ΣIOL(peak) | "L" total peak output current P00–P07, P10–P17, P30–P37 (Note 1) | | | 80 | mA |
| ΣIOL(peak) | "L" total peak output current P20–P27 (Note 1) | | | 80 | mA |
| ΣIOL(peak) | "L" total peak output current P40–P47, P50–P57, P60–P67 (Note 1) | | | 80 | mA |
| ΣIOH(avg) | "H" total average output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37 (Note 1) | | | –40 | mA |
| ΣIOH(avg) | "H" total average output current P40–P47, P50–P57, P60–P67 (Note 1) | | | –40 | mA |
| ΣIOL(avg) | "L" total average output current P00–P07, P10–P17, P30–P37 (Note 1) | | | 40 | mA |
| ΣIOL(avg) | "L" total average output current P20–P27 (Note 1) | | | 40 | mA |
| ΣIOL(avg) | "L" total average output current P40–P47, P50–P57, P60–P67 (Note 1) | | | 40 | mA |
| IOH(peak) | "H" peak output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 (Note 2) | | | –10 | mA |
| IOL(peak) | "L" peak output current P00–P07, P10–P17, P30–P37, P40–P47, P50–P57, P60–P67 (Note 2) | | | 10 | mA |
| IOL(peak) | "L" peak output current P20–P27 (Note 2) | | | 20 | mA |
| IOH(avg) | "H" average output current P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 (Note 3) | | | –5 | mA |
| IOL(avg) | "L" average output current P00–P07, P10–P17, P30–P37, P40–P47, P50–P57, P60–P67 (Note 3) | | | 5 | mA |
| IOL(avg) | "L" average output current P20–P27 (Note 3) | | | 10 | mA |

Notes 1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

2: The peak output current is the peak current flowing in each port.

3: The average output current IOL(avg), IOH(avg) are average value measured over 100 ms.

Electrical characteristics

Table 23 Electrical characteristics (1)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-----------------|---|---|---------|------|-----------------|------|
| | | | Min. | Typ. | Max. | |
| VOH | “H” output voltage P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 (Note 1) | IOH = 10 mA VCC = 4.0 to 5.5 V | VCC–2.0 | | | V |
| | | IOH = 1.0 mA VCC = 1.8 to 5.5 V | VCC–1.0 | | | V |
| VOL | “L” output voltage P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P67 | IO _L = 10 mA VCC = 4.0 to 5.5 V | | | 2.0 | V |
| | | IO _L = 1.6 mA VCC = 1.8 to 5.5 V | | | 1.0 | V |
| VOL | “L” output voltage P20–P27 | IO _L = 20 mA VCC = 4.0 to 5.5 V | | | 2.0 | V |
| | | IO _L = 1.6 mA VCC = 1.8 to 5.5 V | | | 0.4 | V |
| VT+–VT– | Hysteresis CNTR0, CNTR1, CNTR2, INT0–INT4 | | | 0.4 | | V |
| VT+–VT– | Hysteresis RxD1, SCLK1, SIN2, SCLK2, RxD3, SCLK3 | | | 0.5 | | V |
| VT+–VT– | Hysteresis RESET | | | 0.5 | | V |
| I _{IH} | “H” input current P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P67 | V _I = V _{CC} (Pin floating. Pull-up transistors “off”) | | | 5.0 | μA |
| I _{IH} | “H” input current RESET, CNV _{SS} | V _I = V _{CC} | | | 5.0 | μA |
| I _{IH} | “H” input current X _{IN} | V _I = V _{CC} | | 4.0 | | μA |
| I _{IL} | “L” input current P00–P07, P10–P17, P20–P27, P30–P37, P40–P47, P50–P57, P60–P67 | V _I = V _{SS} (Pin floating. Pull-up transistors “off”) | | | –5.0 | μA |
| I _{IL} | “L” input current RESET, CNV _{SS} | V _I = V _{SS} | | | –5.0 | μA |
| I _{IL} | “L” input current X _{IN} | V _I = V _{SS} | | –4.0 | | μA |
| I _{IL} | “L” input current (at Pull-up) P00–P07, P10–P17, P20–P27, P30, P31, P34–P37, P40–P47, P50–P57, P60–P67 | V _I = V _{SS} V _{CC} = 5.0 V | –80 | –210 | –420 | μA |
| | | V _I = V _{SS} V _{CC} = 3.0 V | –30 | –70 | –140 | μA |
| VRAM | RAM hold voltage | When clock stopped | 1.8 | | V _{CC} | V |

Note 1: P35 is measured when the P35/TxD3 P-channel output disable bit of the UART3 control register (bit 4 of address 003316) is 0”.
P45 is measured when the P45/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is 0”.

Table 24 Electrical characteristics (2)

(V_{CC} = 2.7 to 5.5 V, T_a = 20 to 85 °C, f(X_{IN})=32.768kHz (Stopped in middle-speed mode), Output transistors “off”, AD converter not operated)

| Symbol | Parameter | Test conditions | | | Limits | | | Unit | | |
|---|----------------------|---|----------------------|---|--------------------------------|------------------------|------|------|-----|----|
| | | | | | Min. | Typ. | Max. | | | |
| I _{CC} | Power source current | High-speed mode | V _{CC} = 5V | f(X _{IN}) = 16.8 MHz | | 5.5 | 8.3 | mA | | |
| | | | | f(X _{IN}) = 12.5 MHz | | 4.5 | 6.8 | mA | | |
| | | | | f(X _{IN}) = 8.4 MHz | | 3.5 | 5.3 | mA | | |
| | | | | f(X _{IN}) = 4.2 MHz | | 2.2 | 3.3 | mA | | |
| | | | | f(X _{IN}) = 16.8 MHz (in WIT state) | | 2.2 | 3.3 | mA | | |
| | | | V _{CC} = 3V | f(X _{IN}) = 8.4 MHz | | 2.7 | 4.1 | mA | | |
| | | | | f(X _{IN}) = 4.2 MHz | | 1.8 | 2.7 | mA | | |
| | | | | f(X _{IN}) = 2.1 MHz | | 1.1 | 1.7 | mA | | |
| | | | Middle-speed mode | V _{CC} = 5V | f(X _{IN}) = 16.8 MHz | | 3.0 | 4.5 | mA | |
| | | | | | f(X _{IN}) = 12.5 MHz | | 2.4 | 3.6 | mA | |
| | | f(X _{IN}) = 8.4 MHz | | | | 2.0 | 3.0 | mA | | |
| | | f(X _{IN}) = 16.8 MHz (in WIT state) | | | | 2.1 | 3.2 | mA | | |
| | | V _{CC} = 3V | | f(X _{IN}) = 12.5 MHz | | 1.7 | 2.6 | mA | | |
| | | | | f(X _{IN}) = 8.4 MHz | | 1.5 | 2.3 | mA | | |
| | | Low-speed mode | V _{CC} = 5V | f(X _{IN}) = stopped | | 410 | 630 | μA | | |
| | | | | In WIT state | | 4.5 | 6.8 | μA | | |
| | | | V _{CC} = 3V | f(X _{IN}) = stopped | | 400 | 600 | μA | | |
| | | | | In WIT state | | 3.7 | 5.6 | μA | | |
| | | In STP state (All oscillation stopped) | | | | T _a = 25 °C | | 0.55 | 3.0 | μA |
| | | | | | | T _a = 85 °C | | 0.75 | | μA |
| Increment when A/D conversion is executed | | f(X _{IN}) = 16.8 MHz, V _{CC} = 5V In Middle-, high-speed mode | | | | 1000 | | μA | | |

A/D converter characteristics

Table 25 A/D converter recommended operating conditions

 (V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Conditions | Limits | | | Unit |
|------------------|--|-----------------------------------|--------|------|---|------|
| | | | Min. | Typ. | Max. | |
| V _{CC} | Power source voltage (When A/D converter is used) | 8-bit A/D mode (Note 1) | 2.7 | 5.0 | 5.5 | V |
| | | 10-bit A/D mode (Note 2) | 2.7 | 5.0 | 5.5 | |
| V _{REF} | Analog reference voltage | | 2.0 | | V _{CC} | V |
| AV _{SS} | Analog power source voltage | | | 0 | | V |
| V _{IA} | Analog input voltage | | 0 | | V _{CC} | V |
| f(XIN) | Main clock oscillation frequency (When A/D converter is used) | 2.7 ≤ V _{CC} < 4.0 V | 0.5 | | $\frac{(9 \times V_{CC} - 0.3) \times 1.05}{3}$ | MHz |
| | | 4.0 ≤ V _{CC} < 4.5 V | 0.5 | | $\frac{(24 \times V_{CC} - 60) \times 1.05}{3}$ | |
| | | 4.5 ≤ V _{CC} ≤ 5.5 V | 0.5 | | 16.8 | |

Note 1: 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038) is "1".
Note 2: 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 003816) is "0".

Table 26 A/D converter characteristics

 (V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|--------------------|---|---|--------|------|------|-----------------------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | 8-bit A/D mode (Note 1) | | | 8 | bit |
| | | 10-bit A/D mode (Note 2) | | | 10 | |
| – | Absolute accuracy (excluding quantization error) | 8-bit A/D mode (Note 1) 2.7 ≤ V _{REF} ≤ 5.5 V | | | ±2 | LSB |
| | | 10-bit A/D mode (Note 2) 2.7 ≤ V _{REF} ≤ 5.5 V | | | ±4 | |
| t _{CONV} | Conversion time | 8-bit A/D mode (Note 1) | | | 50 | 2t _c (XIN) |
| | | 10-bit A/D mode (Note 2) | | | 61 | |
| RLADDER | Ladder resistor | | 12 | 35 | 100 | kΩ |
| I _{VREF} | Reference power source input current | at A/D converter operated V _{REF} = 5.0 V | 50 | 150 | 200 | μA |
| | | at A/D converter stopped V _{REF} = 5.0 V | | | 5 | μA |
| I _{I(AD)} | A/D port in-out current | | | | 5 | μA |

Note 1: 8-bit A/D mode: When the conversion mode selection bit (bit 7 of address 0038) is "1".
Note 2: 10-bit A/D mode: When the conversion mode selection bit (bit 7 of address 003816) is "0".

D/A converter characteristics

Table 27 D/A converter characteristics

 (V_{CC} = 2.7 to 5.5 V, V_{REF} = 2.7 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|-------------------|--|--------------------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | |
| – | Resolution | | | | 8 | bit |
| – | Absolute accuracy | 4.0 ≤ V _{REF} ≤ 5.5 V | | | 1.0 | % |
| | | 2.7 ≤ V _{REF} < 4.0 V | | | 2.5 | % |
| t _{su} | Setting time | | | | 3 | μs |
| RO | Output resistor | | 2 | 3.5 | 5 | kΩ |
| I _{VREF} | Reference power source input current (Note 1) | | | | 3.2 | mA |

Note 1: Using one D/A converter, with the value in the DA conversion register of the other D/A converter being 0.

Power source circuit timing characteristics

Table 28 Power source circuit timing characteristics

 (V_{CC} = 2.7 to 5.5 V, V_{REF} = 2.7 V to V_{CC}, V_{SS} = AV_{SS} = 0 V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|---------|-----------|---|-------------------------------|------|------|------|
| | | | Min. | Typ. | Max. | |
| td(P R) | – | Internal power source stable time at power-on | 2.7 ≤ V _{CC} < 5.5 V | | 2 | ms |

Timing requirements and switching characteristics

Table 29 Timing requirements (1)

(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | | Limits | | | Unit |
|-----------|---|-------------------------------|--|------|------|-----------|
| | | | Min. | Typ. | Max. | |
| tw(RESET) | Reset input | " L " pulse width | td(P-R) ms + 16 | | | XIN cycle |
| tc(XIN) | Main clock XIN input cycle time | 4.5 ≤ V _{CC} ≤ 5.5 V | 59.5 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 10000/(86V _{CC} -219) | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 26 × 10 ³ /(82V _{CC} -3) | | | |
| twh(XIN) | Main clock XIN input " H " pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 25 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 4000/(86V _{CC} -219) | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 10000/(82V _{CC} -3) | | | |
| twl(XIN) | Main clock XIN input " L " pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 25 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 4000/(86V _{CC} -219) | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 10000/(82V _{CC} -3) | | | |
| tc(XCIN) | Sub-clock XCIN input cycle time | | 20 | | | μs |
| twh(XCIN) | Sub-clock XCIN input " H " pulse width | | 5 | | | μs |
| twl(XCIN) | Sub-clock XCIN input " L " pulse width | | 5 | | | μs |
| tc(CNTR) | CNTR0–CNTR2 input cycle time | 4.5 ≤ V _{CC} ≤ 5.5 V | 120 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 160 | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 250 | | | |
| twh(CNTR) | CNTR0–CNTR2 input " H " pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 48 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 64 | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 115 | | | |
| twl(CNTR) | CNTR0–CNTR2 input " L " pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 48 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 64 | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 115 | | | |
| twh(INT) | INT00, INT01, INT1, INT2, INT3, INT40, INT41 input " H " pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 48 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 64 | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 115 | | | |
| twl(INT) | INT00, INT01, INT1, INT2, INT3, INT40, INT41 input " L " pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 48 | | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 64 | | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 115 | | | |

Table 30 Timing requirements (2)(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|-------------------------------------|---|-------------------------------|------|------|------|
| | | Min. | Typ. | Max. | |
| tc(SCLK1), tc(SCLK3) | Serial I/O1, serial I/O3 clock input cycle time (Note) | 4.5 ≤ V _{CC} ≤ 5.5 V | 250 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 320 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 500 | | |
| tWH(SCLK1), tWH(SCLK3) | Serial I/O1, serial I/O3 clock input "H" pulse width (Note) | 4.5 ≤ V _{CC} ≤ 5.5 V | 120 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 150 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 240 | | |
| tWL(SCLK1), tWL(SCLK3) | Serial I/O1, serial I/O3 clock input "L" pulse width (Note) | 4.5 ≤ V _{CC} ≤ 5.5 V | 120 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 150 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 240 | | |
| tsu(RxD1-SCLK1), tsu(RxD3-SCLK3) | Serial I/O1, serial I/O3 clock input setup time | 4.5 ≤ V _{CC} ≤ 5.5 V | 70 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 90 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 100 | | |
| th(SCLK1-RxD1), th(SCLK3-RxD3) | Serial I/O1, serial I/O3 clock input hold time | 4.5 ≤ V _{CC} ≤ 5.5 V | 32 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 40 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 50 | | |
| tc(SCLK2) | Serial I/O2 clock input cycle time | 4.5 ≤ V _{CC} ≤ 5.5 V | 500 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 650 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 1000 | | |
| tWH(SCLK2) | Serial I/O2 clock input "H" pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 200 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 260 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 400 | | |
| tWL(SCLK2) | Serial I/O2 clock input "L" pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V | 200 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 260 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 400 | | |
| tsu(SIN2-SCLK2) | Serial I/O2 clock input setup time | 4.5 ≤ V _{CC} ≤ 5.5 V | 100 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 130 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 200 | | |
| th(SCLK2-SIN2) | Serial I/O2 clock input hold time | 4.5 ≤ V _{CC} ≤ 5.5 V | 100 | | ns |
| | | 4.0 ≤ V _{CC} < 4.5 V | 130 | | |
| | | 2.7 ≤ V _{CC} < 4.0 V | 150 | | |

Note : When bit 6 of address 001A₁₆ and bit 6 of address 0032₁₆ are "1" (clock synchronous).
Divide this value by four when bit 6 of address 001A₁₆ and bit 6 of address 0032₁₆ are "0" (UART).

Table 31 Switching characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0V, T_a = 20 to 85 °C, unless otherwise noted)

| Symbol | Parameter | Test conditions | Limits | | | Unit |
|--|---|---|--|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _{WH} (SCLK1) t _{WH} (SCLK3) | Serial I/O1, serial I/O3 clock output "H" pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | t _C (SCLK1)2-30, t _C (SCLK3)2-30 | | | ns |
| | | | t _C (SCLK1)2-35, t _C (SCLK3)2-35 | | | |
| | | | t _C (SCLK1)2-40, t _C (SCLK3)2-40 | | | |
| t _{WL} (SCLK1) t _{WL} (SCLK3) | Serial I/O1, serial I/O3 clock output "L" pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | t _C (SCLK1)2-30, t _C (SCLK3)2-30 | | | ns |
| | | | t _C (SCLK1)2-35, t _C (SCLK3)2-35 | | | |
| | | | t _C (SCLK1)2-40, t _C (SCLK3)2-40 | | | |
| t _d (SCLK1-TxD1) t _d (SCLK3-TxD3) | Serial I/O1, serial I/O3 output delay time (Note) | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | | 140 | ns |
| | | | | | 200 | |
| | | | | | 350 | |
| t _v (SCLK1-TxD1) t _v (SCLK3-TxD3) | Serial I/O1, serial I/O3 output valid time (Note) | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | -30 | | | ns |
| | | | -30 | | | |
| | | | -30 | | | |
| t _r (SCLK1) t _r (SCLK3) | Serial I/O1, serial I/O3 rise time of clock output | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | | 30 | ns |
| | | | | | 35 | |
| | | | | | 40 | |
| t _f (SCLK1) t _f (SCLK3) | Serial I/O1, serial I/O3 fall time of clock output | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | | 30 | ns |
| | | | | | 35 | |
| | | | | | 40 | |
| t _{WH} (SCLK2) | Serial I/O2 clock output "H" pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | t _C (SCLK2)2-160 | | | ns |
| | | | t _C (SCLK2)2-200 | | | |
| | | | t _C (SCLK2)2-240 | | | |
| t _{WL} (SCLK2) | Serial I/O2 clock output "L" pulse width | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | t _C (SCLK2)2-160 | | | ns |
| | | | t _C (SCLK2)2-200 | | | |
| | | | t _C (SCLK2)2-240 | | | |
| t _d (SCLK2-SOUT2) | Serial I/O2 output delay time | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | | 200 | ns |
| | | | | | 250 | |
| | | | | | 300 | |
| t _v (SCLK2-SOUT2) | Serial I/O2 output valid time | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | 0 | | ns |
| | | | | 0 | | |
| | | | | 0 | | |
| t _f (SCLK2) | Serial I/O2 fall time of clock output | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | | 30 | ns |
| | | | | | 35 | |
| | | | | | 40 | |
| t _r (CMOS) | CMOS rise time of output | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | 10 | 30 | ns |
| | | | | 12 | 35 | |
| | | | | 15 | 40 | |
| t _f (CMOS) | CMOS fall time of output (Note) | 4.5 ≤ V _{CC} ≤ 5.5 V 4.0 ≤ V _{CC} < 4.5 V 2.7 ≤ V _{CC} < 4.0 V | | 10 | 30 | ns |
| | | | | 12 | 35 | |
| | | | | 15 | 40 | |

Fig. 93

(Note)

Note: When the P45/TxD1 P-channel output disable bit of the UART1 control register (bit 4 of address 001B16) is 0".

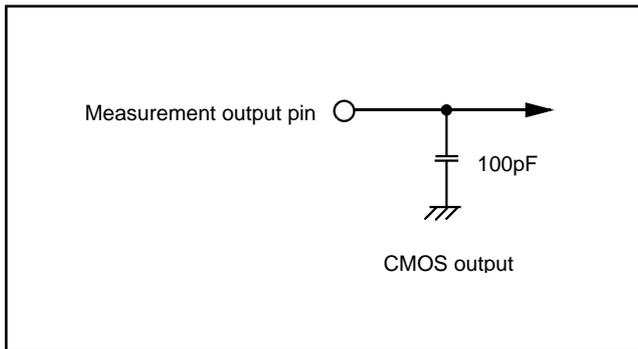


Fig.93 Circuit for measuring output switching characteristics (1)

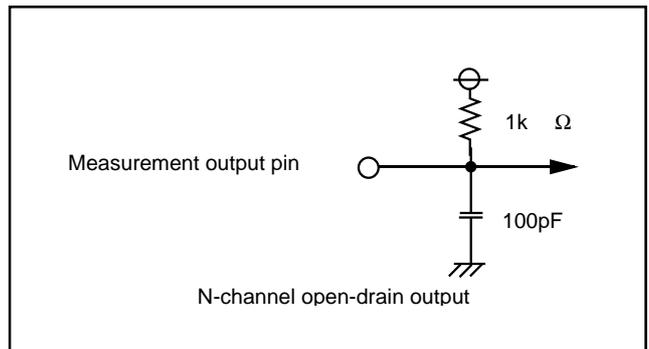


Fig.94 Circuit for measuring output switching characteristics (2)

EOL announced Product

Single-chip mode timing diagram

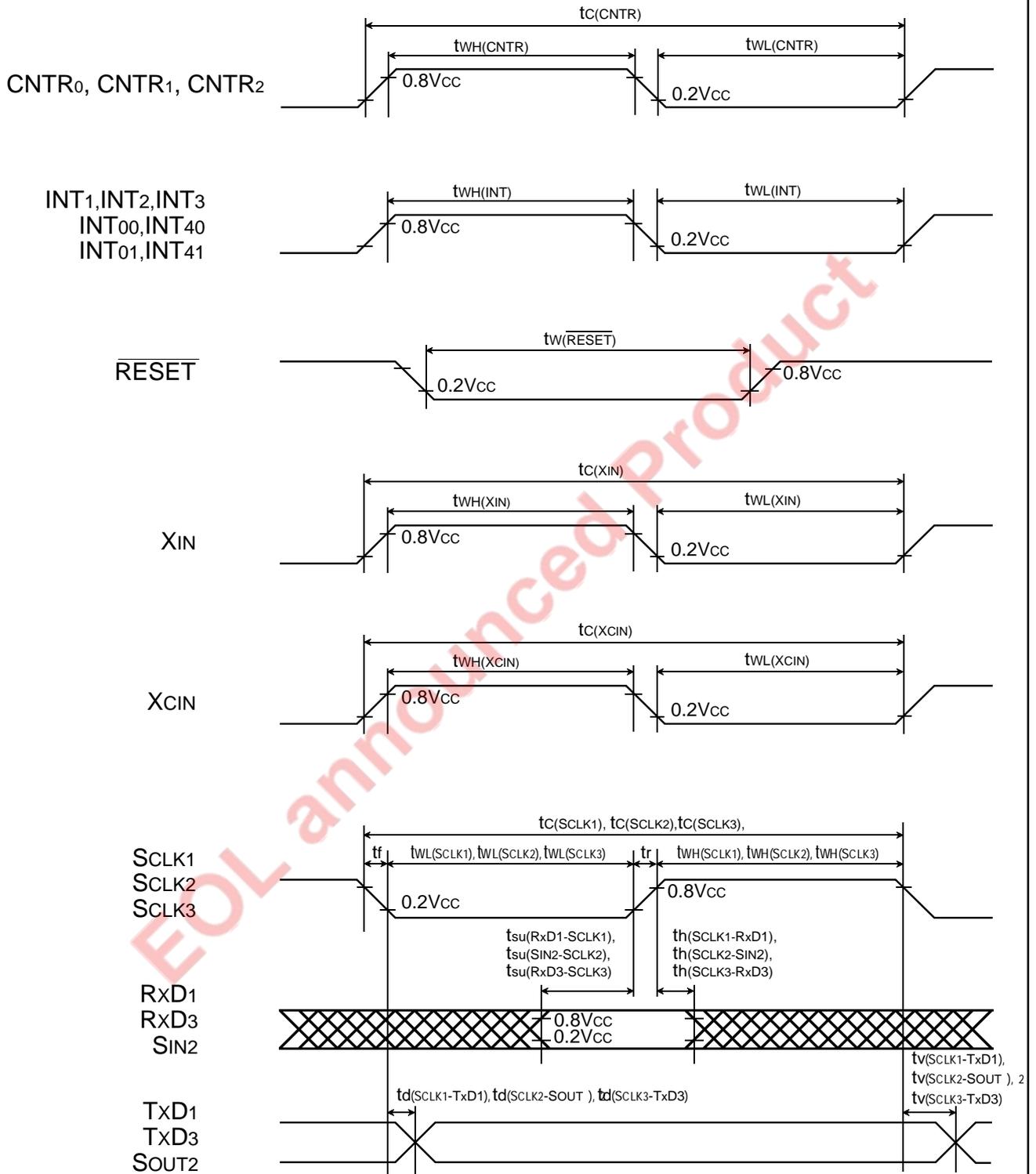


Fig. 95 Timing diagram (in single-chip mode)

Table 32 Multi-master I²C-BUS bus line characteristics

| Symbol | Parameter | Standard clock mode | | High-speed clock mode | | Unit |
|---------------------|--|---------------------|------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | |
| t _{BUF} | Bus free time | 4.7 | | 1.3 | | μs |
| t _{HD;STA} | Hold time for START condition | 4.0 | | 0.6 | | μs |
| t _{LOW} | Hold time for SCL clock = 0" | " 4.7 | | 1.3 | | μs |
| t _R | Rising time of both SCL and SDA signals | | 1000 | 20+0.1C _b | 300 | ns |
| t _{HD;DAT} | Data hold time | 0 | | 0 | 0.9 | μs |
| t _{HIGH} | Hold time for SCL clock = 1" | " 4.0 | | 0.6 | | μs |
| t _F | Falling time of both SCL and SDA signals | | 300 | 20+0.1C _b | 300 | ns |
| t _{SU;DAT} | Data setup time | 250 | | 100 | | ns |
| t _{SU;STA} | Setup time for repeated START condition | 4.7 | | 0.6 | | μs |
| t _{SU;STO} | Setup time for STOP condition | 4.0 | | 0.6 | | μs |

Note: C_b = total capacitance of 1 bus line

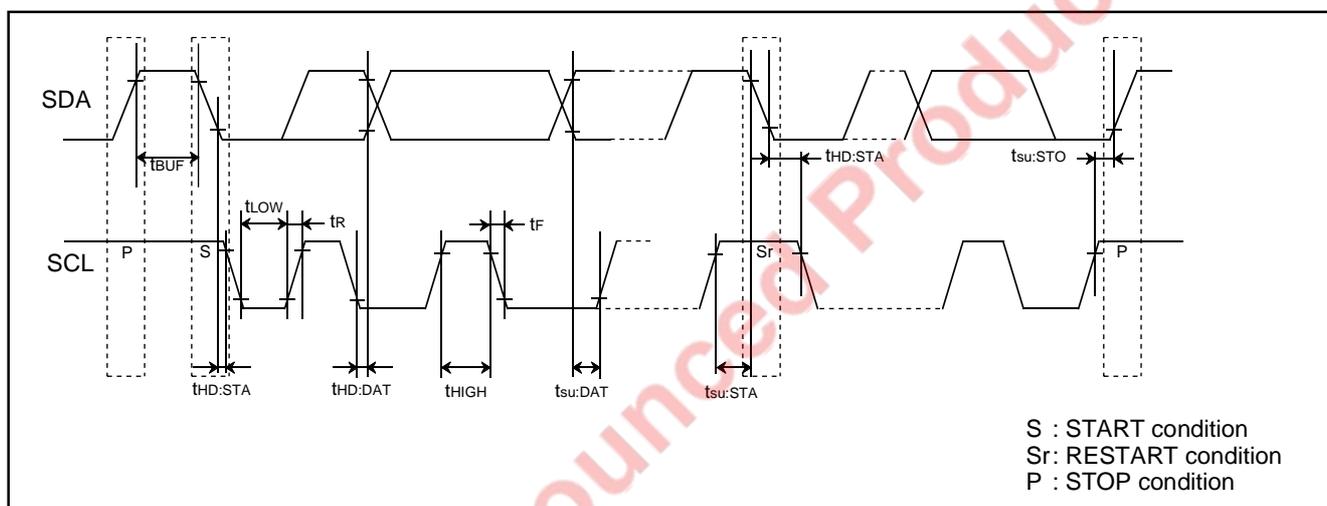
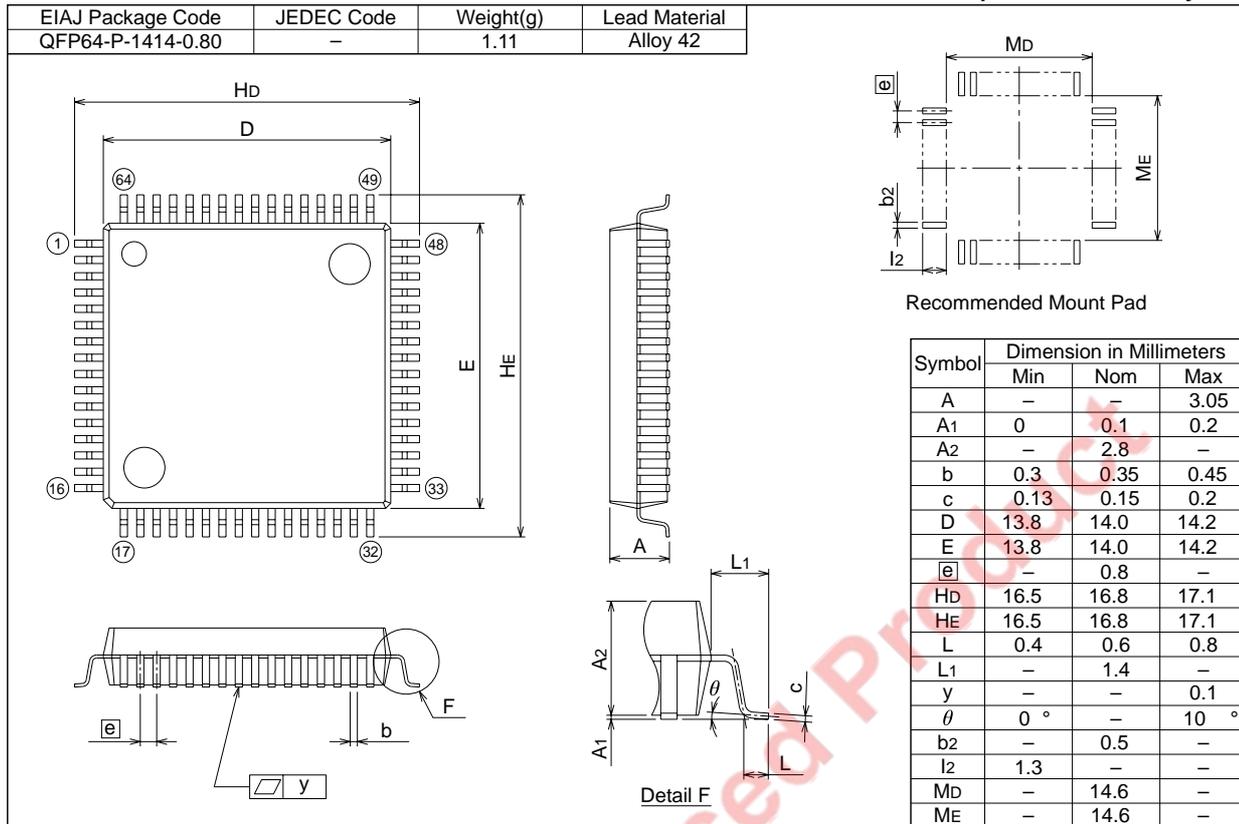


Fig. 96 Timing diagram of multi-master I²C-BUS

PACKAGE OUTLINE

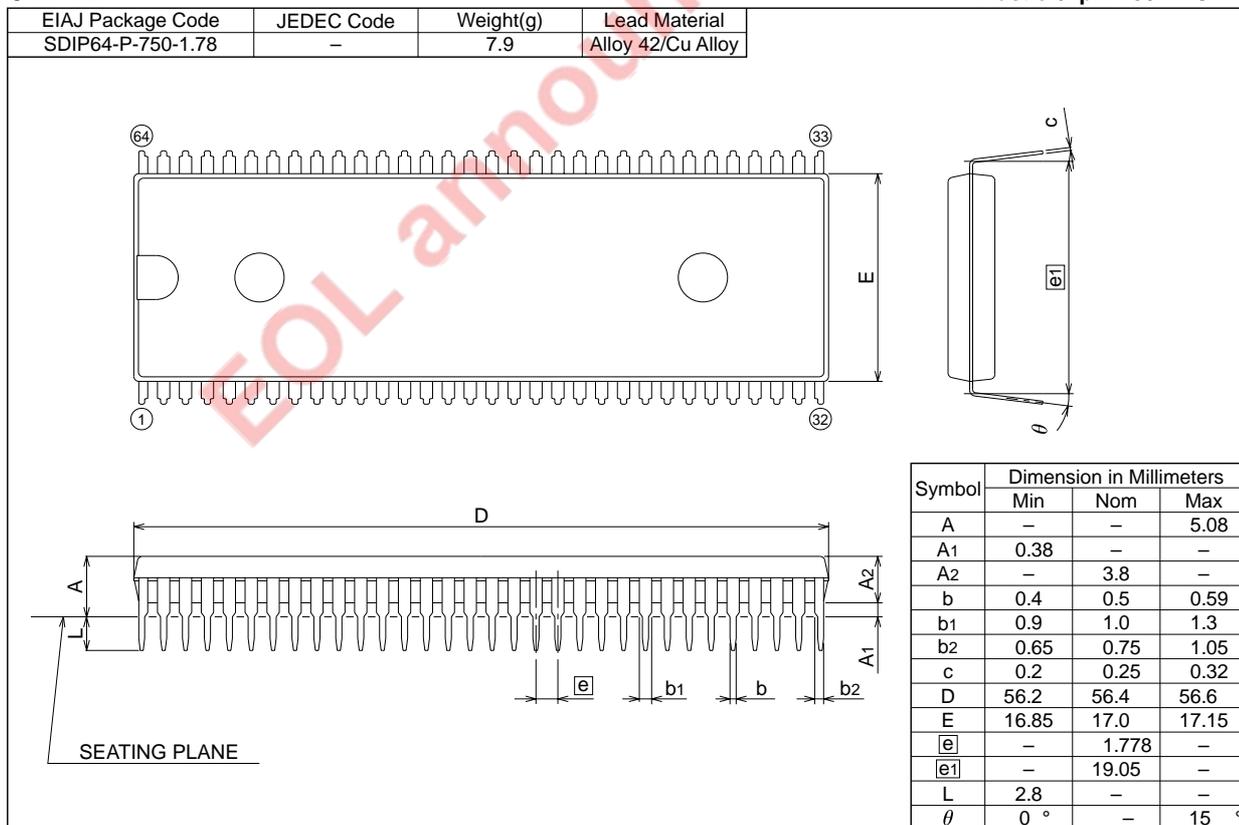
64P6N-A

Plastic 64pin 14X 14mm body QFP



64P4B

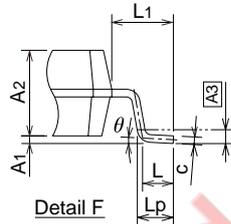
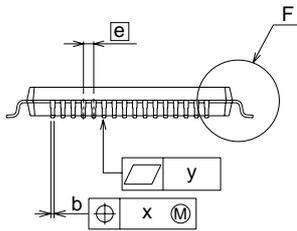
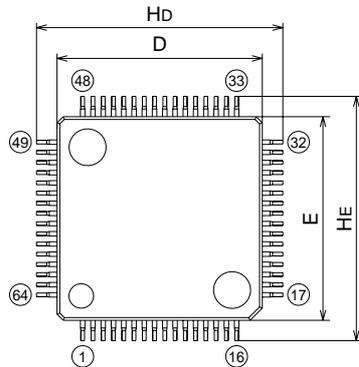
Plastic 64pin 750mil SDIP



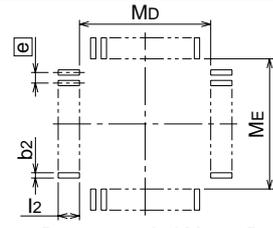
64P6Q-A

Plastic 64pin 10X 10mm body LQFP

| | | | |
|-------------------|------------|-----------|---------------|
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
| LQFP64-P-1010-0.5 | — | — | Cu Alloy |



Detail F



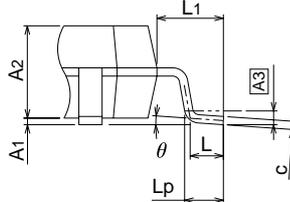
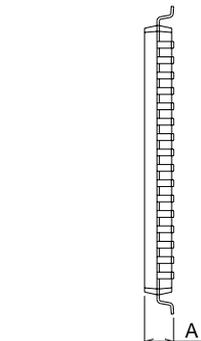
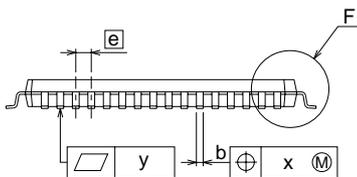
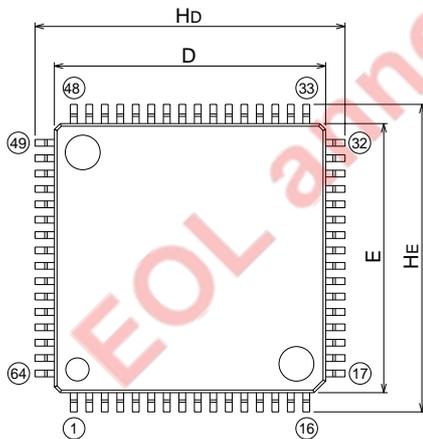
Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|-------|-----------------|
| | Min | Nom | Max |
| A | — | — | 1.7 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | — | 1.4 | — |
| b | 0.13 | 0.18 | 0.28 |
| c | 0.105 | 0.125 | 0.175 |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| e | — | 0.5 | — |
| Hd | 11.8 | 12.0 | 12.2 |
| HE | 11.8 | 12.0 | 12.2 |
| L | 0.3 | 0.5 | 0.7 |
| L1 | — | 1.0 | — |
| Lp | 0.45 | 0.6 | 0.75 |
| A3 | — | 0.25 | — |
| x | — | — | 0.08 |
| y | — | — | 0.1 |
| θ | 0 _i | — | 10 _i |
| b2 | — | 0.225 | — |
| l2 | 1.0 | — | — |
| Md | — | 10.4 | — |
| ME | — | 10.4 | — |

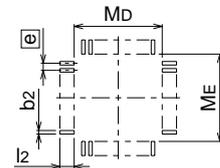
64P6U-A

Plastic 64pin 14X 14mm body LQFP

| | | | |
|-------------------|------------|-----------|---------------|
| EIAJ Package Code | JEDEC Code | Weight(g) | Lead Material |
| LQFP64-P-1414-0.8 | — | — | Cu Alloy |



Detail F



Recommended Mount Pad

| Symbol | Dimension in Millimeters | | |
|--------|--------------------------|-------|----------------|
| | Min | Nom | Max |
| A | — | — | 1.7 |
| A1 | 0 | 0.1 | 0.2 |
| A2 | — | 1.4 | — |
| b | 0.32 | 0.37 | 0.45 |
| c | 0.105 | 0.125 | 0.175 |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| e | — | 0.8 | — |
| Hd | 15.8 | 16.0 | 16.2 |
| HE | 15.8 | 16.0 | 16.2 |
| L | 0.3 | 0.5 | 0.7 |
| L1 | — | 1.0 | — |
| Lp | 0.45 | 0.6 | 0.75 |
| A3 | — | 0.25 | — |
| x | — | — | 0.2 |
| y | — | — | 0.1 |
| θ | 0 _i | — | 8 _i |
| b2 | — | 0.5 | — |
| l2 | 0.95 | — | — |
| Md | — | 14.4 | — |
| ME | — | 14.4 | — |

REVISION HISTORY

3804 Group (Spec.H) Data Sheet

| Rev. | Date | Description | |
|------|--------------|--|---|
| | | Page | Summary |
| 1.00 | Dec.10, 2004 | – | First edition issued |
| 1.01 | Jan.25, 2005 | 2 11 22 31 33 93,94,95,96 | <p>Fig.1, 2 pin configurations are partly revised. P32→P32/SDA, P33→P33/SCL</p> <p>“ (2) Bits 1, 2, 3 of address 0010₁₆: Middle-speed Mode Automatic Switch Function” is partly revised.</p> <p>“●Middle-speed mode automatic switch by SCL/SDA Interrupt” is added.</p> <p>Note 2 of Fig.9 is added.</p> <p>INTERRUPTS is partly revised.</p> <p>■Note is partly added.</p> <p>■Precautions of “ (3) Pulse output mode” is partly revised.</p> <p>■Precautions of “ (6) Programmable waveform generating mode” is partly revised.</p> <p>■Precautions of “ (7) Programmable one-shot generating mode” is partly revised.</p> <p>Fig.87, 88, 89, 90 are partly revised. P32→P32/SDA, P33→P33/SCL</p> |

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Renesas Technology Europe Limited
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7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.
Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001