To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT POWER TRANSISTORS
2SK2136, 2SK2136-Z

SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE

DESCRIPTION

The 2SK2136, 2SK2136-Z are N-channel Power MOS Field Effect Transistors designed for high voltage switching applications.

FEATURES

- Low On-state Resistance
  $R_{DS(on)}$ = 0.18 Ω MAX. (V_{GS} = 10 V, I_D = 10 A)
- Low C_{iss} C_{iss} = 1 100 pF TYP.
- High Avalanche Capability Ratings

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

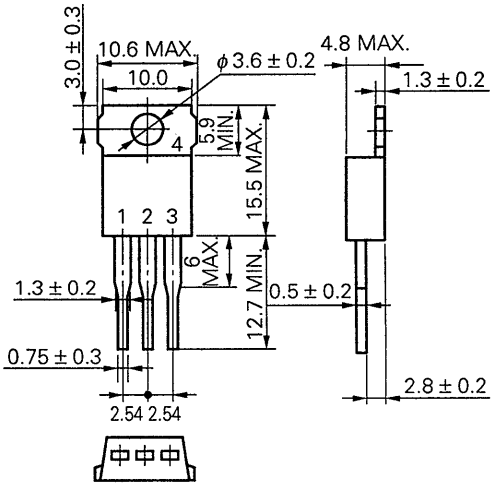
Drain to Source Voltage	V_{DSS}	200	V
Gate to Source Voltage	V_{GSS}	±30	V
Drain Current (DC)	$I_{D(DS)}$	±20	A
Drain Current (pulse)	$I_{D(pulse)}$*	±80	A
Total Power Dissipation (T_C = 25 °C)	P_{T1}	75	W
Total Power Dissipation (T_a = 25 °C)	P_{T2}	1.5	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	−55 to +150	°C
Single Avalanche Current	I_{AS}**	20	A
Single Avalanche Energy	E_{AS}**	80	mJ

* PW ≦ 10 μs, Duty Cycle ≦ 1 %

** Starting T_{ch} = 25 °C, R_G = 25 Ω, V_{GS} = 20 V → 0

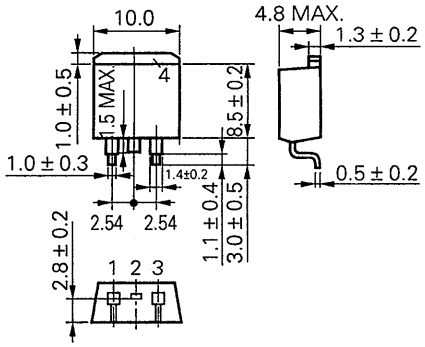
PACKAGE DIMENSIONS
(Unit : mm)

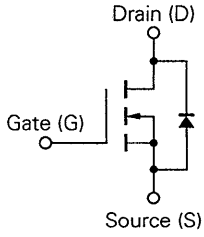
2SK2136



MP–25 (TO–220AB)

2SK2136-Z





1. Gate
2. Drain
3. Source
4. Fin (Drain)

(Diode in the figure is the parasitic diode)

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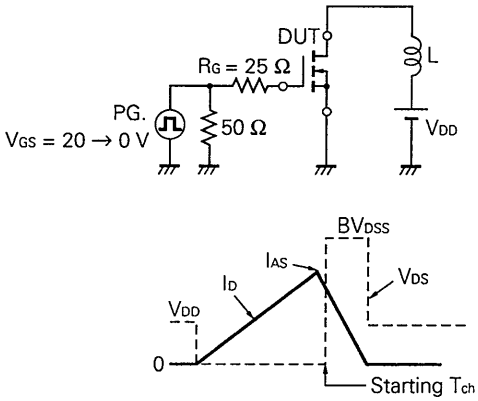
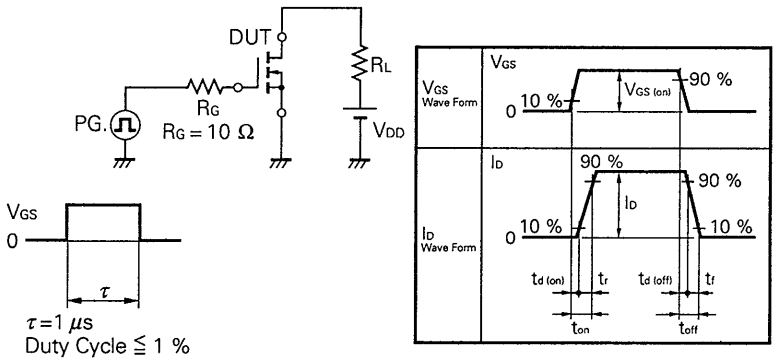
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	$R_{DS(on)}$			0.18	Ω	V_{GS} = 10 V, I_D = 10 A
Gate to Source Cutoff Voltage	$V_{GS(off)}$	2.0		4.0	V	V_{DS} = 10 V, I_D = 1 mA
Forward Transfer Admittance	$\|y_{fs}\|$	4.0			S	V_{DS} = 10 V, I_D = 10 A
Drain Leakage Current	I_{DSS}			100	μA	V_{DS} = 200 V, V_{GS} = 0
Gate to Source Leakage Current	I_{GSS}			±100	nA	V_{GS} = ±30 V, V_{DS} = 0
Input Capacitance	C_{iss}		1 100		pF	V_{DS} = 10 V V_{GS} = 0 f = 1 MHz
Output Capacitance	C_{oss}		540		pF	
Reverse Transfer Capacitance	C_{rss}		190		pF	
Turn-On Delay Time	$t_{d(on)}$		20		ns	V_{GS} = 10 V V_{DD} = 100 V I_D = 10 A, R_G = 10 Ω R_L = 10 Ω
Rise Time	t_r		85		ns	
Turn-Off Delay Time	$t_{d(off)}$		60		ns	
Fall Time	t_f		25		ns	
Total Gate Charge	Q_G		30		nC	V_{GS} = 10 V I_D = 20 A V_{DD} = 160 V
Gate to Source Charge	Q_{GS}		7.0		nC	
Gate to Drain Charge	Q_{GD}		15		nC	
Diode Forward Voltage	$V_{F(S-D)}$		1.0		V	I_F = 20 A, V_{GS} = 0
Reverse Recovery Time	t_{rr}		210		ns	I_F = 20 A di/dt = 50 A/μs
Reverse Recovery Charge	Q_{rr}		1.0		μC	

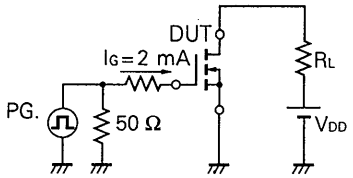
Test Circuit 1 : Avalanche Capability



Test Circuit 2 : Switching Time

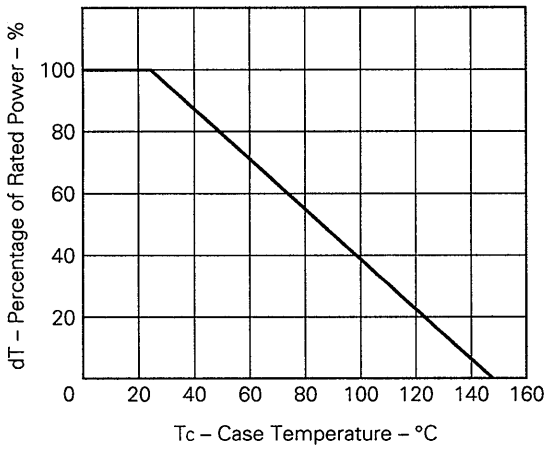


Test Circuit 3 : Gate Charge

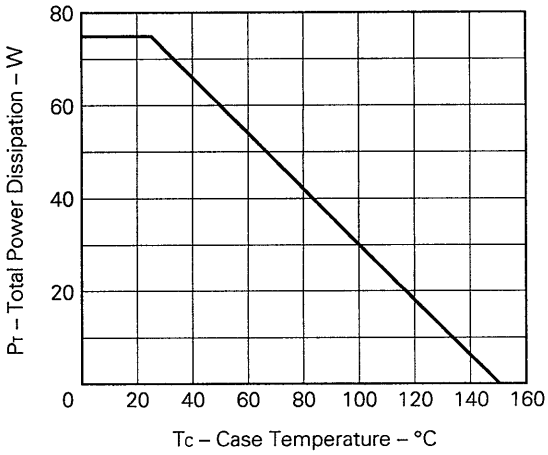


TYPICAL CHARACTERISTICS (T_a = 25 °C)

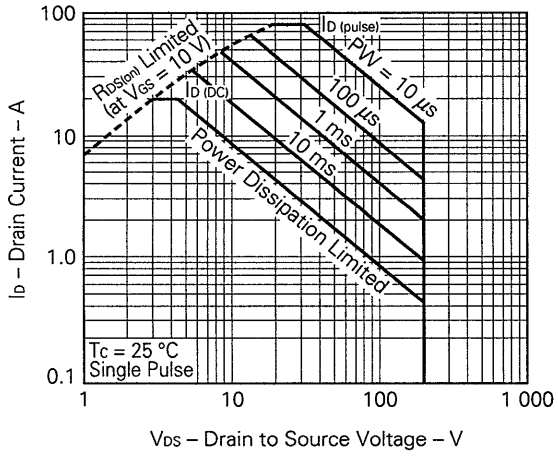
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



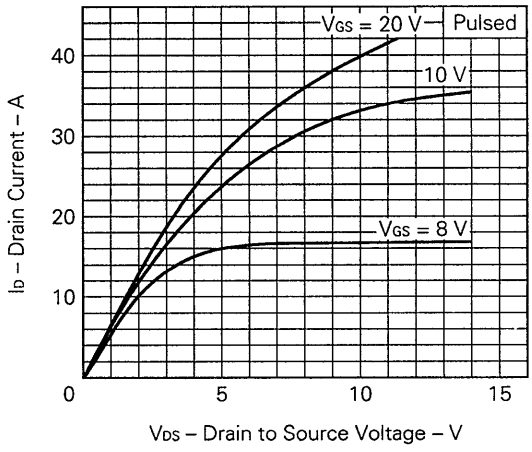
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



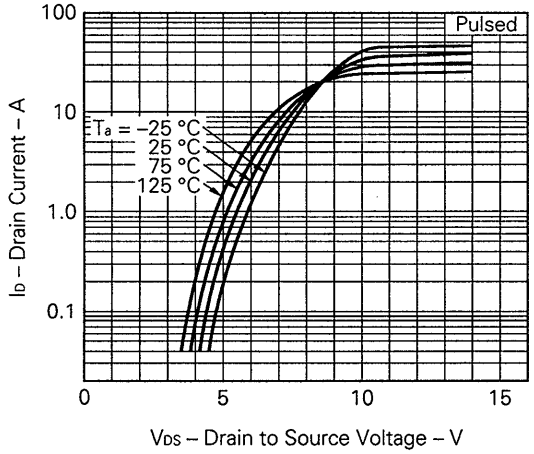
FORWARD BIAS SAFE OPERATING AREA



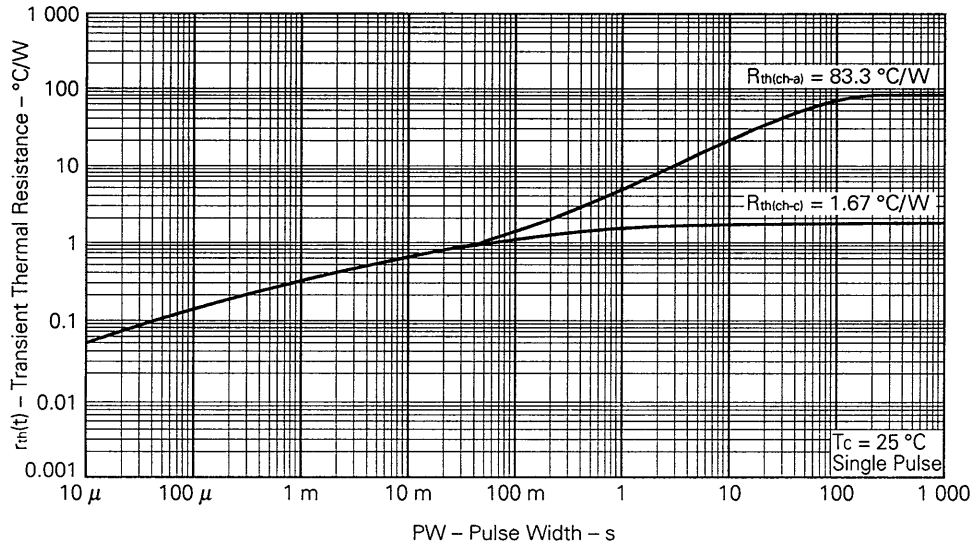
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



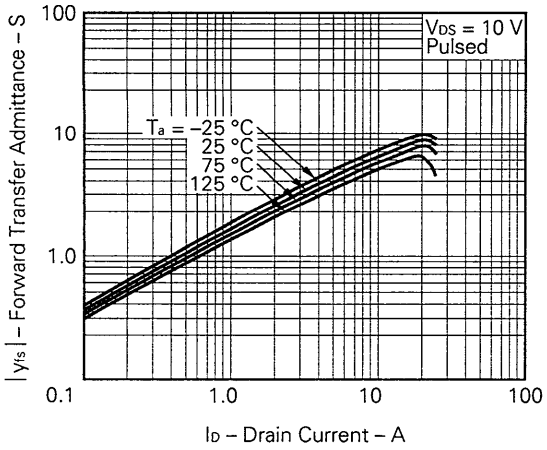
TRANSFER CHARACTERISTICS



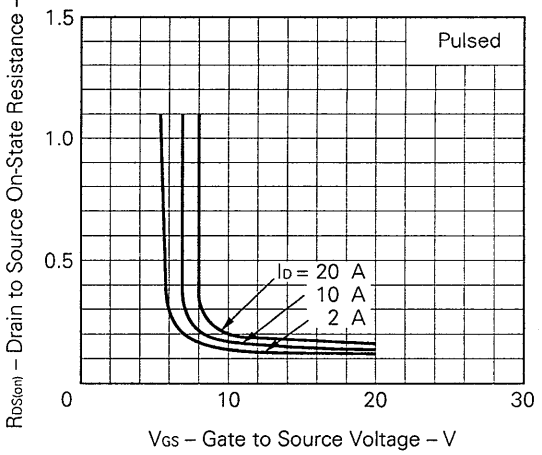
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



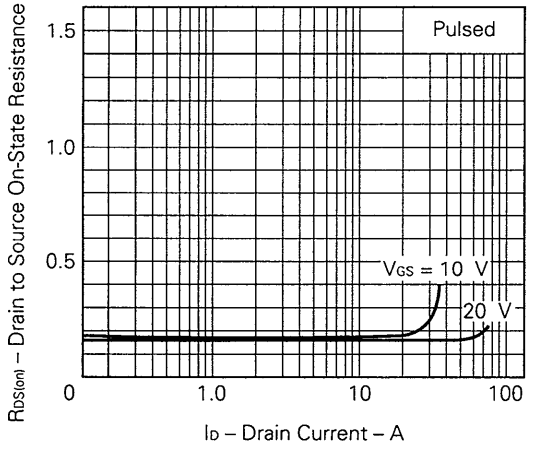
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



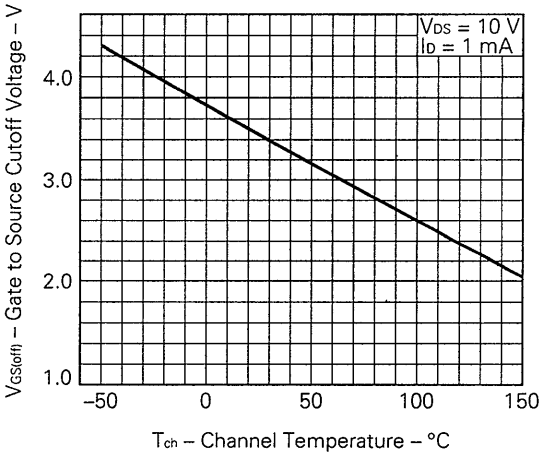
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



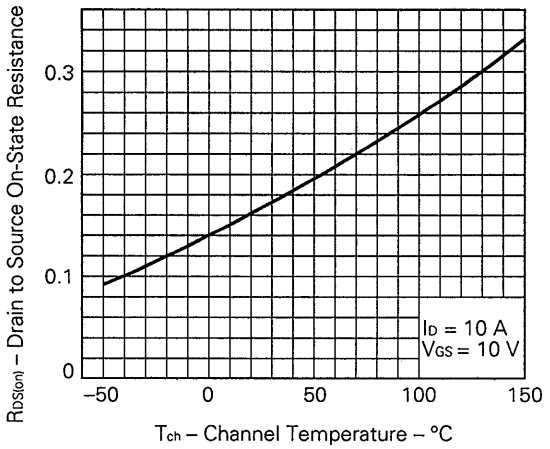
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



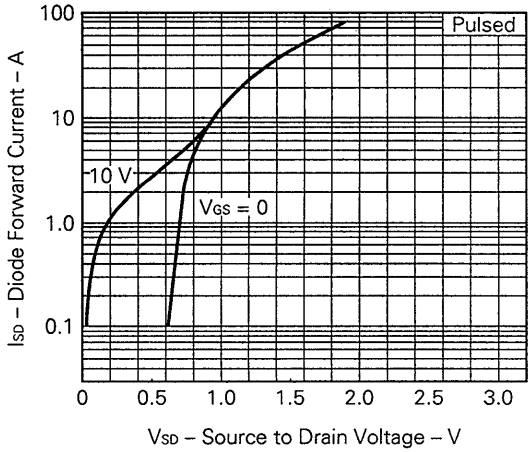
GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



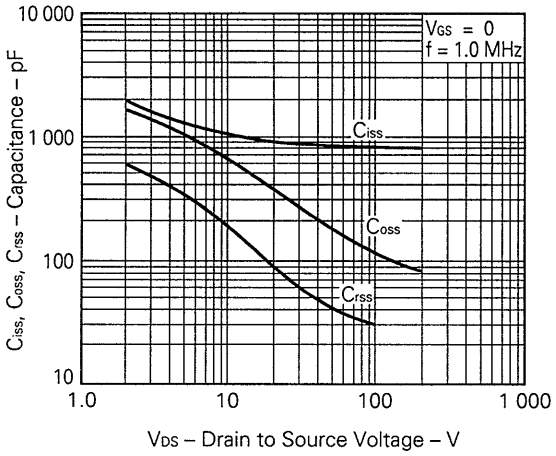
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



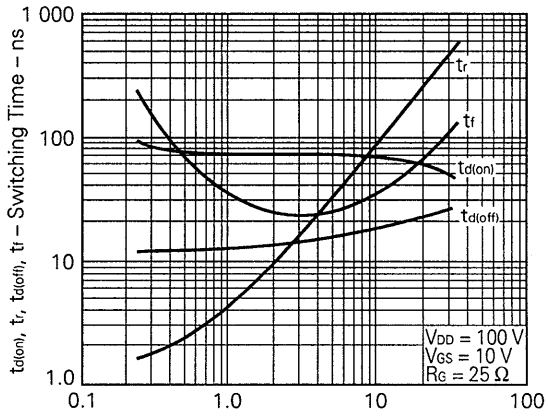
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



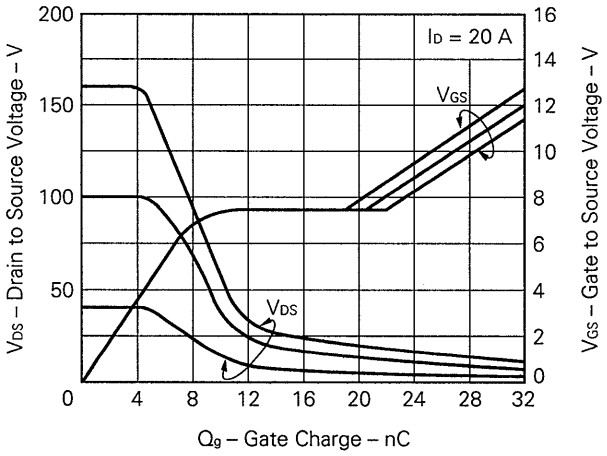
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



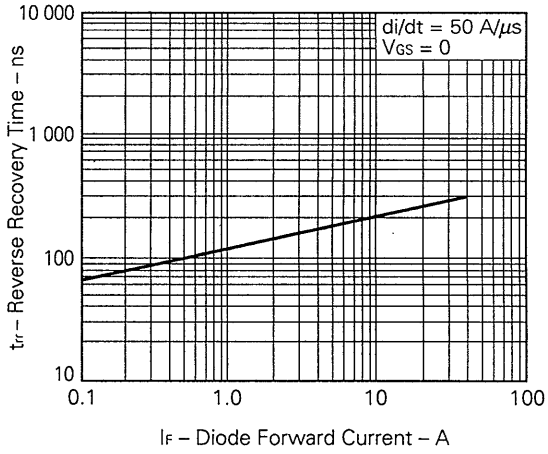
SWITCHING CHARACTERISTICS



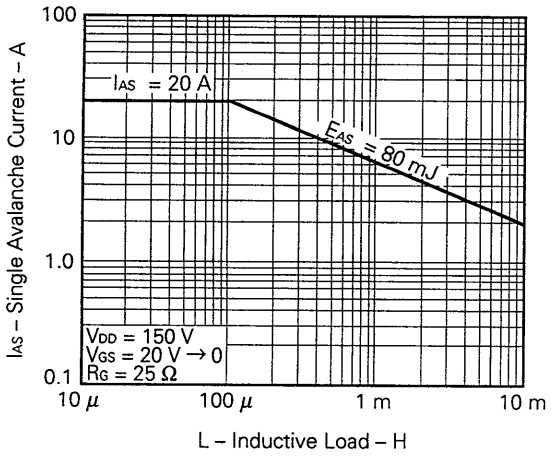
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



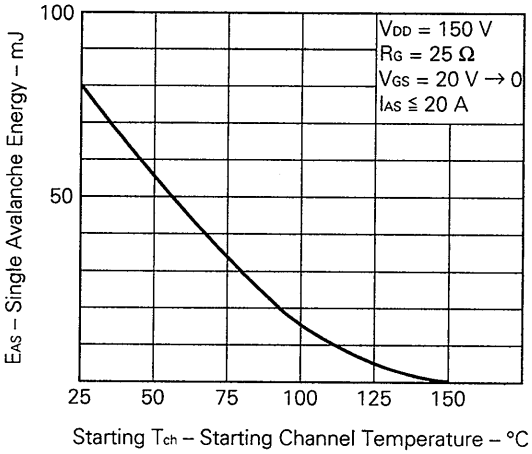
REVERSE RECOVERY TIME vs. REVERSE DRAIN CURRENT



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY vs.
STARTING CHANNEL TEMPERATURE



[MEMO]

Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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